

CS 6290 - Project 2

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Part 1

A

Miss Rate - 5.86% for the default configuration and 7.32% for the 16 kB L1 cache.

Speedup = $895.684/849.554 = 1.054$, about a 5% improvement

B

When we have a smaller cache, we have to do extra work. This is directly related to the miss rate, this involves figuring out what to remove from L1 cache, doing an appropriate writeback to L2 cache(which may cause another eviction and writeback from the L2 cache and so on). This extra work causes the execution to take longer.

C

Miss Rate - 5.83%, Speedup = $851.000/849.554 = 1.001$, about a 0.1% improvement

D

I would choose a 32kB single ported cache. This is because adding an extra port has minimal improvement(from Part C), but doubling the cache size has a much more substantial improvement(from part A).

E

Speedup = $1105.200/849.554 = 1.30$, 30%

F

Speedup = $851.514/849.554 = 1.002$, 0.2%

G

I'd pick the 4MB Single port cache. Adding an extra port has a minimal speedup(< 1%) while doubling the cache size avoids incurring the 200 cycle hit for memory access for a lot more requests, gaining a substantial 30% speedup.

Part 2

H

The simulation time is exactly the same, ie no speedup. We do not suffer a performance hit by removing dirty bits, as it appears that this cache does the writeBack asynchronously. When it does the writeBack, it simply sets writeBackPending for this line, and the actual writeBack is only done later(during readRemote or returnAccess). Thus due to the asynchronous nature, we only overlap the penalty for the extra writeBack with other requests to the L2 cache, and thus suffer no extra penalty.

I

With the dirty bit present, total number of accesses = lineFill + writeBack = 10193909 + 4140719 = 14334628. Without the dirty bit, total number of accesses = lineFill + writeBack = 10193909 + 10193397 = 20387306. Thus total number of access goes up by 42%!

Part 3

J

P(0)_DL1:readMiss=8333729

P(0)_DL1:writeMiss=1860180

P(0)_DL1:compulsoryMiss=230795

Total = 10193909. Compulsory = 2.26%, Non-compulsory = 97.74%

K

P(0)_DL1:readMiss=10703192

P(0)_DL1:writeMiss=2162535

P(0)_DL1:compulsoryMiss=230795

Total = 12865727. Compulsory = 1.79%, Non-compulsory = 98.21%

Total number of misses increased by 26.2%, compulsory misses stayed the same, non-compulsory misses went up by 26.8%

L

P(0)_DL1:readMiss=16346338

P(0)_DL1:writeMiss=4027934

P(0)_DL1:compulsoryMiss=230795

Total = 20374272. Compulsory = 1.13%, Non-compulsory = 98.87%

Total number of misses increased by 99.87%, compulsory misses stayed the same, non-compulsory misses went up by 102.18%(more than doubled!)