A Review of Recent Research on Heat Transfer in Three-Dimensional Integrated Circuits (3D ICs)

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Abstract— Three-dimensional integrated circuits (3D IC) technology has emerged in the past few decades, driven in part by the techno-economic difficulties of dimensional scaling and the increasing interconnect delay in microelectronics. In a 3D IC, vertical integration of multiple transistor planes, either through monolithic integration or through bonding of multiple strata offers reduced interconnect delay and enhanced design flexibility. However, vertical integration in a 3D IC also results insevere thermal management challenges. Thermal management of a 3D IC is exacerbated by the multi-layer nature of the 3D IC. Further, new components such as Through Silicon Vias (TSVs) offer opportunities for novel thermal management. This paper presents a critical review of research literature related to heat transfer in 3D ICs, focusing specifically on thermal modeling, thermal-electrical co-design and thermal management of a 3D IC. Key literature from recent years is categorized and summarized. A discussion on the future outlook for research in these areas is presented. It is expected that this review paper will be helpful for researchers in academia and industry for understanding the state-of-the-art in various areas related to heat transfer in 3D ICs.

Index Terms— Three-dimensional integrated circuits, thermal management, co-design, heat transfer.

I. Introduction

STARTING with the invention of the transistor [1], continued improvement in performance of semiconductor microelectronic devices was, for a long time, sustained by process technology innovation that facilitated the microfabrication of progressively smaller transistors and interconnection. This remarkably sustained, exponential reduction in transistor size and increase in speed, as envisaged by Moore's law [2], continued for several decades. However, as transistors become faster and faster, the speed of interconnection between transistors eventually started becoming the rate-limiting step. In addition, for techno-economic reasons, continued scaling down of the transistor size became increasingly cost-prohibitive. This has led, in the past few decades, to 'more-than-Moore' innovations for continued improvement in the performance of semiconductor devices that does not rely completely on transistor scale-down [3]. The

traditional framework of all transistors built on the same plane has also been challenged, and multiple approaches and advantages of vertically integrated transistor planes have been demonstrated. This approach, often referred to as a three-dimensional integrated circuit (3D IC) [4]–[6], has attracted considerable research in several directions. While 3D IC technology offers several key advantages compared to traditional, planar chips, progress in the adoption of 3D ICs in commercial products has been steady rather than spectacular. Amongst the various technical reasons behind this is the significantly increased challenge in thermal management of a 3D IC. Thermal management challenges in a 3D IC are more closely coupled with electrical performance and manufacturing than is the case in traditional planar ICs. These coupled phenomena often present critical trade-offs and constraints that must be correctly recognized and accounted for, in order to maximize device performance, reliability and lifetime.

A. Key advantages of 3D IC architecture

Vertically stacked 3D ICs offer several advantages over traditional 2D ICs [5]. Interconnection in a 2D IC with increasingly complex circuit components can result in the usage of small but densely packed wires over large interconnect distances between functional blocks, leading to substantial rise in signal propagation delay due to increased resistance and capacitance, also known as RC time delays [7]. On the other hand, vertical interconnection using Through Silicon Vias (TSVs) or microconnects [8] in a 3D IC may lead to smaller wire lengths, and therefore improved interconnection latency. Reduction in interconnect length also reduces power requirements along with improvement in signal transmission latency and yield of the circuit [8], [9]. For example, a 23% reduction in interconnect power consumption has been reported in a three-tier circuit compared to a single-tier circuit [10]. It has also been shown that the interconnect power and delay can be further reduced by increasing the wire pitch, which reduces capacitance and resistance per unit length [4].

Referring to traditional 2D IC designs for devices like processors, conventional input/output (I/O) pins were used to

connect memory and logic blocks generally arranged in the same plane. In contrast, in 3D ICs, such interconnection is provided by TSVs, which reduces the critical path length and thus enhances the memory bandwidth of 3D processors [11]. Other key advantages of 3D IC architecture include reduced package pin count and reduced form factor. Form factor of an IC relates to the size and shape of the circuitry, which can be improved substantially due to the usage of the third dimension in a 3D IC. Such features of 3D integration may lead to an overall improved chip design process [11].

3D integration also enables significant design flexibility. By separately designing, for example, the memory and logic chips, it may become possible to reuse the same chip for multiple applications. For example, the same memory chip could be integrated with multiple logic chips intended for multiple applications, thereby reducing the time and cost for memory design [8]. The two chips being integrated do not need to belong to the same technology node, and therefore, non-critical features can continue to be manufactured in lower-cost manufacturing facilities.

B. Manufacturing and Packaging of 3D ICs

Two distinct approaches for manufacturing of 3D ICs have been investigated. The first is a sequential process, in which multiple transistor planes of the 3D IC are fabricated sequentially on top of the same silicon substrate [12], [13]. This approach is often referred to as monolithic 3D IC manufacturing. In contrast, the second approach calls for bonding and stacking of multiple die and/or wafers that are first fabricated independent of each other.

The monolithic process uses either seed crystallization or laser recrystallization, and produces highly dense interconnection between adjacent layers of the 3D IC [13], [14]. Even nanoscale monolithic inter-tier vias have been demonstrated [15]. This approach does not require die alignment or assembly [16]. However, a key challenge in monolithic 3D IC manufacturing is that of maintaining the quality of lower layers while subsequently fabricating the upper layers primarily due to the high temperature needed in the fabrication process [12]. In order to overcome this challenge, molecular bonding at relatively lower temperature (around 200 °C) has been used [17]. Other alternatives to avoid undesirable impacts on lower layers include the use of germanium, which has lower crystallization temperature and melting point compared to silicon, the use of pulse anneal for dopant activation and implementation of high-κ gate dielectric [13]. The use of Ultratech approach, laser spike annealing (LSA), laser annealing [18] and ion cut technology [19] have also been investigated for minimizing thermal damage to underlying structures.

In contrast, wafer or die-level 3D integration does not suffer from the key problems in monolithic 3D integration, due to which, it is by far the dominant process choice for 3D ICs [17], [20]. In this case, individual die/wafers are manufactured separately and then bonded to each other to provide electrical connectivity between die/wafers. 3D integration has been carried out in face-to-face, face-to-back and back-to-back configurations, where 'face' and 'back' refer to the transistor plane and backside of the Silicon substrate [8].

The two key substrate bonding processes used for 3D integration are metal-to-metal bonding and dielectric bonding. Dielectric bonding, also known as SiO_2 or oxide diffusion bonding is carried out at room temperature, and thus minimizes thermal coefficient of expansion (TCE) mismatch errors [21]. On the other hand, metallic bonding [20] provides direct electrical connection via TSVs and microbumps, better corrosion resistance and a self-aligning phenomenon, but is limited in terms of scalability due to TCE mismatch of the interstratum connections [22]. A hybrid bonding that combines metallic and dielectric bonding has also been investigated to combine the advantages of both approaches [22].

Three distinct approaches have been proposed for 3D integration – wafer-to-wafer, die-to-wafer and die-to-die integration [23]. Wafer-to-wafer and die-to-wafer integration approaches have lower yield than die-to-die integration, which offers the Known Good Die (KGD) advantage [24]. However, die-to-die integration may be slower than the other two approaches.

TSVs and die-to-die microbumps are the two key integrating components of a 3D IC chip stack. While a TSV is primarily used for connecting circuits on two different levels of a 3D IC, the microbump connects two adjacent chips through bonding processes described above. These components are clearly depicted in the Figure 1, in which the bonding between die 1 and 2 shows an example of face-to-face configuration whereas between die 2 and 3 shows a face-to-back configuration [25]. A TSV is typically manufactured by etching a high-aspect ratio hole through the die and filling it with conductive metal [20]. TSVs, along with microbumps on the die/wafer surface enable electrical connectivity between die/wafers. Die thinning through grinding or etching is often carried out in order to facilitate the TSV manufacturing process [17]. The original wafer is often mounted on a handle wafer prior to thinning to avoid breakage.
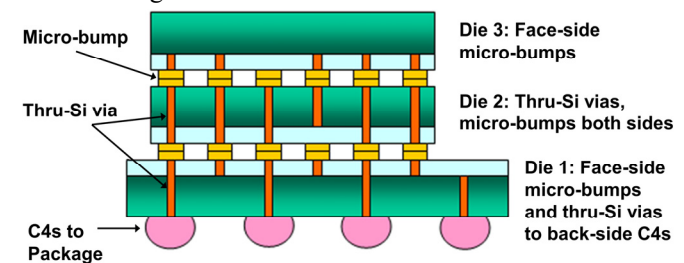

Fig. 1. Schematic of a bonded 3D chip with three stacked chips [25].

Controlling the TSV shape, minimizing the occurrences of voids during metal filling and preventing metal deposition at TSV edges are some of the key challenges needed to be overcome in TSV processing [26]. Improper wafer alignment is a key reason for TSV failure [27], and approaches such as transparent substrates, wafer backside alignment, through wafer via holes, infrared alignment and inter-substrate alignment have been used for wafer alignment [28]. Each TSV displaces transistor space on the Silicon, and therefore, a number of

interesting optimization problems related to the placement, design and sizing of TSVs have been investigated [29].

C. Key thermal management challenges in 3D ICs

Unfortunately, the enhanced packing density in a 3D IC that leads to reduced interconnect length, reduced power consumption, and other advantages also results in significant thermal management challenges. Higher heat generation in a concentrated area fundamentally results in greater temperature rise, which may cause performance reduction and, in an extreme case, physical damage to the circuit. Since one end of a 3D IC chip stack is usually taken up for electrical interconnection, only one end may be available for thermal dissipation. There may be limited pathways available for heat removal, particularly from chips in the middle of the stack. Supplying coolant fluid into intermediate chips for single-phase or two-phase cooling is also inherently quite challenging. Thermal conduction through TSVs is another heat transfer pathway, for which, co-optimization of TSVs is critical. Accurate thermal modeling, thermal-electrical co-design and co-optimization, and effective thermal management approaches for heat dissipation are, therefore, needed to address the thermal challenge in 3D ICs.

While the cooling of 3D IC structure can be carried out using a simple heat sink arrangement for low power applications, advanced cooling techniques such as single phase or two-phase liquid cooling may be required for higher heat generation [30]. Regulating the flow rate in liquid cooling can prevent thermal hot spots along with optimization of overall energy consumption for the cooling system [31]. In general, minimizing pressure drops along the integrated microchannel cooling network is as key challenge [32].

The effective utilization of features specific to 3D ICs, such as TSVs for heat dissipation is an important consideration. Thermal-aware floorplanning can manage heat loads by optimum distribution of circuit components and TSVs, in order to reduce junction temperatures across the IC [33], [34]. Several studies have also been are also carried out to simultaneously address thermal and electrical design challenges [35]. TSVs have been used as a heat removal mechanism [36], [37]. In addition, hybrid approaches that couple TSVs with microfluidic cooling [38], silicon micropin fin [39] or air gaps [40] have also been reported.

This paper presents a critical review of heat transfer and thermal management challenges in a 3D IC, with particular focus on literature from the past few years since the publication of last major review papers on this topic [30], [41], [42]. The next section discusses key research on modeling approaches for heat transfer in 3D ICs. Research on the impact of heat transfer on various aspects of 3D IC design is summarized in Section 3. Subsequently, section 4 summarizes key approaches for heat removal and thermal management for a 3D IC. Major challenges and future outlook for research in this area is discussed in Section 5. The closely coupled nature of manufacturing, electrical design and thermal management design of a 3D IC is recognized throughout, with emphasis on

review of papers that address these multi-disciplinary challenges. Due to significant overlap between the key focus areas of this paper, several papers may be discussed in multiple sections.

II. MODELING OF HEAT TRANSFER PROCESSES IN 3D IC

Similar to traditional microelectronic chips, the ability to accurately predict temperature distribution in a 3D IC is critical for accurate 3D IC design [43]. Further, such a predictive capability is also helpful for run-time performance optimization. Modeling of heat transfer processes in a 3D IC may be carried out using a variety of techniques. Broadly, these are divided into analytical and numerical computation approaches. Analytical techniques rely on deriving exact solutions of the energy conservation equation that, in addition to boundary conditions, governs the temperature field. Numerical computations, on the other hand, seek to approximately solve these equations by discretizing the geometry. While analytical techniques are desirable because of exactness and ease of integration with other design tools, it is often difficult to account for complex geometries, temperature-dependent properties and other complications. On the other hand, numerical techniques, while inherently inexact, may, with appropriate design, offer temperature predictions with acceptable accuracy. In addition to analytical or numerical models that address only the thermal characteristics of the 3D IC, tools that combine thermal and electrical design are also critical. This section is organized into sub-themes based on thermal modeling applications discussed in the literature. First, heat transfer modeling of the entire 3D ICs is discussed, followed by analytical and numerical modeling of 3D IC cooling. Modeling of specific components such as TSVs is discussed next, followed by a discussion of work on inter-die thermal contact resistance. Further focusing on modeling of specific thermal properties such as effective thermal resistance or effective thermal conductivity of the 3D IC.

Extensive literature is available on both analytical and numerical approaches for heat transfer modeling in a 3D IC. The body of literature is somewhat more limited for analytical approaches. Table 1 summarizes the key findings and techniques used in the literature on thermal modeling of 3D ICs. A thermal model of a 3D IC was developed to compare thermal performance with an equivalent 2D IC [44]. It was shown that while the 3D IC structure has a lower power usage advantage due to shorter interconnects, it may face greater thermal management problems due to insufficient heat removal. It was suggested that heat dissipation components such as TSVs and copper bonds play a more important role than effective thermal resistance to keep the chip temperature within acceptable limits [44]. Another thermal simulation of 3D ICs, referred to as logi-thermal simulation was carried out by coupling the logic and thermal parameters [45]. The use of this simulation tool for efficient component placement in 3D ICs was demonstrated. Further, a transient thermal simulation for 3D ICs using weighted Laguerre polynomials as basis functions has been proposed [46]. Galerkin's method was used to suppress the effect of time step on simulation stability. Thermal simulations

with adaptive time step have also been developed in standard programming languages such as C++ [47], which is important for ultimate integration of thermal prediction tools with other design tools. An adaptive time step simulation was designed to account for both thermal and functional behavior of 3D ICs. Models for temperature-dependent electromigration and leakage power have been developed [48]. It has been claimed that power dissipation and thermal distribution across the chip can be efficiently calculated and compared to other conventional methods, which do not consider these temperature-dependent factors. Another thermal simulation study named 3D-TarGA (Three Dimensional – Temperature gradient aware – architectural level) thermal analysis was proposed to account for a variety of considerations such as thermal convection, radiation, conductivity and leakage power [49]. This simulator was claimed to adequately account for the inter-dependence of thermal and other physical effects in the 3D IC and was shown to agree well with experimental benchmarks in terms of maximum IC temperature [49]. Recently, a thermal simulation tool named as Overheat 3D-IC was developed based on the quasi-3D thermal design approach [50]. This tool reduces the computational time by reducing the main 3D heat transfer equation into a group of coupled 2D equations targeting separate inter-die layers. This thermal simulation tool has claimed that it can reduce the computational time to just 10% that of the other commercially available thermal simulators with maximum of 20% relative error in calculation of maximum chip temperature [50].

Thermal distribution across the multi-die 3D IC also depends on the dimensions of subsequent die arranged vertically one over the other. Literature suggests that differences in lateral sizes of neighboring die [51] or the variations in die thickness [52] may lead to significant change in hotspot locations and intensities. An analytical heat transfer model for thermal distribution in a 3D IC with unequally sized die [51] has suggested that a 3D IC with higher dissimilarity in lateral die dimensions results in a higher maximum chip temperature. On the other hand, another work focusing on the impact of variation in die thickness and inter-die bonding materials [52] has claimed that thinner dies lead to a higher probability of large localized temperatures. In contrast, relatively thicker die may act as a heat spreader and facilitate lateral heat transfer. It has been shown that utilizing underfill materials with high thermal conductivity can dramatically improve thermal performance of 3D ICs [52]. Additionally in another study, an analytical model for heat transfer in 3D ICs was developed to optimize the relative arrangement of hotspots to achieve uniform temperature distribution and minimal peak temperature [53]. Thermal conduction analysis has been combined with sequential quadratic programming algorithm to account for the impact of TSVs, heat spreader and thermal interface material [54]. The use of this tool for sensitivity-based optimization for heat transfer in a multi-layered 3D IC has been demonstrated. A thermal model for dissimilar semiconductor chiplets integrated into a single 3D IC has been proposed [55]. This approach carries out placement of heterogeneous interconnects using customized codes, followed by extraction of thermal

TABLE I
A SUMMARY OF TECHNIQUES AND FINDINGS OF RESEARCH PAPERS ON THERMAL MODELING OF 3D ICS

Paper	Research Technique	Key Goals/Results
[56]	Fast compact transient thermal modeling: 3D-ICE	Accounts for microfluidic cooling and accurately predicts the thermal distribution with relative error of 3.4%.
[47]	Thermal distributions for 3D IC using adaptive simulation time step approach	Simulation time is reduced by a bigger margin due to the continuously varying time step value depending on past iteration results.
[49]	Temperature gradient aware thermal simulator (3D-TarGA)	Considers the thermal effects due to conduction, convection and radiation along with the leakage power in the 3D IC.
[45]	Logi-thermal simulation for predicting thermal distributions across the 3D IC	To identify the thermal issues and to assist in the component placement algorithms.
[46]	Transient simulation using weighted Laguerre polynomials to predict the thermal behavior of 3D IC	Stability of the method is not dependent on the time steps, due to which it performs better than the conventional methods.
[51]	Thermal distribution for 3D ICs with unequal die sizes using an analytical model	Higher the dissimilarity in die dimensions, higher will be the maximum chip temperature.
[60]	A thermal resistance network for the 3D ICs using heat conduction equation in spherical coordinates	Within 5% of experimental benchmark in the 0.27-2.18 W range of heating power.
[59]	Analytical-numerical modeling for 3D IC thermal behavior	Equivalent thermal resistance for the junction to air pathway
[67]	Equivalent thermal conductivity model for 3D ICs, anisotropic in nature	Considered lateral as well as vertical thermal transmission along the copper wires, TSVs and microbumps, agreed within 7.5% with a finite element code.
[52]	Effect of die thickness on thermal distributions across 3D IC	3D ICs with thinner dies might results into intensified hotspots but comparatively thicker die would work as a heat spreader in lateral directions.
[62]; [63]	Numerical modeling of interdie thermal resistance of the 3D ICs and experimental measurements	Measurement of inter-die thermal contact resistance.

properties of the layout material. A fast thermal modeling approach called 3D-ICE has been proposed for 3D ICs with inter-tier microchannel cooling [56]. The stated approach using compact transient thermal model has been claimed to be time saving and accurate with 3.4% error in peak temperature after validating the same against a commercial CFD tool. The 3D-ICE approach could reduce the simulation time dramatically when compared to a conventional CFD method, due to its capability of parallel operations on multicore architectures [56]. Other analytical thermal models for a multi-die stack integrated with inter-die microfluidic cooling have also been proposed [57]. Recently, a thermal modelling numerical tool – TIMiTIC

– Thermal simulator of Integrated Microchannel cooling for Three dimensional Integrated Circuits was used to optimize the profile for power dissipation to reduce the peak temperature by 10 °C [58].

Thermal properties of the 3D IC structure, such as effective thermal resistance or equivalent thermal conductivity can help develop accurate thermal models. An analytical model was developed to calculate the thermal resistance of the junction-to-air pathway of a 3D IC, assuming one-dimensional heat flow [59]. An interesting thermal analysis was carried out for the thermal resistance network in a 3D IC utilizing the principle of heat conduction in spherical coordinates [60]. A maximum relative error of 5% compared to experimental results was demonstrated in the 0.27-2.18 W range of heating power. A thermal resistance analysis was carried out for a 3D IC integrated with TSV interposers and microfluidic cooling embedded in the bottommost TSV interposers in the stack [61]. On the other hand, a thermal model was proposed to determine the interdie thermal resistance in a 3D IC [62]. Thermal resistance was determined using high speed temperature measurement on one die while the neighboring die is heated, and comparison with a numerical model [62]. A similar technique was used to evaluate the thermal resistance of interconnecting microbumps in a customized 3D IC chip with and without underfill [63]. Another study involved an experimental benchmarking of a Cu/dielectric wafer-to-wafer bonded 3D IC, on the basis of which, steady state and transient thermal models were developed [64]. This study confirmed that the use of Cu/dielectric bonding reduced die-to-die thermal resistance. A compact thermal model was developed using finite volume method to model the impact of the power distribution network as a heat source [65]. This model determined an equivalent thermal conductivity of a power distribution network, which was then utilized for temperature calculations. Further, a numerical model was developed to predict the thermal behavior of 3D ICs based on equivalent, anisotropic thermal conductivity. This model considered several parameters such as TSV dimensions, thickness of linear material and type of thermal interface material, etc. [66]. Similarly, another numerical model for equivalent, anisotropic thermal conductivity of a 3D IC has been proposed, assuming heat transfer in vertical and lateral directions in the structure [67]. As shown in Figure 2, the heat conduction path considered for analysis accounts for copper redistribution wires, through silicon vias and microbumps [67].

In light of the several modeling approaches available, as described above, the decision of which approach to adopt for a specific application must consider the degree of accuracy desired and computational resources available. In addition, whether the temperature computation needs to be implemented in real time is also an important consideration.
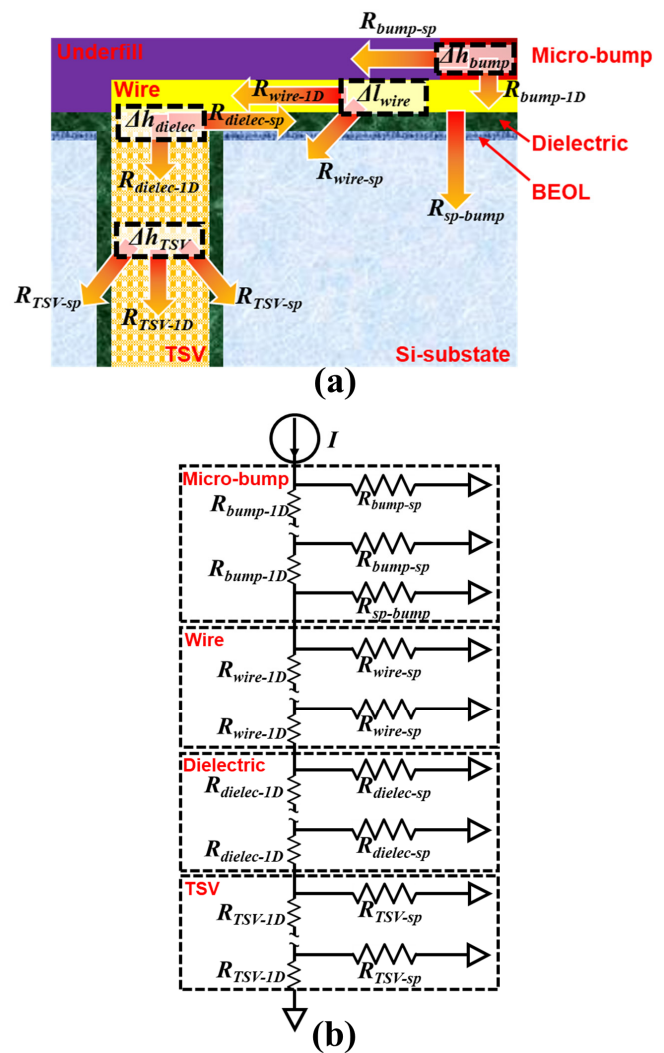

Fig. 2. (a) Basic structures of high thermal conduction path; (b) Compact thermal resistance network of high thermal conduction path (adapted from [67]).

III. THERMAL CONSIDERATIONS IN 3D IC DESIGN

A 3D IC offers key advantages such as lower latency due to reduced wire-length and reduced power consumption compared to a convectional 2D IC. However, higher thermal resistance in vertical direction due to lower thermal conductivity of dielectric interlayers, inter-layer thermal contact resistance and higher power density in smaller, concentrated areas result in critical thermal challenges, which can severely throttle chip performance and limit the benefits gained by 3D integration [68]. These challenges are best addressed in the design stage of 3D ICs instead of being an afterthought [69], [70]. The key 3D IC design steps – floorplanning, placement and routing – must take thermal considerations into account for thermal-electrical co-design and co-optimization [71]. Such kind of thermal aware methods are also used to rectify 3D IC reliability issues based on TSV operations [72]. Accurate prediction of the temperature distribution is particularly important, since a direct temperature measurement is often not possible [33], [73]–[75], [76]. The use of TSVs as well as thermal through-silicon vias (TTSVs) for promoting heat transfer in the vertical direction has been widely

proposed [33]. Efficient placement of TSVs/TTSVs has been carried out to maximize thermal benefit while also achieving reduced wirelength, effective usage of available silicon area, well-managed routing and overlapping of components [77]. Table 2 summarizes the key literature in the area of thermal design and thermal-electrical codesign, including the comparison of outcomes in terms of improvements in key performance parameters with the respective benchmark circuits listed for each paper. This section is organized as follows – starting with the thermal aware placement and floorplanning algorithms for TSVs and other cells in 3D ICs. Further, a detailed discussion on co-optimization of thermal and electrical aspects of a 3D IC, which includes power consumption, signal delay and heat dissipation requirements for designing the placement strategies. The challenges in design phase of a microfluidic cooling-based 3D ICs is also discussed in this section. At the end, effect of thermal stresses and thermal stress aware placement strategies were discussed, which was followed by discussion on a phenomenon in 3D ICs called electromigration.

The introduction of 3D IC technology has necessitated key changes in the IC design procedure, which now requires determination of wirelength and number of TSVs, as well as the floorplanning and placement of the TSVs with respect to other circuit components on the chip. Figure 3 depicts the general

TABLE II

A SUMMARY OF THE IMPROVEMENTS IN PERFORMANCE PARAMETERS IN THE FIELD OF THERMAL DESIGN AND THERMAL-ELECTRICAL CODESIGN OF 3D ICs FOCUSING ON PLACEMENT OR FLOORPLANNING TECHNIQUES. T_{MAX}, T_{AVG} AND dT/dx ARE PEAK TEMPERATURE, AVERAGE TEMPERATURE AND TEMPERATURE GRADIENT, RESPECTIVELY. L_W, N_{TSV} AND A_{CHIP} ARE LENGTH OF WIRE, NUMBER OF THROUGH SILICON VIAS AND CHIP AREA, RESPECTIVELY.

Paper	Technique	Comparison	Change (%)					
			T_{MAX}	T_{AVG}	L_W	N_{TSV}	A_{CHIP}	dT/dx
[34]	Iterative thermal force directed approach	A benchmark circuit with placement without thermal forces	-12	-1.3	5			-17
[85]	T3Place: Transformation from 2D to 3D placement	Relaxed conflict net (RCN) graph-based layer assignment	-37		8	6		
[69]	Quadratic uniformity modelling approach	3D placement with thermal considerations	-15	-3	6			
[33]	Pseudo 3D placement considering impact of TSVs	Baseline case	-34		6			
[78]	TSV spread and alignment	Baseline case	-0.3	-2.7	9.3			
	Coupling aware placement	Baseline case	-11	-1.6	9			
[74]	Fast thermal analysis 3D floorplanning with TSV placement	No temperature optimization	-13		1.4	0.1		
[75]	Temperature aware floorplanning without TTSV placement	Baseline case [49]	-46		5	40	7	

design flow for 3D IC placement, from TSV insertion all the way to iterative optimization of positioning of TSVs and other components [78]. These tools typically also compute and seek to optimize the thermal impact of the TSVs. A system-level thermal aware simulation named Pathfinder3D has been developed to generate a 3D IC floorplan using thermal properties of the components [68]. Pathfinder3D facilitates balancing various design alternatives to discover possible tradeoffs among power, temperature and performance of the chip without any thorough execution of the generated floorplan based on available static and dynamic thermal profiles. This simulation utilizes a physical thermal extractor known as WireX, which produces a thermal netlist from the tentative generated floorplan, using thermal properties of the components. Further, using AccessNoxim simulator, an Adaptive Thermal Aware Routing (ATAR) algorithm [79] was developed to reduce the maximum chip temperature based on the standard chip manufacturing norms. ATAR utilizes the weighted sum approach to calculate the propagating cost to prevent livelock and deadlock, and achieve uniform thermal distributions with well-managed on-chip traffic experimentally. Several other similar algorithms such as Traffic and Thermal Aware Routing (TTAR) [80], Dynamic Thermal Balance Routing (DTBR) [81] and Thermal Aware Fully Adaptive Routing Algorithm [82] have also been developed. Recently, a modified genetic algorithm was developed to optimize thermal aware 3D IC multilevel routing towards minimizing temperature rise and minimizing path selection to control the wirelength [83]. This algorithm carries out an effective routing process, in which, the TSVs is placed in the available white space of the entire 3D IC, and the final chip package area and routing resources are calculated based on the number of TSVs assigned. Similarly, a thermal aware placement method was developed based on optimization of maximum temperature and interconnect length [84]. This method has the capability not just to alter the positions of individual components on chip area but also interchange the different layers of 3D ICs.
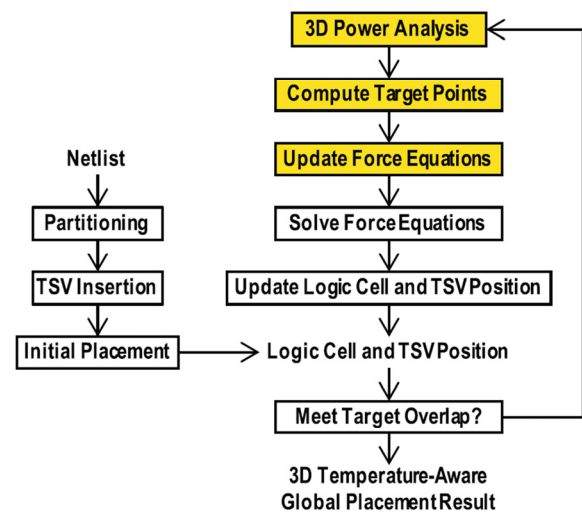

Fig. 3. Design flow for 3D IC global placement [78].

Strategies for thermal aware placement and floorplanning

generally rely on the positioning of cells and TSVs in such a way that thermal hotspots are avoided, and lower thermal gradients are achieved. In one of the studies, an iterative, thermal force directed approach was implemented to position the cells away from the higher temperature regions, using finite element analysis to monitor post-iteration transient thermal distributions across the chip [34]. The approach starts with initiating the placement of all cells in a random fashion, then improving the average cell temperature and wirelength iteratively based on the thermal gradient across the chip. Postprocessing is mostly focused on reducing the percent overlap of cells, starting with z-direction. Validation results based on benchmark circuits and testbenches for this thermal aware placement confirm the improvement in thermal gradient and reduced peak on-chip temperature with a little increase in wirelength [34]. Further, an approach with thermal aware placement of cells in 3D IC, also known as T3Place [85] has been proposed. This approach transforms the conventional placement strategy for a 2D IC into a 3D placement plan and optimizes the maximum chip temperature, wirelength and number of TSVs. Various transformation techniques have been studied. This includes a local stacking transformation technique that results in minimum wirelength, and a folding-based transformation, which achieves the lowest number of TSVs in the 3D floorplan. To achieve a reasonable tradeoff between number of TSVs and wirelength, the window-based stacking transformation and additional refinement of the 3D placement using relaxed conflict net (RCN) graph-based layer assignment method has been proposed [85]. A discrete cosine transformation (DCT) approach in conjunction with a quadratic function based on thermal dissipation and cell placement has been used efficiently in a thermal aware placement uniformity model [69]. In this case, the unified cell distribution and thermal dissipation are updated iteratively. This quadratic uniformity modelling approach is focused on preventing hotspots with a well-balanced thermal aware 3D placement that also minimizes the overlapping of cells and reduces wirelength. Lately, a hierarchical floorplanning approach based on TTSV area and positioning optimization was proposed using simulated annealing [86]. This approach has claimed to reduce the peak chip temperature by 6 °C by increasing the wirelength by 3.5%. A Q-learning based thermal aware routing algorithm was developed for 3D ICs, which stated to have a better performance than most recent thermal-aware algorithms [87]. Some of the other 3D floorplanning approaches include one that utilizes a bio-inspired hybrid thermal management algorithm [88]. This algorithm combines thermal aware floorplanning with liquid micro-channel cooling to reduce hotspots in a densely packed IC [88].

While the general goal of such floorplanning algorithms is to achieve uniform thermal distribution, some hotspots are inevitable, especially since thermal optimization is being carried out in conjunction with optimizing other performance parameters as well. The effect of placement of liquid microchannels near high temperature regions has been investigated [88]. In this hybrid algorithm, an initial floorplan is designed without considering the thermal conditions of any

functional unit and is then optimized based on thermal condition of each functional unit. The functional unit positions are interchanged with each other iteratively to reduce the on-chip peak temperature. In a recently proposed thermal aware floorplanning approach without TTSV implementation [75], simulated annealing was used to optimize the maximum chip temperature. This results in an optimized floorplan that optimize the wirelength and cost of manufacturing along with the maximum chip temperature and the number of TSVs. On the other hand, a 3D floorplanning utilizing fast thermal analysis [74] has also been proposed, which consider TSV allocation to efficiently minimize the on-chip peak temperature as well as wirelength. In this case, thermal estimates are made using bilinear interpolation using pre-simulated thermal profiles. Considering validation results for this floorplanning approach obtained on benchmarking circuits, when compared with no temperature optimization case, the on-chip peak temperature was shown to reduce by 13% along with very small increases in wirelength and number of TSVs by 1.35% and 0.13% respectively.

Recent research literature has also recognized the non-thermal consequences of the inclusion of TSVs in the 3D IC design and has proposed approaches for multiphysics analysis and co-optimization. Each TSV occupies a certain silicon area. If the number and size of TSVs are not controlled, then either the die area must increase significantly or the die area available for circuit placement must go down. Thermal aware TSV co-placement algorithms have considered these aspects in the TSV design process [33]. Considering the benefit of higher thermal conductivity of a TSV, effective distribution of TSVs leads to an improved thermal integrity in 3D ICs keeping TSV power distribution as an optimal condition. Some of the research in this direction has focused on simulating and optimizing 3D IC TSV placement considering the impact of TSVs to achieve ideal gate locations with reduced wirelength [77]. Additionally, the 3D IC placement procedure can further be improved by placing high heat generating components near regions of higher vertical thermal conductivity due to greater TSV density [78]. TTSVs can also be inserted iteratively after analyzing the 3D thermal map of the IC, so that the peak on-chip temperature will be maintained below baseline levels [89]. Such an approach can reduce the number of TSVs required and interconnecting wirelength along with the hotspot temperature.

Since thermal and performance optimization for a 3D IC are so closely coupled with each other, the need for 3D IC codesign on the basis of both thermal and electrical performance has been recognized [70], [90]. This codesign involves optimizing the placement strategies for signal-carrying TSVs [91] as well as TTSVs, microfluidic channels which are responsible for heat dissipation [92]. The 3D IC designer's primary motive is to find a perfect trade-off in routing space allocation of these IC components that will help satisfy both thermal and performance requirements.

Numerous algorithms have been developed for combined analysis of power consumption and heat generation, focusing on parameters such as peak chip temperature, signal delay and power leakage. A multi-objective algorithm for 3D processor

floorplanning has been proposed based on interlayer partitioning and vertical overlapping [93]. This floorplanning algorithm attempts to avoid the thermal runaway of 3D IC due to the effects of temperature and power leakage while balancing thermal-electric performance. Moreover, a partitioning-based analytical placement technique for 3D ICs was developed to focus on the direct effect of power leakage on chip temperature considering wirelength reduction [91]. Thermal placement in this technique maintains an optimal tradeoff between maximum temperature, interlayer TSV quantity and wirelength while keeping interconnection costs as low as possible. It has been reported that for 46% fewer interlayer vias, a 2% reduction in wirelength may be obtained. On the other hand, by increasing interlayer vias by 10% and reducing the wirelength by 1%, a 46% reduction in maximum temperature can be attained [91]. Also, a 3D placement and routing technique was established with the objective to optimize electrical crosstalk and amount of power noise. A 3D global algorithm has also been proposed to consider other requirements such as reduction of peak temperature, whitespace and interconnection costs [90]. A Steiner routing algorithm has been developed for 3D IC codesign in two steps – 3D tree construction and refinement. In this case, the refinement process included repositioning of TSVs following an electrical performance limitation, which were originally planned in the 3D tree construction with thermal optimization of Elmore delay function. This algorithm helps the IC attain an improved thermal-electric performance with low interference and reduced signal noise [94]. Another thermal electrical co-optimization technique combined an electrical delay model and a temperature computation method for 3D ICs using Green's function method. This approach focused on reducing the interconnect wire length and peak temperature simultaneously. Physical and manufacturing design constraints in floorplanning were considered in this co-optimization process [95]. In another 3D IC routing method, thermal-electrical codesign of TSV/TTSV was carried out using an Integrated Multi-Commodity Min-Cost (IMCMC) model to balance signal congestion and temperature within the design space. Using the conditional grid extension method to solve this IMCMC problem, this work reported 8.2% and 30.2% reduction in wire length and signal delay, respectively [96]. Further, a combination of power and thermal models was used to analyze and improve the thermal-electrical performance of a 3D IC. In this case, the power model estimated power consumption using a linear function while the thermal model used ring-oscillator based temperature sensors for estimation of heat dissipation of various IC components [97]. A co-optimization approach has been reported, in which, interconnect floorplanning was carried out using design of experiments and response surface methodology. This paper reported that the microfluidic cooling method is more effective for greater heat removal and reduced signal delay than planning extra TSVs or TTSVs [92].

Microfluidic cooling has been recognized as a prominent approach for heat removal [31], [98], and is discussed in detail in Section 4. Several design challenges associated with microfluidic cooling have also been recognized, and are discussed here. These include higher signal delay due to lengthier interconnecting wires and TSVs and challenges associated with wafer thickness [35]. Since leakage power plays a key role in determining overall heat dissipation, and hence, temperature rise [99], therefore, the design stage of microfluidic cooling mechanism must account for latency and power consumption along with the default thermal objectives. A 3D centric microfluidic heat sink design was discussed in one of the coupled thermoelectric codesign studies, focusing on its impact on TSV capacitance along with thermal resistance and pressure drop interdependencies. It has been reported that, as the interlayer thickness increases, the TSV capacitance also goes up, whereas if the TSV aspect ratio (depth to diameter relation) increases the TSV capacitance gets reduced accordingly [35]. A conjugate analysis of electromagnetism and transient heat transfer has been carried out to simulate an integrated microfluidic cooling based on finite element method (FEM). This co-simulation efficiency can be improved using schemes such as Finite Element Tearing and Interconnecting (FETI) and FETI-enabled parallel computing combined with adaptive time stepping [100]. For a 3D FPGA, another case of microfluidic cooling co-design has reported an increase in operative frequency of around 80% and energy efficiency improvement of 124% when compared with a traditional static heat sink. This work has also reported the relationship between microfluidic channel density in single or multiple interlayers with heat removal and electrical performance [99]. In another physical codesign study for a microfluidic-cooled 3D IC, a hierarchical partitioning-based technique was used to strategically place interlayer MFCs, circuit gates and TSVs simultaneously. The advantages of microfluidic cooling over air cooling were highlighted, ad it was shown that microfluidic cooling results in 40.2% reduction in chip area [101]. Further, a hierarchical model of online thermal management strategy for a liquid-cooled 3D IC was proposed. In this work, the thermal profile for a 3D multiprocessor system on chip (MPSoC) was optimized using dynamic voltage and frequency scaling (DVFS) [102]. Based on experimental validation using benchmarks, thermal variation of less than 10 °C per interlayer and up to 50% energy savings were claimed. In a similar paper that also used DVFS-based thermal management, a reduction in energy requirement for cooling mechanism by around 63% and that of the whole 3D IC by around 21% was reported, without letting the system exceed the set temperature [31]. Figure 4 describes a microfluidic cooling arrangement of a 3D IC using a prototype, a cross-sectional view and a layout of the internal mechanism [31]. Microfluidic pin fin heatsinks embedded in 3D ICs have been proposed along with a thermo-electric codesign focused on balancing electrical performance and energy efficiency with TSV capacity and cooling capability. This paper concluded that the codesign approach improved the performance of 3D ICs by 123% and 143% based on highest bandwidth and maximum cooling arrangements, respectively [103].
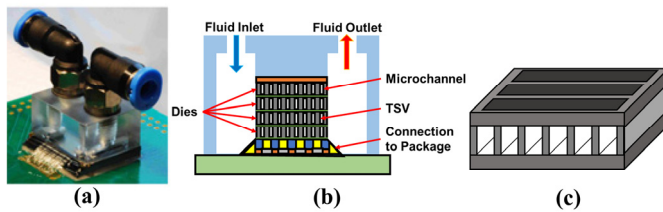
Fig. 4. (a) Prototype; (b) cross-section and; (c) layout of a liquid cooled 3D IC (adapted from [31]).

The generation of thermomechanical stress due to thermal gradient around TSVs leads to serious reliability challenges. A finite element analysis of Copper TSVs has reported that the induced thermal stresses increases as the TSV diameter increases and decreases as the pitch size increases [104]. Due to the thermal gradient and dissimilar thermal expansion coefficients of silicon wafer and TSVs, a thermal stress induces a crack driving force to indulge in the silicon, which is dependent on different silicon crystal orientations and TSV depth-to-diameter aspect ratios [105]. Another analysis of thermal stresses in 3D ICs were carried out to focus on the impact of thermally induced stresses on signal delay, variations circuit timing and leakage power levels. This analysis has demonstrated the effect of variations in gate placement layouts with respect to the TSVs on signal delay limitations; the path delay can be improved if the device gates are placed in the horizontal planes among TSVs [106]. Further, a thermomechanical stress and reliability analysis tool was developed based on linear superposition principle of stress tensors, which is claimed to compute faster than standard finite-element simulation tools in most of the previous studies. This tool suggests that the von Mises stress increases with lower liner thickness and decreases as the TSV pitch increases [107]. A TSV floorplanning strategy to account for and minimize thermomechanical stresses was demonstrated. According to this work, the average thermal stress reduced by 7.6% and 2.2% in block and system level, respectively [73]. A 3D IC codesign involving thermal, electrical and mechanical aspects was proposed, in which a signal delay model was established with the usage of dummy TSVs. It has been reported that if this signal delay model is applied accurately, around 61% reduction in clock skew can be expected [108].

The reliability and performance of IC is negatively affected by changes in silicon mobility rates due to stresses induced around TSV structures [109], [110]. A keep out zone is the designated distance of any device from a TSV, so that the device doesn't get affected due to the induced stress [111], [112]. A thermo-mechanical stress model for copper TSVs in silicon substrate, showed that the sidewall roughness of TSVs influences the 3D IC electrical performance. Leakage current can be reduced with selection of an appropriate etching process to ensure smoother TSV sidewalls [113]. A numerical analysis for thermal stresses induced near TSVs and solder interconnects has established the dependence of TSV and solder joint durability on silicon chip thickness – the higher the chip thickness, the lower is the durability of interconnects [114]. This study used general linear model analysis of variance (GLMANOVA) to investigate the effect of each reliability-related factor such as silicon chip thickness, thermomechanical properties of interconnect materials and TSV aspect ratio. Further, a complement sector model was used to analyze the thermal stresses induced in the 3D IC TSVs. This analysis concluded that thermal stress is directly proportional to the diameter of TSV [115]. Thermomechanical stresses in through-vias in glass substrate have been analyzed [116]. This work showed that the induced thermal stresses increase when the tapered via wall angle increases or the through glass via diameter and glass substrate thickness decrease. Similarly, a number of finite-element studies of thermal stresses in 3D ICs has available. These papers characterize different types of stresses and their effects [117]–[120], and investigate the influence of TSV dimensions [121]. On the other hand, a thermal stress analysis based on a knowledge oriented nonuniform (KONU) refinement strategy with parallel adaptive finite element method has been proposed. This method claims to predict TSV-induced thermal stresses with 12.5 times greater speed and 25% greater accuracy compared to a conventional finite-element based analysis [122]. Additionally, a few attempts have been made to improve the conventional finite element approach by combining it with artificial neural networks to accurately predict the thermal stresses in 3D ICs with less computational overheads [123]–[125]. A numerical model for thermo-mechanical stresses induced inside and around the TSV was carried out. A groove structure around the TSV was proposed to effectively release the TSV-induced thermal stress [126]. Recently, a study based on numerical analysis of 3D IC liquid cooling was carried out which stated the effects of combination of various coolants and different materials of embedded cooling channels, on temperature and stress distribution across the chip area were observed [127], [128]. This study highlights the importance of chip fabrication and cooling mechanism design to reduce the localized thermal stress, which may cause cooling system breakdown. Whereas, a numerical model focusing on optimizing the thermal stresses and temperature distribution has claimed that around 34% of the reduction in maximum thermal stresses can be achieved by altering the microchannel arrangements and addition of micro-pin fins [129].

A placement strategy for 3D IC was proposed based on thermal stress predictions by evaluating different factors such as wire length, electrical performance, induced stresses and carrier mobility based on keep-out zone dimensions [130]. This placement strategy was shown to have lower circuit latency compared to placement based on optimizing the wirelength alone. Another TSV placement technique based on analytical stress migration analysis and von mises stress estimation was developed and claimed to reduce the von Mises stress by 23% with just 3% extra wirelength compared to the conventional placement strategy [131]. In contrast with the extensive literature on modeling and prediction of stresses around a TSV, there is relatively lesser work on experimental measurement. Some of the established methods that have reported for this purpose are micro-Raman spectroscopy [132], precision wafer curvature technique coupled with micro-Raman spectroscopy [133], digital-to-analog test structures [111], X-ray micro-

diffraction mapping [112], [134] and picosecond ultrasonic method [135].

Electromigration (EM) has long been recognized as a key reliability concern in semiconductors [136]. EM, which occurs due to atomic diffusion in metal interconnects can, to some extent, be addressed in the design phase [137]. Several papers have been published on EM and its connection with thermal modeling in the design stage for 3D ICs. A 3D IC design optimization was carried out on the basis of EM issues due to TSVs, using a compact thermal model and simulated annealing scheme. It was shown that the EM-aware approach can achieve 341% improvement in mean time-to-failure by using only 3% extra wirelength [138]. Additional work in the EM–thermal-electrical codesign direction has showed that the EM lifetime can be extended by 324% with performance deterioration of just 1%. This study implemented an EM-aware thermal distribution on chip by inserting TTSVs using a quadratic programming based approach and used a linear programming formulation in conjunction to further reduce the wirelength [139]. The literature on electromigration challenges and mitigation in 3D ICs is somewhat limited.

IV. THERMAL MANAGEMENT APPROACHES FOR 3D ICS

Heat dissipation in a 3D IC is problematic due to the increased density of transistors and interconnection, the use of heterogeneous materials and the introduction of thermal contact resistances between layers, which may be very large depending on the process technology. These factors may lead to several thermal management concerns such as higher junction temperatures, thermal gradients and localized hot-spots that directly affect IC performance, reliability and in some cases, cause catastrophic failure [102]. Several conventional cooling methods such as air cooling, heat pipes, backside heat exchangers or thermoelectric coolers are not appropriate for a 3D IC, in which, there is an inherent difficulty in accessing and removing heat from the internal layers within the 3D IC [140]. Other approaches such as jet impingement cooling and spray cooling also suffer from drawbacks such as the requirement of higher pressures for micro-droplet dispersion [141]. Table 3 summarizes the key outcomes and approaches specified in the research papers on thermal management of 3D ICs. This section is organized as follows – starting with the concepts of microfluidic cooling, its analytical and numerical modeling. Then focusing on the micro-pin fin optimizations in terms of its arrangement as well as geometry. Further a discussion about two-phase cooling has been followed by experimental research work in thermal management of 3D ICs. The importance of thermal through silicon vias with a motive to mitigate the effects of non-uniform heat dissipation is discussed, ending with the discussion of hybrid approaches in cooling techniques of 3D ICs.

Microfluidic cooling is the dominant thermal management mechanism that has been investigated for 3D ICs. Reducing the microchannel cross-section generally helps achieve higher heat transfer coefficient and thus higher thermal performance [140], [141], although this may come at the cost of increased pumping requirement. Early work in the use of liquid cooling of

TABLE III
A SUMMARY OF APPROACHES AND OUTCOMES OF RESEARCH PAPERS ON THERMAL MANAGEMENT TECHNIQUES IN 3D ICS.

Paper	Approach	Outcome
[98]	Co-optimization of floorplanning based on electrical, thermal and physical features of 3D IC with microfluidic cooling.	Performance improvement by 130% compared to an air-cooled CPU.
[158]	Optimization using fast thermal model for liquid cooling networks with flexible topology	Around 84% energy savings in pumping power or reduction in thermal gradient by 38%.
[160]	Independent interlayer microfluidic cooling	Reduction in the junction temperature of a memory-on processor 3D IC by around 25 °C compared to air cooling.
[39]	Microfluidic cooling with combination of TSVs and micro-pin fin heatsinks	Reduction in peak temperature of the circuit by 33% when compared to conventional air-cooled heat sink.
[194]	Microfluidic cooling in conjunction with thermal through silicon vias (TTSVs)	Around 56% energy savings in pump power.
[156]	Non-uniform microchannel distribution	Up to 80% energy savings in cooling system.
[204]	Microfluidic cooling with microgaps and variable pin fin clustering	Maintaining maximum temperature below 65 °C with deionized water at inlet temperature of 21.3 °C.
[147]	Effect of clustering of micro-pin fin in microfluidic cooling	8 °C peak temperature reduction at the expense of 148% increase in pumping power.
[146]	Variable fin density of offset strip fins and variable spacing ribs in microfluidic cooling	30 °C temperature difference and 34 kPa pressure loss for optimum arrangement of variable fin density.
[143]	Microchannel patterning and pruning in microfluidic cooling	Energy savings in the range of 11-61% in terms of cooling system.
[181]	Using vacuum gaps and chip-to-chip communication for thermal isolation	Enables the DRAM to operate at a temperature of 47 °C lower than that of the conventional system.
[202]	Thermal isolation using air gaps in microfluidic cooling	39 °C reduction in peak temperature by compared to conventional design with underfill and microbumps.

integrated circuits used a compact water cooled integrated heat sink on the backside of the substrate [142]. This study used deionized water at 23 °C and 214 kPa through microchannels etched in silicon, while a thin film resistor was used as a simulated heat source. A highest substrate temperature of 71 °C and power density of up to 790 W/cm^2 was achieved. It was shown that increasing the coolant flow rate can effectively reduce thermal resistance. A maximum thermal resistance of 0.09 °C/W per cm^2 was reported. Large pressure gradients along the coolant flow path, sudden drop of thermal performance due to critical heat flux limitation or the discrete flow behavior in terms of coolant phase transformation along the flow have been identified as key challenges [30], [141]. A number of

approaches such as optimization of microchannel design [143]–[145], use of micro-pin fins [146], [147] and achieving controlled flow boiling [148], [149] have been identified.

The design of microfluidic cooling for 3D IC is fundamentally different from the traditional cooling for 2D ICs. The interactions between electrical, thermal and physical design elements becomes more important than ever, leading to the need for effective, multi-disciplinary design tools. The interdependence between microfluid cooling and the electrical, thermal and physical features of a 3D IC have been studied [98]. It has been shown that microfluidic cooling co-optimized with floorplanning of a 3D CPU can improve performance by 130% compared to an air-cooled CPU. Moreover, transient thermal models for liquid cooled 3D ICs have been developed, with emphasis on improving computational efficiency. [150]. One particularly interesting insight from such papers is that for thermal simulations of microfluidic cooling of 3D ICs, replacement of the fluid region with a simpler convective boundary condition may result in significant improvement in simulation time while keeping the error within acceptable limits [151]. Key limitations of this approach include the ability to model only a straight microchannel in a single interlayer and the inability to account for convective heat transfer coefficient that may vary along the flow path. Other compact thermal modeling techniques have also been developed specifically for straight microchannels with laminar flow of coolant, to be utilized for logi-thermal simulation framework [152]. This presented model based on a Successive Node Reduction (SUNRED) algorithm has been validated against a CFD software as well as realistic measurements carried out with different coolant flowrates applied to a micro-fluidically cooled 3D IC, with errors around 5%.

A large body of literature exists on design and optimization of a 3D IC microfluidic cooling in the form of analytical or numerical modeling. Such models are often validated on experimental test benches prior to fabrication [153]. For example, in one particular 3D IC design, copper TSVs integrated with microchannels at an areal density of 2500/cm^2 were shown to result in a thermal resistance of 0.24 °C/W, a significant improvement over a traditional air-cooled chip [32]. A thermal model considering the thermal wake effect combined with channel merging techniques was reported, which resulted in significant improvement in computational time within 5% of error when compared to a well-established tool based on finite volume method (FVM) [154]. Thermal wake is an effect due to drastic variation in fluid temperatures from solid surface to fully developed boundary layer region, which must be taken into consideration for a fast and accurate model to design an efficient microfluidic cooling mechanism for the 3D ICs. A thermal management technique focused specifically on hotspot management has been proposed, which used microchannels interconnected with through silicon fluidic vias (TSFVs) [153], [155]. This study reported an application of this approach to be used in handheld portable devices, since it can be used for mitigating the effect of hotspot but not necessarily for reducing the global temperature of a 3D IC. In contrast, a thermal model has been developed for non-uniform placement of

microchannels in order to mitigate the impact of localized heat generation [156], [157]. This approach accounted for microchannel placement limitations due to thermal imbalance as well as TSV complex distribution and concluded that there may be up to 80% power savings in cooling costs when optimally placed compared to uniform placement over the entire chip area. Another fast thermal model has shown around 84% savings in pumping power or reduction in thermal gradient by 38% when compared to straight microchannels [158]. In addition to such papers that focus on thermal aspects of microfluidic cooling in a 3D IC, analysis of the effect of liquid cooling on electrical parameters of TSVs has also been presented [159]. Based on studies on a micro-pin fin arrangement with distilled water as a coolant, this work recommended that TSVs must be appropriately shielded from the surrounding coolant. Figure 5 shows a schematic as well as SEM of a micropin-fin heat sink with co-axial like TSV configuration, in which a signal TSV is surrounded by multiple ground TSVs connected by an annular metal pad [159].
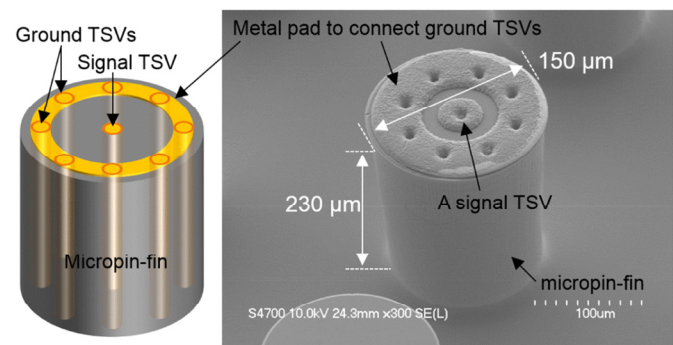

Fig. 5. Schematic and SEM image of micropin-fin with coaxial TSVs [159].

A number of mechanisms motivated by traditional heat exchanger design have been proposed for microfluidic-based cooling of 3D ICs. These include varying the arrangement of microchannels with respect to each other, modifying geometry along the coolant flow path and adding pin fins as flow restrictions to increase the contact surface area. Independent liquid cooling for each tier in a 3D IC has been investigated [160]. By addressing the power level in each tier separately, this approach was shown to reduce the junction temperature of a memory-on processor 3D IC by around 25 °C along with a reduction of junction temperature difference among neighboring tiers by around 5 °C compared to air cooling. In another thermal simulation optimization approach, channel patterning was used to diminish hotspot effects and channel pruning to reduce temperature gradient across the 3D IC [143]. When compared to the standard benchmark, 11-61% reducing in energy costs and 49-59% reduction in pumping pressure was reported. Closed form correlations for converging-diverging microchannels have been used for design microchannel cooling for 3D ICs [144]. In another study, a thermal simulator based on a clustering algorithm was developed in order to model a thermal management approach where the microchannels are arranged in the form of clusters [145]. Based on this thermal model, significant reduction in thermal variations across the IC as well as peak temperature were reported. Micro-strip fins or

ribs integrated in microchannels with variable densities have been shown to help reduce temperature variations when compared to a continuous pin fin arrangement. A numerical study has studied the impact of density of offset strip fins and variable spacing ribs, and reported a temperature difference of around 30 °C and 34 kPa of pressure losses as the highest recorded performance of their variable fin density arrangement [146]. A compact thermal model has been presented for optimization of microgaps and dimensional analysis of micro-pin fins [161]. This study reported higher convective heat transfer and thus better thermal performance with smaller pin fins in the case of non-uniform heat generation, which also reduces leakage current. In a related another numerical study of a thermal management technique for a 3D IC with microfluidic cooling, the effect of clustering the micro-pin fins was studied [147]. Even though a decrease in the peak temperature of around 8 °C was observed, it was accompanied by an increase in pumping power of around 148%, since the pin fin clustering leads to higher flow resistance. Hierarchical partitioning based thermal strategy for micro-pin fins embedded in microfluidic cooling of 3D IC has been studied. This work highlights the importance of considering TSV and metal gate placements to co-optimize the interconnect length and temperature variation along the 3D IC [162]. This analysis resulted in around 75% reduction in inter-strata temperature difference, around 25% reduction of maximum junction temperature at the expense of 13% extra cost of interconnect length. A recent study has shown that the orientation and location of fins plays a major role in terms of heat dissipating capabilities of the thermal management system [163]. This study concludes that the fins positioned near and oriented towards the hotspots makes it more efficient. On the other hand, an annular cavity micro-pin fin arrangement was tested numerically and experimentally [164]. This system has proven that it reduces the maximum chip temperature by 9 °C and thermal resistance by 34.5%, when compared to standard fully solid fins.

Two-phase cooling involving boiling of the coolant flow has been widely investigated for 3D IC cooling [42]. In general, two-phase cooling can be a promising alternative to single-phase liquid cooling due to the high heat dissipation capabilities of evaporative mechanism [30], despite several known challenges. Considering the limiting factor of critical heat flux (CHF) of the coolant, if the IC produced heat flux surpasses the CHF of coolant then the cooling mechanism might come across the possibility of dry-out due to the vapor blanket formed on the hot surface [149]. Therefore, in order to achieve the best performance out of a two-phase cooling system and to avoid damage due to sudden rise in localized hotspots, a coolant selection with CHF higher than the designed IC heat flux is recommended. A thermal model has been developed to theoretically predict the performance of flow boiling along microfluidic straight channels for 3D IC cooling [148]. This model predicts spatial temperatures in logic and memory regions based on their respective power dissipation levels, claiming peak temperature to be around 85 °C and heat dissipation capability up to 135 W/cm². Further, thermal analysis of two-phase cooling in microchannels with non-

uniform heat generation has been presented. Performance comparison with single phase cooling approach has been carried out based on their effects on TSV dimensions and interconnect densities [165]. Analysis of refrigerants such as R123 and R245ca for two-phase cooling has been carried out, showing better performance than single-phase coolants operational around 300 W/cm², in terms of reliability and suppressing the localized hotspots. A CFD analysis focused on comparison of single-phase cooling and two-phase cooling with water and R134a, respectively, has been reported [149]. This study has concluded that the two-phase cooling will be superior to single-phase cooling only in the scenario when applied heat generation is below 12 kW/m², keeping mass flow rate identical in both cases. A thermal model was proposed for an evaporative interlayer cooling system for a 3D IC, focusing on effect of hotspot placement on overall thermal management [166]. This finite-difference model showed the importance of an interlayer heat spreader for successful balance between thermal loads generated and heat dissipation in the system. Further, a compact thermal simulation tool – STEAM – was developed and validated against experimental data recorded in past studies, this iterative simulation claims that the relative error for temperature prediction for hotspots and spatial heat fluxes were around 7% and 10%, respectively [167]. A conjugate model was developed to determine fluid flow as well as heat transfer parameters for the two-phase microchannel cooling system, based on a thermal test vehicle [168]. Figure 6 depicts a general schematic of test vehicle connected to a test system [168]. From the experimental validation, it was concluded that the variations for thermal as well as fluid pressure predictions were well within an accepted range of values. A similar numerical study was carried out to observe the effect of flow boiling on microchannel pin fins with variable density, using a dielectric refrigerant HFE-7200 as a coolant [169]. Coupled multiphysics models comprising phase change and volume of fluid models have been developed; to study bubble path variations, changes in vapor quality and other thermal and fluid flow aspects due to non-uniform heat flux distribution [170] and diverging microchannels [171]. Diverging microchannels were proven to perform well under instable flow boiling conditions when compared to that of straight microchannels [171]. Further, it was also reported that compared to rectangular microchannels, zigzag microchannels help suppress flow instability and enhance heat transfer in a two-phase microfluidic cooling system[172]. Recently, an attempt of utilizing a two phase cooling system with HFO 1234ze nanofluid was carried out to maintain the maximum temperature below the designed threshold – 70 °C, this study was also validated in simulated environments along with real system comparisons [173].
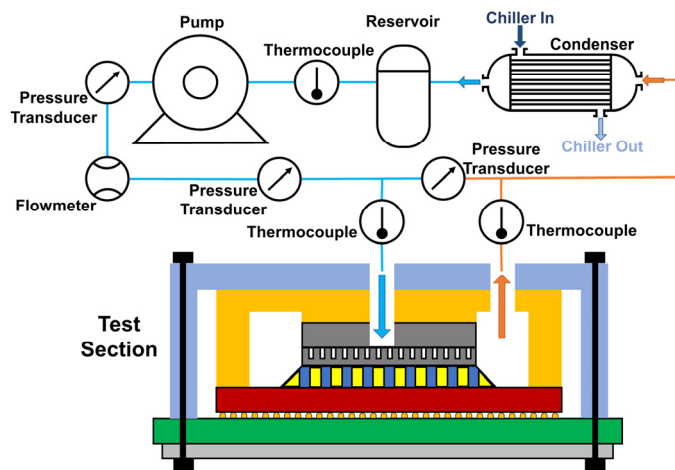
Fig. 6. Schematic of a test vehicle connected to a test system (adapted from [168]).

In addition, several papers have carried out experimental investigation of microfluidic cooling of 3D ICs, focusing on experimental parameters like coolant flow rate, thermal resistance, achievable temperatures, etc. A similar experimental study for single-phase microfluidic cooling used water at 22 °C in one case and a fluorinated fluid capable of operating at sub-ambient temperatures ranging from -40 °C to 20 °C in another case, resulting in cooling capabilities of 500 W/cm^2 and 270 W/cm^2, respectively [174]. In this work, an improvement in the thermal resistance from 15.9 °C-mm^2/W to 12 °C-mm^2/W for water-based microfluidic cooling was reported with the use of an In solder based thermal interface material (TIM) instead of a silver epoxy layer. Further, experimental estimation of thermal performance of microfluidic cooling in 3D IC was carried out in comparison with an air-cooled system. The two competing approaches were tested against different combinations of arrangements and power levels [175]. A significantly lower thermal resistance for microfluidic cooling was reported compared to air cooling of the 3D IC (8 °C-mm^2/W vs. 55 °C-mm^2/W). Moreover, to mitigate the complexities of etching microchannels onto the backside of a thin silicon substrate, an alternative approach was suggested in which, backside cooling is combined with a microchannel integrated add-on die considering the localized hotspots [176]. Direct contact of coolant with the chip backside resulted into a viable alternative to complicated silicon etched microchannels. Thermal resistance of 28 °C-mm^2/W with temperature difference of 55 °C for 20 W power dissipation was reported. Additional experimental study was proposed which focused on the thermal performance of silicon integrated micro-pin fin arrays and its comparison with that of conventional microchannels [177]. The convective heat transfer coefficient was measured to be 18.2 kW/m^{2}K and validated with numerical analysis carried out in ANSYS Fluent. An experimental study was carried out with a microfluidic cooling system having arrays of micropin fins, which suggested to operate the flow conditions keeping Reynolds number below 300 after validating the experimental results with standard correlations [178].

In addition to microfluidic liquid cooling, the use of thermal through-Silicon vias (TTSVs) has also been widely

investigated. In contrast with microfluidic cooling, TTSVs offer passive thermal management, even though there may still be significant space constraints associated with TTSVs [179], [180]. In addition, isolation of critical IC components from high heat generation in the surrounding [181], [182] and use of high thermal conductivity materials for effective heat dissipation [183], [184] has also been reported. Thermal through silicon vias (TTSVs) are also considered as an effective way of heat dissipation by improving the heat transfer path from hotspots to the heat sink with implementation of techniques like placing TTSVs in an efficient arrangement using a thermal simulation [179], using redistribution layer along with TTSVs in the 3D IC silicon-oxide interlayers [180], etc.

It has been reported that the use of Copper as the TSV material improved vertical heat transfer across stacked chips compared to conventional TSVs [36]. In this study, an empirical equivalent relationship for the heat transfer effect of TSVs in 3D ICs has been proposed. In a related work, equivalent models of 3D ICs with TSV-integrated interposer was developed. Specifically, equivalent anisotropic thermal conductivity value were determined for copper-TSV interposer with SiO2 lining [185]. Moreover, a switching algorithm for the signals transmitted via TSV clusters has been developed with the goal of distributing heat generation uniformly over the chip area and suppress hotspots[186]. Experimental validation of a thermal finite-element model was carried out on a 3D IC test chip featuring Cu-Cu bonds and TSVs [187].

The effects of TSV placement and various associated trade-offs have also been widely researched. Much of the literature in this direction has already been covered in Section 3. In the specific context of thermal dissipation through TSVs, thermally-aware TSV placement and corresponding logic cell positioning has been recognized to be an important design process to enable a high thermal conductivity path for heat dissipation [37], [78] and optimizing lateral heat transfer [188].

Several other approaches for thermal management related to TTSVs have also been explored. For example, graphene-based TTSVs and heat spreaders have been explored through simulations [189]. This proposed analysis has concluded that even if the CNT-based 3D IC structure is thermally superior to graphene [163], yet graphene-based finned TTSV structure may be preferred when higher interconnecting signal integrity is required. Since no experimental work was reported, the practical feasibility of incorporating graphene in the process flow remains to be established. Whereas, a study based on the Nano-Engineered Computing Systems Technology (N3XT) stated that the carbon nanotube field-effect transistors (CNFETs) performs well in thermal as well as electrical aspects of a monolithic 3D IC with higher electron mobility and good control over charge carrier concentration [190]. Other graphene-related aspects have also been reported, including the use of graphene as an efficient heat spreader [183], an interlayer in the form of multilayered graphene nanoribbons [191] or a thermal interface material [184]. These studies have claimed that graphene may significantly enhance heat dissipation, even when used in small quantities [183], [184]. Heat dissipation using additional components integrated with 3D IC such as

thermally conductive sidewalls, interchip or bottom plates has also been reported [192]. An improvement of around 40% compared to a conventional 3D IC integrated with heat sink only has been reported. Replacement of conventional TSVs with simple copper wires and solders across through silicon hole (TSH) interposers has been investigated [193]. Improved thermal cycling and electrical performance of 3D ICs was reported with the use of TSH interposers on a fabricated test vehicle, in which, the etched TSV is used for passing solid wire connections instead of being plated with metal. Figure 7 displays the SEM cross-sectional image of the SiP which includes most of the key components like TSH interposer, PCB, package substrate, top and bottom chip, etc. [193].
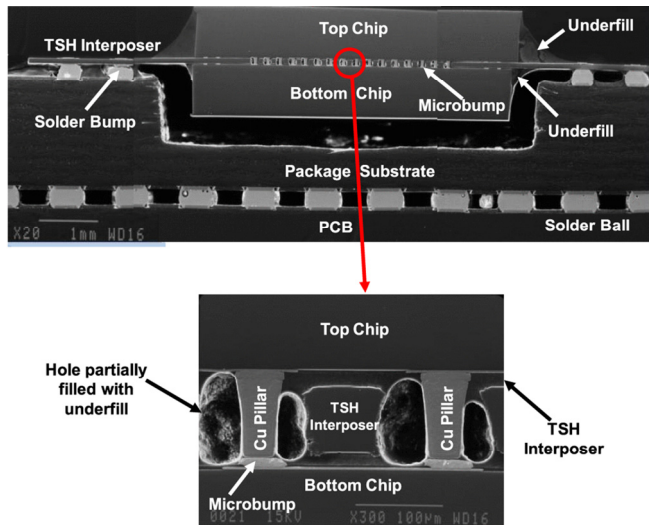

Fig. 7. A cross-sectional SEM image of the SiP [193].

On the other hand, a concept of thermally isolating the sensitive IC components like DRAM from high-power heat generating devices on chip was also developed. This concept has achieved the thermal isolation by implementing vacuum gaps in combination with non-contact chip-to-chip communications [181], this study reported that the vacuum gaps enables the DRAM to operate at a temperature 47 °C lower than that of the conventional system. Another study includes arrangement of the TSVs in the shape of a ring around the device to be shielded from surrounding heat generation [182], and successfully suppresses thermal coupling in a highly complex 3D IC structures.

Several hybrid thermal management approaches have also been investigated for 3D ICs, with the motivation of taking advantage of synergies that may exist between individual cooling mechanisms For example, the performance of microfluid cooling in conjunction with thermal through silicon vias (TTSVs) as a hybrid heat dissipation system has been investigated [38], [194]. While TTSVs help improve the capability of vertical heat conduction, microfluidic cooling helps remove heat from the 3D IC structure using a heat transfer liquid as a heat carrier. This study claimed that the proposed hybrid system performs better than their individual mechanisms and achieves 56% savings in pump energy while maintaining higher heat dissipation capabilities [194]. Similar studies of hybrid thermal management combining microfluidic cooling

and TTSVs have also reported similar enhancement in cooling performance of the system, either through numerical models [195], [196] or by fabrication and measurements on a customized experimental setup [197]. In another related study, thermal-electrical co-design of TSVs and microchannel cooling using micropin fin heat sink has been described [39]. Figure 8 shows a picture of the TSV arrangement with micropin fin heatsink setup in this work [39]. An optimum design for micropin fin dimensions, TSV configuration and coolant flow rate was carried out, resulting in 33% reduction in peak temperature in the circuit compared to a conventional air-cooled heat sink. A key challenge in such hybrid approaches is in accommodating a large number of TSVs in the 3D IC along with efficient microchannel arrangements. Towards this, the feasibility of replacing TSVs with wireless interconnects has been explored [198]. This study has claimed greater efficiency in data communication as well as energy consumption using wireless interconnects compared to traditional TSVs.

Further, a thermally active interposer along with microfluidic cooling has been proposed. It has been claimed that this approach of embedding microfluidic channels into the silicon interposer can minimize the number of layers of thermal interlayer materials used [199]. Similar studies on experimental measurements on a fabricated test vehicle have been reported to confirm the effectiveness of silicon interposers with TSV integrated microfluidic cooling [200] or micropin fin heatsink [201]. These measurements have shown that silicon interposer with microfluidic cooling has good thermal isolation between layers compared to conventional air cooling. Another method for thermal isolation of 3D ICs using air gaps integrated in the microfluidic cooling along with a copper-spreader acting as a thermal bridge has been proposed [40], [202]. Using air gap isolation, this method claimed to reduce the peak temperature by 38.9 °C compared to a conventional design with just underfill and microbumps. An extension of this work was carried out by including mechanically flexible interconnects along with the air gap arrangement [203], based on which, a 35.9% reduction in junction temperature of low power tier was achieved when compared with the conventional microbump-underfill based design. Additionally, implementation of microgaps in conjunction with variable pin fin arrangements integrated in a single-phase microfluidic cooling system has been proposed. Experimental investigation of this approach and comparison against a comprehensive numerical model has been reported [204]. This paper claimed that the hotspots can be suppressed by using a deionized water at 21.3 °C as coolant and thus, keeping the maximum temperature below 65 °C and maintaining pressure drop along the microchannels in acceptable range.

The decision of which thermal dissipation technique to implement for a certain 3D IC must account for a variety of considerations, including the nature and complexity of the 3D IC, number of chips, powermap, reliability and other characteristics, as well as cost. Custom requirements for niche applications such as military electronics must also be taken into consideration.
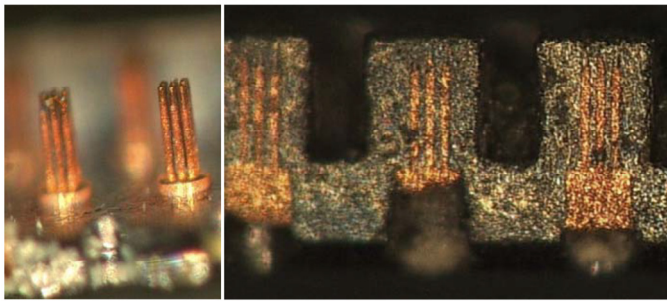
Fig. 8. TSV arrangement with micropin fin heatsink setup [39].

V. FUTURE OUTLOOK AND KEY CHALLENGES

Despite much technological advances in multiple directions related to thermal management of 3D ICs, as summarized in sections above, several technological challenges still remain. Some of these challenges are related to fundamental physical processes, while others are related to implementation of 3D ICs for various applications.

There continues to be a need for analytical models for heat transfer in 3D ICs that may be easily integrated with other tools for rapid temperature computation. This may help in both pre-Silicon design as well as run-time performance optimization. Numerical simulation-based temperature computation is not appropriate for this purpose, since simulations often require commercial software to run on. In contrast, closed-form analytical solutions can be easily integrated with other codes. When such analytical solutions are available in a complicated form, such as an infinite series solution, a study of the trade-offs between accuracy and computation cost will be helpful. Benchmarking of such analytical solutions for temperature distribution with experimental measurements is also likely to be of much practical importance.

Microfluidic cooling is one of the most promising thermal management techniques for 3D ICs. There remain several key technological challenges associated with microfluidic cooling that must be addressed before the technology can be made mainstream. From a scientific perspective, understanding and optimally making use of the physics of liquid-to-gas phase change processes for improved heat removal is crucial, including in scenarios such as thin film evaporation. More work is needed on the integration of microfluidic cooling with electrical functions of the 3D IC, and in the use of enhanced surfaces such as micropin fins, offset strip fins, etc. Practical challenges such as dynamic reallocation of microfluidic cooling resources to various tiers on a 3D IC in response to load changes must be understood and addressed. Long-term reliability of microfluidic cooling needs to be better understood. It needs to be fully understood if microfluidic cooling might cause enhancement in existing failure mechanisms or cause entirely new ones. Droplet-based microfluidics, which is being investigated widely for analytical biochemistry, may also be useful for thermal management of 3D ICs [205]. Another promising technology is related to thin film evaporative cooling. In addition to fluids-based cooling, other novel thermal management mechanisms must also be investigated. In particular, solid-state cooling technologies such as

thermoelectric cooling, while difficult to implement in a 3D IC, offer a key advantage of no moving parts or moving fluid compared to microfluidic cooling. New materials innovations and investigation of compatibility with existing materials are needed.

Microfluidic cooling can handle higher heat fluxes even under low pressures if the microchannel height is not limited due to maximum TSV height, since longer TSVs leads to higher signal latency. Additionally, high pressure drop is a key challenge with microfluidic cooling, which also results in undesirable mechanical stress. Practical approaches may be needed for addressing such challenges, such as optimizing the flow path, using hydrophobic film on inside surface of microchannels, etc. Such substantial pressure drops along the flow length also affects the saturation temperature of the coolant in a two-phase microfluidics cooling system, which results in objectionable interrupted flow behavior.

Localized overheating commonly known as hotspot is one of the prominent issues in 3D ICs, which causes temperature non-uniformity across the chip and makes thermal management difficult with conventional IC cooling techniques. Dynamic hotspot prediction with the help of efficient thermal modelling techniques remains a critical challenge for 3D IC thermal design and run-time performance management. Considering white space allocation, i.e., TSV placement and wirelength reduction in terms of 3D IC floorplanning is a vital practice to be followed. TSVs assist the heat dissipation if placed efficiently, achieving higher electrical performance along with excellent heat removal. Much work has been carried out on development of design and computation tools that combine electrical and thermal features. As thermal management technologies evolve, such tools need to be updated in order to accurately model such new thermal management approaches.

The Through-Silicon Via continues to be central pillar of 3D IC technology. Despite extensive work reported on the dual role of TSVs for thermal and electrical conduction, more work can be done to fully utilize the dual capabilities of a TSV. Theoretical modeling of the dual functions of a TSV is of much interest, as it may help understand the fundamentals of this challenging, multi-physics problem and drive co-optimization.

Mechanical stress generation in a 3D IC due to thermal gradients and dissimilar thermal coefficient of expansion of TSVs and silicon substrate remains a key practical challenge. The induced mechanical stress is influenced by a variety of factors, including material selection, TSV dimensions, pitch sizes and overall floorplanning strategy. In addition to reliability, mechanical stress may also negatively impact signal transmission, redundant power dripping and circuit timing. Increasingly accurate stress prediction tools need to be developed and used closely with other design tools.

Lately, there is a growing interest in monolithic 3D (M3D) integration to produce more efficient ICs having lower signal delay and reduced electrical interference [206], [207]. Looking at this IC fabrication method as a potential candidate for future vertically stacked complex ICs; multiple efforts have been observed in the recent literature to enhance the overall aspects, mostly electrical, and to mitigate the current issues of the M3D

integrations [190], [208]–[211]. However, there is very limited amount of research work available discussing thermal issues and their remedies in M3D integrations.

In general, early insertion of thermal management into the 3D IC design process is critical, similar to traditional ICs. This will ensure early recognition and identification of thermal management challenges that may arise in next-generation 3D ICs and help thermal management keep up with rapid advances in the manufacturing and packaging of 3D ICs expected in the coming years.

VI. CONCLUSIONS

3D ICs have attracted a considerable volume of research literature in a variety of sub-disciplines within electrical, computer and mechanical engineering. This review paper summarizes key developments pertaining to heat transfer in 3D ICs. The overall goal of this paper has been to summarize key research developments reported in the areas of thermal modeling, thermal-electrical co-design and thermal management of a 3D IC. It is expected that the summary of current state-of-the-art, as well as the discussion on future outlook in these areas will help researchers in academia and industry working on these and related challenges pertaining to 3D ICs.

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