Mod10Counter

CODE:

```
`timescale 1ns / 1ps
module mod10counter(
input clk, rst,
output reg [3:0] count);
always@(posedge clk)begin
   if(rst)
      count<=4'b0;
   else begin
      if (count == 4'b1001) // Reset after reaching 9 (1001)
         count <= 4'b0000;
      else
         count <= count + 1'b1;
   end
end
endmodule
```