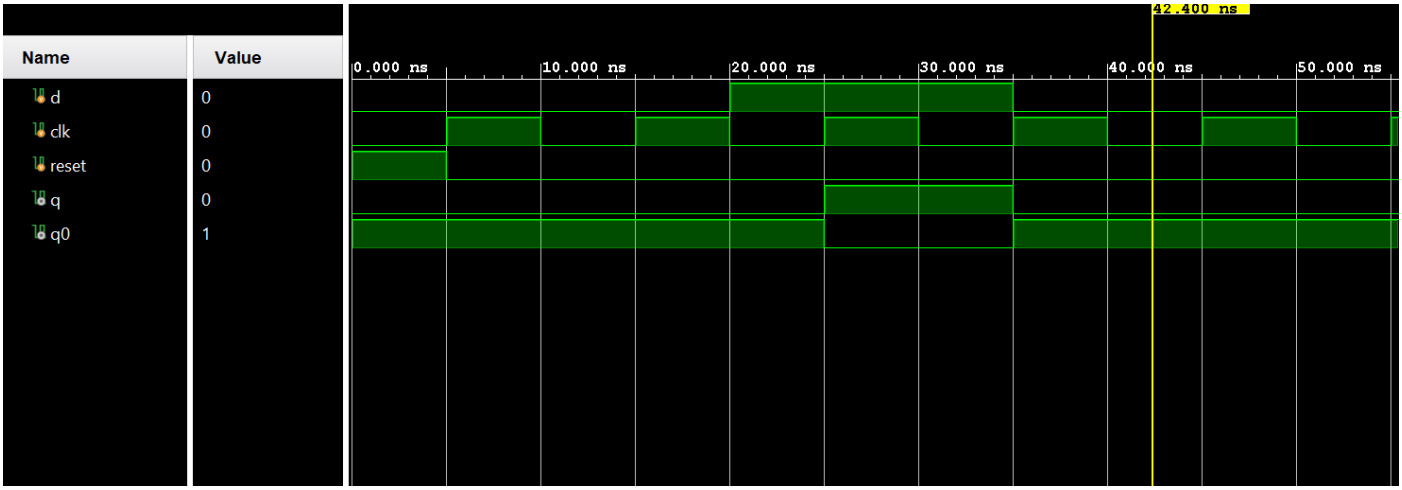
Design a D flip-flop with asynchronous reset.

CODE:

```
`timescale 1ns / 1ps
module dff(
input d, clk, reset,
output reg q,
output q0);
always@(posedge clk or posedge reset)begin
   if(reset)
      q<=0;
   else
      q<=d;
end
assign q0 = ~q;
endmodule
```

TESTBENCH:

```
`timescale 1ns / 1ps
module dff_tb();
reg d, clk, reset;
wire q, q0;
dff uut(d,clk,reset,q,q0);
initial begin
   clk = 0;
end
always #5 clk = ~clk;
initial begin
   reset = 1;
   #5 reset = 0;
end
initial begin
   d = 0;
   #20 d = 1;
   #15 d = 0;
end
initial begin
   $monitor("Time: %0t | d: %b | clk: %b | reset: %b | q: %b | q0: %b",
            $time, d, clk, reset, q, q0);
end
endmodule
```


Name
Value
d
0
clk
0
reset
0
q
0
q0
1
42.400 ns
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns