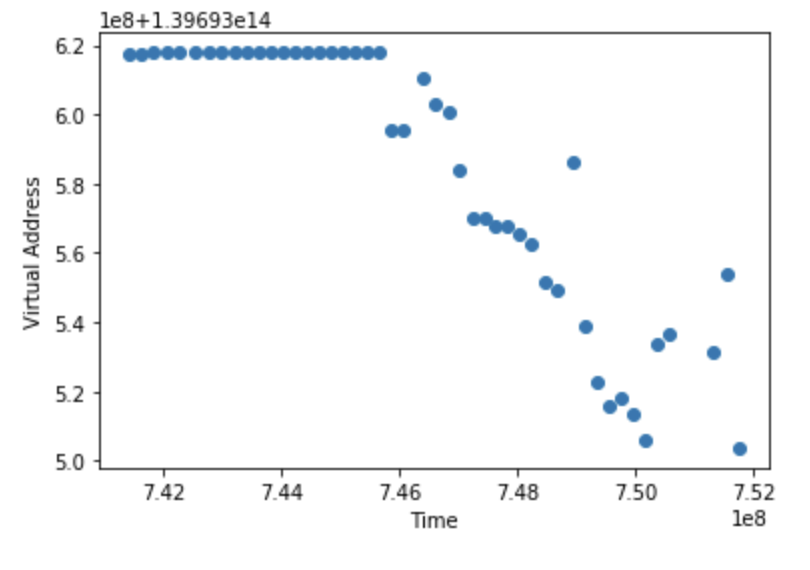
Observations:

1. Custom page fault application: it accesses memory alternatively between the initial address and max address. As a result, we can see the plot has page faults distributed over the ends.

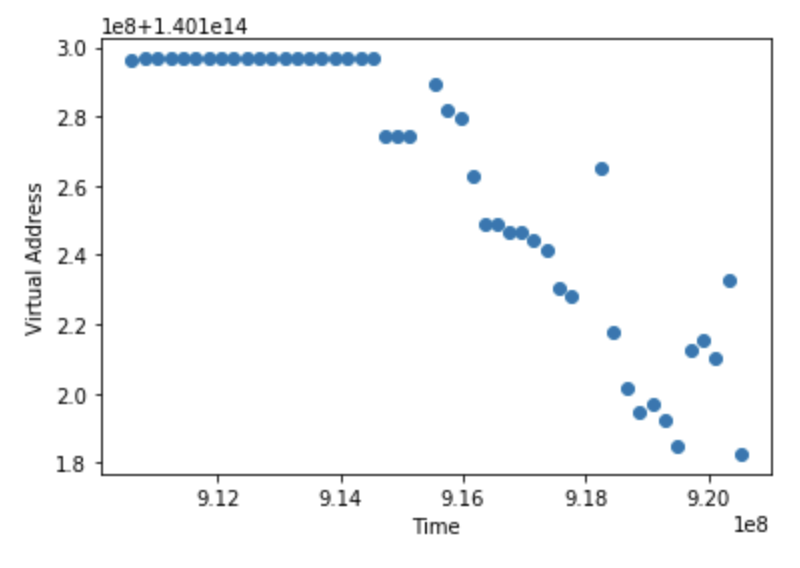
A screenshot of a cell phone

Description automatically generated

1. Sysbench CPU: Initially the page fault is created when it first accesses at 6.2. Then the memory is accessed at a different location and then a page fault is created at that location and the memory is accessed in this pattern. Therefore, there are page faults distributed at different locations when memory accesses are done near the virtual address 6.2 back and forth.



1. Sysbench memory: This graph is also similar to the previous pattern but with slightly different locations.



1. iPerf Network: This is a I/O network test and the graph shows the the page faults are very few indicating the memory accesses are mostly successful and are within the memory.

