228W1A0424

Electronics and Communication Engineering
B.Tech
Velagapudi Ramakrishna Siddhartha Engineering College, Vijayawada

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GitHub Profile
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Objective

Driven Electronics and Communication Engineering student with hands-on experience in RTL design, FPGA-based system implementation, and digital verification. Seeking a challenging role in VLSI design to apply my skills in HDL programming, low-power digital architectures, and ASIC development while contributing to high-performance semiconductor solutions.

Education

- **Velagapudi Ramakrishna Siddhartha Engineering College** *2022- Present*
  B.Tech-ECE Vijayawada, India
  - CGPA: 8.80
- **SRI Bhavishya Jr College** *2020-2022*
  Intermediate Vijayawada, India
  - Percentage: 95.1%
- **Sri Chaitanya School** *2020*
  Secondary Education Vijayawada, India
  - Percentage: 100%

Projects

- **Design and Implementation of Low-Power Approximate Multipliers** *March 2025*
  Presented conference at SRM EPIC 2025
  - Tools & Technologies Used: Xilinx Vivado, Nexys-4 DDR FPGA.
  - Developed an 8-bit low-power approximate multiplier using a novel 4:2 compressor with an error-correction module, reducing hardware complexity while maintaining $< 0.5\%$ error. Achieved 9% dynamic power, 87% static power, and 31% LUT reduction on FPGA, demonstrating high SNR/PSNR for image-processing and IoT applications.
- **Implementation of 4:2 Compressor-Based Approximate Multipliers in Image Processing Applications** *Oct 2025*
  Tools & Technologies Used: Vivado, MATLAB
  - Developing a 4:2 compressor-based approximate multiplier for low-power image processing, integrating MATLAB-to-Vivado workflow for pixel-level accuracy evaluation.
  - Achieves high visual fidelity (PSNR > 45 dB) while reducing computational complexity, making it suitable for embedded and portable vision systems.
- **Design, Synthesis, and Physical Implementation of a 32-bit Wallace Tree Multiplier** *Jun 2025*
  Tools & Technologies Used: Synopsys (VCS, Verdi, Design Compiler)
  - Designed and implemented a 32-bit Wallace Tree Multiplier, performing RTL coding, synthesis, and timing optimization using Synopsys Design Compiler.
  - Executed floorplanning, placement, routing, and STA to analyze area, delay, and power trade-offs, achieving an optimized physical design.

Internship

VLSI Design Intern May 2025 – June 2025 (6 Weeks)
Siddhartha Academy of Higher Education, Vijayawada
ChipIN & MeitY – Chips to Startup (C2S) Programme

- Worked on RTL design and verification of combinational and sequential digital circuits such as adders, multiplexers, ALUs, and FSMs using Verilog.
- Implemented and tested a 32-bit Ripple Carry Adder (RCA) and Wallace Tree Multiplier, followed by synthesis and physical design using Synopsys Design Compiler and IC Compiler II.
- Completed the full digital physical design flow: floorplanning, power mesh creation (M1, M6–M8), placement, clock tree synthesis (CTS), routing, timing closure, and congestion optimization.

- Performed simulation, debugging, and functional verification using Synopsys VCS and Verdi, ensuring correctness and clean verification reports.
- Designed basic analog circuits (such as CMOS inverter and differential pair) and performed layout creation, DRC/LVS checks, and parasitic analysis using Cadence Virtuoso.
- **Tools Used:** Synopsys VCS, Verdi, Design Compiler (DC), IC Compiler II (ICC2), Cadence Virtuoso.

Skills

- **Programming Languages:** C, Verilog, Python, SystemVerilog (Basics)
- **Tools & Software:** Cadence (Genus, Virtuoso), Synopsys (VCS, Verdi, Design Compiler), Vivado, MATLAB
- **VLSI Design Skills:** RTL to GDSII Flow, Analog Layout Design

Publications

- **Conference Paper:** "Design and Implementation of Low-Power Approximate Multipliers" (Under Review)
  2nd International Conference on Electronic & Photonic Integrated Circuits (SRM EPIC-2025).

Positions of Responsibility

- **Placement Cell Volunteer, ECE Department** 2023-Present

Achievements

- **Presented a conference paper**
  2nd International Conference on Electronic & Photic Integrated Circuits (SRM EPIC-2025).
- **Ist Prize in Technical Event, UTSAV 2025**

Certifications

- **ASIC Verification using System Verilog (SV)** Oct 2025
  Udemy
- **VLSI Course** Nov 2025
  Simplilearn

Personal Skills

- **Communication Languages:** English,Telugu, Hindi
- **Hobbies:** Reading books, Drawing

Declaration

I hereby declare that the information provided above is true and correct to the best of my knowledge and belief.