Swathi Changalarayappa

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EDUCATION

TEXAS A&M UNIVERSITY
MS in Computer Engineering
May 2019 | College Station, TX
Cum. GPA: 4.0 / 4.0

NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA, SURATHKAL
BTech in Electronics and Communication Engineering
May 2014 | Surathkal, India
Cum. GPA: 8.33 / 10.0

COURSEWORK

GRADUATE
Computer Architecture
Microprocessor Systems Design
Digital Integrated Circuits Design
Artificial Intelligence
Analysis of Algorithms

UNDERGRADUATE
Digital system design
Linear integrated circuits
VLSI design
Logic synthesis and techniques
VLSI design and automation

SKILLS

PROGRAMMING
Verilog • VHDL • C • C++ • TDL • Python • Perl • TCL

TOOLS
Cadence NCSIM • Magillem • Spyglass Atrenta • Autogen • MATLAB

EXPERIENCE

TEXAS INSTRUMENTS | Design Engineer
July 2014 – July 2017 | Bangalore, India

Architecture
- Analyzed architecture of instruction cache based on misses, cycle dependencies and area
- Active interaction with architects in computing early RTL based power using Cadence Joules
- Analyzed performance of system using industrial benchmarks such as Coremark and Dhrystone

Design and Verification
- Performed CPF based low power functional verification at RTL and gate level verification of SOC, released to production
- Designed glue-logic using verilog enabling expected functionality between IPs at SOC in verilog
- Gained expertise in IPXACT 1685 standards while integrating IPs using Magillem tool
- Achieved high quality SOC RTL handoff to synthesis team using spyglass Lint tool
- Performed logic equivalence check between RTL and synthesis/post-layout netlists

Methodology Development and Improvement
- Verified isolation correctness using checkers for low power designs
- Identified automated checks to enable quality IP RTL handoff to SOC

TEXAS INSTRUMENTS | Intern
May 2013 – July 2013 | Bangalore, India
- Improved simulation time by 40% by performing Checkpoint simulation at SOC, method of creating snapshot using Cadence NCSIM simulator

PROJECTS

Perceptron based cache reuse prediction for LL cache in C++
November 2017 | Texas A&M University
Implementation of dead block prediction in last level caches. Speedup acheived: 6.4%

ITTAGE - Indirect branch predictor in C++
October 2017 | Texas A&M University
Implementation of ITTAGE to predict indirect branch target lowering MPKI by 93%

DWT based image compression
November 2013 | NITK Surathkal
MATLAB and verilog implementation of DWT for image compression as a trade off between compression and quality

Elevator design on Spartan FPGA
November 2012 | NITK Surathkal
Verilog implementation of elevator control system for 4 floors with power conservation and safety features