

Swathi Changalarayappa

<https://swathic5.github.io/> | <https://www.linkedin.com/in/swathi-c/> | https://github.com/swathic5swathi_c@tamu.edu | 979.571.2681

EDUCATION

TEXAS A&M UNIVERSITY

MS IN COMPUTER ENGINEERING
May 2019 | College Station, TX
Cum. GPA: 4.0 / 4.0

NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA, SURATHKAL

BTECH IN ELECTRONICS AND COMMUNICATION ENGINEERING
May 2014 | Surathkal, India
Cum. GPA: 8.33 / 10.0

COURSEWORK

GRADUATE

Computer Architecture
Microprocessor Systems Design
Digital Integrated Circuits Design
Artificial Intelligence
Analysis of Algorithms

UNDERGRADUATE

Digital system design
Linear integrated circuits
VLSI design
Logic synthesis and techniques
VLSI design and automation

SKILLS

PROGRAMMING

Verilog • VHDL • C • C++ •
TDL • Python • Perl • TCL

TOOLS

Cadence NCSIM • Magillem •
Spyglass Atrenta • Autogen •
MATLAB

EXPERIENCE

TEXAS INSTRUMENTS | DESIGN ENGINEER

July 2014 – July 2017 | Bangalore, India

ARCHITECTURE

- Analyzed architecture of instruction cache to improve performance by 21% for industrial benchmarks Coremark and Dhrystone
- Estimated RTL based power using Cadence Joules to determine power/performance trade-off for cache configurations

DESIGN AND VERIFICATION

- Performed CPF based low power functional verification at RTL and gate level verification of SOC, released to production
- Designed glue-logic using verilog enabling expected functionality between IPs at SOC level
- Gained expertise in IPXACT 1685 standards while integrating IPs using Magillem tool
- Achieved high quality SOC RTL handoff to synthesis team using spyglass Lint tool
- Performed logic equivalence check between RTL and synthesis/post-layout netlists achieving 0 bugs

METHODOLOGY DEVELOPMENT AND IMPROVEMENT

- Verified isolation correctness using checkers for low power designs leading to 0 isolation bugs on production chip
- Identified automated checks to enable quality IP RTL handoff to SOC

TEXAS INSTRUMENTS | INTERN

May 2013 – July 2013 | Bangalore, India

- Improved simulation time by 40% by performing Checkpoint simulation at SOC, method of creating snapshot using Cadence NCSIM simulator

PROJECTS

PERCEPTRON BASED CACHE REUSE PREDICTION FOR LL CACHE IN C++

November 2017 | Texas A&M University

Implemented dead block predictor for last level caches. Speedup achieved: 6.4%

ITTAGE - INDIRECT BRANCH PREDICTOR IN C++

October 2017 | Texas A&M University

Implemented ITTAGE to predict indirect branch target improving performance by 93%

HARDWARE SOFTWARE CO-DESIGN

November 2017 | Texas A&M University

Developed a device driver in Linux to decode and display IR signal using Xilinx FPGA

ELEVATOR DESIGN ON SPARTAN FPGA

November 2012 | NITK Surathkal

Realized elevator control system for 4 floors with power conservation and safety features on Spartan FPGA