SWATHI CHANGALARAYAPPA

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OBJECTIVE

Seeking an internship for Summer 2018 in areas of frontend VLSI design/verification and computer architecture

EDUCATION

Texas A&M University, College Station, Texas May 2019
Master of Science in Computer Engineering
First semester student

National Institute of Technology Karnataka, Surathkal May 2014
Bachelor of Technology in Electronics and Communication Engineering
GPA: 8.33/10

EXPERIENCE

Design Engineer - Texas Instruments, Bangalore, India July 2014 - July 2017

Design and Verification

· Successfully performed CPF based low power functional verification at RTL and gate level verification of SOC, which was released to production
· Designed glue-logic to enable expected functionality between IPs at SOC
· Gained expertise in IPXACT 1685 standards while working on integration using Magillem tool
· Generated multi-master multi-slave bus matrix using ARM AMBA kit
· Achieved high quality SOC RTL handoff to synthesis team using spyglass Lint tool
· Performed logic equivalence check between RTL and synthesis/post-layout netlists

Architecture

· Performed architecture analysis based on hits/misses, cycle dependencies and area for instruction cache
· Assisted architects in computing early RTL based power using Cadence Joules to decide upon the cache configurations according to system requirements
· Analyzed performance of system using industrial benchmarks such as Coremark and Dhrystone

Intern - Texas Instruments, Bangalore, India May 2013 - July 2013

· Improved the simulation time by 40% using Checkpoint simulation, a method of creating a snapshot using Cadence NCSIM simulator

TECHNICAL STRENGTHS

Languages	C, Verilog, VHDL, TDL, Perl, Tcl, Python
Tools	MATLAB, Autogen, Magillem, Cadance NCSIM, Spyglass Atrenta

PRESENTATIONS

· Paper on "A formal approach towards early RTL quality checks" during Cadence Club Jasper conference
· Poster on "Smart walking stick for the blind" during Texas Instruments, Analog Design Contest

ACADEMIC PROJECTS

· Performed physical layout of 4-bit complex number multiplication using Booth-Wallace algorithm
· Designed a Discrete Wavelet Transform(DWT) based image compression tool using MATLAB and Verilog
· Designed a 2 level super scalar processor using Verilog by ensuring appropriate halting during dependencies
· Implemented 4 floor elevator control system on Xilinx FPGA. Enhanced system for energy efficiency and safety

ACTIVITIES

Joint Convenor - The Artists' Forum, NITK Surathkal July 2010 - May 2014

· Led a team of 50 students during two major art projects - 3D art and wall graffiti
· Chaired the Fine Arts Committee of Annual Cultural fest, Incident - 2014