ECEN 5803- Mastering Embedded System Architecture

Homework set 4

Due Date: 2021/11/08

Theory and Analysis:

1. **Memory Addressing**
   a. Design the asynchronous non-multiplexed bus interface between a Spansion S29GL128SFLASH memory and TI AM3358 MPU, by consulting datasheet and reference manuals for both.
   b. Draw the connections between the devices, showing connections to the FLASH chip select CE#, write enable WE#, output enable OE#, write protect WP#, RESET#, address bus A0-A22 and data bus DQ0-DQ15 from the processor. You may use a CAD tool, or draw the schematic for the 2 chips by hand.
   c. Draw the timing diagram for a read cycle, showing the FLASH chip select CE#, write enable WE#, output enable OE#, address bus A0-A22 and data bus DQ0-DQ15signals. Assume the processor runs at 100 MHz for the GPMC FCLK clock.
   d. From the timing diagram, determine the number of wait states required and write it here:
      _____
   e. List the configuration registers that must be determined and programmed in the AM3358 for this interface to work.

2. **Baud Rates**
   a. What is the difference between a bit rate and a baud rate? Give an example in which they are not the same.

   b. If you are operating with a system clock of 8.000 MHz +/- 0.01 %, at what baud rates can a divide by n baud rate generator provide reliable communication for a UART? Work your way down from a baud rate of 921600. Determine n, the divider for 3 common baud rates using this clock.

3. **Saturating Arithmetic**
   The ARM Cortex-M4 has saturating arithmetic assembly language functions, which should give it a performance advantage when doing math compared to the M0+. This type of math is useful in general, but also particularly when implementing block floating point. In saturating arithmetic, any overflow is set to the maximum allowable value and any underflow is set to the lowest value. The question is, does the compiler make use of these special assembly language instructions?
   a. Implement in C a function(s) to do saturated unsigned addition for 8, 16, and 32 bit numbers. Compile this for both the M4 (ST) and M0+ (Freescale). Compare the code size of the compilations. Which is smaller?
   b. Repeat (a) for saturated unsigned multiplication.
   c. Repeat (a) for saturated signed subtraction.

4. **Saturating Arithmetic**
   Implement C-callable assembly language functions to do saturated unsigned addition for 8, 16, and 32 bit numbers. Make use of saturated instructions. Compile this for the M4 (ST), and note the code size of the compilation. Repeat for saturated unsigned multiplication and signed subtraction.

5. **Saturating Arithmetic**

Test your functions in the previous 2 problems with these numbers:

a. Addition: 0x80+0x80, 0x00+0xFF, 0xFF+ 0xFF, 0xF1+0x0F, x8000+0x8000, 0x000F+0xFFF0, 0xFFFF+0xFFFF, 0xFFF1+0x000F, 0x80000000+0x80000000, 0xFFFFFFF1+0x0000000F
b. Multiplication: 0xFF x 0x02, 0xFF x 0x01, 0x0F x 0x0F; 0xFFFF*0x0002, 0xFFFF x 0x0001, 0x00FF x 0x00FF, 0xFFFFFFFF x 0x00000002, 0xFFFFFFFF x 0x00000001, 0x0000FFFF x 0x0000FFFF
c. Subtraction: 127-128, 127-127, -127 – (-127), 127 – (-128); 32767-32768, -32767 – (-32767), 32767 – (-32768)

Book Questions: Review 4.3, 4.21, 4.23, 18.3

Problems: 4.1, 18.1

Review 4.3 What are the two major categories of memory device that are utilized in embedded applications?

Review 4.21 What kinds of information are typically identified in a memory map?

Review 4.23 What kinds of memory devices would one typically find in each of the categories in the memory hierarchy discussed in the chapter?

Problem 4.1 A memory system is needed in a new design to support a small amount of data storage outside of the processor. The design is to be based on the 16 K bit CY7C128A SRAM organized as 2 K x 8.
(a) Provide a high-level block diagram for such an interface. (b) Provide a high-level timing diagram for the interface to the SRAM from the microprocessor, assuming that separate address and data busses are available. Define any control signals that may be necessary. (c) Design the interface based on the timing diagram from part (a). (d) Analyze the memory performance for a write and a read operation of 1, 10, and 100 bytes.

Review 18.3 What are the primary signals that comprise the EIA-232 interface standard? Give a brief description of each and its function in a data exchange.

Problem 18.1 The chapter discusses four different, commonly used, networked architectures. The Electronic Industries Association (EIA) specifies a number of others that can be found as part of various embedded applications. Three of these include the EIA-422, 423, and 485 architectures.
How are these different from the four models discussed in this chapter?
Where might such models be used in an embedded application?

Grading Rubric

1) [10 points]
   a) Correct wiring connections - 3
   b) Timing Diagram correct – 3
   c) Correct number of wait states - 2
   d) Registers correct - 2
2) [8 points]
   a) Good example - 3
   b) Correct Table - 5
3) [4 points] Saturated.c code
4) [3 points] Saturated Assembly code
5) [3 points] Saturate Test Results correct
6) [3 points] each Problem question from the book.
7) [1 point] each Review question from the book.