

MICROELECTRONICS TECHNOLOGY AND VLSI DESIGN



IC FABRICATION
TECHNIQUES
AND PROCEDURES
FOR FABRICATION OF
SCHOTTKY DIODE

CONTENTS

INTRODUCTION	1
ACKNOWLEDGEMENT	2
MICROELECTRONICS LAB	3
WAFER SPECIFICATION	4
CLEANING PROCESSES	5-7
OXIDATION	8-11
SEMICONDUCTOR LITHOGRAPHY (PHOTOLITHOGRAPHY)	12-29
DIFFUSION	20-24
METALLIZATION	25-31
APPLICATION OF IC FABRICATION BY MANUFACTURING SCHOTTKY DIODE	32-35
CONNECTION DIAGRAM	36
EXPERIMENTAL RESULTS	37-38
CONCLUSION	39
BIBLIOGRAPHY	40

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11/17/18



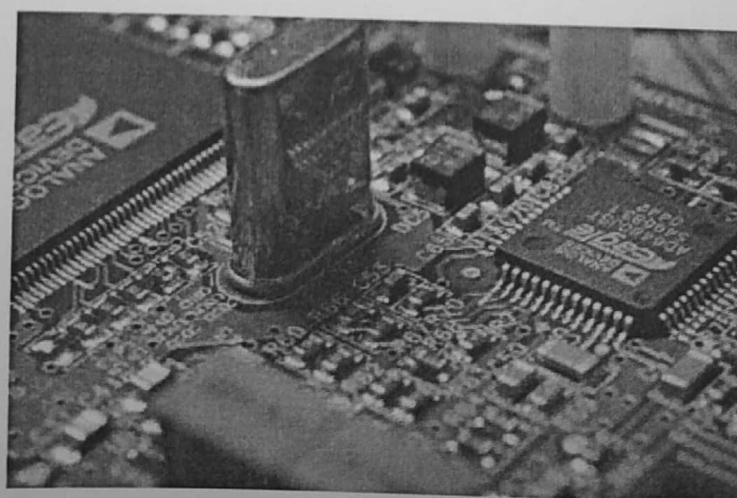
INTRODUCTION

An integrated circuit or monolithic integrated circuit (also referred to as an IC, chip, or a microchip) is a set of electronic circuits on one small plate ("chip") of semiconductor material, normally silicon. This can be made much smaller than a discrete circuit made from independent components. ICs can be made very compact, having up to several billion transistors and other electronic components in an area the size of a fingernail. The width of each conducting line in a circuit can be made smaller and smaller as the technology advances; in 2008 it dropped below 100 nanometers and now is tens of nanometers.

ICs have two main advantages over discrete circuits: (a) cost and (b) performance.

Cost is low because the chips, with all their components, are printed as a unit by photolithography rather than being constructed one transistor at time. Furthermore, packaged ICs use much less material than discrete circuits.

Performance is high because the IC's components switch quickly and consume little power (compared to their discrete counterparts) as a result of the small size and close proximity of the components. As of 2012, typical chip areas range from a mm few square millimeters to around 450 mm², with up to 9 million transistors per mm²



ACKNOWLEDGEMENT

First and foremost, we would like to congratulate Jadavpur University, for being one of the very few VLSI research centers established in India.

Secondly, we wish to express our sincere gratitude to Mr. Subir Kumar Sarkar , the course coordinator for providing us with this opportunity to explore the depths of VLSI technology.

Any teaching program must inevitably benefit greatly from interaction between students and the instructor. This has certainly been the case of the coursework on which this report is based and we owe much to all the teaching and non-teaching staffs of Jadavpur University, who had been involved in the process. In this context we would like to mention the name of Mr. ASHOKE MONDAL for guiding us throughout the course.

Finally, I acknowledge with gratitude the in-flagging support and patience of my team members, without them all these would be a distant really.

Microelectronics Lab

Micro fabrication is the process of fabrication of miniature structures of micrometer scales and smaller. we know that the radius of a dust particle is 10^{-5} cm. So, it is mandatory to keep the microelectronics lab free from dust particles. For this we have to maintain the following precautions.

- There must be 6-7 pullout type doors. Through this door when a staff enters air comes out and comparatively less dust enters.
- Staff enter and leave through airlocks (sometimes including an air shower stage), and wear protective clothing such as hoods, face masks, gloves, boots, and coveralls to protect themselves from harmful gases while fabrication.
- A basin should be there for cleaning our hands.
- In lab fan filters are installed in the ceiling ground. The air entering a lab from outside is filtered to exclude dust and the air inside is constantly recirculated through High efficiency particulate air (HEPA) and/or Ultralow particulate air (ULPA) to remove internally generated contaminants.
- Cleanrooms are classified according to the number and size of particles permitted per volume of air. There are
 - a) 10 class (10 particle exist in 1cm^2 area)
 - b) 100 class (100 particle exist in 1cm^2 area)
 - c) 1000 class (1000 particle exist in 1cm^2 area)

So, a clean bench has to be set up in the lab. Through it the air of lab comes in and passes through the micro filter.

Thus, we keep the microelectronics lab almost dust free.

Wafer specification

- Thickness of the wafer is 0.4 to 0.5 microns
- One side or both side of the wafer should be polished. Polished wafers have excellent flatness and cleanliness by polishing chemically and mechanically the wafers sliced out of silicon ingot. The external getting layer could be produced on the back surface of the polished layer.
- P+ wafers and N+ wafers have resistances of $<1\text{ohm/cm}^2$. P wafers and N wafers have resistances of $>1\text{ohm/cm}^2$.
- Diameter of the wafer must be 1" less than the furnace diameter.
- Wafer Flats:

Purpose and Function:

- a) Orientation of automatic equipment.
 - b) Indicate type and orientation of the crystal.
- ❖ Primary flat: The flat of largest length located at the circumference of the wafer. The primary has a specific crystal orientation relative to the wafer surface - major flat.
 - ❖ Secondary flat: Indicates the crystal orientation and doping of the wafer.

Orientation must be $\langle 100 \rangle$ and $\langle 111 \rangle$

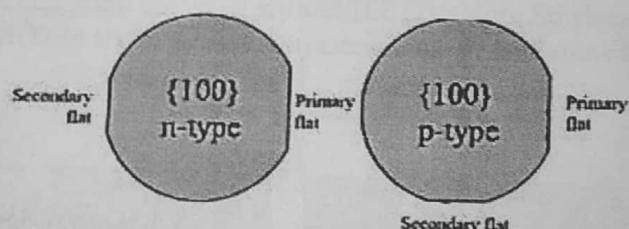


FIG 7: flat at 180 deg for n type and 90 deg for p type.

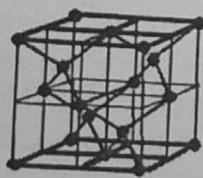


FIG 9: {100} planes

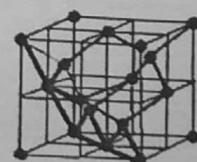


FIG 10: {111} planes

From the above figures it is seen clearly that in $\langle 100 \rangle$ we cut the wafers from both of horizontal sides and vertical sides and in $\langle 111 \rangle$ we cut the wafers from only horizontal sides. So, orientation type $\langle 100 \rangle$ is more used in microelectronics.

CLEANING PROCESSES

High quality wafers are in demand, as increasingly high integration of VLSIs

Became a commercial practice. This is especially true with highly clean wafers with little metallic impurity and particulate and organic matters on the surface. For producing the highly clean wafers, it is necessary to establish wafer surface cleaning technologies through experimental and theoretical analysis of the behavior of the surface impurities.

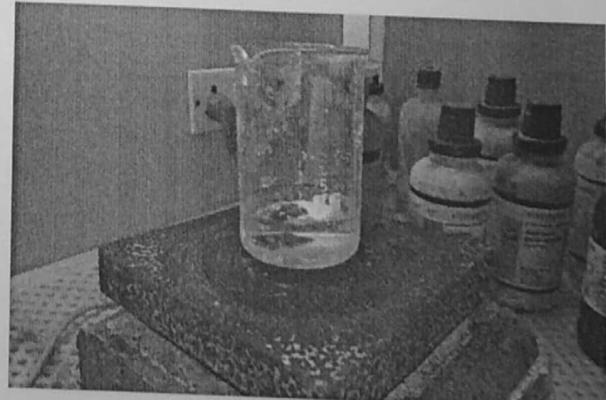
The wafer can be cleaned using two processes –

- 1) Acid Clean Process (used in industries)
- 2) Plasma Dry Clean Process (costly process)

We will use Acid Clean Process.

Acid Clean Process involves-

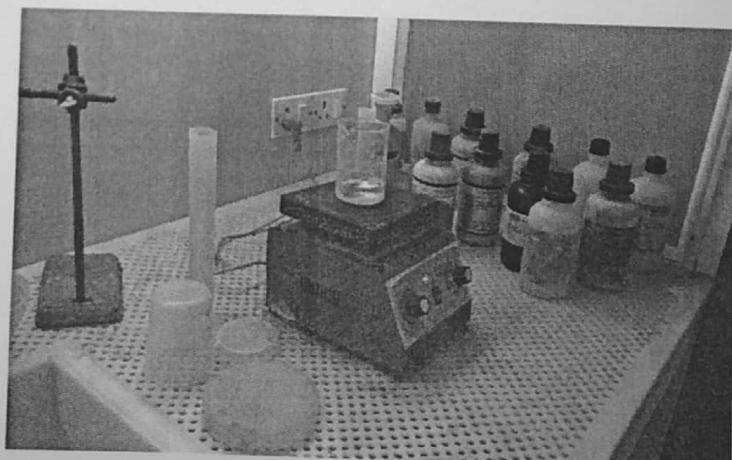
- a) DUST: To remove the dust from the wafer we add TCE (Trichloro Ethylene) to the wafer and boil it for 5 mins. And then keep the mixture in Ultrasonic cleaner for 3 mins for completely removal of dust.



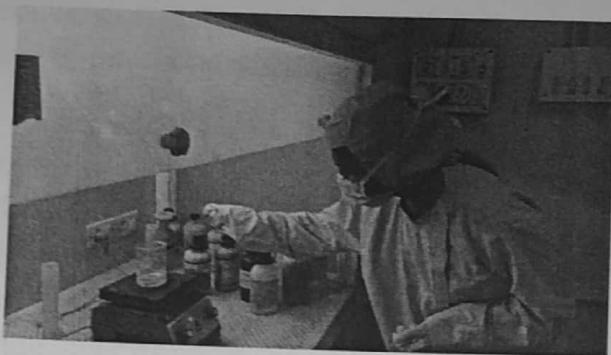
- b) OIL AND GREASE: We take the dust free wafer sample and add acetone to it and then boil it for 5mins and after boiling keep the mixture in Ultrasonic Cleaner for 3mins for complete removal of oil and grease.



- c) INORGANIC COMPOUND: Mix Sulphuric acid (H_2SO_4) and Hydrogen peroxide (H_2O_2) in 1:1 ratio and wait until the reaction stops. Add the sample to the mixture. then clean it in de-ionized water.



- d) ORGANIC COMPOUND (ACIDIC): Mix water hydrogen peroxide and ammonium hydroxide (alkaline, highly volatile) in 5:1:1 ratio. Add the sample. Heat it at 70°C for 10mins and then pass it to cold water.



- e) ORGANIC COMPOUND (ALKALINE): Mix H_2O , H_2O_2 , HCN in a ratio of 6:1:1. Then heat it at 70°C for 10 mins and then clean it in de-ionized water.
- f) REMOVAL OF SiO_2 : Sample dip in 10% HF (only this acid can catch Si& SiO_2) for 2-3 min

A clean sample is hydrophobic in nature. If, water is sticking to the sample after cleaning then it concludes that the sample is still unclean.

OXIDATION

Oxidation refers to the conversion of the silicon wafer to silicon oxide. The ability of Si to form an oxide layer is very important since this is one of the reasons for choosing Si over Ge.

Si exposed to ambient conditions has a native oxide on its surface. The native oxide is approximately 3nm thick at room temperature. But this is too thin for most applications and hence a thicker oxide needs to be grown. SiO_2 is the grown layer. This helps in protecting the wafer from contamination, both physical and chemical. Thus, it acts as passivating layer. The oxide layer protects the wafer surface from scratches and it also prevents dust from interacting with the wafer surface, and thus minimize contamination.

Silicon oxide thickness chart

Thickness, in Å	Application
60-100	Tunneling gates
150-500	Gate oxides, capacitor dielectrics
200-500	LOCOS pad oxide
2000-5000	Hard masks, surface passivation
3000-10000	Field oxides

Role of oxidation

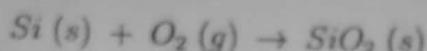
1. It is used for surface passivation.
2. It protects the junction from moisture and other atmospheric contaminants.
3. It serves as an insulator on the wafer surface.
4. It is used to isolate one device from other.
5. SiO_2 acts as the active gate electrode in MOS device structure.

In oxidation the wafer is exposed to oxygen and the oxygen molecules diffuse into the wafer. A chemical reaction occurs between oxygen and the silicon wafer. After this a layer of oxide grows on the wafer surface.

Oxidation Techniques

In the case of grown oxide layers, there are two main growth mechanisms:-

1. **Dry oxidation** - Si reacts with O₂ to form SiO₂.

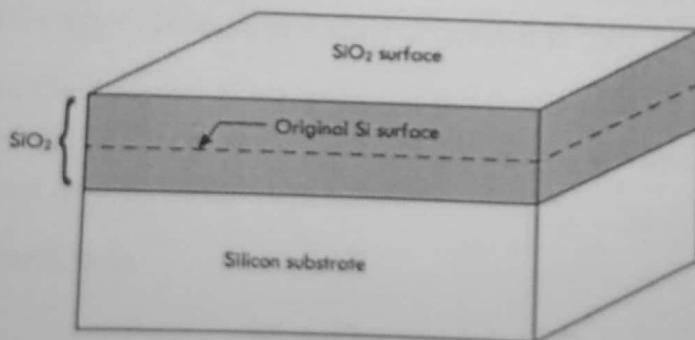


2. **Wet oxidation** - Si reacts with water (steam) to form SiO₂.



In both cases, Si is supplied by the underlying wafer. Dry and wet oxidation need high temperature (900-1200 degree °C) for growth, though the kinetics are different, which is why this process is called thermal oxidation. Since the underlying Si is consumed, the Si/SiO₂ interface moves deeper into the wafer.

There is also a volume expansion since the densities of the oxide layer and Silicon are different. Thus, the final thickness is higher than the initial Si thickness.



Movement of the silicon-oxide interface as oxide thickness grows.

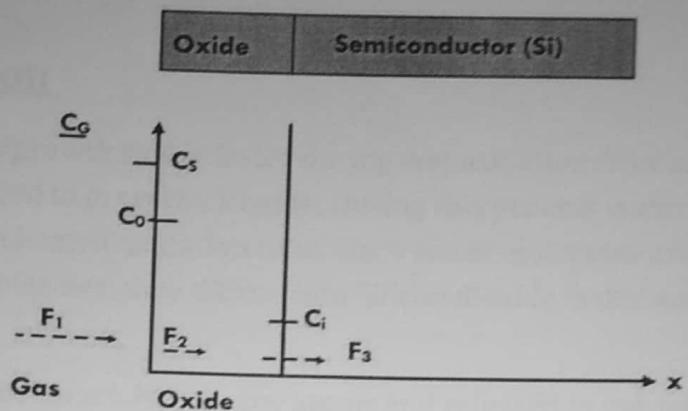


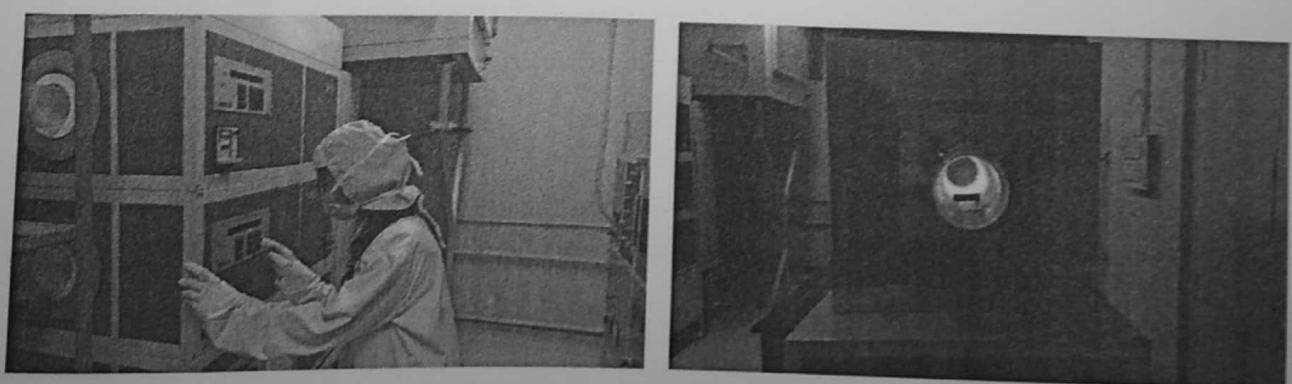
Figure 3: A one dimensional growth model for oxide formation with the fluxes and concentrations marked. There is a certain concentration of the diffusing species, oxygen or steam, in the gas phase, and it is in equilibrium with the concentration in the oxide layer and the oxide-silicon interface.

Dry Oxidation

During dry oxidation, dry oxygen gas is introduced into the process tube where it reacts with Silicon. Since dry oxidation is a slow process it is only used to grow thin oxides.

In dry oxidation, the amount of water in the processing tube is kept minimum. If the water level exceeds 25-50 parts per million (ppm), the oxidation rate increases and a thick layer of poor quality oxide is produced.

The chemical reaction is

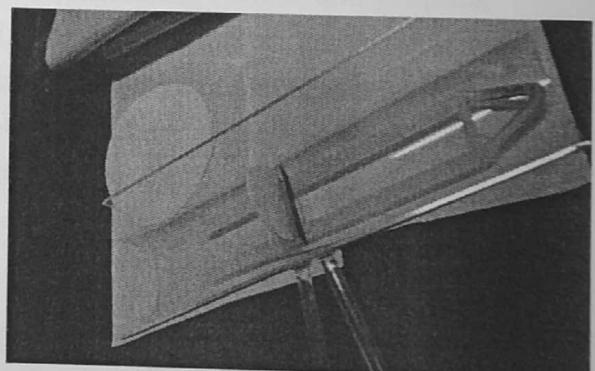
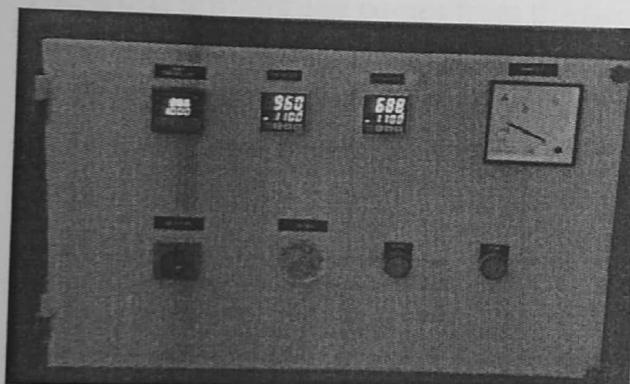


Wet Oxidation

The silicon dioxide growth rate is faster during wet oxidation. Wet oxidation is therefore the preferred method to grow thick oxide. During this process water vapour is introduced into the heated oxidation tube. Since water molecules are smaller in size than the oxygen molecules, they diffuse into Silicon dioxide faster and the oxide growth rate increases.

As the silicon dioxide forms, it traps the atoms and released in subsequent processing steps hydrogen atoms within it. These hydrogens do not affect the quality of the oxide.

The reaction of wet oxidation is: -



Semiconductor Lithography (Photolithography)

The fabrication of an integrated circuit (IC) requires a variety of physical and chemical processes performed on a semiconductor (e.g., silicon) substrate. In general, the various processes used to make an IC fall into three categories: film deposition, patterning, and semiconductor doping. Films of both conductors (such as polysilicon, aluminum, and more recently copper) and insulators (various forms of silicon dioxide, silicon nitride, and others) are used to connect and isolate transistors and their components. Selective doping of various regions of silicon allow the conductivity of the silicon to be changed with the application of voltage. By creating structures of these various components millions of transistors can be built and wired together to form the complex circuitry of a modern microelectronic device. Fundamental to all of these processes is lithography, i.e., the formation of three-dimensional relief images on the substrate for subsequent transfer of the pattern to the substrate.

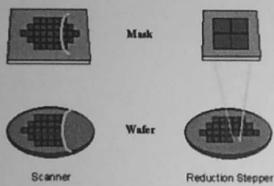
The word lithography comes from the Greek lithos, meaning stones, and graphia, meaning to write. It means quite literally writing on stones. In the case of semiconductor lithography (also called photolithography) our stones are silicon wafers and our patterns are written with a light sensitive polymer called a photoresist. Each pattern being printed on the wafer is aligned to the previously formed patterns and slowly the conductors, insulators, and selectively doped regions are built up to form the final device.

The importance of lithography can be appreciated in two ways. First, due to the large number of lithography steps needed in IC manufacturing, lithography typically accounts for about 30 percent of the cost of manufacturing. Second, lithography tends to be the technical limiter for further advances in feature size reduction and thus transistor speed and silicon area. Obviously, one must carefully understand the trade-offs between cost and capability when developing a lithography process. Although lithography is certainly not the only technically important and challenging process in the IC manufacturing flow, historically, advances in lithography have gated advances in IC cost and performance.

1. Substrate Preparation

Substrate preparation is intended to improve the adhesion of the photoresist material to the substrate. This is accomplished by one or more of the following processes: substrate cleaning to remove contamination, dehydration bake to remove water, and addition of an adhesion promoter. Projection lithography derives its name from the fact that an image of the mask is projected onto the wafer. Projection lithography became a viable alternative to contact/proximity printing in the mid 1970s when the advent of computer-aided lens design and improved optical materials allowed the production of lens elements of sufficient quality to meet the requirements of the semiconductor industry. In fact, these lenses have become so perfect that lens defects, called aberrations, play only a small role in determining the quality of the image. Such an optical system is said to be diffraction limited, since it is diffraction effects and not lens aberrations which, for the most part, determine the shape of the image. Scanning projection printing, pioneered by the Perkin-Elmer company [1.5], employs reflective optics (i.e., mirrors rather than lenses) to project a slit of light from the mask onto the wafer as the mask and wafer are moved simultaneously by the slit. Exposure dose is determined by the intensity of the light, the slit width, and the speed at which the wafer is scanned. These early scanning systems, which use polychromatic light from a mercury arc lamp, are 1:1, i.e., the mask and image sizes are equal. Step-and-repeat cameras (called steppers for short) expose the wafer one rectangular section (called the image field) at a time and can be 1:1 or reduction. These systems employ refractive optics (i.e., lenses) and are usually quasi-monochromatic. Both types of systems (Figure 1-5) are capable of high-resolution imaging, although reduction imaging is required for the highest resolutions. Scanners replaced proximity printing by the mid-seventies for device geometries below 4 to 5 μm . By the early 1980s, steppers began to dominate as device designs pushed below 2 μm . Steppers have continued to dominate lithographic patterning throughout the 1990s as minimum feature sizes reached the 250nm levels. However, by the early 1990s a hybrid step-and-scan approach was introduced by SVG Lithography, the successor to Perkin-Elmer. The step-and-scan approach uses a fraction of a normal stepper field (for example, 25mm x

8mm), then scans this field in one direction to expose the entire 4 x reduction mask. The wafer is then stepped to a new location and the scan is repeated. The smaller imaging field simplifies the design and manufacture of the lens, but at the expense of a more complicated reticle and wafer stage. Step-and-scan technology is the technology of smallest image that can be projected onto the wafer, and the resolving capability of the photoresist to make use of that image.



2. Photoresist Coating

A thin, uniform coating of photoresist at a specific, well controlled thickness is accomplished by the seemingly simple process of spin coating. The photoresist, rendered into a liquid form by dissolving the solid components in a solvent, is poured onto the wafer, which is then spun on a turntable at a high speed producing the desired film. Stringent requirements for thickness control and uniformity and low defect density call for particular attention to be paid to this process, where a large number of parameters can have significant impact on photoresist thickness uniformity and control. There is the choice between static dispense (wafer stationary while resist is dispensed) or dynamic dispense (wafer spinning while resist is dispensed), spin speeds and times, and accelerations to each of the spin speeds. Also, the volume of the resist dispensed and properties of the resist (such as viscosity, percent solids, and solvent composition) and the substrate (substrate material and topography) play an important role in the resist thickness uniformity.

3. Pre Heat (Post-Apply Bake)

After coating, the resulting resist film will contain between 20 – 40% by weight solvent. The pre heat process, also called a post-apply bake or a prebake, involves drying the photoresist after spin coat by removing this excess solvent. The main reason for reducing the solvent content is to stabilize the resist film. At room temperature, an unbaked photoresist film will lose solvent by evaporation, thus changing the properties of the film with time. By baking the resist, the majority of the solvent is removed and the film becomes stable at room temperature. There are four major effects of removing solvent from a photoresist film:

- (1) Film thickness is reduced
- (2) Post-exposure bake and development properties are changed.
- (3) Adhesion is improved
- (4) The film becomes less tacky and thus less susceptible to particulate contamination.

Typical preheat processes leave between 3 and 8 percent residual solvent in the resist film, sufficiently small to keep the film stable during subsequent lithographic processing. Unfortunately, there are other consequences of baking most photoresists. At temperatures greater than about 90°C the photosensitive component of a typical resist mixture, called the photoactive compound (PAC), may begin to decompose [1.3.1.4]. Also, the resin, another component of the resist, can crosslink and/or oxidize at elevated temperatures. Both of these effects are undesirable. Thus, one must search for the optimum preheat conditions that will maximize the benefits of solvent evaporation and minimize the detriments of resist decomposition. For chemically amplified resists, residual solvent can significantly influence diffusion and reaction properties during the post-exposure bake, necessitating careful control over the post-apply bake process. Fortunately, these modern resists do not suffer from significant decomposition of the photosensitive components during prebake. There are several methods that can be used to bake photoresists. The most obvious method is an oven bake. Convection oven baking of conventional photoresists at 90°C for 20 minutes was typical during the 1970s and early 1980s. Although the use of convection ovens

for the prebaking of photoresist was once quite common, currently the most popular bake method is the hot plate. The wafer is brought either into intimate vacuum contact with or close proximity to a hot, high-mass metal plate. Due to the high thermal conductivity of silicon, the photoresist is heated to near the hot plate temperature quickly (in about 5 seconds for hard contact, or about 20 seconds for proximity baking). The greatest advantage of this method is an order of magnitude decrease in the required bake time over convection ovens, to about one minute, and the improved uniformity of the bake. In general, proximity baking is preferred to reduce the possibility of particle generation caused by contact with the backside of the wafer. When the wafer is removed from the hotplate, baking continues as long as the wafer is hot. The total bake process cannot be well controlled unless the cooling of the wafer is also well controlled. As a result, hotplate baking is always followed immediately by a chill plate operation, where the wafer is brought in contact or close proximity to a cool plate (kept at a temperature slightly below room temperature). After cooling, the wafer is ready for its lithographic exposure.

4. Alignment and Exposure

The basic principle behind the operation of a photoresist is the change in solubility of the resist in a developer upon exposure to light (or other types of exposing radiation). In the case of the standard diazonaphthoquinone positive photoresist, the photoactive compound (PAC), which is not soluble in the aqueous base developer, is converted to a carboxylic acid on exposure to UV light in the range of 350 - 450nm. The carboxylic acid product is very soluble in the basic developer. Thus, a spatial variation in light energy incident on the photoresist will cause a spatial variation in solubility of the resist in developer. Contact and proximity lithography are the simplest methods of exposing a photoresist through a master pattern called a photomask (Figure 1-4). Contact lithography offers high resolution (down to about the wavelength of the radiation), but practical problems such as mask damage and resulting low yield make this process unusable in most production environments. Proximity printing reduces mask damage by keeping the mask a set distance above the wafer (e.g., 20 μm). Unfortunately, the resolution limit is increased to greater than 2 to 4 μm , making

proximity printing insufficient for today's technology. By far the most common method of exposure is projection printing.

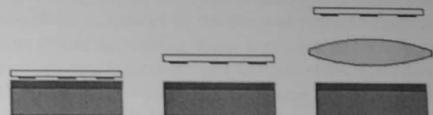


Figure 1-4. Lithographic printing in semiconductor manufacturing has evolved from contact printing (in the early 1960s) to projection printing (from the mid 1970s to today).

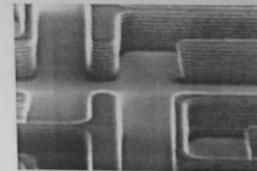


Figure - Photore sist pattern on a silicon substrate showing prominent standing waves

5. Development

Once exposed, the photoresist must be developed. Most commonly used photoresists use aqueous bases as developers. In particular, tetramethyl ammonium hydroxide (TMAH) is used in concentrations of 0.2 - 0.26 N. Development is undoubtedly one of the most critical steps in the photoresist process. The characteristics of the resist-developer interactions determine to a large extent the shape of the photoresist profile and, more importantly, the linewidth control. The method of applying developer to the photoresist is important in controlling the development uniformity and process latitude. In the past, batch development was the predominant development technique. A boat of some 10-20 wafers or more are developed simultaneously in a large beaker, usually with some form of agitation. With the push towards in-line processing, however, other methods have become prevalent. During spin development wafers

are spun, using equipment similar to that used for spin coating, and developer is poured onto the rotating wafer. The wafer is also rinsed and dried while still spinning. Spray development has been shown to have good results using developers specifically formulated for this dispense method. Using a process identical to spin development, the developer is sprayed, rather than poured, on the wafer by using a nozzle that produces a fine mist of developer over the wafer (Figure 1-8). This technique reduces developer usage and gives more uniform developer coverage. Another in-line development strategy is called puddle development. Again, using developers specifically formulated for this process, the developer is poured onto a stationary wafer that is then allowed to sit motionless for the duration of the development time. The wafer is then spin rinsed and dried. Note that all three in-line processes can be performed in the same piece of equipment with only minor modifications, and combinations of these techniques are frequently used.

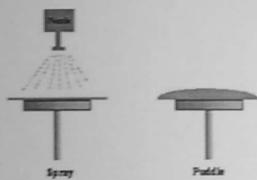


Figure 1-8. Different developer application techniques are commonly used

7. Striping

After the imaged wafer has been processed (e.g., etched, ion implanted, etc.) the remaining photoresist must be removed. There are two classes of resist stripping techniques: wet stripping using organic or inorganic solutions, and dry (plasma) stripping. A simple example of an organic stripper is acetone. Although commonly used in laboratory environments, acetone tends to leave residues on the wafer (scrubbing) and is thus unacceptable for semiconductor processing. Most commercial organic strippers are phenol-based and are somewhat better at avoiding scum formation. However, the most common wet strippers for positive photoresists are inorganic acid-based systems used at elevated temperatures. Wet stripping has several inherent problems. Although the proper choice of strippers for various applications can usually eliminate gross scrubbing, it is almost impossible to remove the final monolayer of photoresist from the wafer by wet chemical means. It is often necessary to follow a wet strip by a plasma descum to completely clean the wafer of resist residues. Also, photoresist which has undergone extensive hardening (e.g., deep-UV hardening) and been subjected to harsh processing conditions (e.g., high energy ion implantation) can be almost impossible to strip chemically. For these reasons, plasma stripping has become the standard in semiconductor processing. An oxygen plasma is highly reactive towards organic polymers but leaves most inorganic materials (such as are found under the photoresist) untouched.

6. Etching

Etching of the given sample by 10% HF solution for 5 minutes.

DIFFUSION

HOT PROBE METHOD:

A **hot point probe** is a method of determining quickly whether a semiconductor sample is n(negative type), p(positive type). A voltmeter or ammeter is attached to the sample, and a heat source, such as a soldering iron, is placed on one of the leads. The heat source will cause charge carriers (electrons in an n-type, electron holes in a p-type) to move away from the lead. The heat from the probe creates an increased number of higher energy carriers which then diffuse away from the contact point. This will cause a current/voltage difference. For example, if the heat source is placed on the positive lead of a voltmeter attached to an n-type semiconductor, a positive voltage reading will result as the area around the heat source/positive lead becomes positively charged.

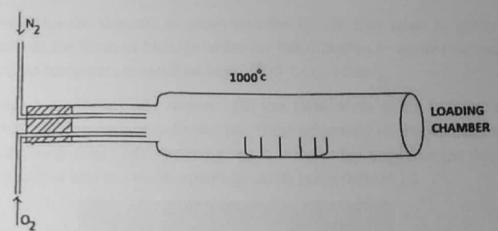
REQUIMENT OF DIFFUSION:

1. Temperature: 1000°C
2. Gas:
 - N₂: 1L/minute
 - O₂: 1L/minute
3. Time:
 - Pre-dip: 15 minute
 - Driving: 3 hours

4.10%HF

Activation:

Boron nitride absorbs moisture. So, it should be heated for 20-25 hours at 1000°C in ambient. Boron hydroxide is formed on its surface, which prevents it from reacting. So, it is kept in an oven until it is used. It is called Activation.



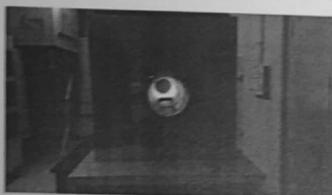
DOPANT DIFFUSION: PRE-DEP

The goal of the dopant predisposition diffusion is to move dopant atom for a source of the wafer, and then allow the dopant to diffuse into wafer. The source of dopant can be several forms solid(boron nitride and phosphorus oxide ceramic discs), liquid(boron tribromide and POCl_3), or gas(diborane or phosphine).

This module covers the cleaning of wafers with standard metals for LPCVD (such as LTO) or metal deposition. This module assumes that the wafers do not have resist on them. For resist stripping please look at the section Photoresist Stripping.

In order for the dopants to move into the silicon, they must be given energy, usually in the form of heat. In order for the diffusion to occur in a reasonable time, the temperature must be high($9000^{\circ}\text{C} < 1' < 1200^{\circ}$).

At this temperature the dopant (in the form of an oxide) reacts with the exposed silicon surface to form junctions selectively on the wafer through the photolithography highly doped glass. It is from this glass that the dopants can then diffuse into the wafer openings in the oxide defined by.

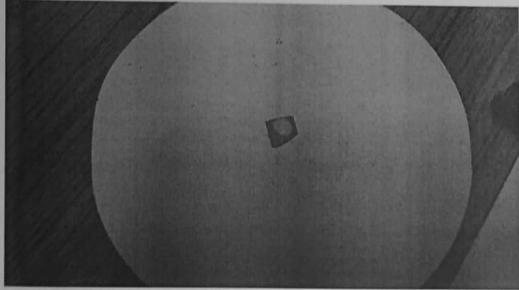


DOPANT DIFFUSION: DRIVE

After the Predeposition diffusion the dopants are situated close to the surface of the wafer. However, they must diffuse even further to lower the overall concentration in order for some of the devices to work properly. The first diffusion (predisposition) introduces dopants into the wafer. The second diffusion (drive) redistributes the dopants and allows the dopants to diffuse into the wafer more deeply (up to ~3 micrometers). In addition, oxygen and water vapor are introduced during the drive diffusion to grow a new oxide over the areas which were exposed to bare silicon during the process. This new oxide can be patterned again so that other selective diffusion.



After diffusion a layer of boron silicate is created ($\text{Si}+\text{B}+\text{O}_2 \rightarrow \text{Boron silicate}$) on the wafer surface. It is etched by 10% HF for few seconds.



Metallization

Metallization is the final step in the wafer processing sequence. Metallization is the process by which the components of IC's are interconnected by aluminium conductor. This process produces a thin-film metal layer that will serve as the required conductor pattern for the interconnection of the various components on the chip. Another use of metallization is to produce metallized areas called bonding pads around the periphery of the chip to produce metallized areas for the bonding of wire leads from the package to the chip. The bonding wires are typically 25 micro meters diameter gold wires, and the bonding pads are usually made to be around 100×100 micro meters square to accommodate fully the flattened ends of the bonding wires and to allow for some registration errors in the placement of the wires on the pads.

Aluminium

Aluminium (Al) is the most commonly used material for the metallization of most IC's, discrete diodes, and transistors. The film thickness is as about 1 micro meters and conductor widths of about 2 to 25 micro meters are commonly used. The use of aluminum offers the following advantages:

- It has as relatively good conductivity.
- It is easy to deposit thin films of Al by vacuum evaporation.
- It has good adherence to the silicon dioxide surface.
- Aluminium forms good mechanical bonds with silicon by sintering at about 500°C or by alloying at the eutectic temperature of 577°C .



Metallization Processes

Metallization process can be classified into two types:

1. CVD and
2. Physical Vapour Deposition

Chemical Vapor Deposition (CVD) is the deposition of a solid material onto a heated substrate through decomposition or chemical reaction of compounds contained in the gas passing over the substrate. Many materials such as, silicon nitride, silicon dioxide, non-crystalline silicon, and single crystal silicon, can be deposited through CVD method.

Deposition Methods

In the evaporation method, which is the simplest, a film is deposited by the condensation of the vapour on the substrate. The substrate is maintained at a lower temperature than that of the vapour. All metals vaporize when heated to sufficiently high temperatures. Several methods of heating are employed to attain these temperatures. For Al deposition, resistive, inductive (RF), electron bombardment [electron-gun] or laser heating can be employed. For refractory metals, electron-gun is very common.

In sputtering deposition method, the target material is bombarded by energetic ions to release some atoms. These atoms are then condensed on the substrate to form a film. Sputtering, unlike evaporation is very well controlled and is generally applicable to all materials metals, alloys, semiconductors and insulators. RF-dc and dc-magnetron sputtering can be used for metal deposition.



Page 26

Deposition Apparatus

The metallization is usually done in vacuum chambers. A mechanical pump can reduce the pressure to about 10 to 0.1 Pa. Such pressure may be sufficient for LPCVD. An oil-diffusion pump can bring the pressure down to 10^{-5} Pa and with the help of a liquid nitrogen trap as low as 10^{-7} Pa. A turbomolecular pump, can bring the pressure down to 10^{-8} - 10^{-9} Pa. Such pumps are oil-free and are useful for molecular-beam epitaxy where oil contamination must be avoided.

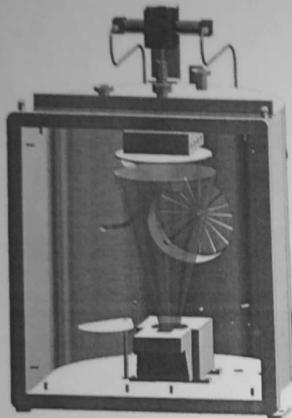
TYPES OF EVAPORATION SYSTEM

- A. Vacuum Thermal Evaporation System



Page 27

B. Vacuum Electron Beam Evaporation System



C. Vacuum Radio Frequency Generator



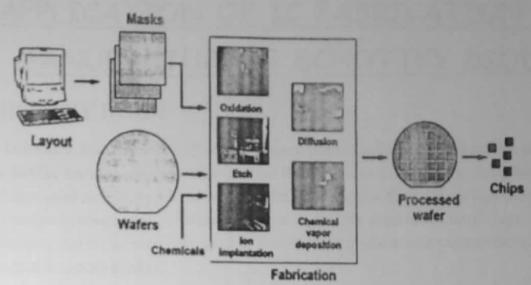
PROCEDURE

1. Check if all the valves are closed. Switch ON the mains.
2. Switch on the Rotary Pump. Open the Gas Blast. Also switch on the Pirani Gauge (GH 1). Press to ON the rotary pump Green light glows if rotary pump is on press to on the diffusion Green light glows if diffusion pump is on.
3. Close the GAs Ballast after 5 minutes. When the pressure drops below 0.02mbar open the Backing Valve slowly (the pressure increases and starts decreasing again).
4. Once the pressure reaches 0.02mbar open the coolant water supply. Switch on the diffusion pump. The pump needs to be heated for 20-25 minutes.
5. Meantime open the air admittance valve slowly, hoist the chamber. Clean the chamber and the boat/filament contacts, replace the glass near the window, check the contacts, load the metal (Al, Cu, etc.) into tungsten boat/filament, load the samples, hoist down the chamber and close the air admittance valve.
6. After about 20-25 minutes the diffusional pump will be operational. Close the Backing Valve and open the roughing valve slowly. Switch on to GH 2. Wait till the Pirani Gauge reads 0.01mbar.





Page 30



Page 31

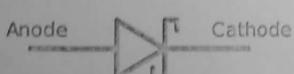
APPLICATION OF IC FABRICATION BY MANUFACTURING SCHOTTKY DIODE

SCHOTTKY DIODE

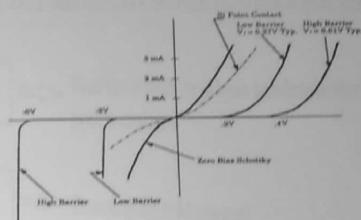
The **Schottky diode** (named after the German physicist Walter H. Schottky), also known as **Schottky barrier diode** or **hot-carrier diode**, is a semiconductor diode formed by the junction of a semiconductor with a metal. It has a low forward voltage drop and a very fast switching action. The cat's-whisker detectors used in the early days of wireless and metal rectifiers used in early power applications can be considered primitive Schottky diodes.

When sufficient forward voltage is applied, current flows in the forward direction. A silicon diode has a typical forward voltage of 600–700 mV, while the Schottky's forward voltage is **150–450 mV**. This lower forward voltage requirement allows higher switching speeds and better system efficiency. A metal–semiconductor junction is formed between a metal and a semiconductor, creating a Schottky barrier (instead of a semiconductor–semiconductor junction as in conventional diodes). Typical metals used are molybdenum, platinum, chromium or tungsten, and certain silicides (e.g., palladium silicide and platinum silicide), whereas the semiconductor would typically be n-type silicon.^[1] The metal side acts as the anode, and n-type semiconductor acts as the cathode of the diode. This Schottky barrier results in both very fast switching and low forward voltage drop.

The choice of the combination of the metal and semiconductor determines the forward voltage of the diode. Both n- and p-type semiconductors can develop Schottky barriers.



SCHOTTKY CURVES

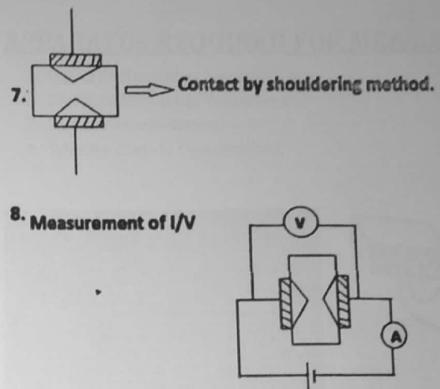


FABRICATION OF SCHOTTKY DIODE

We demonstrate fabrication of a Schottky junction diode with direct growth graphene on n-Si by the solid phase reaction approach. Metal-assisted crystallization of a-C thin film was performed to synthesize transfer-free graphene directly on a SiO₂ patterned n-Si substrate. Graphene formation at the substrate and catalyst layer interface is achieved in presence of a Co catalytic and CoO carbon diffusion barrier layer. The as-synthesized material shows a linear current–voltage characteristic confirming the metallic behavior of the graphene structure. The direct grown graphene on n-Si substrate creates a Schottky junction with a potential barrier of 0.44 eV and rectification diode characteristic. Our finding shows that the directly synthesized graphene on Si substrate by a solid phase reaction process can be a promising technique to fabricate an efficient Schottky junction device.

STEPS FOR IC FABRICATION (SCHOTTKY DIODE)

1.  → Test for P type or N type semiconductor by Hot probe method
2.  → Cleaning by Acid process
3.  → Metal(Ag-if N-type) deposition by vacuum thermal evaporation system.
4.  → Metal(Ag) diffusion by heat treatment at 700°C for 45 sec.
5.  → Metal(Al) deposition by vacuum thermal evaporation system.
6.  → Metal(Al) diffusion by heat treatment at 550°C for 45 sec

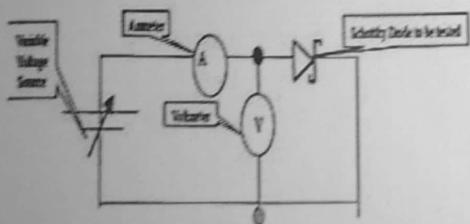
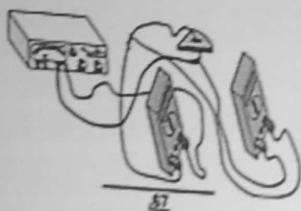


STEPS FOR FABRICATION OF SCHOTTKY DIODE

1. TESTING THE TYPE OF DOPANT BY HOT PROBE METHOD
2. ACID CLEANING PROCESS
3. FIRST METAL DEPOSITION
4. FIRST METAL DIFFUSION
5. SECOND METAL DEPOSITION
6. SECOND METAL DIFFUSION
7. CREATION OF CONTACT BY SOULDERING
8. IDENTIFICATION OF THE SCHOTTKY DIODE

APPARATUS REQUIRED FOR MEASUREMENT

1. Digital Multimeter as Ammeter
2. Digital Multimeter as Voltmeter
3. Variable Voltage Source
4. Schottky diode to be supervised.



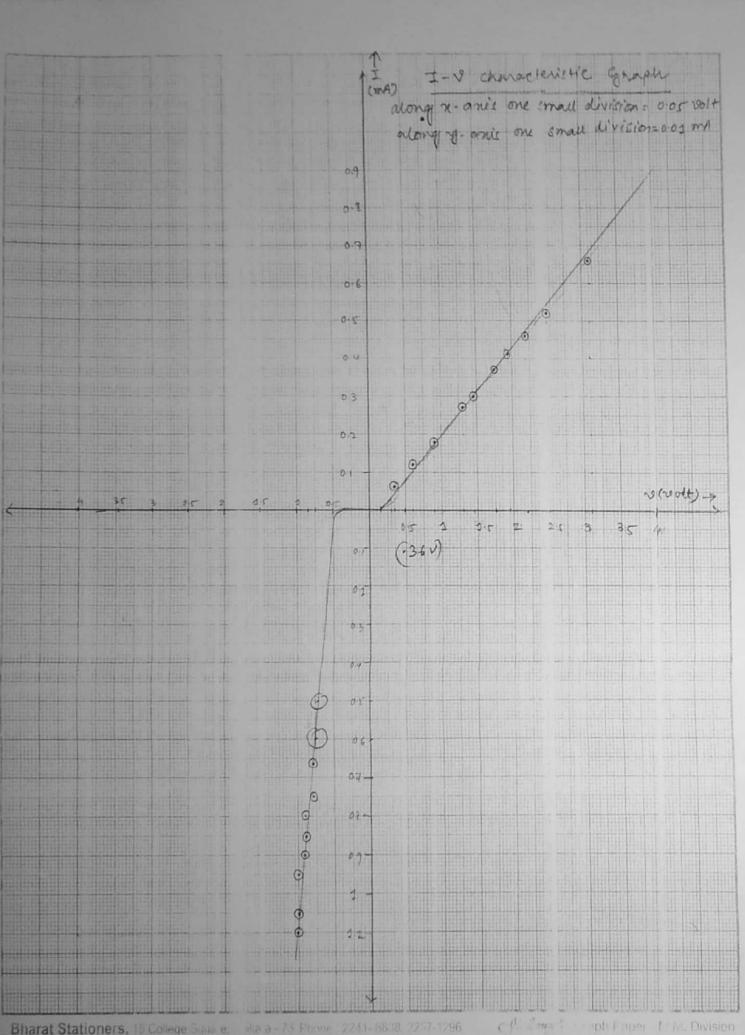
EXPERIMENTAL RESULTS

REVERSE-BIASED CONDITION

VOLTAGE(V)	CURRENT(mA)
0.74	0.50
0.856	0.57
0.98	0.66
1.62	1.06
1.94	1.26
2.0	1.36
2.32	1.50
2.54	1.63
2.79	1.78
2.83	1.81

FORWARD-BIASED CONDITION

VOLTAGE(V)	CURRENT(mA)
0.36	0.07
0.629	0.12
0.89	0.18
1.33	0.27
1.46	0.30
1.76	0.37
1.95	0.40
2.22	0.46
2.51	0.52
3.1	0.66



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CONCLUSION

Fabrication of Schottky barrier diode in standard CMOS process through MPW. The barrier height of the Al-n Si contacts was about 0.44eV. The measured I-V, C-V and S parameter of the realized SBDs is shown in this paper. The advantages of this SBD design are low cost and can be integrated into commercial standard CMOS process. In the future work, more emphasis will be focused on extension of the reverse breakdown voltage and frequency range of the SBDs designed on standard CMOS process.

Research on interactions of physical mechanisms in ferrite-semi-conductor structures leads to:

- On various types of bipolar and field transistors.
- At low, average, and high levels of capacity in continuous and pulse modes.
- In a wide frequencies range (VHF, UHF, MWF, EHF, HHF).
- For various kinds and spectra of signals (regular, pseudo-noise, noise, as multipurpose synthesizers of frequencies).
- For various types of ferrite micro resonators and their orientations in an external magnetic field.
- For various modes of generation, amplification, multiplication, division and frequency modulation of a signal of the basic frequency. For registration of small values of a magnetic induction vector and a mechanical displacement vector

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