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G H Raisoni College of Engineering and Management, Pune

(An Autonomous Institution)

F.Y B. Tech (Engineering)

SECOND Term (2020-21)

CAE-I (2020 Pattern)

Modeling of Digital Circuits (UECL106)

[Time:1 Hour] **[Max. Marks: 15]**

COURSE OUTCOME:

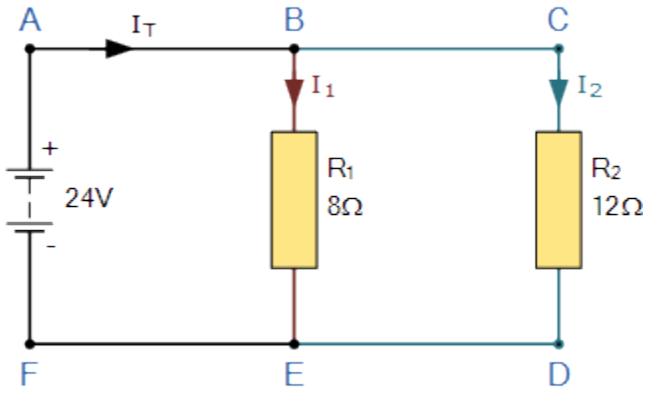
Upon successful completion of this course, student will be able to:

1. Solve the problems on Number system codes and their conversions.
2. Create and design canonical logic forms.
3. To demonstrate basic knowledge VHDL fundamentals.
4. Design VHDL Programs.
5. Design real time digital applications.

Instructions to the candidates:

1. (CO1/CO2)at the beginning of question/sub question indicates the course outcome related to the question.
2. All questions compulsory.
3. Neat diagrams must be drawn wherever necessary.
4. Figures to the right indicate full marks.
5. Assume suitable data, if necessary.

CO	*Sub Questions*		*Marks*
CO1	*a)*	Explain the KCL law in detail with diagram	[2]
	b)	Explain the passive components in details. Explain its properties.	[2]
	c)	Calculate the current I_T in the circuit diagram shown below	[3]



CO2	*a)*	Write down the four advantages of K-map.	[2]
	b)	State De Morgan's Theorems for three inputs (P, Q and R)	[3]
	c)	Simplify the Boolean function and build a logic circuit $F = (L + M)(LN + L\bar{N}) + LM + \bar{M}$	[3]
		OR	
	d)	Convert given decimal number to (i) Binary, (ii) Octal and (iii) Hexadecimal number system Given number is 101 *Note: Mention the steps for conversion. Marks are not given to direct answers.*	[3]