Camlin Page

OPEN ENDED EXPERIMENT

EXPERIMENT NO.: 8

Aim: To set up a transistor series regulator.

Equipment: Multicim Software, variable supply, resistor, transistor, zener voltage, current.

Theory: The output voltage of a practical power supply changes with load current, generally dropping as load current increases. The power supply specifications include a full load current rating, which is the maximum current that can be drawn from the supply.

The terminal voltage when full load current is drawn is called the full load voltage (VFL). The no load voltage (VNL) is the terminal voltage when zero current is drawn from the supply, that is the open circuit terminal voltage.

An unregular/unregulator power supply has poor regulations i.e., output voltage changes with load variations. If a power supply does has poor regulations it posses high internal impedance. A simple emitter follower regulator. It is also called as series regulators since the control element is in series with the load. It is also called as the pass transistor because it conducts or passess all the load current through the regulator. It is usually a power transistor. The zener provides the voltage reference, and base to emitter,

voltage to the transistor is the control voltage.

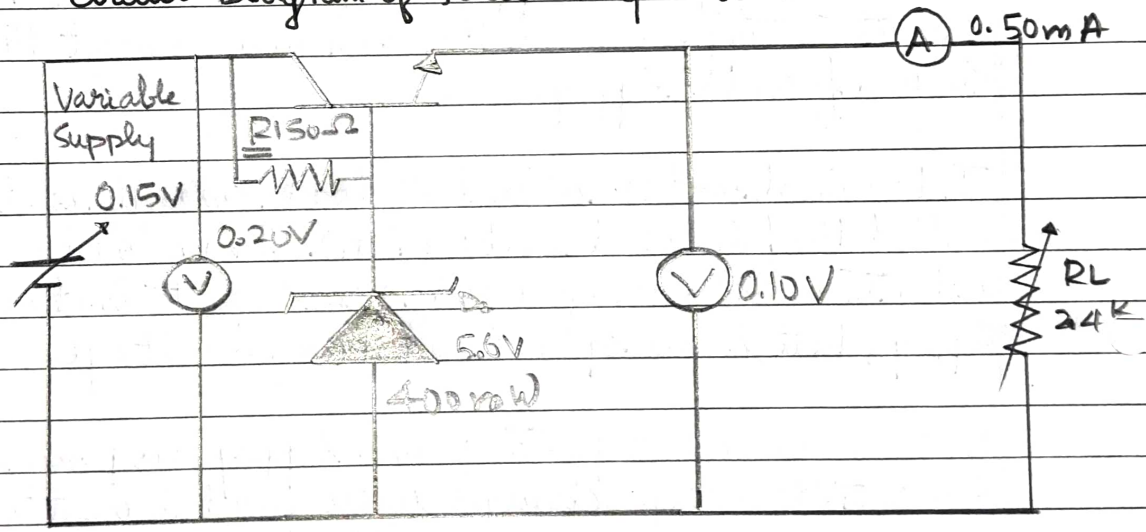
The value of Rs current must be sufficiently small, to keep the zener in its reverse breakdown region.

Writing Kirchoff's voltage law to output circuit.

$V_o + V_{BE} - V_z = 0$

i.e., $V_{BE} = V_z - V_o$.

Circuit Diagram of Series Regulator



If V_z is perfectly constant, the above equation is valid at all times, and any change in V_o must cause change in V_{BE}, in order to maintain equality.

When current demand is increased by decreasing R_L, V_o tends to decrease. This will increase.

The forward bias of the transistor thereby increasing level of conduction. Thus, the output current is increased to keep $I_L R_L$ a constant. The reverse process occurs when R_L is increased. Thus, the above circuit keeps the output voltage constant even if the load varies widely.

Procedure:

1.) Draw the same circuit on the breadboard OR multisim as shown in figure above.

2.) Keep the input voltage constant at Vimin, i.e. 10V.

3.) Vary the load resistance.

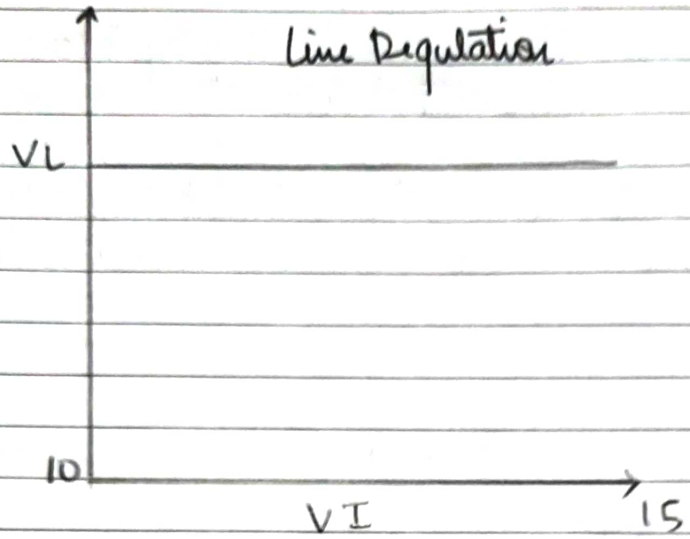
4.) Draw the Plot between I_L and V_o.

Observation:

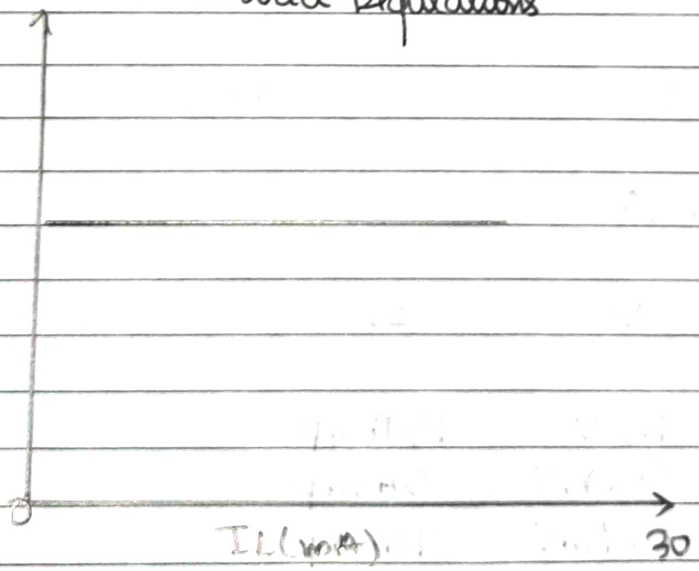
Sr No.	V_o	I_L
1.	1.3 V	15 Amp
2.	566 mV	5A mp
3.	677mV	7A mp

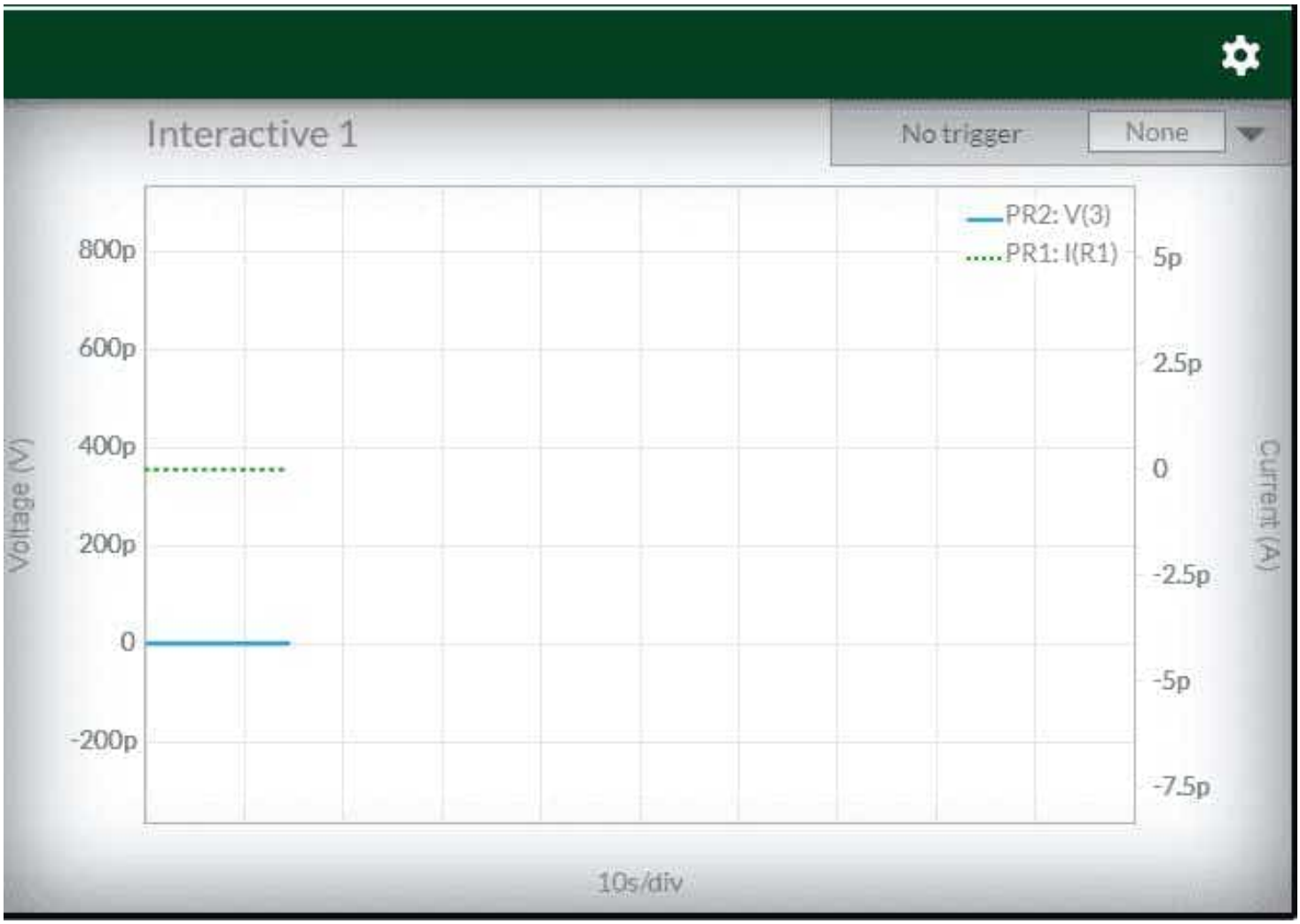
Conclusion: From the above enpriment we can eventually conclude that we have eventually conclude that we have learnt about I_L and V_o Relation & their Plot.

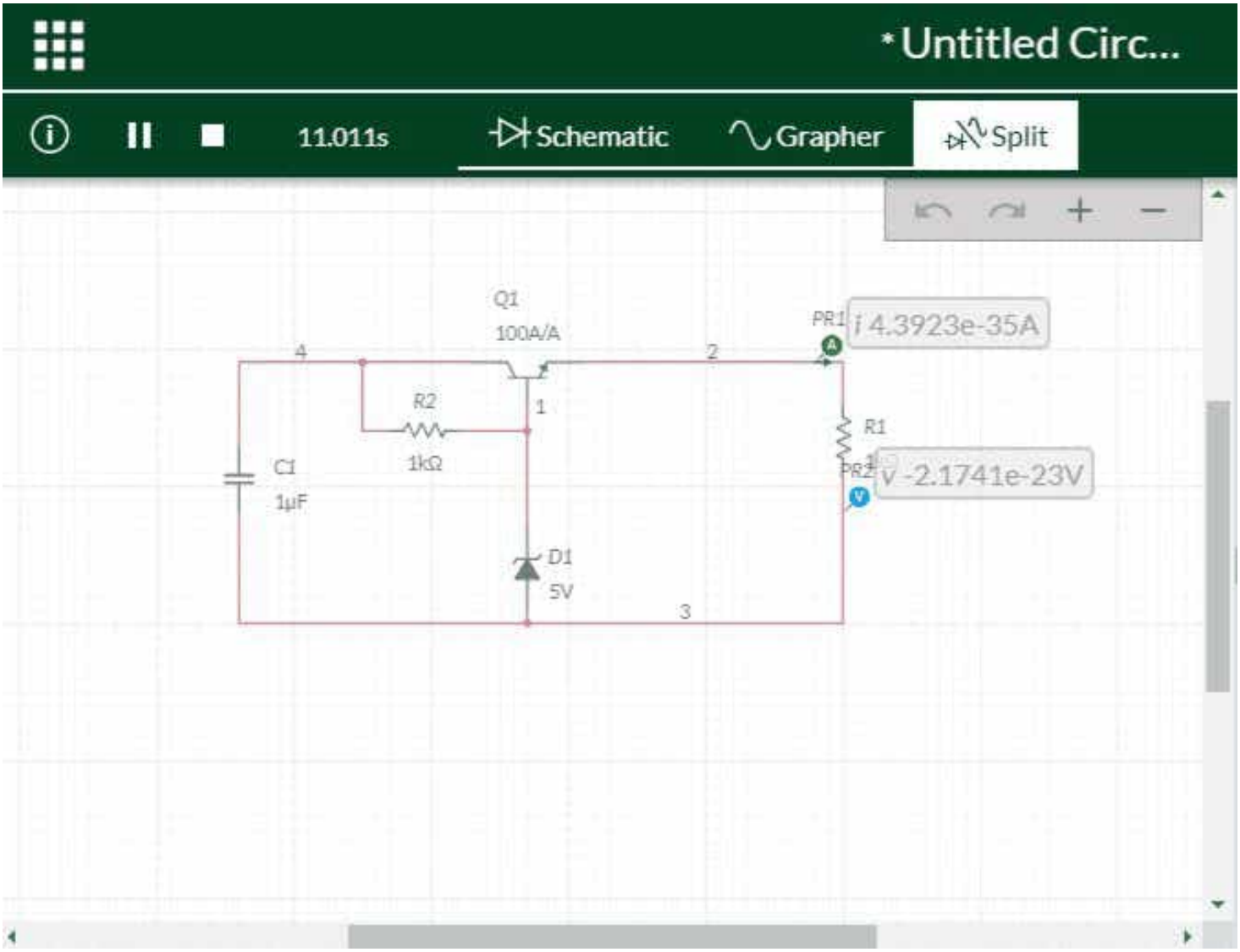
Line Regulation



Load Regulations




Interactive 1
No trigger
None
PR2: V(3)
PR1: I(R1)
800p
600p
400p
200p
0
-200p
5p
2.5p
0
-2.5p
-5p
-7.5p
Voltage (V)
Current (A)
10s/div


*Untitled Circ...
11.011s
Schematic
Grapher
Split
Q1
100A/A
PR1
i 4.3923e-35A
4
2
R2
1
1kΩ
R1
C1
1µF
PR2
v -2.1741e-23V
D1
5V
3