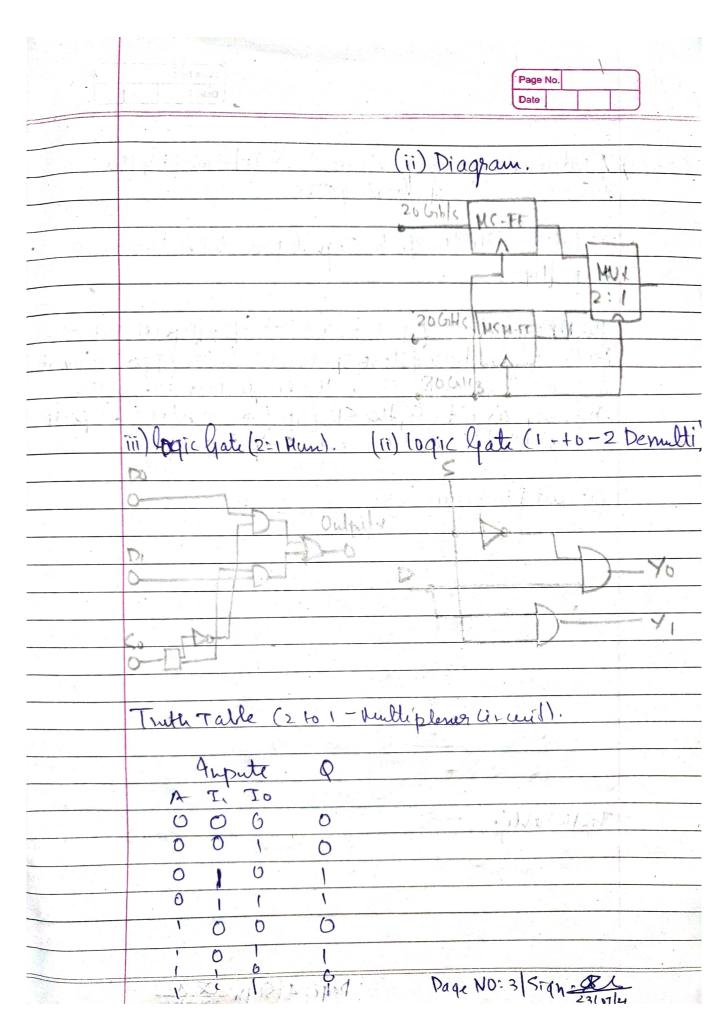
	Page No. Date					
	Gr H Raisoni Collège of Engineering 2 Management Wagneri, Dune					
	Waghiri, Pune					
	CAE-II SUMMER 2021					
	Department F.y B. Tech					
/	Torm Scalin Term 11 Dates cram: 22/07/2021					
14 1	Sugar Name Modeling of digital arcut (UE (1 103)					
-1.9	Roll NO: (70 Name: Swayam Torode					
	Regulation No: 2020 AIFT 11010 47					
(-0)						
(03 a)	The half adder circuit has two inputs: It and B, which add two imput digits and generates a carry and a					
	add two input digits and generate a carry and a					
1	It add two binary degits where the input bits are tormed					
1 1 1 1	as alingued and added and the rigidly will be output					
	At adds her binary digits where the input bits was tormed as amount and added and the rigidly will be output on is the sum and the other is carry.					
-	and AND gates is applied to both inputes to produce					
	carry. In applied to both inpute to produce					
	Lockery (a)					
	The 2-bit half adder kutte fall is as below:					
	A B Sum Corry					
	0 1 1					
	1 0 1					
	1 0					
-						
	Pager (Signe 2 1 12 12					
The state of the s	27/11/10					

		Page No.					
		Date					
and the second s							
	0+0=0	1 A 1					
	0+1=1 1200 81211112						
	1+6 = 1	+ Love NAV					
	1+1=10						
1		D-1 con la natione But le					
164	Trux are tere least poisible single lit combinations. B result for 1+1 is 10, the lun must be re-written a output. Thus the equation can be written as:						
۴, ۴	result for 1+1 10 lu, the xum in	my be 14 - W and any					
	output. Thus the equation can be	Writter as.					
1 1/2	0+0=0	()					
	. 0.10. 2. 0 17/23/22/24 17/2	State of the state					
	140=01	1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1					
¥	The output 1 of 10 is carry-out (SUH) is the normal output and carry with carry-out.						
17.42.	The output 1 of 10 h cary - och	SOFI AND ACCOUNTS					
	and Carry with Carry-on						
F)	1:2 Demun	2:1 Hunot					
b)	L. Z. Denne K	THA MA					
<u>₩ + + €, ₹, ≥</u>	(i) Symbol -	(i) Symbol -					
,	E COSO MOST	5					
	Tools to a solubph in it	" plant had will"					
	Auput 1:2	WO man 6 1					
,	D DEVILLE SV2	W, 112					
		1.00					
		2.1 Hun.					
	Schools						
	C.						

	Poge	No: 2 Kigun along					



	Par, In		Page No.		
(030)	A latch is a munory element. It is formed by the inter connection of logic gates.				
	The latite with the doct				
	The NAND gate SP flipf fuedback from both of ite This wint is und to Rt munory circuit. So, H is , S' and E' and co	or is a basic outpute back ore the Ringle or SR flip fly wrent outp	flip flop uluis to its opposi data bit in shar total 3	liprovida rejuput. tu inpute	
	Circuit Diagram:				
	2 BOB BUY	2 1	1/21 2/2 / T		
	Truth Talli: ->				
		<u> </u>			
	A MINISTER STATE	Dage: 4/Sig	h' 27/07/21		

		LA LITERAL DE			
					Page No.
SECONOMINAL SECONOMINA					Date
State	5	R	Q	01	Description
Set	1	0 .	011		Storsi
D 1		1	0		No Chang
Rest	0	1		0	Rest p'sso
moralid	7		1	0	No change
Iwali	0	0	-		Awalid Condition
			-		
(04 a) VUDI 8	tando	l. n 123	u laid	00	interest 1 con 1
nadwa	re du	(rint	in la	Aprila	integrated circuit
langua	16 rend	tomo	dela	diailal	Eysten by dataflow,
bhau	toral.	and	etrui	tural s.	here il modeling.
This lo	uquaq	wa	efrigt.	introde	here of modeling.
depart	neut	of defe	rise (D	0D) un	dus the VHSIC program.
		' '			
b) Turiar	esome	prides	med a	thribut	te for scalar types,
				. x	ATABLE NO.
Name		U	inition		
x high		-	1 '	bound of	
× 1000					X. santhursh
y'left ylan	1	-II	affin	ex bou	defr. graded.
X righ	<i>k</i>	1W	ngw	WOSE OF	sund of 4
Turk	10,1	M 157	11. 80.	Y'80	Tura merus Tu man la
Jung au	and	01 2001	1	10	auge meane Tu range fre.
				and the hole december we	while how
					sally in this
					The state of the s
A A	212	M spe	9	Page	No:5 San: 81

	State of the state	Page No.]		
A second second		Date	J		
,		7:12			
(04 C.)	Basic Code Diagram & VI	IDL.			
	1 1				
		1 17 to 1.	1		
1.	LIBEARY -	The state of the s			
	dularatione		-		
	- Calain allow	-			
		1.1			
A	THIT IT I	Basic VHDL Code			
,	LENITY	Basil VIII Cock			
		The second of th			
		· ·			
	ARCHITCHTURG				
-4	ARCHITCE TUECH	to the bay of the last			
	Rans O. A. Blankadan	to divinition on la class	pol - 0 - 0		
	Basic bulding blocks of M.	the assurption commission	agua uto		
	five groups.				
	Entity x 1 david a	H. Xi			
	brilisture				
	Parkage 1				
	Configuration	District - property			
	Library				
N NA	A A . 1.0- 1	0 0 0 0	0		
	A digital system is usually designed as a luis orchial collection module. Pack module corresponds to a design entity in VHDL. Each design entry has two parts.				
	Collulion moduler. Vach	modere correspondi to a	anigu		
	entity in VHDL. Each au	ign emby has two parts.	4.9		
- Kan	*				
Section 1					