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G H Raisoni College of Engineering and Management, Pune

(An Autonomous Institution)
F.Y B. Tech (Engineering)
SECOND Term (2020-21)
CAE-II (2020 Pattern)

Modeling of Digital Circuits (UECL106)

[Time: 1 Hour] **[Max. Marks: 15]**

COURSE OUTCOME:

Upon successful completion of this course, student will be able to:

1. Solve the problems on Number system codes and their conversions.
2. Create and design canonical logic forms.
3. To demonstrate basic knowledge VHDL fundamentals.
4. Design VHDL Programs.
5. Design real time digital applications.

Instructions to the candidates:

1. (CO3/CO4) at the beginning of question/sub question indicates the course outcome related to the question.
2. All questions compulsory.
3. Neat diagrams must be drawn wherever necessary.
4. Figures to the right indicate full marks.
5. Assume suitable data, if necessary.

CO	*Sub Questions*		*Marks*
CO3	*a)*	Draw a combination circuits for a full adder and explain it in detail with truth table.	[2]
		OR	
	a)	Draw a combination circuits for a half adder and explain it in detail with truth table.	[2]
	b)	Differentiate the 1:2 Demux and 2:1 Mux using symbol, diagram, basic logic gates, truth table, applications, inputs/outputs.	[3]
	c)	What is the latch in flip flops? Explain S-R flip flop with block diagram and truth table.	[3]
CO4	*a)*	Explain VHDL in short?	[2]
	b)	Explain the basic attributes in VHDL.	[2]
	c)	Draw and explain fundamental sections of basic VHDL codes.	[3]