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G H Raisoni College of Engineering & Management
Wagholi, Pune
CAE-II SUMMER 2021

Department F.Y B.Tech
Term/Section Term II Date of exam: 22/07/2021
Subject Name Modeling of digital Circuit (UECL103)
Roll NO: 170 Name: Swayam Tirode
Registration No: 2020AIFT1101047

CO3 a) The half adder circuit has two inputs: A and B, which add two input digits and generate a carry and a sum.
It adds two binary digits where the input bits are termed as augend and addend and the result will be output one is the sum and the other is carry.

To perform sum operation, XOR is applied to both the two inputs and AND gate is applied to both inputs to produce carry.

The 2-bit half adder truth table is as below:

Input		Sum	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

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0+0 = 0
0+1 = 1
1+0 = 1
1+1 = 10

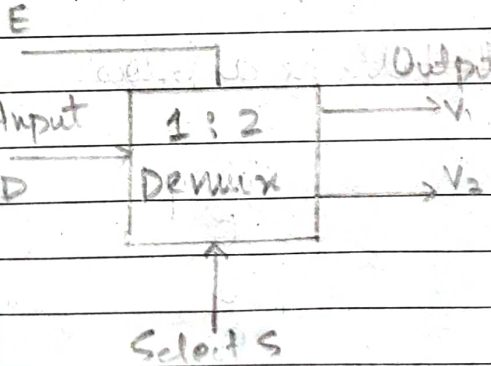
Thus are the least possible single bit combinations. But the result for 1+1 is 10, the sum must be re-written as a 2-bit output. Thus the equation can be written as:

0+0 = 00
0+1 = 01
1+0 = 01
1+1 = 10

The output 1 of 10 is carry-out 'COUT' is the normal output and carry is the carry-out.

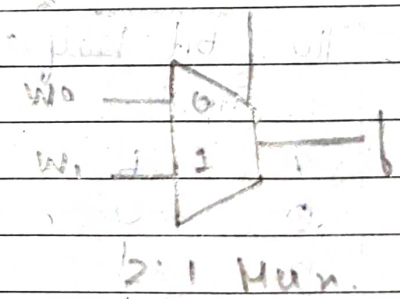
b.) 1:2 Demux

(i) Symbol –



2:1 Mux

(i) Symbol –



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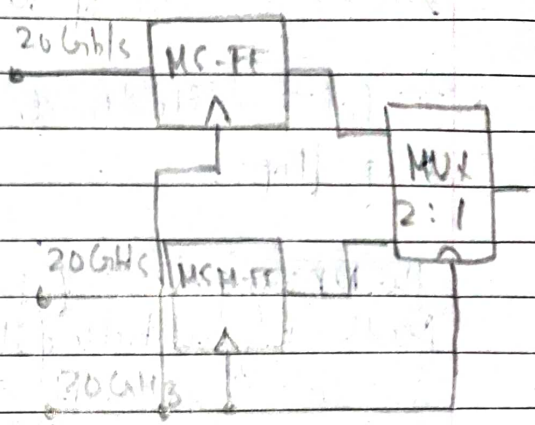
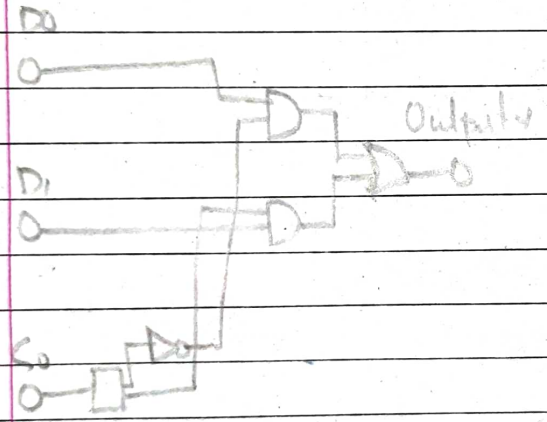
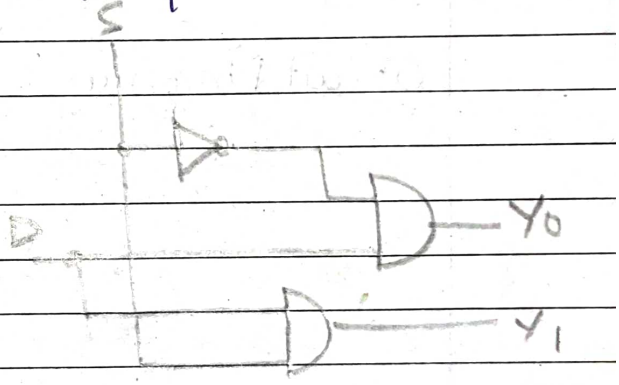
(ii) Diagram.



iii) Logic Gate (2:1 Mux).



(ii) logic Gate (1-to-2 Demulti



Truth Table (2 to 1 - Multiplexer circuit).

Inputs			Q
A	I_1	I_0	
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

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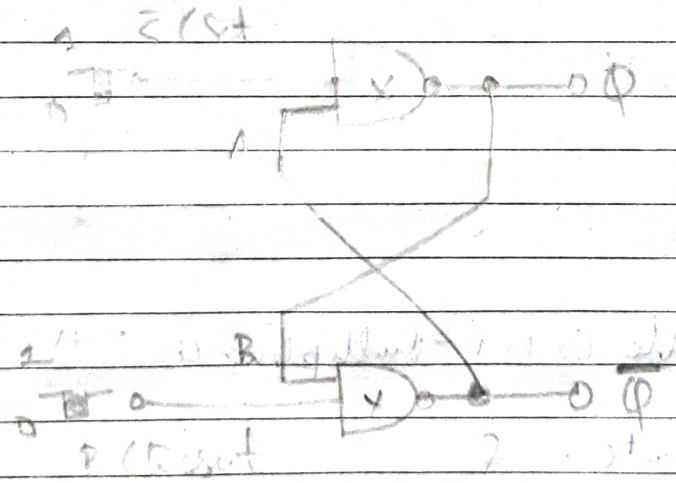
(03 c.) A latch is a memory element. It is formed by the interconnection of logic gates.

The latch with the clock signal provided is known as Flip-flops.

The NAND gate SR flip flop is a basic flip flop which provides feedback from both of its outputs back to its opposing input. This circuit is used to store the single data bit in the memory circuit. So, the SR flip flop has total 3 inputs i.e., 'S' and 'R' and current output 'Q'.

Circuit Diagram:



Truth Table: →

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State	S	R	Q	Q'	Description
Set	1	0	0	1	Set Q'>>1
	1	1	0	1	No change
Reset	0	1	1	0	Reset Q'>>0
	1	1	1	0	No change
Invalid	0	0	1	1	Invalid Condition.

(Q4 a.) VHDL stands for very-high speed integrated circuit hardware description language. It is a programming language used to model a digital system by dataflow, behavioral and structural style of modeling. This language was first introduced in 1981 for the department of defense (DOD) under the VHSIC program.

b.) There are some predefined attributes for scalar types,

Name	Definition
x'high	The upper bound of x.
x'low	The lower bound of x.
x'left	The leftmost bound of x.
x'right	The rightmost bound of x.

They are also for array Eg: x'range means the range for x.

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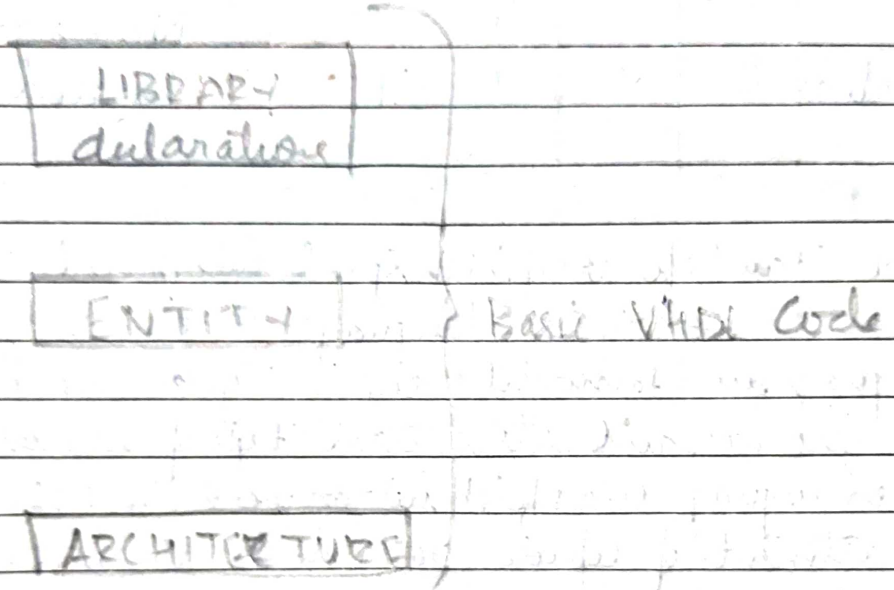
(Q4 c.) Basic Code Diagram of VHDL.



Basic building blocks of VHDL description can be classified into five groups:

Entity
Architecture
Package
Configuration
Library

A digital system is usually designed as a hierarchical collection modules. Each module corresponds to a design entity in VHDL. Each design entity has two parts.