SweeHua Law

SoC Architect

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sweehua

sweehua

Resume PDF

EDUCATION

BEng in Electrical & Electronic
University Malaya
2002 - 2006

LANGUAGES

Mandarin (Professional)

English (Professional)

Malay (Professional)

Teochew dialect (Native)

Hokkien dialect (Conversation)

Cantonese dialect (Conversation)

INTERESTS

Home Server Self-hosting

HIIT Training

CAREER PROFILE

FPGA Secure Configuration SoC Lead Architect, specialize in SoC System, embedded hardware-software system Integration/co-design, & FPGA architecture. Was a technical lead & team manager delivering FPGA designs & soft-IPs. Wide experience in various SoC & RISC processor architecture such as ARM, MIPS & NIOS, RISC-V, AMBA protocol, Network On Chip Interconnect, system Level debug. Strong engineering professional with a Bachelor of Engineering (BEng) focused in Electrical & Electronic Engineering.

EXPERIENCE

Lead FPGA Configuration SoC Architect

2018 - Present

PSG, Intel Corporation

Lead architect of FPGA configuration SoC - Secure Device Manager (SDM). SDM is a device root-of-trust processor system with security features that perform configuration bitstream authentication, encryption, integrity check and side channel protection, with various volatile & non-volatile key storage such as Fuse, BBRAM.

- Intel Structural Asic SDM
- Intel Agilex FPGA SDM

Functional Safety Silicon SoC Architect

2017

PSG, Intel Corporation

- Defined soc system architecture that meet ISO26262 ASIL-D specification, perform FMEA & FMEDA analysis.

FPGA Configuration SoC Architect

2016 - 2017

PSG, Intel Corporation

Intel Stratix 10 SDM Architect, defined SoC Interconnect architectture, CPU sub-system, crypto data path. SoC silicon debug & bring up expert.

Embedded Hardware Team Manager & Technical Lead

2009 - 2015

Altera Corporation (PSG, Intel Corporation)

Managing a team, responsible for design & enhance Soft-Processors & embedded soft-IP, develop various reference designs for FPGA.

- Develop & enhance Nios II Processors and 40 soft-IPs
- Build FPGA SoC Reference Design includes Ethernet RGMII/SGMII System, PCIe Gen2/Gen3 Rootport system, on both Nios II processor & ARM Processor, running Embedded Linux.
- Lead front-end RTL team to design Altera first harden SoC with ARM CPU, Cyclone V Hard Processor System
- Emulation Lead, to verify ARM SoC system.
- Micro-architect, and technical design lead to build an 8-thread barrel processor core, and then create event-driven packet processing system that has up to 32 cores.
- MIPS32 4KEc Verification Lead, to create a processor verification framework and automation, perform processor verification to obtain certification from MIPS Corporation for the MIPS32 4KEc architecture that Altera licensed.

FPGA Soft-IP Design & Verification Engineer

2006 - 2009

Altera Corporation (PSG, Intel Corporation)

FPGA Design Engineer in Altera Corporation.

- Nios II Soft-Processor verification in C & assembly language
- Develop various FPGA Soft-IP such as timer, SGDMA, GPIO, Uart, Jtag Uart, Half Rate DDR Memory Bridge. Perform functional simulation (directed test, BFM, constraint random testbench & OVM)
- FPGA refence design development & bring up.

SIDE PROJECTS

Niosduino - Arduino IDE tools & library to compile & download code to Nios II

Linux Kernel Patch - Submitting Patch to Linux Kernel

SKILLS & PROFICIENCY