Integration Manual –CmMtrCurr

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# Dependencies

## SWCs

|  |  |
| --- | --- |
| Module | Required Feature |
|  |  |

Note : Referencing the external components should be avoided in most cases. Only in unavoidable circumstance external components should be refered. Developer should track the references.

## Functions to be provided to Integration Project

CurrDQPer1

# Configuration

## Build Time Config

|  |  |  |
| --- | --- | --- |
| Modules | Notes |  |
| None |  |  |

## Configuration Files to be provided by Integration Project

CmMtrCurr\_Cfg.h ( Refer CmMtrCurr\_Cfg\_Template.h in tools folder)

(Data synchronization must be provided at the integration level between 2 ms periodic and Motor Control ISR Periodic’s)

Outputs from the CmMtrCurr (Motor Control ISR) periodic must be synchronized with the outputs from

ES51 Signal correction outputs (Motor Control ISR) and buffered and mapped to 2 ms Task.

### Da Vinci Config Configuration Changes

|  |  |  |
| --- | --- | --- |
| Constant | Notes | SWC |
| MTRCURRPHASEBC | PhaseB and Phase C used in Curr Measurement |  |
| MTRCURRPHASECB | PhaseC and Phase B used in Curr Measurement |  |
| MTRCURRPHASEAC | PhaseA and Phase C used in Curr Measurement |  |
| MTRCURRPHASECA | PhaseC and Phase A used in Curr Measurement |  |
| MTRCURRPHASEAB | PhaseA and Phase B used in Curr Measurement |  |
| MTRCURRPHASEBA | PhaseB and Phase A used in Curr Measurement |  |

Note: Only one of the configuration can be selected based on the requirements. Make sure order matches oreder in ADC data read ie MTRCURRPHASEBC - “BC” represents current\_1 is phase B and current\_2 is phase C .

### Manual Configuration Changes

|  |  |  |
| --- | --- | --- |
| Constant | Notes | SWC |
| none |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

# Integration

## Required Global Data Inputs

## Specific Include Path present

Yes

# Runnable Scheduling

This section specifies the required runnable scheduling.

|  |  |  |
| --- | --- | --- |
| Init | Scheduling Requirements | Trigger |
| CmMtrCurr\_Init | None | RTE |

|  |  |  |
| --- | --- | --- |
| Runnable | Scheduling Requirements | Trigger |
| CmMtrCurr\_Per2 | None | RTE(2MilliS) |
| CmMtrCurr\_Per1 | None | RTE(100 MilliS) |
| CurrDQPer1 | After DigMSB Signal processing | ISR (50MicroS) |
|  |  |  |
|  |  |  |

**.**

# Memory Mapping

## Mapping

|  |  |  |
| --- | --- | --- |
| Memory Section | Contents | Notes |
| CMMTRCURR\_START\_SEC\_VAR\_CLEARED\_16 |  |  |
| CMMTRCURR\_START\_SEC\_VAR\_CLEARED\_8 |  |  |
| CMMTRCURR\_START\_SEC\_VAR\_CLEARED\_BOOLEAN |  |  |
| CMMTRCURR\_START\_SEC\_VAR\_CLEARED\_32 |  |  |
| SA\_CMMTRCURR\_CODE |  |  |
| RTE\_START\_SEC\_SA\_CMMTRCURR\_APPL\_CODE |  |  |

\* Each …START\_SEC… constant is terminated by a …STOP\_SEC… constant as specified in the AUTOSAR Memory Mapping requirements.

## Usage

|  |  |  |
| --- | --- | --- |
| Feature | RAM | ROM |
|  |  |  |

Table 1: ARM Cortex R4 Memory Usage

## RTE NvM Blocks

|  |
| --- |
| Block Name |
| None |

Note : Size of the NVM block if configured in developer

## Non RTE NvM Blocks

|  |
| --- |
| Block Name |
| None |

Note : Size of the NVM block if configured in developer

# Compiler Settings

## Preprocessor MACRO

None

## Optimization Settings

None

# Revision Control Log

|  |  |  |  |
| --- | --- | --- | --- |
| **Rev #** | **Change Description** | **Date** | **Author** |
| 1 | Initial version | 7-Sep- 13 | nzt9hv |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |