Integration Manual --

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# Dependencies

## SWCs

|  |  |
| --- | --- |
| Module | Required Feature |
| CDD\_Data | Global variables for DC Phs Comp (from PwmCdd) |

## Configuration Files to be provided by Integration Project

None

## Functions to be provided by Integration Project

None

# Configuration

## Build Time Config

|  |  |  |
| --- | --- | --- |
| Constant | Notes | SWC |
|  |  |  |

## Generator Config

|  |  |  |
| --- | --- | --- |
| Constant | Notes | SWC |
|  |  |  |

# Integration

## Global Data

The following global symbols must be defined in CDD\_Data.c and .h (populated by PwmCdd):

* uint16: CDD\_DCPhsComp\_Cnt\_G\_u16[3]
* uint16: CDD\_PWMPeriod\_Cnt\_G\_u16

## Component Conflicts

This component replaces an existing NHET component. The ePWM component contains the NHET program specific to ePWM operation. In addition, the Ap\_ePWM2 developer component replaces the Ap\_Nhet2 component.

## Include Path

The “include” directory of this SWC needs to be included in the integration project include search path.

## ADC2 Changes

The ePWM module must be configured to start ADC conversions for the ADC2 module. This is configured by setting the following register values for the ADC2 module:

* G0SRC = 3 (EPWM\_A1)
* G1SRC = 1 (EPWM\_B)

This is done in parallel with pin multiplexing changes to route the appropriate SOCA and SOCB signals to the ADC2 module. See FDD 33E for more information.

## Configurator Changes

### DIO and IOHwAb

If NHET was previously used to generate PWM signals, reassignments are required (as the ePWM outputs will conflict with assigned DIO pins). This is hardware-dependent; refer to the program’s Resource Allocation sheet or schematic. The following pins are used by ePWM and the ePWM-specific NHET on the TMS570LS1227 PGE (144 pin) package (see the datasheet for more information):

|  |  |
| --- | --- |
| Pin | Function |
| 6 | N2HET1[11], MIBSPI3NCS[4], **N2HET2[18]**, ETPWM1SYNCO |
| 14 | GIOA[5], EXTCLKIN, **ETPWM1A** |
| 15 | GIOA[6], N2HET2[4], **ETPWM1B** |
| 22 | GIOA[7], N2HET2[6], **ETPWM2A** |
| 23 | N2HET1[1], SPI4ENA, **N2HET2[8]** |
| 24 | N2HET1[3], SPI4NCS[0], **N2HET2[10]** |
| 25 | N2HET1[0], SPI4CLK, **ETPWM2B** |
| 30 | N2HET1[2], SPI4SIMO, **ETPWM3A** |
| 31 | N2HET1[5], SPI4SOMI, N2HET2[12], **ETPWM3B** |
| 33 | N2HET1[7], N2HET2[14], **ETPWM7B** |

### Port

#### Pin Direction Settings

The changes in DIO (hardware-dependent) may require updates to the pin direction and other settings for the newly configured DIO signals.

#### Multiplexing Changes

Several multiplexing options must be configured for both external routing (peripherals to pins) and internal routing (peripherals to peripherals).

The following changes must be made within configurator:

* Multiplexing for DIO changes (hardware-dependent)
* Multiplexing for NHET component change
  + This should result in PINMUX1[8-15] being set to 0x04
  + While N2HET2[8] and [10] can be configured, configurator does not generate these values correctly (see the manual configuration below)
* ADC Trigger Table – select ADC Trigger Table 2
  + This should result in PINMUX30[0-7] being set to 0x02

The following changes must be made with manual edits to Port\_PBcfg.c:

|  |  |  |  |
| --- | --- | --- | --- |
| Register | Bits | Value | Selected Option |
| PINMUX2 | 24-31 | 0x04 | ETPWM1A |
| PINMUX3 | 16-23 | 0x04 | ETPWM1B |
| PINMUX4 | 0-7 | 0x04 | ETPWM2A |
| PINMUX4 | 16-23 | 0x10 | N2HET2[8] (configurator errata) |
| PINMUX4 | 24-31 | 0x10 | N2HET2[10] (configurator errata) |
| PINMUX5 | 0-7 | 0x04 | ETPWM2B |
| PINMUX5 | 8-15 | 0x04 | ETPWM3A |
| PINMUX5 | 16-23 | 0x08 | ETPWM3B |
| PINMUX6 | 0-7 | 0x10 | ETPWM7B |
| PINMUX31\* | 16-31 | 0x0202 | ADC2 Trigger Event Selection |
| PINMUX35\* | 24-31 | 0x00 | SOC4A\_SEL cleared |
| PINMUX37\* | 0-31 | 0x01010102 | Sync time bases, enable clocks for ePWM 0 to 3 |
| PINMUX38\* | 0-31 | 0x01000001 | Enable clocks for ePWM 4 and 7 |

\* Configurator does not define symbols for these registers. Define the following symbols manually:

#define PORT\_BASE\_ADDR\_PINMUX\_31 ((Port\_RegisterPtrType)(0xFFFFEB8C))

#define PORT\_BASE\_ADDR\_PINMUX\_35 ((Port\_RegisterPtrType)(0xFFFFEB9C))

#define PORT\_BASE\_ADDR\_PINMUX\_37 ((Port\_RegisterPtrType)(0xFFFFEBA4))

#define PORT\_BASE\_ADDR\_PINMUX\_38 ((Port\_RegisterPtrType)(0xFFFFEBA8))

A default value of 0x01 should be used for bytes not otherwise defined.

# Runnable Scheduling

This section specifies the required runnable scheduling.

|  |  |  |
| --- | --- | --- |
| Runnable | Scheduling Requirements | Trigger |
| Nhet\_Init1 | Place in EcuStartup\_Init1 (EcuStartup.c) along with ePWM\_Init1, following the memory initialization routine SchM\_InitMemory. | Init |
| ePWM\_Init1 | Place in EcuStartup\_Init1 (EcuStartup.c) along with Nhet\_Init1, following the memory initialization routine SchM\_InitMemory. | Init |
| ePWM\_Per1 | Must be placed in the motor control ISR, following PwmCdd (or whichever function populates the global variables used by ePWM). | Cyclic (ISR) |
| ePWM2\_Trns1 | Schedule on transition into the WARMINIT state | Event (RTE) |
| ePWM2\_Trns2 | Schedule on transition into the DISABLE state | Event (RTE) |

# Memory Mapping

## Mapping

|  |  |  |
| --- | --- | --- |
| Memory Section | Contents | Notes |
| EPWM\_START\_SEC\_CODE | Runnable Code |  |
| NHET\_START\_SEC\_CODE | Runnable Code |  |

\* Each …START\_SEC… constant is terminated by a …STOP\_SEC… constant as specified in the AUTOSAR Memory Mapping requirements.

## Usage

|  |  |  |
| --- | --- | --- |
| Feature | RAM | ROM |
| Full driver |  |  |

Table 1: ARM Cortex R4 Memory Usage

# Revision Control Log

|  |  |  |  |
| --- | --- | --- | --- |
| **Rev #** | **Change Description** | **Date** | **Author** |
| 1 | Initial version | 15-Feb-13 | OT |