Integration Manual – Digital Column Position Sensor

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# Dependencies

## SWCs

|  |  |
| --- | --- |
| Module | Required Feature |
| I2cNxtr | All functions |

Note : Referencing the external components should be avoided in most cases. Only in unavoidable circumstance external components should be refered. Developer should track the references.

## Global Functions(Non RTE) to be provided to Integration Project

None

# Configuration

## Build Time Config

|  |  |  |
| --- | --- | --- |
| Modules | Notes |  |
| None |  |  |

## 

## Configuration Files to be provided by Integration Project

### Da Vinci Parameter Configuration Changes

|  |  |  |
| --- | --- | --- |
| Parameter | Notes | SWC |
| None |  |  |

### DaVinci Interrupt Configuration Changes

|  |  |  |  |
| --- | --- | --- | --- |
| ISR Name | VIM # | Priority Dependency | Notes |
| None |  |  |  |

### Manual Configuration Changes

The following settings need to be configured in I2cNxtr\_Cfg.h – a template of which can be found in the include directory of the I2cNxtr component.

|  |  |  |
| --- | --- | --- |
| Constant | Notes | SWC |
| D\_COMMBUFFERSIZE\_CNT\_U08 | 3 | I2cNxtr |
| I2c\_Notification | DigColPsInt\_InterruptNotification | I2cNxtr |
| D\_I2CREG\_STRCPTR | i2cREG1 | I2cNxtr |
| D\_VCLK\_HZ\_F32 | Set to corresponding VCLK frequency, commonly 8000000.0 for a 160.0 MHz part. | I2cNxtr |

# Integration

## Required Global Data Inputs

None

## Required Global Data Outputs

None

## Specific Include Path present

Yes

# Runnable Scheduling

This section specifies the required runnable scheduling.

|  |  |  |
| --- | --- | --- |
| Init | Scheduling Requirements | Trigger |
| DigColPs\_Init1 | None | RTE(Init) |

|  |  |  |
| --- | --- | --- |
| Runnable | Scheduling Requirements | Trigger |
| DigColPs\_Per1 | Early in 2 ms task to minimize jitter | RTE (2 ms) |
| DigColPs\_Per2 | None | RTE (4 ms) |

**.**

# Memory Mapping

## Mapping

|  |  |  |
| --- | --- | --- |
| Memory Section | Contents | Notes |
| DIGCOLPS\_START\_SEC\_VAR\_CLEARED\_32 | float32 |  |
| DIGCOLPS\_START\_SEC\_VAR\_CLEARED\_16 | uint16 |  |
| DIGCOLPS\_START\_SEC\_VAR\_CLEARED\_8 | uint8, sint8 |  |
| DIGCOLPS\_START\_SEC\_VAR\_CLEARED\_BOOLEAN | Boolean |  |
| DIGCOLPS\_START\_SEC\_VAR\_CLEARED\_UNSPECIFIED | LPF32KSV\_Str |  |

\* Each …START\_SEC… constant is terminated by a …STOP\_SEC… constant as specified in the AUTOSAR Memory Mapping requirements.

## Usage

|  |  |  |
| --- | --- | --- |
| Feature | RAM | ROM |
| None |  |  |

Table 1: ARM Cortex R4 Memory Usage

## Non RTE NvM Blocks

|  |
| --- |
| Block Name |
| None |

Note : Size of the NVM block if configured in developer

## RTE NvM Blocks

|  |
| --- |
| Block Name |
| Rte\_Pim\_DigColPsEOL |

Note : Size of the NVM block if configured in developer

# Compiler Settings

## Preprocessor MACRO

None

## Optimization Settings

None

# Revision Control Log

|  |  |  |  |
| --- | --- | --- | --- |
| **Rev #** | **Change Description** | **Date** | **Author** |
| 1 | Initial component creation | 22-Aug-13 | Jared |