Integration Manual – I2cNxtr

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# Dependencies

## SWCs

|  |  |
| --- | --- |
| Module | Required Feature |
| None |  |

Note : Referencing the external components should be avoided in most cases. Only in unavoidable circumstance external components should be referred. Developer should track the references.

## Global Functions(Non RTE) to be provided to Integration Project

* I2c\_Init
* I2c\_Enable
* I2c\_Reset
* I2c\_SetupMasterTransmit
* I2c\_SetupMasterReceive
* I2c\_SwitchMasterReceive
* I2c\_SetCount
* I2c\_SetOwnAdd
* I2c\_SetSlaveAdd
* I2c\_SetFunctional
* I2c\_SetBaudrate
* I2c\_IsTxReady
* I2c\_SendByte
* I2c\_Send
* I2c\_IsRxReady
* I2c\_RxError
* I2c\_ReceiveByte
* I2c\_SetRecv
* I2c\_SetDirection
* I2c\_SetBit
* I2c\_GetBit
* I2c\_EnableNotification
* I2c\_DisableNotification
* I2c\_GenStartCond
* I2c\_GenStopCond
* I2c\_GetIntVect
* I2c\_GetStatus
* I2c\_SetStatus

# Configuration

## Build Time Config

|  |  |  |
| --- | --- | --- |
| Modules | Notes |  |
| None |  |  |

## 

## Configuration Files to be provided by Integration Project

### Da Vinci Parameter Configuration Changes

|  |  |  |
| --- | --- | --- |
| Parameter | Notes | SWC |
| None |  |  |

### DaVinci Interrupt Configuration Changes

|  |  |  |  |
| --- | --- | --- | --- |
| ISR Name | VIM # | Priority Dependency | Notes |
| Isr\_I2c | 66 | None | See comment below about enable/disable for very low priority interrupts. |

### Interrupt Enable/Disable Functions

Verify that interrupt 66 can be enabled and disabled in interrupts.c. It was found that only interrupts up to 63 could be enabled and disabled with current code. Below is a suggestion of how the enable function should look:

FUNC**(**void**,** INTERRUPT\_CODE**)** EnableIrq**(**uint8 irqRequest**)**

**{**

**if** **(**irqRequest **<** 32**)**

**{**

osWritePeripheral32**(**OS\_MEM\_AREA\_VIM**,** **(**osuint32**)&(**VIM**->**REQMASKSET0**),**

**(((**osuint32**)**1**)** **<<** **(**irqRequest**)));**

**}**

**else** **if** **(**irqRequest **<** 64**)**

**{**

irqRequest **-=** 32**;**

osWritePeripheral32**(**OS\_MEM\_AREA\_VIM**,** **(**osuint32**)&(**VIM**->**REQMASKSET1**),**

**(((**osuint32**)**1**)** **<<** **(**irqRequest**)));**

**}**

**else**

**{**

irqRequest **-=** 64**;**

osWritePeripheral32**(**OS\_MEM\_AREA\_VIM**,** **(**osuint32**)&(**VIM**->**REQMASKSET2**),**

**(((**osuint32**)**1**)** **<<** **(**irqRequest**)));**

**}**

**}**

And similarly for the disable function:

FUNC**(**void**,** INTERRUPT\_CODE**)** DisableIrq**(**uint8 irqRequest**)**

**{**

**if** **(**irqRequest **<** 32**)**

**{**

osWritePeripheral32**(**OS\_MEM\_AREA\_VIM**,** **(**osuint32**)&(**VIM**->**REQMASKCLR0**),**

**(((**osuint32**)**1**)** **<<** **(**irqRequest**)));**

**}**

**else** **if** **(**irqRequest **<** 64**)**

**{**

irqRequest **-=** 32**;**

osWritePeripheral32**(**OS\_MEM\_AREA\_VIM**,** **(**osuint32**)&(**VIM**->**REQMASKCLR1**),**

**(((**osuint32**)**1**)** **<<** **(**irqRequest**)));**

**}**

**else**

**{**

irqRequest **-=** 64**;**

osWritePeripheral32**(**OS\_MEM\_AREA\_VIM**,** **(**osuint32**)&(**VIM**->**REQMASKCLR2**),**

**(((**osuint32**)**1**)** **<<** **(**irqRequest**)));**

**}**

**}**

Additionally, EnableI2CInterrupt and DisableI2CInterrupt will need to be defined in interrupts.c in a fashion similar to the other Enable\* and Disable\* interrupts.

### Manual Configuration Changes

|  |  |  |
| --- | --- | --- |
| Constant | Notes | SWC |
| D\_COMMBUFFERSIZE\_CNT\_U08 | Transmit and receive buffer size in bytes. | I2cNxtr |
| I2c\_Notification | Callback notification issued when I2C interrupt occurs. | I2cNxtr |
| D\_I2CREG\_STRCPTR | Pointer to register structure containing I2C registers. | I2cNxtr |
| D\_VCLK\_HZ\_F32 | VCLK frequency used when calculating I2C baud rate. | I2cNxtr |

# Integration

## Required Global Data Inputs

None

## Required Global Data Outputs

None

## Specific Include Path present

Yes

# Runnable Scheduling

This section specifies the required runnable scheduling.

|  |  |  |
| --- | --- | --- |
| Init | Scheduling Requirements | Trigger |
| None | None | N/A |

|  |  |  |
| --- | --- | --- |
| Runnable | Scheduling Requirements | Trigger |
| None | None | N/A |

**.**

# Memory Mapping

## Mapping

|  |  |  |
| --- | --- | --- |
| Memory Section | Contents | Notes |
| I2CNXTR\_START\_SEC\_VAR\_CLEARED\_UNSPECIFIED | I2cTransferType |  |
|  |  |  |

\* Each …START\_SEC… constant is terminated by a …STOP\_SEC… constant as specified in the AUTOSAR Memory Mapping requirements.

## Usage

|  |  |  |
| --- | --- | --- |
| Feature | RAM | ROM |
| None |  |  |

Table 1: ARM Cortex R4 Memory Usage

## Non RTE NvM Blocks

|  |
| --- |
| Block Name |
| None |

Note : Size of the NVM block if configured in developer

## RTE NvM Blocks

|  |
| --- |
| Block Name |
| None |

Note : Size of the NVM block if configured in developer

# Compiler Settings

## Preprocessor MACRO

None

## Optimization Settings

None

# Revision Control Log

|  |  |  |  |
| --- | --- | --- | --- |
| **Rev #** | **Change Description** | **Date** | **Author** |
| 1 | Initial component creation | 22-Aug-13 | Jared |