Integration Manual – Absolute Handwheel Position – Turns Counter, I2C, and SensorlessVehicle Dynamics

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# Dependencies

## SWCs

|  |  |
| --- | --- |
| Module | Required Feature |
| <Name of SWC> | <Addition of global data, function\*. |

Note : Referencing the external components should be avoided in most cases. Only in unavoidable circumstance external components should be refered. Developer should track the references.

## Global Functions(Non RTE) to be provided to Integration Project

None

# Configuration

## Build Time Config

|  |  |  |
| --- | --- | --- |
| Modules | Notes |  |
| None |  |  |

## Configuration Files to be provided by Integration Project

Ap\_AbsHwPos\_Cfg.h (generated using Ap\_AbsHwPos\_Cfg.h.tt)

### Da Vinci Parameter Configuration Changes

|  |  |  |
| --- | --- | --- |
| Parameter | Notes | SWC |
| AbsHwPosGeneral\AbsHwPosCPEnable | Enable checkpoints if needed | AbsHwPos |

### DaVinci Interrupt Configuration Changes

|  |  |  |  |
| --- | --- | --- | --- |
| ISR Name | VIM # | Priority Dependency | Notes |
| <None> |  |  |  |

### Manual Configuration Changes

|  |  |  |
| --- | --- | --- |
| Constant | Notes | SWC |
| <None> |  |  |

# Integration

## Required Global Data Inputs

CumMechMtrPosCRF\_Deg\_f32

AlignedCumMechMtrPosCRF\_Deg\_f32

TurnsCntrValidity\_Cnt\_u08

I2CHwAbsPos\_HwDeg\_f32

I2CHwAbsPosValid\_Cnt\_lgc

SensorlessHwPos\_HwDeg\_f32

SensorlessAuthority\_Uls\_f32

ComplError\_HwDeg\_f32

DiagStatusHwPosReducedPerf\_Cnt\_lgc

ManufMode\_Cnt\_enum

## Required Global Data Outputs

HandwheelPosition\_HwDeg\_f32

HandwheelAuthority\_Uls\_f32

RelHwPos\_HwDeg\_f32

HwPosSource\_Cnt\_u16

SrlComHwPos\_HwDeg\_f32

SrlComHwPosStatus\_Cnt\_u16

## Specific Include Path present

No

# Runnable Scheduling

This section specifies the required runnable scheduling.

|  |  |  |
| --- | --- | --- |
| Init | Scheduling Requirements | Trigger |
| AbsHwPos\_Init1 | Called from RTE before first call of periodic function | RTE at init |

|  |  |  |
| --- | --- | --- |
| Runnable | Scheduling Requirements | Trigger |
| AbsHwPos\_Per1 | Call before 2ms periodic that uses RelHwPos\_HwDeg\_f32 | RTE 2 ms |
| AbsHwPos\_Per2 | Call after 2ms periodic that outputs VDHwPos\_HwDeg\_f32 | RTE 2 ms |
| AbsHwPos\_Per3 | None | RTE 4 ms |
| AbsHwPos\_Per4 | None | RTE 10 ms |
| AbsHwPos\_SCom\_CustSetTrim | Common Manufacturing | On event |
| AbsHwPos\_SCom\_CustClrTrim | Common Manufacturing | On event |
| AbsHwPos\_SCom\_NxtSetTrim | Common Manufacturing | On event |
| AbsHwPos\_SCom\_NxtClearTrim | Common Manufacturing | On event |

**.**

# Memory Mapping

## Mapping

|  |  |  |
| --- | --- | --- |
| Memory Section | Contents | Notes |
| ABSHWPOS\_START\_SEC\_VAR\_CLEARED\_UNSPECIFIED |  |  |
| ABSHWPOS\_START\_SEC\_VAR\_CLEARED\_BOOLEAN |  |  |
| ABSHWPOS\_START\_SEC\_VAR\_CLEARED\_16 |  |  |
| ABSHWPOS\_START\_SEC\_VAR\_CLEARED\_32 |  |  |
| RTE\_START\_SEC\_AP\_ABSHWPOS\_APPL\_CODE |  |  |

\* Each …START\_SEC… constant is terminated by a …STOP\_SEC… constant as specified in the AUTOSAR Memory Mapping requirements.

## Usage

|  |  |  |
| --- | --- | --- |
| Feature | RAM | ROM |
| <Memmap usuage info> |  |  |

Table 1: ARM Cortex R4 Memory Usage

## Non RTE NvM Blocks

|  |
| --- |
| Block Name |
| <None > |

Note : Size of the NVM block if configured in developer

## RTE NvM Blocks

|  |
| --- |
| Block Name |
| EOLVehCntrOffset |

Note : Size of the NVM block if configured in developer

# Compiler Settings

## Preprocessor MACRO

<Define all the preprocessor Macros needed and conditions when needed>.

## Optimization Settings

<Define Optimization levels that are needed and conditions when needed>.

# Revision Control Log

|  |  |  |  |
| --- | --- | --- | --- |
| **Rev #** | **Change Description** | **Date** | **Author** |
| 1.0 | Initial version | 26-Nov-13 | KMC |
| 2.0 | Updated per ES5G rev 006 - Renamed the inputs VD\_HwPos and VD\_Authority to Sensorless\_HwPos and Sensorless\_Authority to match updated SF42 outputs | 22-Aug-2014 | SB |