Integration Manual - DigHwTrqSENT

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# Dependencies

## SWCs

|  |  |
| --- | --- |
| Module | Required Feature |
| <None> |  |

Note : Referencing the external components should be avoided in most cases. Only in unavoidable circumstance external components should be refered. Developer should track the references.

## Global Functions(Non RTE) to be provided to Integration Project

< None>

# Configuration

## Build Time Config

|  |  |  |
| --- | --- | --- |
| Modules | Notes |  |
| BC\_DIGHWTRQSENT\_FAULTINJECTIONPOINT | Fault injection points |  |

## Configuration Files to be provided by Integration Project

Sa\_DigHwTrqSENT\_Cfg.h for checkpoint enables

### Da Vinci Parameter Configuration Changes

|  |  |  |
| --- | --- | --- |
| Parameter | Notes | SWC |
| <None> |  |  |

### DaVinci Interrupt Configuration Changes

|  |  |  |  |
| --- | --- | --- | --- |
| ISR Name | VIM # | Priority Dependency | Notes |
| <None> |  |  |  |

### Manual Configuration Changes

|  |  |  |
| --- | --- | --- |
| Constant | Notes | SWC |
| <None> |  |  |

# Integration

## Required Global Data Inputs

T1\_HwNm\_f32 from FDD ES-34B

T2\_HwNm\_f32 from FDD ES-34B

## Required Global Data Outputs

HwTorque\_HwNm\_f32

SysCHwTorque\_HwNm\_f32

## Specific Include Path present

No

# Runnable Scheduling

This section specifies the required runnable scheduling.

|  |  |  |
| --- | --- | --- |
| Init | Scheduling Requirements | Trigger |
| DigHwTrqSENT\_Init1() | None | Init |

|  |  |  |
| --- | --- | --- |
| Runnable | Scheduling Requirements | Trigger |
| DigHwTrqSENT\_Per1 | After update of T1\_HwNm\_f32 and T2\_HwNm\_f32 | 2 ms |
| DigHwTrqSENT\_Per2 | None | 4 ms |
| DigHwTrqSENT\_Per3 | None | 100 ms |
| DigHwTrqSENT\_SCom\_ClrTrqTrim | triggered by server invocation for OperationPrototype <ClrTrqTrim> of PortPrototype <DigHwTrqSENT\_SCom> | On event |
| DigHwTrqSENT\_SCom\_SetTrqTrim | triggered by server invocation for OperationPrototype <SetTrqTrim> of PortPrototype <DigHwTrqSENT\_SCom> | On event |
| DigHwTrqSENT\_SCom\_TrimData | triggered by server invocation for OperationPrototype <TrimData> of PortPrototype <DigHwTrqSENT\_SCom> | On event |
| DigHwTrqSENT\_SCom\_WriteData | triggered by server invocation for OperationPrototype <WriteData> of PortPrototype <DigHwTrqSENT\_SCom> | On event |

**.**

# Memory Mapping

## Mapping

|  |  |  |
| --- | --- | --- |
| Memory Section | Contents | Notes |
| DIGHWTRQSENT\_START\_SEC\_VAR\_CLEARED\_32 |  |  |
| DIGHWTRQSENT\_START\_SEC\_VAR\_CLEARED\_UNSPECIFIED |  |  |
| DIGHWTRQSENT\_START\_SEC\_VAR\_SAVED\_ZONEH\_32 |  | Zone H EEPROM |

\* Each …START\_SEC… constant is terminated by a …STOP\_SEC… constant as specified in the AUTOSAR Memory Mapping requirements.

## Usage

|  |  |  |
| --- | --- | --- |
| Feature | RAM | ROM |
| <Memmap usuage info> |  |  |

Table 1: ARM Cortex R4 Memory Usage

## Non RTE NvM Blocks

|  |
| --- |
| Block Name |
| <None > |

Note : Size of the NVM block if configured in developer

## RTE NvM Blocks

|  |
| --- |
| Block Name |
| DigHwTrqSENTTrim |

Note : Size of the NVM block if configured in developer

# Compiler Settings

## Preprocessor MACRO

<Define all the preprocessor Macros needed and conditions when needed>.

## Optimization Settings

<Define Optimization levels that are needed and conditions when needed>.

# Revision Control Log

|  |  |  |  |
| --- | --- | --- | --- |
| **Rev #** | **Change Description** | **Date** | **Author** |
| 1 | Initial version | 01-Jul-13 | KMC |
| 2 | Updated per Design Review CR 11619 – Corrected Runnable Names – Removed “Sa\_” from Init, Per functions | 03-Mar-14 | SB |
| 3 | Turned on track changes and corrected rev 2 changes | 01-Apr-14 | SB |
| 4 | Implemented ES04C Rev 006 | 09-Jun-14 | SB |
| 5 | Implemented ES04C Rev 007 and added the function DigHwTrqSENT\_Scom\_WriteData | 08-Aug-14 | VS |