Integration Manual –

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# Dependencies

## SWCs

|  |  |
| --- | --- |
| Module | Required Feature |
| None |  |

## Global Functions(Non RTE) to be provided to Integration Project

< Global function (except the ones that are defined in RTE modules) that is defined in this component but used by other function>

# Configuration

## Build Time Config

|  |  |  |
| --- | --- | --- |
| Modules | Notes |  |
| None |  |  |

## 

## Configuration Files to be provided by Integration Project

<Configuration file that will generated from this components that will require Da Vinci Config generation or manual generation. Describe each parameter >

### Da Vinci Parameter Configuration Changes

|  |  |  |
| --- | --- | --- |
| Parameter | Notes | SWC |
| None |  |  |

### DaVinci Interrupt Configuration Changes

|  |  |  |  |
| --- | --- | --- | --- |
| ISR Name | VIM # | Priority Dependency | Notes |
| None |  |  |  |

### Manual Configuration Changes

|  |  |  |
| --- | --- | --- |
| Constant | Notes | SWC |
| None |  |  |

# Integration

## Required Global Data Inputs

ExpectedOnTimeA\_Cnt\_u32

ExpectedOnTimeB\_Cnt\_u32

ExpectedOnTimeC\_Cnt\_u32

LRPRCorrectedMtrPosCaptured\_Rev\_f32

LRPRModulationIndexCaptured\_Uls\_f32

LRPRPhaseadvanceCaptured\_Cnt\_s16

MeasuredOnTimeA\_Cnt\_u32

MeasuredOnTimeB\_Cnt\_u32

MeasuredOnTimeC\_Cnt\_u32

MotorVelMRFUnfiltered\_MtrRadpS\_f32

MtrElecMechPolarity\_Cnt\_s08

PDActivateTest\_Cnt\_lgc

MtrDrvrInitStart\_Cnt\_lgc

VswitchClosed\_Cnt\_lgc

## Required Global Data Outputs

SVDiag\_LowPhReasErrorAcc\_Cnt\_u16

SVDiag\_HighResPhsReasDisable\_u8

SVDiag\_LowResPhsReasDisable\_u8

SVDiag\_MtrDrvInitComp\_Cnt\_lgc

SVDiag\_GateDriveFltAcc\_Cnt\_u16

SVDiag\_GenGateDriveFltAcc\_Cnt\_u16

SVDiag\_OnStateFltAcc\_Cnt\_u16

## Specific Include Path present

None

# Runnable Scheduling

This section specifies the required runnable scheduling.

|  |  |  |
| --- | --- | --- |
| Init | Scheduling Requirements | Trigger |
| DigPhsReasDiag\_Init | Executed once after the RTE is started before first call of MtrDrvDiag\_Per1 | RTE (at Startup) |

|  |  |  |
| --- | --- | --- |
| Runnable | Scheduling Requirements | Trigger |
| DigPhsReasDiag\_Per1 | Not in OFF, DISABLE, or WARMINIT modes | Rte 2ms task |
| DigPhsReasDiag\_Trans1 | In OPERATE mode | On entering mode |
| MtrDrvDiag\_Per1 | Not in DISABLE or OFF modes | Rte 2ms task |
| MtrDrvDiag\_Per2 | Not in OPERATE or WARMINIT modes | Rte 2ms task |
| MtrDrvDiag\_Trns1 | In WARMINIT mode | On entering mode |

# Memory Mapping

## Mapping

|  |  |  |
| --- | --- | --- |
| Memory Section | Contents | Notes |
| < Memory mapping Info> |  |  |
| DIGPHSREASDIAG\_START\_SEC\_VAR\_CLEARED\_32 |  |  |
| DIGPHSREASDIAG\_START\_SEC\_VAR\_CLEARED\_BOOLEAN |  |  |
| DIGPHSREASDIAG\_START\_SEC\_VAR\_CLEARED\_16 |  |  |
| DIGPHSREASDIAG\_START\_SEC\_VAR\_CLEARED\_8 |  |  |
| MTRDRVDIAG\_START\_SEC\_VAR\_CLEARED\_32 |  |  |
| MTRDRVDIAG\_START\_SEC\_VAR\_CLEARED\_16 |  |  |
| MTRDRVDIAG\_START\_SEC\_VAR\_CLEARED\_BOOLEAN |  |  |
| MTRDRVDIAG\_START\_SEC\_VAR\_CLEARED\_UNSPECIFIED |  |  |

\* Each …START\_SEC… constant is terminated by a …STOP\_SEC… constant as specified in the AUTOSAR Memory Mapping requirements.

## Usage

|  |  |  |
| --- | --- | --- |
| Feature | RAM | ROM |
| Full |  |  |

Table 1: ARM Cortex R4 Memory Usage

## Non RTE NvM Blocks

|  |
| --- |
| Block Name |
| None |

Note : Size of the NVM block if configured in developer

## RTE NvM Blocks

|  |
| --- |
| Block Name |
| None |

Note : Size of the NVM block if configured in developer

# Compiler Settings

## Preprocessor MACRO

<Define all the preprocessor Macros needed and conditions when needed>.

## Optimization Settings

<Define Optimization levels that are needed and conditions when needed>.

# Revision Control Log

|  |  |  |  |
| --- | --- | --- | --- |
| **Rev #** | **Change Description** | **Date** | **Author** |
| 1 | Initial version | 3-Oct-13 | VT |