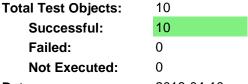
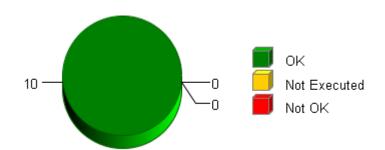


## **Summary**

## **Overall Test Object Results (including Coverage)**



**Date:** 2018-04-10 **Time:** 18:51:13+0530



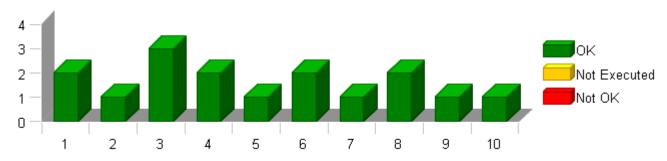
### **Selected Project Items**

Test Collection "CBD\_UnitTest"

#### **Used Test Environments**

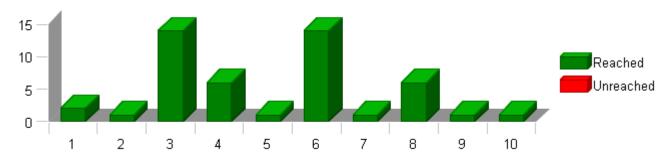
TI TMS 570 PLS UDE (Default)

## **Test Case Results for Each Test Object (without Coverage)**



The table above shows each test object on the x axis and the number of test cases of the respective test object on the y axis. Each bar is divided into passed, not executed and failed test cases. The test case results do not take into account any coverage result (i.e. if all test cases of a test object are passed in this table but the coverage is failed, the overall test object result will be failed).

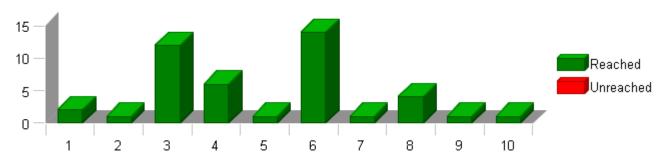
## Statement (C0) Coverage: Total Statements for Each Test Object



The table above shows each test object on the x axis and the number of statements of the respective test object on the y axis. Each bar is divided into reached statements (i.e. statements that have been executed during the test) and unreached statements.

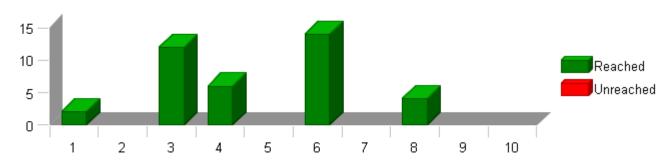


## Branch (C1) Coverage: Total Branches for Each Test Object



The table above shows each test object on the x axis and the number of branches of the respective test object on the y axis. Each bar is divided into reached branches (i.e. branches that have been executed during the test) and unreached branches.

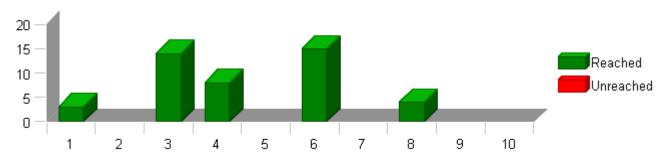
## **Decision Coverage: Total Decision Outcomes for Each Test Object**



The table above shows test objects on the x axis and the number of possible outcomes of all decisions of the respective test object on the y axis. To achieve full DC coverage, each decision must evaluate to both true and false.

Each bar is divided into reached and unreached decision outcomes.

## MC/DC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MC/DC coverage, each decision requires all contained atomic conditions to evaluate to both true and false independently of all other conditions. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

### **TEST OVERVIEW REPORT**



## **Test Object List**

The following table lists all test objects with their test case and coverage results. The cumulated results for modules, folders and test collections are also displayed, the indentation within the name column indicates the parent relationship of the elements.

Please note that only test objects are numbered within the first column. This number is referenced on the x axis within the overview charts for test case and coverage results available on previous pages (if included into the report).

No.	Name	C0	C1	DC	MC/DC	Test Cases Result
	Demlf	100 %	100 %	100 %	100 %	16 of 16 passed
	CBD_UnitTest	100 %	100 %	100 %	100 %	16 of 16 passed
	Demlf	100 %	100 %	100 %	100 %	16 of 16 passed
1	Demlf_CheckVoltageRange	100 %	100 %	100 %	100 %	2 of 2 passed
2	Demlf_DemShutdown	100 %	100 %	-	-	1 of 1 passed
3	Demlf_DTCStatusChanged	100 %	100 %	100 %	100 %	3 of 3 passed
4	Demlf EvaluateLogicalCondition	100 %	100 %	100 %	100 %	2 of 2 passed
5	Demlf Init	100 %	100 %	-	-	1 of 1 passed
6	Demlf Per	100 %	100 %	100 %	100 %	2 of 2 passed
7	Demlf_RestartDem	100 %	100 %	-	-	1 of 1 passed
8	Demlf SetEventStatus	100 %	100 %	100 %	100 %	2 of 2 passed
9	Demlf SetOperationCycleState	100 %	100 %	-	-	1 of 1 passed
10	Demlf VehSpdControl	100 %	100 %	-	-	1 of 1 passed

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2018-04-10, 18:49:26+0530





 Project
 Demlf

 Module
 Demlf

 Test Object
 Demlf\_SetEventStatus

## Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MC/DC Coverage	100 %

### **Statistics**

Total Testcases	2	
Successful	2	~
Failed	0	
Not Executed	0	

## **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config \TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\Demif\src\Ap_Demif.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I\$(PROJECTROOT)\Demlflutp\contract -I\$(PROJECTROOT)\Demlflutp\contract\Ap_Demlf -I\$ (PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include

Name	Text
Module 'Demi <b>f</b> '	Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_Demlf.c Code File(s) Version:3 Module Design Document:Demlf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):104 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference.

Attributes					
Name	Value				
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5				
Float Precision	9				
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj				
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src				
Linker File	\$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd				
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl				
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4				
Time Unit	cycles				
Timer Enabled	false				
Timer Prescale	0				
Timer Resolution	1				
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg				

2018-04-10, 18:49:26+0530



Attributes	
Name	Value
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



#### Test Case 1: Metric Test

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

TS 1.1 564.00 Cycles TS 1.2 553.00 Cycles

Description Vector Description:

TS 1.1 Shortest Execution Path=>if (RTE\_CONST\_NTC\_STATUS\_FAILED == EventStatus)=>False TS 1.2 Longest Execution Path=>if (RTE\_CONST\_NTC\_STATUS\_FAILED == EventStatus)=>True if (0u == (CTClnhibitionMask\_Cnt\_M\_u08[EventId] & CTClnhibitionState\_Cnt\_M\_u08))=>True

Test Step 1.1 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	0		
Dem_SetEventStatus()	0		
EventId	0		
EventStatus	0		
Name	Actual Value	Expected Value	Result
DemIf_SetEventStatus()	0	0	<b>✓</b>

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~	

Test Step 1.2 (Repeat Count = 1)			✓
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	0		
Dem_SetEventStatus()	0		
EventId	0		
EventStatus	1		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~	



#### Test Case 2: Range Test

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

CPU Cycles:

TS 2.1 579.00 Cycles
TS 2.2 550.00 Cycles
TS 2.2 550.00 Cycles
TS 2.3 567.00 Cycles
TS 2.4 536.00 Cycles
TS 2.5 518.00 Cycles
TS 2.6 536.00 Cycles
TS 2.7 536.00 Cycles
TS 2.8 518.00 Cycles
TS 2.9 536.00 Cycles
TS 2.10 536.00 Cycles
TS 2.11 518.00 Cycles
TS 2.12 536.00 Cycles
TS 2.13 536.00 Cycles
TS 2.13 536.00 Cycles
TS 2.14 31.00 Cycles
TS 2.14 31.00 Cycles

#### Vector Description: Description

TS 2.1All Min TS 2.2All Max TS 2.3EventId=>Min TS 2.4EventId=>Max
TS 2.5EventId=>Pos TS 2.6EventStatus=>Min TS 2.7EventStatus=>Max
TS 2.7EventStatus=>Max
TS 2.8EventStatus=>Pos
TS 2.9Dem\_SetEventStatus=>Min
TS 2.10Dem\_SetEventStatus=>Max
TS 2.11Dem\_SetEventStatus=>Mid

Test Step 2.1 (Repeat Count = 1)			✓.
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	0		
Dem_SetEventStatus()	0		
EventId	0		
EventStatus	0		
Name	Actual Value	Expected Value	Result
Demlf SetEventStatus()	0	0	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~

Test Step 2.2 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	255		
Dem_SetEventStatus()	255		
EventId	255		
EventStatus	3		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	255	255	✓

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	

Test Step 2.3 (Repeat Count = 1)			✓
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	0		
Dem_SetEventStatus()	0		
EventId	0		
EventStatus	1		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	<b>✓</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~



Test Step 2.4 (Repeat Count = 1)			V
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	231		
Dem_SetEventStatus()	13		
EventId	255		
EventStatus	2		
Name	Actual Value	Expected Value	Result
DemIf_SetEventStatus()	13	13	~

Test Step Call Trace					V
Α	ctual Function	Count	Expected Function	Count	Result
D	em_SetEventStatus	1	Dem_SetEventStatus	1	~

Test Step 2.5 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	12		
Dem_SetEventStatus()	127		
EventId	90		
EventStatus	1		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	127	127	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~

Test Step 2.6 (Repeat Count = 1)			✓
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	43		
Dem_SetEventStatus()	45		
EventId	34		
EventStatus	0		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	45	45	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~

Test Step 2.7 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	224		
Dem_SetEventStatus()	116		
EventId	56		
EventStatus	3		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	116	116	~

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~	



Test Step 2.8 (Repeat Count = 1)			
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	42		
Dem_SetEventStatus()	31		
EventId	67		
EventStatus	1		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	31	31	~

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~	

Test Step 2.9 (Repeat Count = 1)			
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	123		
Dem_SetEventStatus()	0		
EventId	12		
EventStatus	0		
Name	Actual Value	Expected Value	Result
DemIf_SetEventStatus()	0	0	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~

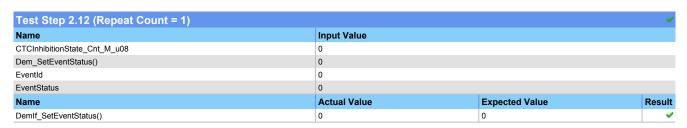
Test Step 2.10 (Repeat Count = 1)			
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	124		
Dem_SetEventStatus()	255		
EventId	45		
EventStatus	3		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	255	255	<b>✓</b>

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~	

Test Step 2.11 (Repeat Count = 1)			
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	31		
Dem_SetEventStatus()	113		
EventId	84		
EventStatus	1		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	113	113	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~





Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~	

Test Step 2.13 (Repeat Count = 1)			
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	255		
Dem_SetEventStatus()	21		
EventId	255		
EventStatus	3		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	21	21	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~

Test Step 2.14 (Repeat Count = 1)		✓	
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	128		
Dem_SetEventStatus()	2		
EventId	1		
EventStatus	1		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~

Test Step Call Trace			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

2018-04-10, 18:41:25+0530



Demlf\_DemShutdown

Project Demlf
Module Demlf

Test Object DemIf\_DemShutdown

## Instrumentation: Test Object Only

Statement (C0) Coverage 100 %
Branch (C1) Coverage 100 %

#### **Statistics**

Total Testcases	1	
Successful	1	~
Failed	0	
Not Executed	0	

### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_Demlf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config \TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\Demif\src\Ap_DemIf.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I\$(PROJECTROOT)\Demlf\utp\contract -I\$(PROJECTROOT)\Demlf\utp\contract\Ap_Demlf -I\$ (PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include

Comments/Descrip	tion/Specification
Name	Text
Module 'Demlf	Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_Demlf.c Code File(s) Version:3 Module Design Document:Demlf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):1051 Total RAM Used (Bytes):104 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference.

<b>Attributes</b>	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4
Time Unit	cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

2018-04-10, 18:41:25+0530



Demlf\_DemShutdown

## Test Case 1: Range Test

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

TS 1.1 536.00 Cycles

Description Vector Description:

TS1.1 Only Call trace is checked

## Test Step 1.1 (Repeat Count = 1)

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Dem_Shutdown	1	Dem_Shutdown	1	~

2018-04-10, 18:46:08+0530





 Project
 Demlf

 Module
 Demlf

 Test Object
 Demlf\_Init

## Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

#### **Statistics**

Total Testcases	1	
Successful	1	~
Failed	0	
Not Executed	0	

### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_Demlf\UnitTestEnv\config \TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\Demif\src\Ap_Demif.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I\$(PROJECTROOT)\Demlf\utp\contract -I\$(PROJECTROOT)\Demlf\utp\contract\Ap_Demlf -I\$ (PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include

Name	Text
Module 'Demif	Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_Demlf.c Code File(s) Version:3 Module Design Document:Demlf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):104 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference.

<b>Attributes</b>	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4
Time Unit	cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



#### Test Case 1: Range Test

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

TS 1.1 558.00 Cycles TS 1.2 558.00 Cycles TS 1.3 558.00 Cycles

Description Vector Description:

TS 1.1 Rte\_Call\_SystemTime\_GetSystemTime\_mS\_u32=>Min TS 1.2 Rte\_Call\_SystemTime\_GetSystemTime\_mS\_u32=>Max TS 1.3 Rte\_Call\_SystemTime\_GetSystemTime\_mS\_u32=>Pos

Test Step 1.1 (Repeat Count = 1)			✓
Name	Input Value		
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_Ge	etSystemTime_mS_u32_CurrentTime	
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_GetSystemTime\_mS\_u32\_CurrentTime$	arget_Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32_CurrentTime 0		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	0	0	~
CTCInhibitionBsi_Cnt_M_u32	0	0	~
CTCInhibitionCav_Cnt_M_u32	0	0	~
CTCInhibitionCmm_Cnt_M_u32	0	0	~
CTCInhibitionEsc_Cnt_M_u32	0	0	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	~

Test Step 1.2 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_Demlf_SystemTime_Ge	etSystemTime_mS_u32_CurrentTime	
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	4294967295		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	4294967295	4294967295	~
CTCInhibitionBsi_Cnt_M_u32	4294967295	4294967295	<b>✓</b>
CTCInhibitionCav_Cnt_M_u32	4294967295	4294967295	~
CTCInhibitionCmm_Cnt_M_u32	4294967295	4294967295	<b>✓</b>
CTCInhibitionEsc_Cnt_M_u32	4294967295	4294967295	•

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	~

Test Step 1.3 (Repeat Count = 1)			~
Name	Input Value		
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_Ge	etSystemTime_mS_u32_CurrentTime	
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_GetSystemTime\_mS\_u32\_CurrentTime$	arget_Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32_CurrentTime 200		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	200	200	~
CTCInhibitionBsi_Cnt_M_u32	200	200	~
CTCInhibitionCav_Cnt_M_u32	200	200	~
CTCInhibitionCmm_Cnt_M_u32	200	200	~
CTCInhibitionEsc Cnt M u32	200	200	<b>-</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte Call Ap Demlf SystemTime GetSystemTime mS u32	1	Rte Call Ap Demlf SystemTime GetSystemTime mS u32	1	~

2018-04-10, 18:47:39+0530





Project	Demlf
Module	Demlf
Test Object	Demlf_Per

## Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MC/DC Coverage	100 %

### **Statistics**

Total Testcases	2	
Successful	2	~
Failed	0	
Not Executed	0	

## **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config \TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\Demif\src\Ap_Demif.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I\$(PROJECTROOT)\Demlf\utp\contract -I\$(PROJECTROOT)\Demlf\utp\contract\Ap_Demlf -I\$ (PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include

Name	Text
Module 'Demi <b>f</b> '	Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_Demlf.c Code File(s) Version:3 Module Design Document:Demlf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):104 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference.

Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4
Time Unit	cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg

2018-04-10, 18:47:39+0530



DemIf\_Per

Attributes	
Name	Value
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



```
Specification

Performance Metrics (With "None"
Instrumentation and WithPS Environment)

CPU Cycles:

TS 1.1 4166.00 Cycles
TS 1.2 4110.00 Cycles
TS 1.2 4110.00 Cycles

TS 1.1 Shortest Execution Path=>if (ElapseTime_Cnt_T_u16 < k_EscActvTimeout_mS_u16)=>False
if (ElapseTime_Cnt_T_u16 < k_BsiActvTimeout_mS_u16)=>False
if (ElapseTime_Cnt_T_u16 < k_CavActvTimeout_mS_u16)=>False
if (ElapseTime_Cnt_T_u16 < k_CavActvTimeout_mS_u16)=>False
if (ElapseTime_Cnt_T_u16 < k_CavActvTimeout_mS_u16)=>False
if (ElapseTime_Cnt_T_u16 < k_CmmActvTimeout_mS_u16)=>False
if ((TRUE == BusOff_Cnt_T_lgc)=>False)
if (TRUE == ElectronicIntegration_Cnt_M_lgc)
if (TRUE == ElectronicIntegration_Cnt_T_u16 < k_EscActvTimeout_mS_u16)=>True
if (ElapseTime_Cnt_T_u16 < k_CavActvTimeout_mS_u16)=>True
```

Test Step 1.1 (Repeat Count = 1)			V	
Name	Input Value			
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_G	ET_signal		
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_D	otrmnElapsedTime_mS_u16_ElapsedT	ime	
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime			
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf	target Rte Inst Ap Demlf		
Rte_Mode_Ap_Demlf_SystemState_Mode()	0			
VehSpdControl_Cnt_M_lgc	0			
k_AasActvTimeout_mS_u16	0			
k_AasActvVBattMax_Volt_f32	0			
k_AasActvVBattMin_Volt_f32	0			
k_BsiActvTimeout_mS_u16	0			
k_BsiActvVBattMax_Volt_f32	0			
k_BsiActvVBattMin_Volt_f32	0			
k_CavActvTimeout_mS_u16	0			
k_CavActvVBattMax_Volt_f32	0			
k_CavActvVBattMin_Volt_f32	0			
k_CmmActvTimeout_mS_u16	0			
k_CmmActvVBattMax_Volt_f32	0			
k_CmmActvVBattMin_Volt_f32	0			
k_EscActvTimeout_mS_u16	0			
k_EscActvVBattMax_Volt_f32	0			
k_EscActvVBattMin_Volt_f32	0			
target_Demlf_Per_BatteryVoltage_Volt_f32.value	0			
target_Demlf_Per_BusOff_Cnt_lgc.value	0			
target_Demlf_Per_CTerm_Cnt_lgc.value	0			
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0			
target_Demlf_Per_EtatMt_Cnt_u08.value	0			
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0			
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime_ms_u16_ElapsedTime_u16_ElapsedTime_ms_u16_ElapsedTime_ms_u16_ElapsedTime_ms_u16_ElapsedTime_ms_u16_ElapsedTime_ms_u16_ElapsedTime_ms_u16_ElapsedTime_ms_u16_ElapsedTime_ms_u16_ElapsedTime_ms_u16_ElapsedTime_ms_u16_ElapsedTime_ms_u16_ElapsedTime_ms_u16_ElapsedTime_ms_u16_ElapsedTime_ms_u16_ElapsedTime_ms_u16_ElapsedTime_ms_u16_ElapsedTime_m	m 0			
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	0			
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32			
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc			
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc			
target_Rte_Inst_Ap_Demlf.Demlf_Per_ElectronicIntegration_Cnt_lgc	target_Demlf_Per_ElectronicIntegration_Cr	nt_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08			
Name	Actual Value	Expected Value	Result	
CTCInhibitionAas_Cnt_M_u32	0	0	-	
CTCInhibitionBsi_Cnt_M_u32	0	0	-	
CTCInhibitionCav_Cnt_M_u32	0	0	-	
CTCInhibitionCmm_Cnt_M_u32	0	0	<b>✓</b>	
CTCInhibitionEsc_Cnt_M_u32	0	0	-	
CTCInhibitionState_Cnt_M_u08	0	0	·	



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	•
DemIf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	•
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	•
Rte_Mode_Ap_Demlf_SystemState_Mode	1	Rte_Mode_Ap_Demlf_SystemState_Mode	1	<b>✓</b>
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	<b>✓</b>

Test Step 1.2 (Repeat Count = 1)			<b>√</b>
Name	Input Value		
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OF	P_GET_signal	
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTim	e_DtrmnElapsedTime_mS_u16_Elapse	edTime
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTim	e_GetSystemTime_mS_u32_CurrentTi	me
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	2		
VehSpdControl_Cnt_M_lgc	0		
k_AasActvTimeout_mS_u16	800		
k_AasActvVBattMax_Volt_f32	16		
k_AasActvVBattMin_Volt_f32	8		
k_BsiActvTimeout_mS_u16	600		
k_BsiActvVBattMax_Volt_f32	16		
k_BsiActvVBattMin_Volt_f32	8		
k_CavActvTimeout_mS_u16	800		
k_CavActvVBattMax_Volt_f32	16		
k_CavActvVBattMin_Volt_f32	8		
k CmmActvTimeout mS u16	600		
k CmmActvVBattMax Volt f32	16		
k CmmActvVBattMin Volt f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	19.9340992		
target_Demlf_Per_BusOff_Cnt_lgc.value	1		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_DemIf_Per_ElectronicIntegration_Cnt_Igc.value	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	0		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	1		
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_Elapsed	Tim 0		
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTim	e 3633311787		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt	_f32	
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_lgc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_Demif.Demif_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt_lgc		
target Rte Inst Ap Demlf.Demlf Per ElectronicIntegration Cnt Igc	target Demlf Per ElectronicIntegration	Cnt Igc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas Cnt M u32	3633311787	3633311787	-
CTCInhibitionBsi_Cnt_M_u32	3633311787	3633311787	•
CTCInhibitionCav Cnt M u32	3633311787	3633311787	-
CTCInhibitionCmm_Cnt_M_u32	3633311787	3633311787	<b>✓</b>
CTCInhibitionEsc Cnt M u32	3633311787	3633311787	-
CTCInhibitionState Cnt M u08	223	223	•

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	~
Demlf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	•
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_Demlf_SystemState_Mode	1	~
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~
Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16	5	Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16	5	<b>~</b>



#### **Test Case 2: Range Test**

#### Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

CPU Cycles:

CPU Cycles:

TS 2.1 4063.00 Cycles
TS 2.2 4089.00 Cycles
TS 2.3 4067.00 Cycles
TS 2.3 4067.00 Cycles
TS 2.5 4067.00 Cycles
TS 2.5 4067.00 Cycles
TS 2.6 4067.00 Cycles
TS 2.7 4067.00 Cycles
TS 2.8 4067.00 Cycles
TS 2.10 4067.00 Cycles
TS 2.11 4067.00 Cycles
TS 2.14 4067.00 Cycles
TS 2.14 4067.00 Cycles
TS 2.15 4067.00 Cycles
TS 2.14 4067.00 Cycles
TS 2.14 4051.00 Cycles
TS 2.15 4067.00 Cycles
TS 2.16 4029.00 Cycles
TS 2.17 4051.00 Cycles
TS 2.18 4051.00 Cycles
TS 2.21 4059.00 Cycles
TS 2.22 4051.00 Cycles
TS 2.23 4029.00 Cycles
TS 2.24 4051.00 Cycles
TS 2.25 4029.00 Cycles
TS 2.26 4051.00 Cycles
TS 2.27 4029.00 Cycles
TS 2.28 4029.00 Cycles
TS 2.29 4051.00 Cycles
TS 2.28 4029.00 Cycles
TS 2.29 4051.00 Cycles
TS 2.31 4029.00 Cycles
TS 2.32 4029.00 Cycles
TS 2.31 4029.00 Cycles
TS 2.32 4051.00 Cycles
TS 2.32 4051.00 Cycles
TS 2.32 4051.00 Cycles

#### Description

#### Vector Description:

TS 2.1 All Min TS 2.2All Max

TS 2.2All Max
TS 2.3Demlf\_Per\_BatteryVoltage\_Volt\_f32=>Min
TS 2.4Demlf\_Per\_BatteryVoltage\_Volt\_f32=>Max
TS 2.5Demlf\_Per\_BatteryVoltage\_Volt\_f32=>Pos
TS 2.6Demlf\_Per\_BatteryVoltage\_Volt\_f32=>Pos
TS 2.6Demlf\_Per\_ElectronicIntegration\_Cnt\_Igc=>Min
TS 2.7Demlf\_Per\_ElectronicIntegration\_Cnt\_Igc=>Max
TS 2.8Demlf\_Per\_BusOff\_Cnt\_Igc=>Min
TS 2.9Demlf\_Per\_BusOff\_Cnt\_Igc=>Max
TS 2.10Rte\_Call\_SystemTime\_GetSystemTime\_mS\_u32=>Min
TS 2.11Rte\_Call\_SystemTime\_GetSystemTime\_mS\_u32=>Max
TS 2.12Rte\_Call\_SystemTime\_GetSystemTime\_mS\_u32=>Pos
TS 2.13Rte\_Call\_SystemTime\_DtrmnElapsedTime\_mS\_u16=>Min
TS 2.14Rte\_Call\_SystemTime\_DtrmnElapsedTime\_mS\_u16=>Max
TS 2.15Rte\_Call\_SystemTime\_DtrmnElapsedTime\_mS\_u16=>Pos
TS 2.16VehSpdControl\_Cnt\_M\_Igc=>Min

TS 2.16VehSpdControl\_Cnt\_M\_lgc=>Min TS 2.17VehSpdControl\_Cnt\_M\_lgc=>Max TS 2.18k\_EscActvTimeout\_mS\_u16=>Min

TS 2.19k\_EscActvTimeout\_mS\_u16=>Max TS 2.20k\_EscActvTimeout\_mS\_u16=>Pos TS 2.21k\_BsiActvTimeout\_mS\_u16=>Min

TS 2.22k\_BsiActvTimeout\_mS\_u16=>Max

TS 2.23k\_BsiActvTimeout\_mS\_u16=>Pos TS 2.24k\_CavActvTimeout\_mS\_u16=>Min

TS 2.25k\_CavActvTimeout\_mS\_u16=>Max TS 2.26k\_CavActvTimeout\_mS\_u16=>Pos TS 2.27k\_AasActvTimeout\_mS\_u16=>Min

TS 2.28k\_AasActvTimeout\_mS\_u16=>Max

TS 2.29k\_AasActvTimeout\_mS\_u16=>Pos TS 2.30k\_CmmActvTimeout\_mS\_u16=>Min

TS 2.31k\_CmmActvTimeout\_mS\_u16=>Max TS 2.32k\_CmmActvTimeout\_mS\_u16=>Pos

Test Step 2.1 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	0
VehSpdControl_Cnt_M_lgc	0
k_AasActvTimeout_mS_u16	0
k_AasActvVBattMax_Volt_f32	0
k_AasActvVBattMin_Volt_f32	0
k_BsiActvTimeout_mS_u16	0
k_BsiActvVBattMax_Volt_f32	0
k_BsiActvVBattMin_Volt_f32	0
k_CavActvTimeout_mS_u16	0
k_CavActvVBattMax_Volt_f32	0
k_CavActvVBattMin_Volt_f32	0
k_CmmActvTimeout_mS_u16	0
k_CmmActvVBattMax_Volt_f32	0

2018-04-10, 18:47:39+0530



Name	Input Value		
k_CmmActvVBattMin_Volt_f32	0		
k_EscActvTimeout_mS_u16	0		
k_EscActvVBattMax_Volt_f32	0		
k_EscActvVBattMin_Volt_f32	0		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	0		
target_Demlf_Per_BusOff_Cnt_lgc.value	0		
target_DemIf_Per_CTerm_Cnt_lgc.value	0		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	0		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime\_mS_u16\_ElapsedT$	0		
target_Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32_CurrentTime	0		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_Demlf_Per_ElectronicIntegration_Cnt	_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	0	0	~
CTCInhibitionBsi_Cnt_M_u32	0	0	~
CTCInhibitionCav_Cnt_M_u32	0	0	~
CTCInhibitionCmm_Cnt_M_u32	0	0	~
CTCInhibitionEsc_Cnt_M_u32	0	0	~
CTCInhibitionState_Cnt_M_u08	0	0	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	~
Demlf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	~
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_Demlf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	<b>~</b>
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	~



Test Step 2.2 (Repeat Count = 1)			V
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_GE	T signal	
Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16(ElapsedTime)	target_Rte_Call_Ap_Demlf_SystemTime_Dt		
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_Demlf_SystemTime_Ge		
Rte Inst Ap Demlf	target_Rte_Inst_Ap_DemIf	,	
Rte_Mode_Ap_Demlf_SystemState_Mode()	4		
VehSpdControl_Cnt_M_lgc	1		
k AasActvTimeout mS u16	65535		
k_AasActvVBattMax_Volt_f32	31		
k_AasActvVBattMin_Volt_f32	31		
k_BsiActvTimeout_mS_u16	65535		
k_BsiActvVBattMax_Volt_f32	31		
k BsiActvVBattMin Volt f32	31		
k CavActvTimeout mS u16	65535		
k CavActvVBattMax Volt f32	31		
k CavActvVBattMin Volt f32	31		
k CmmActvTimeout mS u16	65535		
k_CmmActvVBattMax_Volt_f32	31		
k_CmmActvVBattMin_Volt_f32	31		
k_EscActvTimeout_mS_u16	65535		
k_EscActvVBattMax_Volt_f32	31		
k EscActvVBattMin Volt f32	31		
target Demlf Per BatteryVoltage Volt f32.value	31		
target Demlf Per BusOff Cnt Igc.value	1		
target Demlf Per CTerm Cnt Igc.value	1		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	15		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1		
target_Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	65535		
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	4294967295		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_Igc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration_Cnt	_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas Cnt M u32	0	0	~
CTCInhibitionBsi_Cnt_M_u32	0	0	•
CTCInhibitionCav Cnt M u32	0	0	-
CTCInhibitionCmm Cnt M u32	0	0	<b>V</b>
CTCInhibitionEsc Cnt M u32	0	0	-
CTCInhibitionState Cnt M u08	192	192	-

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	~
Demlf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	~
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	~
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	~

Test Step 2.3 (Repeat Count = 1)	🗸
Name	Input Value
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_Demlf_SystemState_Mode()	1
VehSpdControl_Cnt_M_lgc	0
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8





Name	Input Value		
k_CmmActvTimeout_mS_u16	600		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	0		
target_Demlf_Per_BusOff_Cnt_lgc.value	0		
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_DemIf_Per_ElectronicIntegration_Cnt_Igc.value	0		
target_DemIf_Per_EtatMt_Cnt_u08.value	0		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	1		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime\_msunfaces and the property of the pr$	35422		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_GetSystemTime\_mS\_u32\_CurrentTime$	616684576		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_DemIf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration_Cnt	_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	616684576	616684576	~
CTCInhibitionBsi_Cnt_M_u32	616684576	616684576	~
CTCInhibitionCav_Cnt_M_u32	616684576	616684576	~
CTCInhibitionCmm_Cnt_M_u32	616684576	616684576	~
CTCInhibitionEsc_Cnt_M_u32	616684576	616684576	~
CTCInhibitionState_Cnt_M_u08	0	0	~

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	~	
DemIf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	•	
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~	
Rte_Mode_Ap_Demlf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	~	
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~	
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	~	

Test Step 2.4 (Repeat Count = 1)	
Name	Input Value
Rte Call Ap Demlf Ignition OP GET(signal)	target Rte Call Ap Demlf Ignition OP GET signal
Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16(ElapsedTime)	target Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16 ElapsedTime
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_Demlf_SystemState_Mode()	1
VehSpdControl_Cnt_M_lgc	1
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_Demlf_Per_BatteryVoltage_Volt_f32.value	31
target_Demlf_Per_BusOff_Cnt_lgc.value	1
target_Demlf_Per_CTerm_Cnt_lgc.value	1
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0
target_Demlf_Per_EtatMt_Cnt_u08.value	0
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime\_mSulf\_Elap$	n 44450
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	2274712120
target_Rte_Inst_Ap_Demlf_Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt_lgc

2018-04-10, 18:47:39+0530



Name	Input Value			
target_Rte_Inst_Ap_Demlf.Demlf_Per_ElectronicIntegration_Cnt_lgc	target_Demlf_Per_Electronic	target_Demlf_Per_ElectronicIntegration_Cnt_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_C	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result	
CTCInhibitionAas_Cnt_M_u32	2274712120	2274712120	~	
CTCInhibitionBsi_Cnt_M_u32	2274712120	2274712120	✓	
CTCInhibitionCav_Cnt_M_u32	2274712120	2274712120	<b>✓</b>	
CTCInhibitionCmm_Cnt_M_u32	2274712120	2274712120	<b>✓</b>	
CTCInhibitionEsc_Cnt_M_u32	2274712120	2274712120	<b>✓</b>	
CTCInhibitionState_Cnt_M_u08	64	64	<b>✓</b>	

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	~
Demlf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	<b>✓</b>
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	<b>~</b>
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	<b>~</b>
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	<b>~</b>

Test Step 2.5 (Repeat Count = 1)			
Name	Input Value		
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal		
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_	_DtrmnElapsedTime_mS_u16_ElapsedT	ïme
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_	_GetSystemTime_mS_u32_CurrentTime	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	2		
VehSpdControl_Cnt_M_lgc	0		
k_AasActvTimeout_mS_u16	800		
k_AasActvVBattMax_Volt_f32	16		
k_AasActvVBattMin_Volt_f32	8		
k_BsiActvTimeout_mS_u16	600		
k_BsiActvVBattMax_Volt_f32	16		
k_BsiActvVBattMin_Volt_f32	8		
k_CavActvTimeout_mS_u16	800		
k_CavActvVBattMax_Volt_f32	16		
k_CavActvVBattMin_Volt_f32	8		
k_CmmActvTimeout_mS_u16	600		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	23.1233997		
target_Demlf_Per_BusOff_Cnt_lgc.value	1		
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	0		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime\_mS_u16\_ElapsedT$	13073		
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	1199317560		
target_Rte_Inst_Ap_DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f3	32	
target_Rte_Inst_Ap_DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_DemIf_DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf_DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration_0	Cnt_lgc	
target_Rte_Inst_Ap_DemIf_DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Resul
CTCInhibitionAas Cnt M u32	1199317560	1199317560	
CTCInhibitionBsi_Cnt_M_u32	1199317560	1199317560	
CTCInhibitionCav Cnt M u32	1199317560	1199317560	
CTCInhibitionCmm_Cnt_M_u32	1199317560	1199317560	
CTCInhibitionEsc Cnt M u32	1199317560	1199317560	
CTCInhibitionState Cnt M u08	192	192	



Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	~	
DemIf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	•	
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	•	
Rte_Mode_Ap_Demlf_SystemState_Mode	1	Rte_Mode_Ap_Demlf_SystemState_Mode	1	•	
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~	
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	•	

Test Step 2.6 (Repeat Count = 1)			<b>√</b>	
Name	Input Value			
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target Rte Call Ap Demlf Ignition	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal		
Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16(ElapsedTime)	target Rte Call Ap Demlf System	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime		
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target Rte Call Ap Demlf System	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime		
Rte Inst Ap Demlf	target Rte Inst Ap Demlf			
Rte Mode Ap Demlf SystemState Mode()	3			
VehSpdControl Cnt M Igc	1			
k AasActvTimeout mS u16	800			
k_AasActvVBattMax_Volt_f32	16			
k_AasActvVBattMin_Volt_f32	8			
k_BsiActvTimeout_mS_u16	600			
k_BsiActvVBattMax_Volt_f32	16			
k_BsiActvVBattMin_Volt_f32	8			
k CavActvTimeout mS u16	800			
k CavActvVBattMax Volt f32	16			
k_CavActvVBattMin_Volt_f32	8			
k CmmActvTimeout mS u16	600			
k CmmActvVBattMax Volt f32	16			
k CmmActvVBattMin Volt f32	8			
k_EscActvTimeout_mS_u16	1000			
k_EscActvVBattMax_Volt_f32	16			
k_EscActvVBattMin_Volt_f32	8			
target_Demlf_Per_BatteryVoltage_Volt_f32.value	19.0732002			
target_Demlf_Per_BusOff_Cnt_lgc.value	1			
target_Demlf_Per_CTerm_Cnt_lgc.value	0			
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0			
target Demlf Per EtatMt Cnt u08.value	1			
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0			
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_Elapse	dTim 11127			
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTir	ne 3539035437			
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_	Volt_f32		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc	<del>-</del>		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt_lgc			
target Rte Inst Ap Demlf.Demlf Per ElectronicIntegration Cnt Igc	target Demlf Per ElectronicIntegra			
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08	1		
Name	Actual Value	Expected Value	Result	
CTCInhibitionAas Cnt M u32	3539035437	3539035437	-	
CTCInhibitionBsi_Cnt_M_u32	3539035437	3539035437	•	
CTCInhibitionCav Cnt M u32	3539035437	3539035437	-	
CTCInhibitionCmm_Cnt_M_u32	3539035437	3539035437	•	
CTCInhibitionEsc Cnt M u32	3539035437	3539035437	•	
CTCInhibitionState Cnt M u08	64	64	•	

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	~	
Demlf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	•	
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~	
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_Demlf_SystemState_Mode	1	•	
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~	
Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16	5	Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16	5	<b>V</b>	

Test Step 2.7 (Repeat Count = 1)		<b>~</b>
Name	Input Value	
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime	
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	

2018-04-10, 18:47:39+0530



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Name	Input Value		
Rte Inst Ap Demlf	target_Rte_Inst_Ap_DemIf		
Rte Mode Ap Demlf SystemState Mode()	3		
VehSpdControl Cnt M lgc	0		
k_AasActvTimeout_mS_u16	800		
k_AasActvVBattMax_Volt_f32	16		
k_AasActvVBattMin_Volt_f32	8		
k_BsiActvTimeout_mS_u16	600		
k_BsiActvVBattMax_Volt_f32	16		
k_BsiActvVBattMin_Volt_f32	8		
k_CavActvTimeout_mS_u16	800		
k_CavActvVBattMax_Volt_f32	16		
k_CavActvVBattMin_Volt_f32	8		
k_CmmActvTimeout_mS_u16	600		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	14.1280003		
target_Demlf_Per_BusOff_Cnt_lgc.value	0		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	0		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1		
target Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16 ElapsedTim	34139		
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	2825399010		
target_Rte_Inst_Ap_Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_ElectronicIntegration_Cnt_lgc	target_Demlf_Per_ElectronicIntegration_C	nt_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Resul
CTCInhibitionAas_Cnt_M_u32	3539035437	3539035437	•
CTCInhibitionBsi_Cnt_M_u32	3539035437	3539035437	
CTCInhibitionCav_Cnt_M_u32	3539035437	3539035437	•
CTCInhibitionCmm_Cnt_M_u32	3539035437	3539035437	
CTCInhibitionEsc_Cnt_M_u32	3539035437	3539035437	•
CTCInhibitionState Cnt M u08	128	128	

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	~
DemIf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	~
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_Demlf_SystemState_Mode	1	Rte_Mode_Ap_Demlf_SystemState_Mode	1	~
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~
Rte Call An Demlf SystemTime DtrmnFlansedTime mS u16	5	Rte Call An Demlf SystemTime DtrmnFlansedTime mS u16	5	<b>V</b>

Test Step 2.8 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	4
VehSpdControl_Cnt_M_lgc	0
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16



Name	Input Value		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	15.1973		
target_Demlf_Per_BusOff_Cnt_lgc.value	0		
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_DemIf_Per_ElectronicIntegration_Cnt_Igc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	0		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	1		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime\_mSupplies and the property of the pr$	10391		
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	1774937490		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_ElectronicIntegration_Cnt_lgc	target_Demlf_Per_ElectronicIntegration_Cnt	_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	3539035437	3539035437	~
CTCInhibitionBsi_Cnt_M_u32	3539035437	3539035437	~
CTCInhibitionCav_Cnt_M_u32	3539035437	3539035437	<b>~</b>
CTCInhibitionCmm_Cnt_M_u32	3539035437	3539035437	~
CTCInhibitionEsc_Cnt_M_u32	3539035437	3539035437	~
CTCInhibitionState_Cnt_M_u08	0	0	~

Test Step Call Trace				~2
Actual Function	Count	Expected Function	Count	Result
Rte Call Ap Demlf SystemTime GetSystemTime mS u32	1	Rte Call Ap Demlf SystemTime GetSystemTime mS u32	1	/ V
Demlf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	~
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	~
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	<b>✓</b>

Name	Input Value		
Rte Call Ap Demlf Ignition OP GET(signal)	target Rte Call Ap Demlf Ignition OP GE	T signal	
Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16(ElapsedTime)	target Rte Call Ap Demlf SystemTime Dt		
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_Demlf_SystemTime_Ge	etSystemTime mS u32 CurrentTime	
Rte Inst Ap Demlf	target Rte Inst Ap Demlf		
Rte Mode Ap Demlf SystemState Mode()	3		
VehSpdControl Cnt M lgc	1		
k AasActvTimeout mS u16	800		
k AasActvVBattMax Volt f32	16		
k AasActvVBattMin Volt f32	8		
k_BsiActvTimeout_mS_u16	600		
k_BsiActvVBattMax_Volt_f32	16		
k_BsiActvVBattMin_Volt_f32	8		
k_CavActvTimeout_mS_u16	800		
k_CavActvVBattMax_Volt_f32	16		
k_CavActvVBattMin_Volt_f32	8		
k_CmmActvTimeout_mS_u16	600		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	7.63290024		
target_Demlf_Per_BusOff_Cnt_lgc.value	1		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	1		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	1		
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	10133		
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	2290771965		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt	t_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Resu
CTCInhibitionAas_Cnt_M_u32	2290771965	2290771965	
CTCInhibitionBsi Cnt M u32	2290771965	2290771965	

2018-04-10, 18:47:39+0530



Name	Actual Value	Expected Value	Result
CTCInhibitionCav_Cnt_M_u32	2290771965	2290771965	~
CTCInhibitionCmm_Cnt_M_u32	2290771965	2290771965	~
CTCInhibitionEsc_Cnt_M_u32	2290771965	2290771965	~
CTCInhibitionState_Cnt_M_u08	192	192	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	~
DemIf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	<b>✓</b>
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	~
Rte_Mode_Ap_Demlf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	<b>~</b>
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	~

Name	Input Value			
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Igni	tion OP GET signal		
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime			edTime	
Rte Call Ap Demlf SystemTime GetSystemTime mS u32(CurrentTime)		target_Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime target_Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32_CurrentTime		
Rte Inst Ap Demif	target Rte Inst Ap Demlf	terrime_GetGysterrime_m3_u32_Gurrentm	iiiie	
Rte Mode Ap Demlf SystemState Mode()	3			
VehSpdControl Cnt M Igc	0			
k AasActvTimeout mS u16	800			
k_AasActvVBattMax_Volt_f32	16			
k AasActvVBattMin Volt f32	8			
k BsiActvTimeout mS u16	600			
k BsiActvVBattMax Volt f32	16			
k BsiActvVBattMin Volt f32	8			
k CavActvTimeout mS u16	800			
k CavActvVBattMax Volt f32	16			
k CavActvVBattMin Volt f32	8			
k CmmActvTimeout mS u16	600			
k CmmActvVBattMax Volt f32	16			
k CmmActvVBattMin Volt f32	8			
k EscActvTimeout mS u16	1000			
k EscActvVBattMax Volt f32	16			
k EscActvVBattMin Volt f32	8			
target Demlf Per BatteryVoltage Volt f32.value	15.5703001			
target Demlf Per BusOff Cnt Igc.value	0			
target Demlf Per CTerm Cnt Igc.value	1			
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0			
target_Demlf_Per_EtatMt_Cnt_u08.value	1			
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0			
target_Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16_Elaps	·			
target_Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32_CurrentT				
target Rte Inst Ap Demlf.Demlf Per BatteryVoltage Volt f32	target Demlf Per BatteryVoltage	ne Volt f32		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_lgc	target_Demlf_Per_BusOff_Cnt_	· <del>-</del> -		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target Demlf Per CTerm Cnt			
target_Rte_Inst_Ap_Demlf.Demlf_Per_ElectronicIntegration_Cnt_lgc	target_Demlf_Per_ElectronicInte	-		
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_i			
Name	Actual Value	Expected Value	Resu	
	O Actual value	0	Resu	
CTCInhibitionAas_Cnt_M_u32	·	2290771965		
CTCInhibitionBsi_Cnt_M_u32	2290771965	0		
CTCInhibitionCav_Cnt_M_u32	0	-		
CTCInhibitionCmm_Cnt_M_u32	2290771965	2290771965		
CTCInhibitionEsc_Cnt_M_u32 CTCInhibitionState Cnt M u08	2290771965	2290771965 0		

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	~
Demlf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	~
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_Demlf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	~
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	~



Test Step 2.11 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
Rte Call Ap Demlf Ignition OP GET(signal)	target Rte Call Ap Demlf Ignition OP GE	T signal	
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime		
Rte Call Ap Demlf SystemTime GetSystemTime mS u32(CurrentTime)	target Rte Call Ap Demlf SystemTime GetSystemTime mS u32 CurrentTime		
Rte Inst Ap Demlf	target Rte Inst Ap Demlf		
Rte Mode Ap Demlf SystemState Mode()	0		
VehSpdControl Cnt M Igc	1		
k AasActvTimeout mS u16	800		
k_AasActvVBattMax_Volt_f32	16		
k_AasActvVBattMin_Volt_f32	8		
k_BsiActvTimeout_mS_u16	600		
k_BsiActvVBattMax_Volt_f32	16		
k_BsiActvVBattMin_Volt_f32	8		
k_CavActvTimeout_mS_u16	800		
k_CavActvVBattMax_Volt_f32	16		
k_CavActvVBattMin_Volt_f32	8		
k_CmmActvTimeout_mS_u16	600		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	2.43390012		
target_Demlf_Per_BusOff_Cnt_lgc.value	0		
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	0		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1		
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	17221		
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	4294967295		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_Demlf_Per_ElectronicIntegration_Cnt	t_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	4294967295	4294967295	~
CTCInhibitionBsi Cnt M u32	4294967295	4294967295	<b>✓</b>
CTCInhibitionCav_Cnt_M_u32	4294967295	4294967295	~
CTCInhibitionCmm_Cnt_M_u32	4294967295	4294967295	~
CTCInhibitionEsc_Cnt_M_u32	4294967295	4294967295	~
CTCInhibitionState_Cnt_M_u08	192	192	•

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	~
Demlf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	<b>✓</b>
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_Demlf_SystemState_Mode	1	<b>✓</b>
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~
Rte Call An Demlf SystemTime DtrmnFlansedTime mS u16	5	Rte Call An Demlf SystemTime DtrmnFlansedTime mS u16	5	<b>~</b>

Test Step 2.12 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	3
VehSpdControl_Cnt_M_lgc	1
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8

2018-04-10, 18:47:39+0530



Demlf\_Per

Name	Input Value		
k_CmmActvTimeout_mS_u16	600		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	7.41270018		
target_Demlf_Per_BusOff_Cnt_lgc.value	1		
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	0		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime\_mSu16\_Elap$	14136		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_GetSystemTime\_mS\_u32\_CurrentTime$	1533825676		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_DemIf_Per_BusOff_Cnt_Igc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt	_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1533825676	1533825676	~
CTCInhibitionBsi_Cnt_M_u32	1533825676	1533825676	~
CTCInhibitionCav_Cnt_M_u32	1533825676	1533825676	~
CTCInhibitionCmm_Cnt_M_u32	1533825676	1533825676	~
CTCInhibitionEsc_Cnt_M_u32	1533825676	1533825676	~
CTCInhibitionState_Cnt_M_u08	64	64	~

## Test Step Call Trace

2018-04-10, 18:47:39+0530



Name	Input Value			
target_Rte_Inst_Ap_Demlf.Demlf_Per_ElectronicIntegration_Cnt_lgc	target_Demlf_Per_Electronic	target_Demlf_Per_ElectronicIntegration_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_C	Cnt_u08		
Name	Actual Value	Expected Value	Result	
CTCInhibitionAas_Cnt_M_u32	3633311787	3633311787	✓	
CTCInhibitionBsi_Cnt_M_u32	3633311787	3633311787	✓	
CTCInhibitionCav_Cnt_M_u32	3633311787	3633311787	✓	
CTCInhibitionCmm_Cnt_M_u32	3633311787	3633311787	<b>✓</b>	
CTCInhibitionEsc_Cnt_M_u32	3633311787	3633311787	<b>✓</b>	
CTCInhibitionState_Cnt_M_u08	223	223	✓	

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	~
Demlf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	<b>✓</b>
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	~
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	~

Test Step 2.14 (Repeat Count = 1)			
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal		
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime		
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_G	etSystemTime_mS_u32_CurrentTime	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	1		
VehSpdControl_Cnt_M_lgc	0		
k_AasActvTimeout_mS_u16	800		
k_AasActvVBattMax_Volt_f32	16		
k_AasActvVBattMin_Volt_f32	8		
k_BsiActvTimeout_mS_u16	600		
k_BsiActvVBattMax_Volt_f32	16		
k_BsiActvVBattMin_Volt_f32	8		
k_CavActvTimeout_mS_u16	800		
k_CavActvVBattMax_Volt_f32	16		
k_CavActvVBattMin_Volt_f32	8		
k_CmmActvTimeout_mS_u16	600		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	7.89410019		
target_Demlf_Per_BusOff_Cnt_lgc.value	1		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	0		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime\_mSuperscript{Main_control_co$	65535		
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	2447925560		
target_Rte_Inst_Ap_DemIf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf_DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration_Cn	t_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Resu
CTCInhibitionAas Cnt M u32	2447925560	2447925560	
CTCInhibitionBsi Cnt M u32	2447925560	2447925560	
CTCInhibitionCav Cnt M u32	2447925560	2447925560	٠,
CTCInhibitionCmm Cnt M u32	2447925560	2447925560	,
CTCInhibitionEsc Cnt M u32	2447925560	2447925560	٠,
CTCInhibitionState Cnt M u08	64	64	



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	~
DemIf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	•
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	•
Rte_Mode_Ap_Demlf_SystemState_Mode	1	Rte_Mode_Ap_Demlf_SystemState_Mode	1	•
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	•

Test Step 2.15 (Repeat Count = 1)			V	
Name	Input Value			
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_G	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal		
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime			
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target Rte Call Ap Demlf SystemTime G	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime		
Rte Inst Ap Demlf	target Rte Inst Ap Demlf			
Rte_Mode_Ap_Demlf_SystemState_Mode()	4			
VehSpdControl_Cnt_M_lgc	1			
k_AasActvTimeout_mS_u16	800			
k_AasActvVBattMax_Volt_f32	16			
k_AasActvVBattMin_Volt_f32	8			
k_BsiActvTimeout_mS_u16	600			
k_BsiActvVBattMax_Volt_f32	16			
k_BsiActvVBattMin_Volt_f32	8			
k_CavActvTimeout_mS_u16	800			
k_CavActvVBattMax_Volt_f32	16			
k_CavActvVBattMin_Volt_f32	8			
k CmmActvTimeout mS u16	600			
k CmmActvVBattMax Volt f32	16			
k CmmActvVBattMin Volt f32	8			
k_EscActvTimeout_mS_u16	1000			
k_EscActvVBattMax_Volt_f32	16			
k_EscActvVBattMin_Volt_f32	8			
target_Demlf_Per_BatteryVoltage_Volt_f32.value	14.2438002			
target_Demlf_Per_BusOff_Cnt_lgc.value	1			
target_DemIf_Per_CTerm_Cnt_lgc.value	1			
target_DemIf_Per_ElectronicIntegration_Cnt_Igc.value	0			
target_DemIf_Per_EtatMt_Cnt_u08.value	0			
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	1			
target_Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime	m 1241			
target_Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32_CurrentTime	3091959789			
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32			
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target Demlf Per BusOff Cnt Igc			
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc			
target Rte Inst Ap Demlf.Demlf Per ElectronicIntegration Cnt Igc	target Demlf Per ElectronicIntegration Cr	nt Igc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08			
Name	Actual Value	Expected Value	Result	
CTCInhibitionAas Cnt M u32	2447925560	2447925560	_	
CTCInhibitionBsi_Cnt_M_u32	2447925560	2447925560	-	
CTCInhibitionCav Cnt M u32	2447925560	2447925560		
CTCInhibitionCmm_Cnt_M_u32	2447925560	2447925560	-	
CTCInhibitionEsc Cnt M u32	2447925560	2447925560	-	
CTCInhibitionState Cnt M u08	64	64	_	

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	~
Demlf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	•
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_Demlf_SystemState_Mode	1	•
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~
Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16	5	Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16	5	<b>V</b>

Test Step 2.16 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime

2018-04-10, 18:47:39+0530



Domin_i or			
Name	Input Value		
Rte Inst Ap Demlf	target_Rte_Inst_Ap_DemIf		
Rte Mode Ap Demlf SystemState Mode()	3		
VehSpdControl Cnt M lgc	0		
k AasActvTimeout mS u16	800		
k AasActvVBattMax Volt f32	16		
k_AasActvVBattMin_Volt_f32	8		
k_BsiActvTimeout_mS_u16	600		
k_BsiActvVBattMax_Volt_f32	16		
k_BsiActvVBattMin_Volt_f32	8		
k_CavActvTimeout_mS_u16	800		
k_CavActvVBattMax_Volt_f32	16		
k_CavActvVBattMin_Volt_f32	8		
k_CmmActvTimeout_mS_u16	600		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	5.31850004		
target_Demlf_Per_BusOff_Cnt_lgc.value	0		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	11		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1		
target Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16 ElapsedTim	51058		
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	3923762454		
target_Rte_Inst_Ap_Demlf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_Igc	target_DemIf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cr	t_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Resul
CTCInhibitionAas_Cnt_M_u32	3923762454	3923762454	•
CTCInhibitionBsi_Cnt_M_u32	3923762454	3923762454	•
CTCInhibitionCav_Cnt_M_u32	3923762454	3923762454	•
CTCInhibitionCmm_Cnt_M_u32	3923762454	3923762454	•
CTCInhibitionEsc_Cnt_M_u32	3923762454	3923762454	•
CTCInhibitionState Cnt M u08	0	0	

Name	Input Value
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	3
VehSpdControl_Cnt_M_lgc	1
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_Demlf_Per_BatteryVoltage_Volt_f32.value	5.31850004
target_Demlf_Per_BusOff_Cnt_lgc.value	0
target_DemIf_Per_CTerm_Cnt_lgc.value	1
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0
target_Demlf_Per_EtatMt_Cnt_u08.value	11
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_Elapsed	Tim 51058
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTim	e 3923762454
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32





Name	Input Value		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cr	nt_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cr	nt_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_ElectronicIntegration_Cnt_lgc	target_Demlf_Per_Electronicl	ntegration_Cnt_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cn	ıt_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	3923762454	3923762454	~
CTCInhibitionBsi_Cnt_M_u32	3923762454	3923762454	~
CTCInhibitionCav_Cnt_M_u32	3923762454	3923762454	~
CTCInhibitionCmm_Cnt_M_u32	3923762454	3923762454	~
CTCInhibitionEsc_Cnt_M_u32	3923762454	3923762454	~
CTCInhibitionState_Cnt_M_u08	64	64	~

Test Step 2.18 (Repeat Count = 1)			•	
Name	Input Value			
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_	GET_signal		
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_	target_Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime		
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_Demlf_SystemTime_	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime		
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf	target Rte Inst Ap Demlf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	4			
VehSpdControl_Cnt_M_lgc	1			
k_AasActvTimeout_mS_u16	800			
k_AasActvVBattMax_Volt_f32	16			
k_AasActvVBattMin_Volt_f32	8			
k_BsiActvTimeout_mS_u16	600			
k_BsiActvVBattMax_Volt_f32	16			
k_BsiActvVBattMin_Volt_f32	8			
k_CavActvTimeout_mS_u16	800			
k_CavActvVBattMax_Volt_f32	16			
k_CavActvVBattMin_Volt_f32	8			
k_CmmActvTimeout_mS_u16	600			
k_CmmActvVBattMax_Volt_f32	16			
k_CmmActvVBattMin_Volt_f32	8			
k_EscActvTimeout_mS_u16	0			
k_EscActvVBattMax_Volt_f32	16			
k_EscActvVBattMin_Volt_f32	8			
target_Demlf_Per_BatteryVoltage_Volt_f32.value	2.17689991			
target_Demlf_Per_BusOff_Cnt_lgc.value	0			
target_DemIf_Per_CTerm_Cnt_lgc.value	1			
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0			
target_DemIf_Per_EtatMt_Cnt_u08.value	7			
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0			
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_Elapsed	Tim 53021			
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTim	e 785100198			
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f3	32		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_lgc	target_Demlf_Per_BusOff_Cnt_lgc			
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt_lgc			
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_Demlf_Per_ElectronicIntegration_0	Cnt_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08			
Name	Actual Value	Expected Value	Resul	
CTCInhibitionAas Cnt M u32	785100198	785100198		
CTCInhibitionBsi Cnt M u32	785100198	785100198		
CTCInhibitionCav Cnt M u32	785100198	785100198		
CTCInhibitionCmm Cnt M u32	785100198	785100198		
CTCInhibitionEsc Cnt M u32	785100198	785100198		
CTCInhibitionState Cnt M u08	64	64		

Test Step 2.19 (Repeat Count = 1)	
Name	Input Value
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_Demlf
Rte_Mode_Ap_Demlf_SystemState_Mode()	2
VehSpdControl_Cnt_M_lgc	1
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600



Name	Input Value		
k BsiActvVBattMax Volt f32	16		
k BsiActvVBattMin Volt f32	8		
k CavActvTimeout mS u16	800		
k CavActvVBattMax Volt f32	16		
k CavActvVBattMin Volt f32	8		
k CmmActvTimeout mS u16	600		
k CmmActvVBattMax Volt f32	16		
k CmmActvVBattMin Volt f32	8		
k EscActvTimeout mS u16	65535		
k EscActvVBattMax Volt f32	16		
k EscActvVBattMin Volt f32	8		
target Demlf Per BatteryVoltage Volt f32.value	1.71889997		
target Demlf Per BusOff Cnt Igc.value	0		
target Demlf Per CTerm Cnt Igc.value	1		
target Demlf Per ElectronicIntegration Cnt Igc.value	1		
target Demlf Per EtatMt Cnt u08.value	14		
target Rte Call Ap Demlf Ignition OP GET signal	1		
target Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16 ElapsedTim	33512		
target_Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32_CurrentTime	1652918279		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_Demlf_Per_ElectronicIntegration_Cnt	_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1652918279	1652918279	~
CTCInhibitionBsi_Cnt_M_u32	1652918279	1652918279	~
CTCInhibitionCav_Cnt_M_u32	1652918279	1652918279	~
CTCInhibitionCmm_Cnt_M_u32	1652918279	1652918279	~
CTCInhibitionEsc_Cnt_M_u32	1652918279	1652918279	~
CTCInhibitionState_Cnt_M_u08	193	193	•

Name	Input Value			
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target Rte Call Ap Demlf Ignition OP GET signal			
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime			
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32_CurrentTime			
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf			
Rte_Mode_Ap_Demlf_SystemState_Mode()	4			
VehSpdControl_Cnt_M_lgc	1			
k_AasActvTimeout_mS_u16	800	800		
k_AasActvVBattMax_Volt_f32	16			
k_AasActvVBattMin_Volt_f32	8			
k_BsiActvTimeout_mS_u16	600	600		
k_BsiActvVBattMax_Volt_f32	16			
k_BsiActvVBattMin_Volt_f32	8			
k_CavActvTimeout_mS_u16	800			
k_CavActvVBattMax_Volt_f32	16			
k_CavActvVBattMin_Volt_f32	8			
k_CmmActvTimeout_mS_u16	600			
k_CmmActvVBattMax_Volt_f32	16			
k_CmmActvVBattMin_Volt_f32	8			
k_EscActvTimeout_mS_u16	1000			
k_EscActvVBattMax_Volt_f32	16			
k_EscActvVBattMin_Volt_f32	8			
target_Demlf_Per_BatteryVoltage_Volt_f32.value	7.58209991			
target_Demlf_Per_BusOff_Cnt_lgc.value	0			
target_Demlf_Per_CTerm_Cnt_lgc.value	1			
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	1			
target_Demlf_Per_EtatMt_Cnt_u08.value	8			
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0			
target Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16 ElapsedT	Tim 42407			
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	e 1905186906			
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc			
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt_lgc			
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_Demlf_Per_ElectronicIntegration_C	nt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08			
Name	Actual Value	Expected Value	Resu	
CTCInhibitionAas Cnt M u32	1905186906	1905186906		
CTCInhibitionBsi Cnt M u32	1905186906	1905186906		

2018-04-10, 18:47:39+0530



Name	Actual Value	Expected Value	Result
CTCInhibitionCav_Cnt_M_u32	1905186906	1905186906	<b>✓</b>
CTCInhibitionCmm_Cnt_M_u32	1905186906	1905186906	✓
CTCInhibitionEsc_Cnt_M_u32	1905186906	1905186906	<b>✓</b>
CTCInhibitionState_Cnt_M_u08	192	192	✓



Name	Input Value		
k CmmActvVBattMin Volt f32	8		
k EscActvTimeout mS u16	1000		
k EscActvVBattMax Volt f32	16		
k EscActvVBattMin Volt f32	8		
target Demlf Per BatteryVoltage Volt f32.value	2.67659998		
target Demlf Per BusOff Cnt Igc.value	1		
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0		
target_DemIf_Per_EtatMt_Cnt_u08.value	7		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1		
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime	58660		
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	3172092003		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_lgc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_Demlf_Per_ElectronicIntegration_Cnt_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	3172092003	3172092003	~
CTCInhibitionBsi_Cnt_M_u32	3172092003	3172092003	~
CTCInhibitionCav_Cnt_M_u32	3172092003	3172092003	~
CTCInhibitionCmm_Cnt_M_u32	3172092003	3172092003	~
CTCInhibitionEsc_Cnt_M_u32	3172092003	3172092003	~
CTCInhibitionState_Cnt_M_u08	66	66	~

Name	Input Value		
Rte Call Ap Demlf Ignition OP GET(signal)	Input Value		
Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16(ElapsedTime)	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal		
Rte Call Ap Demlf SystemTime GetSystemTime mS u32(CurrentTime)	target_Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime		
Rte_Can_Ap_Denni_System nine_GetSystem nine_iniS_us2(Current nine)	target_Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32_CurrentTime		
Rte Mode Ap Demlf SystemState Mode()	target_Rte_Inst_Ap_DemIf		
VehSpdControl Cnt M lgc	0		
k_AasActvTimeout_mS_u16	800		
k AasActvVBattMax Volt f32	16		
k AasActvVBattMin Volt f32	8		
k BsiActvTimeout mS u16	600		
k BsiActvVBattMax Volt f32	16		
k BsiActvVBattMin Volt f32	8		
k CavActvTimeout mS u16	800		
k CavActvVBattMax Volt f32	16		
k CavActvVBattMin Volt f32	8		
k CmmActvTimeout mS u16	600		
k CmmActvVBattMax Volt f32	16		
k CmmActvVBattMin Volt f32	8		
k EscActvTimeout mS u16	1000		
k EscActvVBattMax Volt f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	5.91480017		
target_Demlf_Per_BusOff_Cnt_lgc.value	0		
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0		
target Demlf Per EtatMt Cnt u08.value	12		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0		
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTine	n 4345		
target Rte Call Ap Demlf SystemTime GetSystemTime mS u32 CurrentTime	2417842237		
target Rte Inst Ap Demlf.Demlf Per BatteryVoltage Volt f32	target Demlf Per BatteryVoltage Volt f32		
target Rte Inst Ap Demlf.Demlf Per BusOff Cnt Igc	target Demlf Per BusOff Cnt Igc		
target Rte Inst Ap Demlf.Demlf Per CTerm Cnt Igc	target Demlif Per CTerm Cnt Igc		
target Rte Inst Ap Demlf.Demlf Per ElectronicIntegration Cnt Igc	target Demlf Per ElectronicIntegration Cnt Igc		
target Rte Inst Ap Demlf.Demlf Per EtatMt Cnt u08	target Demlf Per EtatMt Cnt u08		
Name	Actual Value	Expected Value	Resu
CTCInhibitionAas Cnt M u32	2417842237	2417842237	
CTCInhibitionBsi Cnt M u32	2417842237	2417842237	
CTCInhibitionCav Cnt M u32	2417842237	2417842237	
CTCInhibitionCmm Cnt M u32	2417842237	2417842237	
CTCInhibitionEsc Cnt M u32	2417842237	2417842237	
CTCInhibitionState Cnt M u08	0	0	



Test Step 2.24 (Repeat Count = 1)	Institute Value		
Name	Input Value	FT : .	
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_G		-
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_Demlf_SystemTime_D		
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_Demlf_SystemTime_G	GetSystemTime_mS_u32_CurrentTim	е
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	0		
VehSpdControl_Cnt_M_lgc	1		
k_AasActvTimeout_mS_u16	800		
k_AasActvVBattMax_Volt_f32	16		
k_AasActvVBattMin_Volt_f32	8		
k_BsiActvTimeout_mS_u16	600		
k_BsiActvVBattMax_Volt_f32	16		
k_BsiActvVBattMin_Volt_f32	8		
k_CavActvTimeout_mS_u16	0		
k_CavActvVBattMax_Volt_f32	16		
k_CavActvVBattMin_Volt_f32	8		
k_CmmActvTimeout_mS_u16	600		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	0.0749000013		
target_Demlf_Per_BusOff_Cnt_lgc.value	1		
target_DemIf_Per_CTerm_Cnt_lgc.value	0		
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	2		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime\_mSu16\_Elap$	m 50842		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_GetSystemTime\_mS\_u32\_CurrentTime$	544823061		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_lgc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_ElectronicIntegration_Cnt_lgc	target_Demlf_Per_ElectronicIntegration_Cr	nt_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Resul
CTCInhibitionAas_Cnt_M_u32	544823061	544823061	
CTCInhibitionBsi_Cnt_M_u32	544823061	544823061	•
CTCInhibitionCav Cnt M u32	544823061	544823061	
CTCInhibitionCmm_Cnt_M_u32	544823061	544823061	
CTCInhibitionEsc Cnt M u32	544823061	544823061	
CTCInhibitionState Cnt M u08	192	192	

Test Step 2.25 (Repeat Count = 1)		
Name	Input Value	
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime	
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf	
Rte_Mode_Ap_DemIf_SystemState_Mode()	3	
VehSpdControl_Cnt_M_lgc	0	
k_AasActvTimeout_mS_u16	800	
k_AasActvVBattMax_Volt_f32	16	
k_AasActvVBattMin_Volt_f32	8	
k_BsiActvTimeout_mS_u16	600	
k_BsiActvVBattMax_Volt_f32	16	
k_BsiActvVBattMin_Volt_f32	8	
k_CavActvTimeout_mS_u16	65535	
k_CavActvVBattMax_Volt_f32	16	
k_CavActvVBattMin_Volt_f32	8	
k_CmmActvTimeout_mS_u16	600	
k_CmmActvVBattMax_Volt_f32	16	
k_CmmActvVBattMin_Volt_f32	8	
k_EscActvTimeout_mS_u16	1000	
k_EscActvVBattMax_Volt_f32	16	
k_EscActvVBattMin_Volt_f32	8	
target_Demlf_Per_BatteryVoltage_Volt_f32.value	0.40959999	
target_Demlf_Per_BusOff_Cnt_lgc.value	0	
target_Demlf_Per_CTerm_Cnt_lgc.value	0	
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	1	



	ı		
Name	Input Value		
target_Demlf_Per_EtatMt_Cnt_u08.value	15		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime\_mSupplies and the property of the pr$	8547		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_GetSystemTime\_mS\_u32\_CurrentTime$	1368639926		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration_Cnt_	_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1368639926	1368639926	~
CTCInhibitionBsi_Cnt_M_u32	1368639926	1368639926	•
CTCInhibitionCav_Cnt_M_u32	1368639926	1368639926	~
CTCInhibitionCmm_Cnt_M_u32	1368639926	1368639926	~
CTCInhibitionEsc_Cnt_M_u32	1368639926	1368639926	-
CTCInhibitionState_Cnt_M_u08	132	132	•

Test Step 2.26 (Repeat Count = 1)			1
Name	Input Value		
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_	signal	
$Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16(ElapsedTime)$	target_Rte_Call_Ap_DemIf_SystemTime_Dtrm	nnElapsedTime_mS_u16_ElapsedTime	
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetS	SystemTime_mS_u32_CurrentTime	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_Demlf_SystemState_Mode()	1		
VehSpdControl_Cnt_M_lgc	1		
k_AasActvTimeout_mS_u16	800		
k_AasActvVBattMax_Volt_f32	16		
k_AasActvVBattMin_Volt_f32	8		
k_BsiActvTimeout_mS_u16	600		
k_BsiActvVBattMax_Volt_f32	16		
k_BsiActvVBattMin_Volt_f32	8		
k_CavActvTimeout_mS_u16	800		
k_CavActvVBattMax_Volt_f32	16		
k_CavActvVBattMin_Volt_f32	8		
k_CmmActvTimeout_mS_u16	600		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	4.39799976		
target_Demlf_Per_BusOff_Cnt_lgc.value	1		
target_DemIf_Per_CTerm_Cnt_lgc.value	1		
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	5		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0		
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	1Tim 4041		
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime_	ne 1967358071		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_Demlf_Per_ElectronicIntegration_Cnt_le	gc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Resu
CTCInhibitionAas_Cnt_M_u32	1967358071	1967358071	
CTCInhibitionBsi_Cnt_M_u32	1967358071	1967358071	
CTCInhibitionCav_Cnt_M_u32	1967358071	1967358071	٠,
CTCInhibitionCmm_Cnt_M_u32	1967358071	1967358071	
CTCInhibitionEsc_Cnt_M_u32	1967358071	1967358071	٠,
CTCInhibitionState Cnt M u08	64	64	

Test Step 2.27 (Repeat Count = 1)		<b>~</b>
Name	Input Value	
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime	
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32_CurrentTime	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf	
Rte_Mode_Ap_Demlf_SystemState_Mode()	3	

2018-04-10, 18:47:39+0530





Name	Input Value		
VehSpdControl_Cnt_M_lgc	0		
k_AasActvTimeout_mS_u16	0		
k_AasActvVBattMax_Volt_f32	16		
k_AasActvVBattMin_Volt_f32	8		
k_BsiActvTimeout_mS_u16	600		
k_BsiActvVBattMax_Volt_f32	16		
k_BsiActvVBattMin_Volt_f32	8		
k_CavActvTimeout_mS_u16	800		
k_CavActvVBattMax_Volt_f32	16		
k_CavActvVBattMin_Volt_f32	8		
k_CmmActvTimeout_mS_u16	600		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	15.6511002		
target_Demlf_Per_BusOff_Cnt_lgc.value	1		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	3		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime\_mS_u16\_ElapsedT$	22989		
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	4288551715		
target_Rte_Inst_Ap_Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_ElectronicIntegration_Cnt_lgc	target_Demlf_Per_ElectronicIntegration_Cnt	:_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1967358071	1967358071	~
CTCInhibitionBsi_Cnt_M_u32	1967358071	1967358071	~
CTCInhibitionCav_Cnt_M_u32	1967358071	1967358071	~
CTCInhibitionCmm_Cnt_M_u32	1967358071	1967358071	~
CTCInhibitionEsc Cnt M u32	1967358071	1967358071	-
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Took Stan 2 20 (Barrack Count = 4)	
Test Step 2.28 (Repeat Count = 1) Name	Input Value
Rte Call Ap Demlf Ignition OP GET(signal)	target Rte Call Ap Demlf Ignition OP GET signal
Rte_Call_Ap_Defini_ignition_OF_GE1(signal)  Rte_Call_Ap_Demif_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target Rte Call Ap Demif SystemTime DtrmnElapsedTime mS u16 ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_Demlf_SystemState_Mode()	3
/ehSpdControl_Cnt_M_lgc	0
<pre>&lt;_AasActvTimeout_mS_u16</pre>	65535
x_AasActvVBattMax_Volt_f32	16
<_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
x_BsiActvVBattMax_Volt_f32	16
c_BsiActvVBattMin_Volt_f32	8
c_CavActvTimeout_mS_u16	800
CavActvVBattMax_Volt_f32	16
CavActvVBattMin_Volt_f32	8
c_CmmActvTimeout_mS_u16	600
c_CmmActvVBattMax_Volt_f32	16
C_CmmActvVBattMin_Volt_f32	8
c_EscActvTimeout_mS_u16	1000
<_EscActvVBattMax_Volt_f32	16
c_EscActvVBattMin_Volt_f32	8
arget_Demlf_Per_BatteryVoltage_Volt_f32.value	1.24150002
arget_Demlf_Per_BusOff_Cnt_lgc.value	0
arget_Demlf_Per_CTerm_Cnt_lgc.value	0
arget Demlf Per ElectronicIntegration Cnt Igc.value	0
arget_Demlf_Per_EtatMt_Cnt_u08.value	14
arget Rte Call Ap Demlf Ignition OP GET signal	0
arget Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16 ElapsedTir	n 28869
arget Rte Call Ap Demlf SystemTime GetSystemTime mS u32 CurrentTime	1311140043
arget Rte Inst Ap Demlf.Demlf Per BatteryVoltage Volt f32	target Demlf Per BatteryVoltage Volt f32
arget Rte Inst Ap Demlf.Demlf Per BusOff Cnt Igc	target Demilf Per BusOff Cnt Igc
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt_lgc

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2018-04-10, 18:47:39+0530





Name	Input Value		
target_Rte_Inst_Ap_Demlf.Demlf_Per_ElectronicIntegration_Cnt_lgc	target_Demlf_Per_Electronic	cIntegration_Cnt_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_C	nt_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1311140043	1311140043	<b>✓</b>
CTCInhibitionBsi_Cnt_M_u32	1311140043	1311140043	<b>✓</b>
CTCInhibitionCav_Cnt_M_u32	1311140043	1311140043	<b>✓</b>
CTCInhibitionCmm_Cnt_M_u32	1311140043	1311140043	<b>✓</b>
CTCInhibitionEsc_Cnt_M_u32	1311140043	1311140043	<b>✓</b>
CTCInhibitionState_Cnt_M_u08	8	8	<b>✓</b>

Test Step 2.29 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_G	ET_signal	
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_D	OtrmnElapsedTime_mS_u16_ElapsedTime	
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_G	GetSystemTime_mS_u32_CurrentTime	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_Demlf_SystemState_Mode()	2		
VehSpdControl_Cnt_M_lgc	1		
k_AasActvTimeout_mS_u16	800		
k_AasActvVBattMax_Volt_f32	16		
k_AasActvVBattMin_Volt_f32	8		
k_BsiActvTimeout_mS_u16	600		
k_BsiActvVBattMax_Volt_f32	16		
k_BsiActvVBattMin_Volt_f32	8		
k_CavActvTimeout_mS_u16	800		
k CavActvVBattMax Volt f32	16		
k_CavActvVBattMin_Volt_f32	8		
k_CmmActvTimeout_mS_u16	600		
k_CmmActvVBattMax_Volt_f32	16		
k CmmActvVBattMin Volt f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k EscActvVBattMin Volt f32	8		
target Demlf Per BatteryVoltage Volt f32.value	24.6821003		
target Demlf Per BusOff Cnt Igc.value	1		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0		
target Demif Per EtatMt Cnt u08.value	12		
target Rte Call Ap Demlf Ignition OP GET signal	1		
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	1356		
target Rte Call Ap Demlf SystemTime GetSystemTime mS u32 CurrentTime	2740672965		
target Rte Inst Ap Demlf.Demlf Per BatteryVoltage Volt f32	target Demlf Per BatteryVoltage Volt f32		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target Demlf Per BusOff Cnt Igc		
target Rte Inst Ap Demlf.Demlf Per CTerm Cnt Igc	target Demlf Per CTerm Cnt Igc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_Demlf_Per_ElectronicIntegration_Cr	nt Igc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas Cnt M u32	2740672965	2740672965	
CTCInhibitionBsi Cnt M u32	2740672965	2740672965	•
CTCInhibitionCav Cnt M u32	2740672965	2740672965	-
CTCInhibitionCmm Cnt M u32	2740672965	2740672965	•
CTCInhibitionEsc Cnt M u32	2740672965	2740672965	-
CTCInhibitionState Cnt M u08	64	64	-

Name	Input Value
Rte Call Ap Demlf Ignition OP GET(signal)	target Rte Call Ap Demlf Ignition OP GET signal
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	1
VehSpdControl_Cnt_M_lgc	0
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k BsiActvVBattMin Volt f32	8



Name	Input Value		
k_CavActvTimeout_mS_u16	800		
k_CavActvVBattMax_Volt_f32	16		
k_CavActvVBattMin_Volt_f32	8		
k_CmmActvTimeout_mS_u16	0		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	0.328999996		
target_Demlf_Per_BusOff_Cnt_lgc.value	1		
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_DemIf_Per_ElectronicIntegration_Cnt_Igc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	12		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0		
target Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16 ElapsedTim	26304		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_GetSystemTime\_mS\_u32\_CurrentTime$	3599977200		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_DemIf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration_Cnt	_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	3599977200	3599977200	~
CTCInhibitionBsi_Cnt_M_u32	3599977200	3599977200	•
CTCInhibitionCav_Cnt_M_u32	3599977200	3599977200	~
CTCInhibitionCmm_Cnt_M_u32	3599977200	3599977200	•
CTCInhibitionEsc_Cnt_M_u32	3599977200	3599977200	~
CTCInhibitionState_Cnt_M_u08	64	64	~

Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_G	ET signal	
Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_D		
Rte Call Ap Demlf SystemTime GetSystemTime mS u32(CurrentTime)	target Rte Call Ap Demlf SystemTime G		
Rte Inst Ap Demlf	target_Rte_Inst_Ap_DemIf	·	
Rte_Mode_Ap_Demlf_SystemState_Mode()	2		
VehSpdControl_Cnt_M_lgc	0		
k_AasActvTimeout_mS_u16	800		
k_AasActvVBattMax_Volt_f32	16		
k_AasActvVBattMin_Volt_f32	8		
k_BsiActvTimeout_mS_u16	600		
k_BsiActvVBattMax_Volt_f32	16		
k_BsiActvVBattMin_Volt_f32	8		
k_CavActvTimeout_mS_u16	800		
k_CavActvVBattMax_Volt_f32	16		
k_CavActvVBattMin_Volt_f32	8		
k_CmmActvTimeout_mS_u16	65535		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	1.57360005		
target_Demlf_Per_BusOff_Cnt_lgc.value	1		
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_DemIf_Per_ElectronicIntegration_Cnt_Igc.value	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	1		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0		
target_Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedT	im 62048		
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	3314516146		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_DemIf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_Demlf_Per_ElectronicIntegration_Cr	nt_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Resu
CTCInhibitionAas_Cnt_M_u32	3314516146	3314516146	
CTCInhibitionBsi_Cnt_M_u32	3314516146	3314516146	
CTCInhibitionCav_Cnt_M_u32	3314516146	3314516146	
CTCInhibitionCmm_Cnt_M_u32	3314516146	3314516146	

2018-04-10, 18:47:39+0530



Demlf\_Per

Name	Actual Value	Expected Value	Result
CTCInhibitionEsc_Cnt_M_u32	3314516146	3314516146	<b>✓</b>
CTCInhibitionState Cnt M u08	208	208	<b>✓</b>

Test Step 2.32 (Repeat Count = 1)			•	
Name	Input Value			
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignitio	n_OP_GET_signal		
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_System	target_Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime		
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_Syste	target_Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32_CurrentTime		
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_Demlf_SystemState_Mode()	3			
VehSpdControl_Cnt_M_lgc	1			
k_AasActvTimeout_mS_u16	800			
k_AasActvVBattMax_Volt_f32	16			
k_AasActvVBattMin_Volt_f32	8			
k_BsiActvTimeout_mS_u16	600			
k_BsiActvVBattMax_Volt_f32	16			
k_BsiActvVBattMin_Volt_f32	8			
k_CavActvTimeout_mS_u16	800			
k_CavActvVBattMax_Volt_f32	16			
k_CavActvVBattMin_Volt_f32	8			
k_CmmActvTimeout_mS_u16	600			
k_CmmActvVBattMax_Volt_f32	16			
k_CmmActvVBattMin_Volt_f32	8	8		
k_EscActvTimeout_mS_u16	1000	1000		
k_EscActvVBattMax_Volt_f32	16	16		
k_EscActvVBattMin_Volt_f32	8	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	8.26420021			
target_Demlf_Per_BusOff_Cnt_lgc.value	1			
target_Demlf_Per_CTerm_Cnt_lgc.value	0			
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	5			
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0			
target Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16 Elapse	edTim 54812			
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_GetSystemTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u33\_CurrentTime$	me 1306746881			
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage	_Volt_f32		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lge	С		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt_lge	С		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_Demlf_Per_ElectronicInteg	ration_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u0	8		
Name	Actual Value	Expected Value	Resul	
CTCInhibitionAas_Cnt_M_u32	1306746881	1306746881	•	
CTCInhibitionBsi_Cnt_M_u32	1306746881	1306746881	•	
CTCInhibitionCav_Cnt_M_u32	1306746881	1306746881		
CTCInhibitionCmm_Cnt_M_u32	1306746881	1306746881	•	
CTCInhibitionEsc_Cnt_M_u32	1306746881	1306746881	•	
CTCInhibitionState_Cnt_M_u08	64	64	•	

2018-04-10, 18:45:44+0530



Demlf\_EvaluateLogicalCondition

Project	Demlf
Module	Demlf
Test Object	Demlf_EvaluateLogicalCondition

### Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MC/DC Coverage	100 %

#### **Statistics**

Total Testcases	2	
Successful	2	✓
Failed	0	
Not Executed	0	

### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config \TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\Demif\src\Ap_Demif.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I\$(PROJECTROOT)\Demlf\utp\contract -I\$(PROJECTROOT)\Demlf\utp\contract\Ap_Demlf -I\$ (PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include

Name	Text
Module 'Demi <b>f</b> '	Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_Demlf.c Code File(s) Version:3 Module Design Document:Demlf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):104 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference.

Attributes				
Name	Value			
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5			
Float Precision	9			
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj			
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src			
Linker File	\$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd			
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl			
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4			
Time Unit	cycles			
Timer Enabled	false			
Timer Prescale	0			
Timer Resolution	1			
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg			

2018-04-10, 18:45:44+0530



Attributes	
Name	Value
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



#### **Test Case 1: Metrics Test**

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

TS 1.1 1103.00 Cycles TS 1.2 1038.00 Cycles

Description Vector Description:

TS 1.1 Shortest Execution Path=>if (IoHwAb\_BoolType\_LowerLimit == Ignition\_Cnt\_T\_enum)=>False if (((uint8)kETAT\_MT\_Starting == EtatMt\_Cnt\_T\_u08)=>False || ((uint8)kETAT\_MT\_Autonomous\_Starting == EtatMt\_Cnt\_T\_u08)=>False)
TS 1.2 Longest Execution Path=> if (IoHwAb\_BoolType\_LowerLimit == Ignition\_Cnt\_T\_enum)=>True if ((FALSE == CTerm\_Cnt\_T\_lgc)=>True && (RTE\_MODE\_StaMd\_Mode\_OPERATE != SystemState\_Cnt\_T\_enum)=>True)

Test Step 1.1 (Repeat Count = 1)			✓	
Name	Input Value			
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Igi	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal		
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf			
Rte_Mode_Ap_DemIf_SystemState_Mode()	4			
Time_ms_T_u32	4294967295			
target_Demlf_Per_CTerm_Cnt_lgc.value	1			
target_Demlf_Per_EtatMt_Cnt_u08.value	15	15		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1			
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt	:_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt	_u08		
Name	Actual Value	Expected Value	Result	
CTCInhibitionAas_Cnt_M_u32	0	0	~	
CTCInhibitionBsi_Cnt_M_u32	0	0	<b>✓</b>	
CTCInhibitionCav_Cnt_M_u32	0	0	<b>✓</b>	
CTCInhibitionCmm_Cnt_M_u32	0	0	<b>✓</b>	
CTCInhibitionEsc_Cnt_M_u32	0	0	✓	

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	~

Test Step 1.2 (Repeat Count = 1)				
Name	Input Value			
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Igr	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal		
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf			
Rte_Mode_Ap_DemIf_SystemState_Mode()	0			
Time_ms_T_u32	0			
target_DemIf_Per_CTerm_Cnt_lgc.value	0			
target_Demlf_Per_EtatMt_Cnt_u08.value	0			
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0			
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt	_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt	_u08		
Name	Actual Value	Expected Value	Result	
CTCInhibitionAas_Cnt_M_u32	0	0	~	
CTCInhibitionBsi_Cnt_M_u32	0	0	<b>✓</b>	
CTCInhibitionCav_Cnt_M_u32	0	0	~	
CTCInhibitionCmm_Cnt_M_u32	0	0	<b>~</b>	
CTCInhibitionEsc Cnt M u32	0	0	<b>✓</b>	

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	<b>✓</b>



#### Test Case 2: Range Test

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

CPU Cycles:

TS 2.1 1032.00 Cycles
TS 2.2 1032.00 Cycles
TS 2.2 1032.00 Cycles
TS 2.3 1032.00 Cycles
TS 2.4 1032.00 Cycles
TS 2.4 1032.00 Cycles
TS 2.5 1032.00 Cycles
TS 2.6 1032.00 Cycles
TS 2.7 1032.00 Cycles
TS 2.9 1032.00 Cycles
TS 2.9 1032.00 Cycles
TS 2.10 1032.00 Cycles
TS 2.11 1032.00 Cycles
TS 2.12 1032.00 Cycles
TS 2.12 1032.00 Cycles
TS 2.13 1032.00 Cycles
TS 2.14 1032.00 Cycles
TS 2.15 1032.00 Cycles
TS 2.15 1032.00 Cycles
TS 2.16 1032.00 Cycles
TS 2.17 1032.00 Cycles
TS 2.17 1032.00 Cycles
TS 2.17 1032.00 Cycles

#### Description

Vector Description:

TS 1.1All Min

TS 1.2All Max

IS 1.2All Max

S 1.3Time\_ms\_T\_u32=>Min

TS 1.4Time\_ms\_T\_u32=>Max

TS 1.5Time\_ms\_T\_u32=>Pos

TS 1.6Demlf\_Per\_CTerm\_Cnt\_lgc=>Min

TS 1.7Demlf\_Per\_CTerm\_Cnt\_lgc=>Max

TS 1.8Demlf\_Per\_EtatMt\_Cnt\_u08=>Min

TS 1.9Demlf\_Per\_EtatMt\_Cnt\_u08=>Max

TS 1.9Demlf\_Per\_EtatMt\_Cnt\_u08=>Max

TS 1.9Demlf\_Per\_EtatMt\_Cnt\_u08=>Max
TS 1.10Demlf\_Per\_EtatMt\_Cnt\_u08=>Pos
TS 1.10Demlf\_Per\_EtatMt\_Cnt\_u08=>Pos
TS 1.11Rte\_Mode\_SystemState\_Mode=>RTE\_MODE\_StaMd\_Mode\_DISABLE
TS 1.12Rte\_Mode\_SystemState\_Mode=>RTE\_MODE\_StaMd\_Mode\_OFF
TS 1.13Rte\_Mode\_SystemState\_Mode=>RTE\_MODE\_StaMd\_Mode\_OPERATE
TS 1.14Rte\_Mode\_SystemState\_Mode=>RTE\_MODE\_StaMd\_Mode\_WARMINIT
TS 1.15Rte\_Mode\_SystemState\_Mode=>RTE\_TRANSITION\_StaMd\_Mode
TS 1.16Rte\_Call\_Ignition\_OP\_GET=>Min
TS 1.17Rte\_Call\_Ignition\_OP\_GET=>Max

Test Step 2.1 (Repeat Count = 1)			V
Name	Input Value		
Rte Call Ap Demlf Ignition OP GET(signal)	target Rte Call Ap Demlf Ign	ition OP GET signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	0		
Time_ms_T_u32	0		
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	0		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt_	<u>lg</u> c	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_	u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	0	0	~
CTCInhibitionBsi_Cnt_M_u32	0	0	✓
CTCInhibitionCav_Cnt_M_u32	0	0	~
CTCInhibitionCmm_Cnt_M_u32	0	0	✓
CTCInhibitionEsc Cnt M u32	0	0	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte Mode Ap Demlf SystemState Mode	1	Rte Mode Ap Demlf SystemState Mode	1	<b>✓</b>

Name	Input Value			
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ign	ition_OP_GET_signal		
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf			
Rte_Mode_Ap_DemIf_SystemState_Mode()	4			
Time_ms_T_u32	4294967295	4294967295		
target_DemIf_Per_CTerm_Cnt_lgc.value	1	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	15			
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	1			
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt_	_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_	u08		
Name	Actual Value	Expected Value	Result	
CTCInhibitionAas_Cnt_M_u32	0	0	•	
CTCInhibitionBsi Cnt M u32	0	0		

2018-04-10, 18:45:44+0530



Name	Actual Value	Expected Value	Result
CTCInhibitionCav_Cnt_M_u32	0	0	~
CTCInhibitionCmm_Cnt_M_u32	0	0	✓
CTCInhibitionEsc Cnt M u32	0	0	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte Mode Ap Demlf SystemState Mode	1	Rte Mode Ap Demlf SystemState Mode	1	<b>✓</b>

Test Step 2.3 (Repeat Count = 1)			✓
Name	Input Value		
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Igr	nition_OP_GET_signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	1		
Time_ms_T_u32	0		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	1		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt	_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_	_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	0	0	<b>✓</b>
CTCInhibitionBsi_Cnt_M_u32	0	0	✓
CTCInhibitionCav_Cnt_M_u32	0	0	<b>✓</b>
CTCInhibitionCmm_Cnt_M_u32	0	0	✓
CTCInhibitionEsc_Cnt_M_u32	0	0	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte Mode Ap Demlf SystemState Mode	1	Rte Mode Ap Demlf SystemState Mode	1	<b>✓</b>

Test Step 2.4 (Repeat Count = 1)			✓
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Igr	nition_OP_GET_signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	2		
Time_ms_T_u32	4294967295		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	2		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt	_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_	_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	4294967295	4294967295	~
CTCInhibitionBsi_Cnt_M_u32	0	0	✓
CTCInhibitionCav_Cnt_M_u32	4294967295	4294967295	~
CTCInhibitionCmm_Cnt_M_u32	0	0	✓
CTCInhibitionEsc_Cnt_M_u32	4294967295	4294967295	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	•

Test Step 2.5 (Repeat Count = 1)		<b>✓</b>
Name	Input Value	
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf	
Rte_Mode_Ap_DemIf_SystemState_Mode()	2	
Time_ms_T_u32	125351	
target_Demlf_Per_CTerm_Cnt_lgc.value	0	
target_Demlf_Per_EtatMt_Cnt_u08.value	3	

2018-04-10, 18:45:44+0530



Name	Input Value		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cn	nt_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cn	t_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	125351	125351	✓
CTCInhibitionBsi_Cnt_M_u32	0	0	✓
CTCInhibitionCav_Cnt_M_u32	125351	125351	<b>✓</b>
CTCInhibitionCmm_Cnt_M_u32	0	0	✓
CTCInhibitionEsc_Cnt_M_u32	4294967295	4294967295	<b>✓</b>

Test Step Call Trace						
Actual Function	Count	Expected Function	Count	Result		
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~		
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_Demlf_SystemState_Mode	1	•		

Test Step 2.6 (Repeat Count = 1)			✓
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Igr	nition_OP_GET_signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	4		
Time_ms_T_u32	252315		
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	4		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt	_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_	_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	125351	125351	~
CTCInhibitionBsi_Cnt_M_u32	0	0	~
CTCInhibitionCav_Cnt_M_u32	125351	125351	~
CTCInhibitionCmm_Cnt_M_u32	0	0	<b>✓</b>
CTCInhibitionEsc_Cnt_M_u32	4294967295	4294967295	~

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~	
Rte_Mode_Ap_Demlf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	~	

Test Step 2.7 (Repeat Count = 1)			
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ign	ition_OP_GET_signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	4		
Time_ms_T_u32	1352463		
target_DemIf_Per_CTerm_Cnt_lgc.value	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	5		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt	_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_	_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1352463	1352463	~
CTCInhibitionBsi_Cnt_M_u32	0	0	<b>✓</b>
CTCInhibitionCav_Cnt_M_u32	1352463	1352463	~
CTCInhibitionCmm_Cnt_M_u32	0	0	<b>✓</b>
CTCInhibitionEsc Cnt M u32	4294967295	4294967295	<b>✓</b>

Test Step Call Trace						
Actual Function	Count	Expected Function	Count	Result		
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~		
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	<b>✓</b>		



Test Step 2.8 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ig	nition_OP_GET_signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	1		
Time_ms_T_u32	324253		
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	0		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cn	t_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cn	t_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1352463	1352463	~
CTCInhibitionBsi_Cnt_M_u32	0	0	~
CTCInhibitionCav_Cnt_M_u32	1352463	1352463	<b>✓</b>
CTCInhibitionCmm_Cnt_M_u32	0	0	<b>✓</b>
CTCInhibitionEsc_Cnt_M_u32	4294967295	4294967295	<b>✓</b>

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~	
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_Demlf_SystemState_Mode	1	•	

Test Step 2.9 (Repeat Count = 1)			✓
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ign	nition_OP_GET_signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	0		
Time_ms_T_u32	676575		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	15		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	1		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt	_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_	_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1352463	1352463	~
CTCInhibitionBsi_Cnt_M_u32	0	0	<b>✓</b>
CTCInhibitionCav_Cnt_M_u32	1352463	1352463	~
CTCInhibitionCmm_Cnt_M_u32	0	0	~
CTCInhibitionEsc_Cnt_M_u32	4294967295	4294967295	<b>✓</b>

Test Step Call Trace						
Actual Function	Count	Expected Function	Count	Result		
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~		
Rte_Mode_Ap_Demlf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	<b>✓</b>		

Test Step 2.10 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Igr	nition_OP_GET_signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	1		
Time_ms_T_u32	32426532		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	11		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt	_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt	_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1352463	1352463	~
CTCInhibitionBsi_Cnt_M_u32	0	0	<b>✓</b>
CTCInhibitionCav_Cnt_M_u32	1352463	1352463	<b>✓</b>
CTCInhibitionCmm_Cnt_M_u32	0	0	<b>✓</b>
CTCInhibitionEsc_Cnt_M_u32	4294967295	4294967295	<b>✓</b>



Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	<b>✓</b>

Test Step 2.11 (Repeat Count = 1)			✓
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Igr	nition_OP_GET_signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_Demlf_SystemState_Mode()	0		
Time_ms_T_u32	57742		
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	6		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt	:_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_	_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	57742	57742	~
CTCInhibitionBsi_Cnt_M_u32	57742	57742	<b>✓</b>
CTCInhibitionCav_Cnt_M_u32	57742	57742	~
CTCInhibitionCmm_Cnt_M_u32	57742	57742	<b>✓</b>
CTCInhibitionEsc_Cnt_M_u32	57742	57742	<b>✓</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte Mode Ap Demlf SystemState Mode	1	Rte Mode Ap Demlf SystemState Mode	1	<b>✓</b>

Test Step 2.12 (Repeat Count = 1)			<b>✓</b>	
Name	Input Value			
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Igr	nition_OP_GET_signal		
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	1			
Time_ms_T_u32	45			
target_Demlf_Per_CTerm_Cnt_lgc.value	0			
target_Demlf_Per_EtatMt_Cnt_u08.value	7			
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0			
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt	:_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt	_u08		
Name	Actual Value	Expected Value	Result	
CTCInhibitionAas_Cnt_M_u32	45	45	~	
CTCInhibitionBsi_Cnt_M_u32	45	45	~	
CTCInhibitionCav_Cnt_M_u32	45	45	~	
CTCInhibitionCmm_Cnt_M_u32	45	45	<b>✓</b>	
CTCInhibitionEsc Cnt M u32	45	45	<b>✓</b>	

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	~	
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_Demlf_SystemState_Mode	1	<b>✓</b>	



Test Step 2.13 (Repeat Count = 1)			<b>✓</b>	
Name	Input Value			
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ign	ition_OP_GET_signal		
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf			
Rte_Mode_Ap_DemIf_SystemState_Mode()	2			
Time_ms_T_u32	7574621	7574621		
target_Demlf_Per_CTerm_Cnt_lgc.value	1			
target_Demlf_Per_EtatMt_Cnt_u08.value	8	8		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	1			
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt	_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_	_u08		
Name	Actual Value	Expected Value	Result	
CTCInhibitionAas_Cnt_M_u32	45	45	<b>✓</b>	
CTCInhibitionBsi_Cnt_M_u32	45	45	<b>✓</b>	
CTCInhibitionCav_Cnt_M_u32	45	45	~	
CTCInhibitionCmm_Cnt_M_u32	45	45	<b>✓</b>	
CTCInhibitionEsc_Cnt_M_u32	45	45	~	

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_Demlf_SystemState_Mode	1	•

Test Step 2.14 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Igr	nition_OP_GET_signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_Demlf_SystemState_Mode()	3		
Time_ms_T_u32	5785		
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	9		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt	_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt	_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	5785	5785	~
CTCInhibitionBsi_Cnt_M_u32	5785	5785	✓
CTCInhibitionCav_Cnt_M_u32	5785	5785	~
CTCInhibitionCmm_Cnt_M_u32	5785	5785	~
CTCInhibitionEsc_Cnt_M_u32	5785	5785	<b>✓</b>

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	~	
Rte_Mode_Ap_Demlf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	<b>✓</b>	

Test Step 2.15 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Igr	nition_OP_GET_signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	4		
Time_ms_T_u32	14165		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	10		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt	:_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt	_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	14165	14165	<b>✓</b>
CTCInhibitionBsi_Cnt_M_u32	5785	5785	<b>✓</b>
CTCInhibitionCav_Cnt_M_u32	14165	14165	<b>✓</b>
CTCInhibitionCmm_Cnt_M_u32	5785	5785	<b>✓</b>
CTCInhibitionEsc_Cnt_M_u32	14165	14165	<b>✓</b>



Test Step Call Trace				~
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte Mode An Demlf SystemState Mode	1	Rte Mode An Demlf SystemState Mode	1	<b>V</b>

Test Step 2.16 (Repeat Count = 1)			•
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Igr	nition_OP_GET_signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	1		
Time_ms_T_u32	415241		
target_DemIf_Per_CTerm_Cnt_lgc.value	1		
target_DemIf_Per_EtatMt_Cnt_u08.value	13		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0		
target_Rte_Inst_Ap_DemIf_DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt	_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_	_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	415241	415241	<b>✓</b>
CTCInhibitionBsi_Cnt_M_u32	5785	5785	<b>✓</b>
CTCInhibitionCav_Cnt_M_u32	415241	415241	<b>✓</b>
CTCInhibitionCmm_Cnt_M_u32	5785	5785	<b>✓</b>
CTCInhibitionEsc Cnt M u32	14165	14165	<b>✓</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	<b>✓</b>

Test Step 2.17 (Repeat Count = 1)			<u> </u>	
Name	Input Value			
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Igr	nition_OP_GET_signal		
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	2			
Time_ms_T_u32	213526			
target_DemIf_Per_CTerm_Cnt_lgc.value	0			
target_DemIf_Per_EtatMt_Cnt_u08.value	12	12		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	1			
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt	_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_	_u08		
Name	Actual Value	Expected Value	Result	
CTCInhibitionAas_Cnt_M_u32	415241	415241	~	
CTCInhibitionBsi_Cnt_M_u32	5785	5785	<b>✓</b>	
CTCInhibitionCav_Cnt_M_u32	415241	415241	~	
CTCInhibitionCmm_Cnt_M_u32	5785	5785	<b>✓</b>	
CTCInhibitionEsc Cnt M u32	14165	14165	<b>✓</b>	

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_Demlf_SystemState_Mode	1	<b>✓</b>

2018-04-10, 18:44:44+0530

Demlf\_DTCS Ch n e



 Project
 Demlf

 Module
 Demlf

 Test Object
 Demlf\_DTCStatusChanged

### Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MC/DC Coverage	100 %

#### **Statistics**

Total Testcases	3	
Successful	3	~
Failed	0	
Not Executed	0	

### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config \TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\Demif\src\Ap_Demif.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I\$(PROJECTROOT)\Demlf\utp\contract -I\$(PROJECTROOT)\Demlf\utp\contract\Ap_Demlf -I\$ (PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include

Name	Text
Module 'Demi <b>f</b> '	Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_Demlf.c Code File(s) Version:3 Module Design Document:Demlf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):104 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference.

Attributes			
Name	Value		
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5		
Float Precision	9		
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj		
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src		
Linker File	\$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd		
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl		
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4		
Time Unit	cycles		
Timer Enabled	false		
Timer Prescale	0		
Timer Resolution	1		
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg		

2018-04-10, 18:44:44+0530



Demlf\_DTCS Ch n e

Attributes	
Name	Value
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

DemIf\_DTCS





```
Test Case 1: Metrics Test
              Performance Metrics (With "None"
Instrumentation and WithPS Environment)
Specification
              TS 1.1 3296.00 Cycles
TS 1.2 2545.00 Cycles
Description
             Vector Description:
```

Test Step 1.1 (Repeat Count = 1)		
Name	Input Value	
CTCFailedBuf_Cnt_M_lgc[0]	0	
CTCFailedBuf_Cnt_M_lgc[1]	0	
CTCFailedBuf Cnt M lgc[2]	0	
CTCFailedBuf Cnt M lgc[3]	0	
CTCFailedBuf_Cnt_M_lgc[4]	0	
CTCFailedBuf_Cnt_M_lgc[5]	0	
CTCFailedBuf_Cnt_M_lgc[6]	0	
CTCFailedBuf_Cnt_M_lgc[7]	0	
CTCFailedBuf Cnt M lgc[8]	0	
CTCFailedBuf_Cnt_M_lgc[9]	0	
CTCFailedBuf_Cnt_M_lgc[10]	0	
	0	
CTCFailedBuf_Cnt_M_lgc[11]		
CTCFailedBuf_Cnt_M_lgc[12]	0	
CTCFailedBuf_Cnt_M_lgc[13]	0	
CTCFailedBuf_Cnt_M_lgc[14]	0	
CTCFailedBuf_Cnt_M_lgc[15]	0	
CTCFailedBuf_Cnt_M_lgc[16]	0	
CTCFailedBuf_Cnt_M_lgc[17]	0	
CTCFailedBuf_Cnt_M_lgc[18]	0	
CTCFailedBuf_Cnt_M_lgc[19]	0	
CTCFailedBuf_Cnt_M_lgc[20]	0	
CTCFailedBuf_Cnt_M_lgc[21]	0	
CTCFailedBuf_Cnt_M_lgc[22]	0	
CTCFailedBuf_Cnt_M_lgc[23]	0	
CTCFailedBuf_Cnt_M_lgc[24]	0	
CTCFailedBuf_Cnt_M_lgc[25]	0	
CTCFailedBuf_Cnt_M_lgc[26]	0	
CTCFailedBuf_Cnt_M_lgc[27]	0	
CTCFailedBuf_Cnt_M_lgc[28]	0	
CTCFailedBuf_Cnt_M_lgc[29]	0	
CTCFailedBuf_Cnt_M_lgc[30]	0	
CTCFailedBuf_Cnt_M_lgc[31]	0	
CTCFailedBuf_Cnt_M_lgc[32]	0	
CTCFailedBuf_Cnt_M_lgc[33]	0	
CTCFailedBuf_Cnt_M_lgc[34]	0	
CTCFailedBuf_Cnt_M_lgc[35]	0	
CTCFailedBuf_Cnt_M_lgc[36]	0	
CTCFailedBuf_Cnt_M_lgc[37]	0	
CTCFailedBuf_Cnt_M_lgc[38]	0	
CTCFailedBuf Cnt M Igc[39]	0	
CTCFailedBuf_Cnt_M_lgc[40]	0	
CTCFailedBuf_Cnt_M_lgc[41]	0	
CTCFailedBuf Cnt M lgc[42]	0	
CTCFailedBuf_Cnt_M_lgc[43]	0	
CTCFailedBuf_Cnt_M_lgc[44]	0	
CTCFailedBut_Crit_M_igc[44]	0	
CTCFailedBuf Cnt M lgc[46]	0	
CTCFailedBuf_Cnt_M_lgc[47]	0	
CTCFailedBuf_Cnt_M_lgc[48]	0	
CTCFailedBuf_Cnt_M_lgc[49]	0	
CTCFailedBuf_Cnt_M_lgc[50]	0	
CTCFailedBuf_Cnt_M_lgc[51]	0	

### **TEST DETAILS REPORT** Ch n e

Demlf\_DTCS

2018-04-10, 18:44:44+0530



	1 - 10-10
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_Igc[53]	0
CTCFailedBuf_Cnt_M_lgc[54]	0
CTCFailedBuf_Cnt_M_lgc[55]	0
CTCFailedBuf_Cnt_M_lgc[56]	0
CTCFailedBuf_Cnt_M_lgc[57]	0
CTCFailedBuf_Cnt_M_lgc[58]	0
CTCFailedBuf_Cnt_M_lgc[59]	0
CTCFailedBuf_Cnt_M_lgc[60]	0
CTCFailedBuf_Cnt_M_lgc[61]	0
CTCFailedBuf_Cnt_M_lgc[62]	0
CTCFailedBuf_Cnt_M_lgc[63]	0
CTCFailedBuf_Cnt_M_lgc[64]	0
CTCFailedBuf_Cnt_M_lgc[65]	0
CTCFailedBuf_Cnt_M_lgc[66]	0
CTCFailedBuf_Cnt_M_lgc[67]	0
CTCFailedBuf_Cnt_M_lgc[68]	0
CTCFailedBuf_Cnt_M_lgc[69]	0
CTCFailedBuf_Cnt_M_lgc[70]	0
CTCFailedBuf_Cnt_M_lgc[71]	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	0
CTCFailedBuf_Cnt_M_lgc[74]	0
CTCFailedBuf_Cnt_M_lgc[75]	0 0
CTCFailed Cnt_M_lgc[76]	0
CTCFailed_Cnt_M_lgc	0
DTC DTCKind	1
DTCStatusNew	0
DTCStatusOld	0
Dem_DTCNumberTable[0]	0
Dem_DTCNumberTable[1]	0
Dem_DTCNumberTable[1] Dem_DTCNumberTable[2]	0
Dem_DTCNumberTable[3]	0
Dem_DTCNumberTable[4]	0
Dem_DTCNumberTable[5]	0
Dem_DTCNumberTable[6]	0
Dem_DTCNumberTable[7]	0
Dem_DTCNumberTable[8]	0
Dem_DTCNumberTable[9]	0
Dem_DTCNumberTable[10]	0
Dem_DTCNumberTable[11]	0
Dem_DTCNumberTable[12]	0
Dem_DTCNumberTable[13]	0
Dem_DTCNumberTable[14]	0
Dem_DTCNumberTable[15]	0
Dem_DTCNumberTable[16]	0
Dem_DTCNumberTable[17]	0
Dem_DTCNumberTable[18]	0
Dem_DTCNumberTable[19]	0
Dem_DTCNumberTable[20]	0
Dem_DTCNumberTable[21]	0
Dem_DTCNumberTable[22]	0
Dem_DTCNumberTable[23]	0
Dem_DTCNumberTable[24]	0
Dem_DTCNumberTable[25]	0
Dem_DTCNumberTable[26]	0
Dem_DTCNumberTable[27]	0 0
Dem_DTCNumberTable[28] Dem_DTCNumberTable[29]	0
Dem_DTCNumberTable[29] Dem_DTCNumberTable[30]	0
Dem_DTCNumberTable[30]	0
Dem_DTCNumberTable[32]	0
Dem_DTCNumberTable[33]	0
Dem_DTCNumberTable[34]	0
Dem_DTCNumberTable[35]	0
Dem_DTCNumberTable[36]	0
Dem_DTCNumberTable[37]	0
Dem_DTCNumberTable[38]	0
Dem_DTCNumberTable[39]	0
Dem_DTCNumberTable[40]	0
Dem_DTCNumberTable[41]	0
Dem_DTCNumberTable[42]	0

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value Dem DTCNumberTable[43] 0 Dem\_DTCNumberTable[44] 0 Dem\_DTCNumberTable[45] 0 Dem\_DTCNumberTable[46] 0 Dem\_DTCNumberTable[47] 0 Dem\_DTCNumberTable[48] 0 Dem\_DTCNumberTable[49] 0 Dem\_DTCNumberTable[50] 0 Dem\_DTCNumberTable[51] 0 Dem DTCNumberTable[52] n Dem\_DTCNumberTable[53] 0 Dem\_DTCNumberTable[54] n Dem\_DTCNumberTable[55] 0 Dem\_DTCNumberTable[56] n Dem\_DTCNumberTable[57] 0 Dem\_DTCNumberTable[58] 0 Dem\_DTCNumberTable[59] 0 Dem\_DTCNumberTable[60] 0 Dem\_DTCNumberTable[61] 0 Dem\_DTCNumberTable[62] 0 Dem\_DTCNumberTable[63] 0 Dem\_DTCNumberTable[64] 0 Dem\_DTCNumberTable[65] 0 Dem\_DTCNumberTable[66] 0 0 Dem\_DTCNumberTable[67] Dem\_DTCNumberTable[68] 0 Dem\_DTCNumberTable[69] 0 Dem\_DTCNumberTable[70] 0 Dem\_DTCNumberTable[71] 0 Dem\_DTCNumberTable[72] 0 Dem\_DTCNumberTable[73] 0 Dem\_DTCNumberTable[74] 0 Dem DTCNumberTable[75] 0 Dem\_DTCNumberTable[76] n Dem\_DTC\_FTB\_Table[0] 255 Dem\_DTC\_FTB\_Table[1] 255 Dem\_DTC\_FTB\_Table[2] 255 Dem\_DTC\_FTB\_Table[3] 255 Dem\_DTC\_FTB\_Table[4] 255 Dem DTC FTB Table[5] 255 Dem\_DTC\_FTB\_Table[6] 255 Dem DTC FTB Table[7] 255 Dem\_DTC\_FTB\_Table[8] 255 Dem\_DTC\_FTB\_Table[9] 255 255 Dem\_DTC\_FTB\_Table[10] Dem\_DTC\_FTB\_Table[11] 255 255 Dem\_DTC\_FTB\_Table[12] Dem\_DTC\_FTB\_Table[13] 255 Dem\_DTC\_FTB\_Table[14] 255 Dem\_DTC\_FTB\_Table[15] 255 Dem\_DTC\_FTB\_Table[16] 255 Dem\_DTC\_FTB\_Table[17] 255 Dem\_DTC\_FTB\_Table[18] 255 Dem\_DTC\_FTB\_Table[19] 255 Dem\_DTC\_FTB\_Table[20] 255 Dem\_DTC\_FTB\_Table[21] 255 Dem\_DTC\_FTB\_Table[22] 255 Dem\_DTC\_FTB\_Table[23] 255 Dem\_DTC\_FTB\_Table[24] 255 Dem\_DTC\_FTB\_Table[25] 255 Dem\_DTC\_FTB\_Table[26] 255 Dem\_DTC\_FTB\_Table[27] 255 Dem\_DTC\_FTB\_Table[28] 255 Dem\_DTC\_FTB\_Table[29] 255 Dem\_DTC\_FTB\_Table[30] 255 Dem DTC FTB Table[31] 255 Dem\_DTC\_FTB\_Table[32] 255 Dem DTC FTB Table[33] 255 Dem\_DTC\_FTB\_Table[34] 255 Dem\_DTC\_FTB\_Table[35] 255 Dem\_DTC\_FTB\_Table[36] 255 Dem\_DTC\_FTB\_Table[37] 255 Dem\_DTC\_FTB\_Table[38] 255

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Name Input Value Dem\_DTC\_FTB\_Table[39] 255 Dem\_DTC\_FTB\_Table[40] 255 Dem DTC\_FTB\_Table[41] 255 Dem\_DTC\_FTB\_Table[42] 255 Dem\_DTC\_FTB\_Table[43] 255 Dem\_DTC\_FTB\_Table[44] 255 Dem\_DTC\_FTB\_Table[45] 255 Dem\_DTC\_FTB\_Table[46] 255 Dem\_DTC\_FTB\_Table[47] 255 Dem\_DTC\_FTB\_Table[48] 255 Dem\_DTC\_FTB\_Table[49] 255 Dem\_DTC\_FTB\_Table[50] 255 Dem\_DTC\_FTB\_Table[51] 255 Dem\_DTC\_FTB\_Table[52] 255 Dem\_DTC\_FTB\_Table[53] 255 255 Dem DTC FTB Table[54] Dem\_DTC\_FTB\_Table[55] 255 Dem\_DTC\_FTB\_Table[56] 255 Dem\_DTC\_FTB\_Table[57] 255 Dem\_DTC\_FTB\_Table[58] 255 Dem\_DTC\_FTB\_Table[59] 255 Dem\_DTC\_FTB\_Table[60] 255 Dem\_DTC\_FTB\_Table[61] 255 Dem\_DTC\_FTB\_Table[62] 255 Dem\_DTC\_FTB\_Table[63] 255 Dem\_DTC\_FTB\_Table[64] 255 Dem\_DTC\_FTB\_Table[65] 255 Dem\_DTC\_FTB\_Table[66] 255 Dem DTC FTB Table[67] 255 Dem\_DTC\_FTB\_Table[68] 255 Dem DTC FTB Table[69] 255 Dem\_DTC\_FTB\_Table[70] 255 Dem DTC FTB Table[71] 255 Dem\_DTC\_FTB\_Table[72] 255 Dem\_DTC\_FTB\_Table[73] 255 Dem\_DTC\_FTB\_Table[74] 255 Dem\_DTC\_FTB\_Table[75] 255 255 Dem\_DTC\_FTB\_Table[76] **Actual Value Expected Value** Name Result CTCFailedBuf\_Cnt\_M\_lgc[0] 0 CTCFailedBuf Cnt M Iqc[1] 0 CTCFailedBuf\_Cnt\_M\_lgc[2] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[3] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[4] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[5] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[6] n n CTCFailedBuf\_Cnt\_M\_lgc[7] 0 0 ~ CTCFailedBuf\_Cnt\_M\_lgc[8] n n CTCFailedBuf\_Cnt\_M\_lgc[9] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[10] n 0 CTCFailedBuf\_Cnt\_M\_lgc[11] 0 0 CTCFailedBuf Cnt M Igc[12] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[13] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[14] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[15] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[16] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[17] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[18] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[19] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[20] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[21] 0 0 0 **~** CTCFailedBuf\_Cnt\_M\_lgc[22] 0 CTCFailedBuf\_Cnt\_M\_lgc[23] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[24] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[25] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[26] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[27] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[28] 0 0 CTCFailedBuf Cnt M Igc[29] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[30] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[31] 0 0 ~ CTCFailedBuf\_Cnt\_M\_lgc[32] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[33] 0 0

2018-04-10, 18:44:44+0530



Demlf\_DTCS Ch n e

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[34]	0	0	~
CTCFailedBuf_Cnt_M_lgc[35]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[36]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[37]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[38]	0	0	~
CTCFailedBuf_Cnt_M_lgc[39]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[40]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[41]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[42]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[43]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[44]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[45]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[46]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[47]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[48]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[49]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[50]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[51]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[52]	0	0	~
CTCFailedBuf_Cnt_M_lgc[53]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[54]	0	0	~
CTCFailedBuf_Cnt_M_lgc[55]	0	0	~
CTCFailedBuf_Cnt_M_lgc[56]	0	0	~
CTCFailedBuf_Cnt_M_lgc[57]	0	0	~
CTCFailedBuf_Cnt_M_lgc[58]	0	0	~
CTCFailedBuf_Cnt_M_lgc[59]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[60]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[61]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[62]	0	0	~
CTCFailedBuf_Cnt_M_lgc[63]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[64]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[65]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[66]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[67]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[68]	0	0	~
CTCFailedBuf_Cnt_M_lgc[69]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[70]	0	0	~
CTCFailedBuf_Cnt_M_lgc[71]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[72]	0	0	~
CTCFailedBuf_Cnt_M_lgc[73]	0	0	~
CTCFailedBuf_Cnt_M_lgc[74]	0	0	~
CTCFailedBuf_Cnt_M_lgc[75]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[76]	0	0	~
CTCFailed_Cnt_M_lgc	0	0	<b>✓</b>
Demlf_DTCStatusChanged()	0	0	~
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc(data)	0	0	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	~

Test Step 1.2 (Repeat Count = 1)		<b>~</b>
Name	Input Value	
CTCFailedBuf_Cnt_M_lgc[0]	0	
CTCFailedBuf_Cnt_M_lgc[1]	1	
CTCFailedBuf_Cnt_M_lgc[2]	1	
CTCFailedBuf_Cnt_M_lgc[3]	1	
CTCFailedBuf_Cnt_M_lgc[4]	1	
CTCFailedBuf_Cnt_M_lgc[5]	1	
CTCFailedBuf_Cnt_M_lgc[6]	1	
CTCFailedBuf_Cnt_M_lgc[7]	1	
CTCFailedBuf_Cnt_M_lgc[8]	1	
CTCFailedBuf_Cnt_M_lgc[9]	1	
CTCFailedBuf_Cnt_M_lgc[10]	1	
CTCFailedBuf_Cnt_M_lgc[11]	1	
CTCFailedBuf_Cnt_M_lgc[12]	1	
CTCFailedBuf_Cnt_M_lgc[13]	1	
CTCFailedBuf_Cnt_M_lgc[14]	1	
CTCFailedBuf_Cnt_M_lgc[15]	1	
CTCFailedBuf_Cnt_M_lgc[16]	1	

2018-04-10, 18:44:44+0530



Demlf\_DTCS Ch n e Input Value

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	1
CTCFailedBuf_Cnt_M_Igc[21]	1
CTCFailedBuf_Cnt_M_lgc[22]	1
CTCFailedBuf_Cnt_M_Igc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	1
CTCFailedBuf_Cnt_M_lgc[35]	1
CTCFailedBuf_Cnt_M_lgc[36]	1
CTCFailedBuf_Cnt_M_lgc[37]	1
CTCFailedBuf_Cnt_M_lgc[38]	1
CTCFailedBuf_Cnt_M_lgc[39]	1
CTCFailedBuf_Cnt_M_lgc[40]	1
CTCFailedBuf_Cnt_M_lgc[41]	1
CTCFailedBuf_Cnt_M_lgc[42]	1
CTCFailedBuf_Cnt_M_lgc[43]	1
CTCFailedBuf_Cnt_M_lgc[44]	1
CTCFailedBuf_Cnt_M_lgc[45]	1
CTCFailedBuf_Cnt_M_lgc[46]	1
CTCFailedBuf_Cnt_M_lgc[47]	1
CTCFailedBuf_Cnt_M_lgc[48]	1
CTCFailedBuf_Cnt_M_lgc[49]	1
CTCFailedBuf_Cnt_M_lgc[50]	1
CTCFailedBuf_Cnt_M_Igc[51]	1
CTCFailedBuf_Cnt_M_lgc[52]	1
CTCFailedBuf_Cnt_M_Igc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1
CTCFailedBuf_Cnt_M_lgc[64]	1
CTCFailedBuf_Cnt_M_lgc[65]	1
CTCFailedBuf_Cnt_M_lgc[66]	1
CTCFailedBuf_Cnt_M_lgc[67]	1
CTCFailedBuf_Cnt_M_lgc[68]	1
CTCFailedBuf_Cnt_M_Igc[69]	1
CTCFailedBuf_Cnt_M_lgc[70]	1
CTCFailedBuf_Cnt_M_lgc[71]	1
CTCFailedBuf_Cnt_M_lgc[72]	1
CTCFailedBuf_Cnt_M_lgc[73]	1
CTCFailedBuf_Cnt_M_lgc[74]	1
CTCFailedBuf_Cnt_M_lgc[75]	1
CTCFailedBuf_Cnt_M_lgc[76]	1
CTCFailed_Cnt_M_lgc	0
DTC	0
DTCKind	1
DTCStatusNew	0
DTCStatusOld	0
Dem_DTCNumberTable[0]	0
Dem_DTCNumberTable[1]	0
Dem_DTCNumberTable[2]	0
Dem_DTCNumberTable[3]	0
Dem_DTCNumberTable[4]	0
Dem_DTCNumberTable[5]	0
Dem_DTCNumberTable[6]	0
Dem_DTCNumberTable[7]	0

### **TEST DETAILS REPORT** Ch n e

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Name	Input Value
Dem_DTCNumberTable[8]	0
Dem_DTCNumberTable[9]	0
	0
Dem_DTCNumberTable[10]	
Dem_DTCNumberTable[11]	0
Dem_DTCNumberTable[12]	0
Dem_DTCNumberTable[13]	0
Dem_DTCNumberTable[14]	0
Dem_DTCNumberTable[15]	0
Dem_DTCNumberTable[16]	0
Dem_DTCNumberTable[17]	0
Dem_DTCNumberTable[18]	0
Dem_DTCNumberTable[19]	0
	0
Dem_DTCNumberTable[20]	
Dem_DTCNumberTable[21]	0
Dem_DTCNumberTable[22]	0
Dem_DTCNumberTable[23]	0
Dem_DTCNumberTable[24]	0
Dem_DTCNumberTable[25]	0
Dem_DTCNumberTable[26]	0
Dem_DTCNumberTable[27]	0
Dem_DTCNumberTable[28]	0
Dem_DTCNumberTable[29]	0
Dem_DTCNumberTable[30]	0
Dem DTCNumberTable[31]	0
	0
Dem_DTCNumberTable[32]	
Dem_DTCNumberTable[33]	0
Dem_DTCNumberTable[34]	0
Dem_DTCNumberTable[35]	0
Dem_DTCNumberTable[36]	0
Dem_DTCNumberTable[37]	0
Dem_DTCNumberTable[38]	0
Dem_DTCNumberTable[39]	0
Dem_DTCNumberTable[40]	0
Dem_DTCNumberTable[41]	0
Dem_DTCNumberTable[42]	0
Dem_DTCNumberTable[43]	0
Dem_DTCNumberTable[44]	0
Dem_DTCNumberTable[45]	0
Dem_DTCNumberTable[46]	0
Dem_DTCNumberTable[47]	0
Dem_DTCNumberTable[48]	0
Dem_DTCNumberTable[49]	0
Dem_DTCNumberTable[50]	0
Dem_DTCNumberTable[51]	0
Dem_DTCNumberTable[52]	0
Dem_DTCNumberTable[53]	0
Dem_DTCNumberTable[54]	0
Dem_DTCNumberTable[55]	0
Dem DTCNumberTable[56]	0
Dem_DTCNumberTable[57]	0
	0
Dem_DTCNumberTable[58]	0
Dem_DTCNumberTable[59]	
Dem_DTCNumberTable[60]	0
Dem_DTCNumberTable[61]	0
Dem_DTCNumberTable[62]	0
Dem_DTCNumberTable[63]	0
Dem_DTCNumberTable[64]	0
Dem_DTCNumberTable[65]	0
Dem_DTCNumberTable[66]	0
Dem_DTCNumberTable[67]	0
Dem_DTCNumberTable[68]	0
Dem_DTCNumberTable[69]	0
Dem_DTCNumberTable[70]	0
	0
Dem_DTCNumberTable[71]	
Dem_DTCNumberTable[72]	0
Dem_DTCNumberTable[73]	0
Dem_DTCNumberTable[74]	0
Dem_DTCNumberTable[75]	0
Dem_DTCNumberTable[76]	0
Dem_DTC_FTB_Table[0]	0
Dem_DTC_FTB_Table[1]	0
Dem_DTC_FTB_Table[2]	0
Dem_DTC_FTB_Table[3]	0

2018-04-10, 18:44:44+0530



DemIf\_DTCS Name Input Value Dem\_DTC\_FTB\_Table[4] 0 Dem\_DTC\_FTB\_Table[5] 0 Dem\_DTC\_FTB\_Table[6] 0 Dem\_DTC\_FTB\_Table[7] 0 Dem\_DTC\_FTB\_Table[8] 0 Dem\_DTC\_FTB\_Table[9] 0 Dem\_DTC\_FTB\_Table[10] 0 Dem\_DTC\_FTB\_Table[11] 0 Dem\_DTC\_FTB\_Table[12] 0 Dem\_DTC\_FTB\_Table[13] n Dem\_DTC\_FTB\_Table[14] 0 Dem\_DTC\_FTB\_Table[15] n Dem\_DTC\_FTB\_Table[16] 0 Dem DTC FTB Table[17] n Dem\_DTC\_FTB\_Table[18] 0 Dem\_DTC\_FTB\_Table[19] 0 Dem\_DTC\_FTB\_Table[20] 0 Dem\_DTC\_FTB\_Table[21] 0 Dem\_DTC\_FTB\_Table[22] 0 Dem\_DTC\_FTB\_Table[23] 0 Dem\_DTC\_FTB\_Table[24] 0 Dem\_DTC\_FTB\_Table[25] 0 Dem\_DTC\_FTB\_Table[26] 0 Dem\_DTC\_FTB\_Table[27] 0 Dem\_DTC\_FTB\_Table[28] 0 Dem\_DTC\_FTB\_Table[29] 0 Dem\_DTC\_FTB\_Table[30] 0 Dem\_DTC\_FTB\_Table[31] 0 Dem\_DTC\_FTB\_Table[32] 0 Dem\_DTC\_FTB\_Table[33] 0 Dem DTC FTB Table[34] 0 Dem\_DTC\_FTB\_Table[35] n Dem DTC FTB Table[36] 0 Dem\_DTC\_FTB\_Table[37] 0 Dem\_DTC\_FTB\_Table[38] 0 Dem\_DTC\_FTB\_Table[39] 0 Dem\_DTC\_FTB\_Table[40] 0 Dem\_DTC\_FTB\_Table[41] 0 Dem\_DTC\_FTB\_Table[42] 0 Dem DTC FTB Table[43] 0 Dem\_DTC\_FTB\_Table[44] 0 Dem DTC FTB Table[45] 0 Dem\_DTC\_FTB\_Table[46] 0 Dem\_DTC\_FTB\_Table[47] 0 Dem\_DTC\_FTB\_Table[48] 0 Dem\_DTC\_FTB\_Table[49] 0 Dem\_DTC\_FTB\_Table[50] 0 Dem\_DTC\_FTB\_Table[51] 0 Dem\_DTC\_FTB\_Table[52] 0 Dem\_DTC\_FTB\_Table[53] 0 Dem\_DTC\_FTB\_Table[54] 0 Dem\_DTC\_FTB\_Table[55] 0 Dem\_DTC\_FTB\_Table[56] 0 Dem\_DTC\_FTB\_Table[57] 0 Dem\_DTC\_FTB\_Table[58] 0 Dem\_DTC\_FTB\_Table[59] 0 0 Dem\_DTC\_FTB\_Table[60] Dem\_DTC\_FTB\_Table[61] 0 Dem\_DTC\_FTB\_Table[62] 0 Dem\_DTC\_FTB\_Table[63] 0 Dem\_DTC\_FTB\_Table[64] 0 Dem\_DTC\_FTB\_Table[65] 0 Dem\_DTC\_FTB\_Table[66] 0 Dem\_DTC\_FTB\_Table[67] 0 Dem\_DTC\_FTB\_Table[68] 0 Dem DTC FTB Table[69] 0 Dem\_DTC\_FTB\_Table[70] 0 Dem DTC FTB Table[71] 0 Dem\_DTC\_FTB\_Table[72] 0 Dem\_DTC\_FTB\_Table[73] 0

0

0

0

Dem\_DTC\_FTB\_Table[74]

Dem\_DTC\_FTB\_Table[75]

Dem\_DTC\_FTB\_Table[76]

2018-04-10, 18:44:44+0530

Demlf\_DTCS Ch n e



CTC-selsel CM M 9590   0	Name	Actual Value	Expected Value	Result
GCC-Sended, Cent. M, legitl CCC-Sended, Cent. M, legitl CC			•	Kesuit
CTCPASSASIL CP_M_USCR				•
CTCFaleduck Cent M. 1949  CTCFaleduck Cent M. 1940  CTCFaleduck Cent M. 1941  CTCFaleduck Cent M				~
STEPANOSIL COLUMN 1987	CTCFailedBuf_Cnt_M_lgc[3]	1	1	~
CTCP-instell, Cry, My, 1907   CTCP-instell, Cry, My, 1907   CTCP-instell, Cry, My, 1908   CTCP	CTCFailedBuf_Cnt_M_lgc[4]	1	1	~
CTCFalestay, Col, May 1999   1	CTCFailedBuf_Cnt_M_lgc[5]	1		~
CTCFaledBuff Corf. M. popts				~
CTCFaseBull Coll M 1988   1				
CICCanades Cont.				
CTCFaseBud Core, N.   19613   1				
CTCFaneSett, Cott, My, Set19				
CTCFaiedul, Cott, M., 19413   1   1   1   1   1   1   1   1   1				
CTCFaledball Crit M, jog15		1	1	~
CTCFainceDut Cm M pot71   1   1   1   1   1   1   1   1   1		1	1	~
CTCFareduct, CM, Mg1910   1   1	CTCFailedBuf_Cnt_M_lgc[15]	1	1	~
CTCFanedurd. Cmt. M. jud989   1	CTCFailedBuf_Cnt_M_lgc[16]	1	1	~
CTCFalendard, CTM, Jug 209   1				
CTCFaledML_CRM_big021				_
CTCFaledud, CM, M, p(22)   1   1   1   1   1   1   1   1   1				
CTGFaledbut_CM_M_gqt20    1				
CTCFalendur_Cm_M_sqt29    1				
CTCFalebut, CM, M, 1928) 1				~
TOTA-RIBERT CPL M, 1927  TOTA-RIBERT CPL M, 1927  TOTA-RIBERT CPL M, 1928  TOTA-RIBERT CPL M, 19				~
CTCFaledBuf_CN_M_lgc28	CTCFailedBuf_Cnt_M_lgc[25]	1	1	~
TOTFaleaded Cott M (spc28) 1	CTCFailedBuf_Cnt_M_lgc[26]	1	1	~
CTCFaledBut_Cnt_M_log(20)	CTCFailedBuf_Cnt_M_lgc[27]	1	1	~
TCTFaledBuf_Cnt_M_get30] 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1				
CTCFaledBull_Cnt_M   gct32				~
TCFaledBuf Cnt, M, 19c(32)  CTCFaledBuf Cnt, M, 19c(33)  1  1  CTCFaledBuf Cnt, M, 19c(33)  1  CTCFaledBuf Cnt, M, 19c(34)  1  CTCFaledBuf Cnt, M, 19c(35)  1  CTCFaledBuf Cnt, M, 19c(37)  CTCFaledBuf Cnt, M, 19c(37)  CTCFaledBuf Cnt, M, 19c(38)  1  CTCFaledBuf Cnt, M, 19c(38)  1  CTCFaledBuf Cnt, M, 19c(40)  CTCFaledBuf Cnt, M, 19c(4				•
CTCFaledBuf_Cnt_M_log(33)   1				
CTCFalledBuf Cnt, M, Igq835				~
CTCFaledBuf_Cnt_M_lgc35		1	1	~
CTCFailedBuf_Crt_M_lgcj37  1	CTCFailedBuf_Cnt_M_lgc[35]	1	1	~
CTCFaledBuf_Cnt_M_lgcj38	CTCFailedBuf_Cnt_M_lgc[36]	1		
CTCFailedBuf_Cnt_M_lgd{39}   1				~
CTCFailedBuf_Cnt_M_lgd41] 1 1 1 1 1 1 1 CTCFailedBuf_Cnt_M_lgd42  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1				•
CTCFailedBuf_Cnt_M_lgc[41]				Ž
CTCFailedBuf_Cnt_M_lgc[42]  1				-
CTCFailedBuf_Cnt_M_lgc(44)  1		1	1	~
CTCFailedBuf_Cnt_M_lgc[45]		1	1	~
CTCFailedBuf_Cnt_M_lgc[46]	CTCFailedBuf_Cnt_M_lgc[44]	1		~
CTCFailedBuf_Cnt_M_lgc[47]				~
CTCFailedBuf_Cnt_M_lgc[48]       1       1       1         CTCFailedBuf_Cnt_M_lgc[49]       1       1       1         CTCFailedBuf_Cnt_M_lgc[50]       1       1       1         CTCFailedBuf_Cnt_M_lgc[51]       1       1       1         CTCFailedBuf_Cnt_M_lgc[52]       1       1       1         CTCFailedBuf_Cnt_M_lgc[53]       1       1       1         CTCFailedBuf_Cnt_M_lgc[54]       1       1       1         CTCFailedBuf_Cnt_M_lgc[55]       1       1       1         CTCFailedBuf_Cnt_M_lgc[56]       1       1       1         CTCFailedBuf_Cnt_M_lgc[58]       1       1       1         CTCFailedBuf_Cnt_M_lgc[58]       1       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1       1 <td< td=""><td></td><td></td><td></td><td>~</td></td<>				~
CTCFailedBuf_Cnt_M_lgc[49]       1       1          CTCFailedBuf_Cnt_M_lgc[50]       1       1   .				
CTCFailedBur_Cnt_M_lgc(50)       1       1          CTCFailedBur_Cnt_M_lgc(51)       1       1          CTCFailedBur_Cnt_M_lgc(52)       1       1          CTCFailedBur_Cnt_M_lgc(53)       1       1          CTCFailedBur_Cnt_M_lgc(54)       1       1          CTCFailedBur_Cnt_M_lgc(55)       1       1          CTCFailedBur_Cnt_M_lgc(56)       1       1          CTCFailedBur_Cnt_M_lgc(57)       1       1          CTCFailedBur_Cnt_M_lgc(58)       1       1          CTCFailedBur_Cnt_M_lgc(60)       1       1          CTCFailedBur_Cnt_M_lgc(61)       1       1          CTCFailedBur_Cnt_M_lgc(62)       1       1          CTCFailedBur_Cnt_M_lgc(63)       1       1          CTCFailedBur_Cnt_M_lgc(64)       1       1          CTCFailedBur_Cnt_M_lgc(65)       1       1          CTCFailedBur_Cnt_M_lgc(66)       1       1          CTCFailedBur_Cnt_M_lgc(67)       1       1          CTCFailedBur_Cnt_M_lgc(69)       1       1       .				
CTCFailedBuf_Cnt_M_lgc[51]       1       1          CTCFailedBuf_Cnt_M_lgc[52]       1       1           CTCFailedBuf_Cnt_M_lgc[53]       1       1  .				
CTCFailedBuf_Cnt_M_lgc[52]       1       1          CTCFailedBuf_Cnt_M_lgc[53]       1       1          CTCFailedBuf_Cnt_M_lgc[54]       1       1          CTCFailedBuf_Cnt_M_lgc[55]       1       1          CTCFailedBuf_Cnt_M_lgc[56]       1       1          CTCFailedBuf_Cnt_M_lgc[57]       1       1          CTCFailedBuf_Cnt_M_lgc[58]       1       1          CTCFailedBuf_Cnt_M_lgc[69]       1       1          CTCFailedBuf_Cnt_M_lgc[60]       1       1          CTCFailedBuf_Cnt_M_lgc[61]       1       1          CTCFailedBuf_Cnt_M_lgc[62]       1       1          CTCFailedBuf_Cnt_M_lgc[63]       1       1          CTCFailedBuf_Cnt_M_lgc[63]       1       1          CTCFailedBuf_Cnt_M_lgc[66]       1       1          CTCFailedBuf_Cnt_M_lgc[68]       1       1          CTCFailedBuf_Cnt_M_lgc[68]       1       1          CTCFailedBuf_Cnt_M_lgc[68]       1       1          CTCFailedBuf_Cnt_M_lgc[68]       1       1       .				~
CTCFailedBuf_Cnt_M_lgc[54]       1       1          CTCFailedBuf_Cnt_M_lgc[55]       1       1           CTCFailedBuf_Cnt_M_lgc[56]       1       1  .		1	1	~
CTCFailedBuf_Cnt_M_lgc[55]       1       1         CTCFailedBuf_Cnt_M_lgc[56]       1       1         CTCFailedBuf_Cnt_M_lgc[57]       1       1         CTCFailedBuf_Cnt_M_lgc[58]       1       1         CTCFailedBuf_Cnt_M_lgc[59]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1	CTCFailedBuf_Cnt_M_lgc[53]	1	1	~
CTCFailedBuf_Cnt_M_lgc[56]       1       1          CTCFailedBuf_Cnt_M_lgc[57]       1       1           CTCFailedBuf_Cnt_M_lgc[58]       1       1  .	CTCFailedBuf_Cnt_M_lgc[54]	1	1	~
CTCFailedBuf_Cnt_N_lgc[57]       1       1         CTCFailedBuf_Cnt_N_lgc[58]       1       1         CTCFailedBuf_Cnt_N_lgc[59]       1       1         CTCFailedBuf_Cnt_N_lgc[60]       1       1         CTCFailedBuf_Cnt_N_lgc[61]       1       1         CTCFailedBuf_Cnt_N_lgc[62]       1       1         CTCFailedBuf_Cnt_N_lgc[63]       1       1         CTCFailedBuf_Cnt_N_lgc[63]       1       1         CTCFailedBuf_Cnt_N_lgc[65]       1       1         CTCFailedBuf_Cnt_N_lgc[66]       1       1         CTCFailedBuf_Cnt_N_lgc[67]       1       1         CTCFailedBuf_Cnt_N_lgc[68]       1       1         CTCFailedBuf_Cnt_N_lgc[69]       1       1         CTCFailedBuf_Cnt_N_lgc[69]       1       1         CTCFailedBuf_Cnt_N_lgc[70]       1       1         CTCFailedBuf_Cnt_N_lgc[71]       1       1				~
CTCFailedBuf_Cnt_M_lgc[58]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1				~
CTCFailedBuf_Cnt_M_lgc[59]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1				•
CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1				
CTCFailedBuf_Cnt_M  gc 61]       1       1         CTCFailedBuf_Cnt_M  gc 62]       1       1         CTCFailedBuf_Cnt_M  gc 63]       1       1         CTCFailedBuf_Cnt_M  gc 64]       1       1         CTCFailedBuf_Cnt_M  gc 65]       1       1         CTCFailedBuf_Cnt_M  gc 66]       1       1         CTCFailedBuf_Cnt_M  gc 67]       1       1         CTCFailedBuf_Cnt_M  gc 68]       1       1         CTCFailedBuf_Cnt_M  gc 69]       1       1         CTCFailedBuf_Cnt_M  gc 70]       1       1         CTCFailedBuf_Cnt_M  gc 71]       1       1				J
CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1				<b>✓</b>
CTCFailedBuf_Cnt_N_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1		1		~
CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1		1	1	~
CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1				~
CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1				~
CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1				~
CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1				2
CTCFailedBuf_Cnt_M_lgc[70]         1         1         ✓           CTCFailedBuf_Cnt_M_lgc[71]         1         1         ✓				~
CTCFailedBuf_Cnt_M_lgc[71]         1         1				~
CTCFailedBuf_Cnt_M_lgc[72] 1   ✓		1		~
	CTCFailedBuf_Cnt_M_lgc[72]	1	1	~

2018-04-10, 18:44:44+0530



Demlf\_DTCS Ch n e

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[73]	1	1	~
CTCFailedBuf_Cnt_M_lgc[74]	1	1	~
CTCFailedBuf_Cnt_M_lgc[75]	1	1	~
CTCFailedBuf_Cnt_M_lgc[76]	1	1	~
CTCFailed_Cnt_M_lgc	1	1	<b>✓</b>
DemIf_DTCStatusChanged()	0	0	~
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc(data)	1	1	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	~

### Test Case 2: Range Test

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

CPU Cycles:

CPU Cycles:

TS 2.1 2437.00 Cycles
TS 2.2 663.00 Cycles
TS 2.3 3222.00 Cycles
TS 2.4 3208.00 Cycles
TS 2.4 3208.00 Cycles
TS 2.5 3208.00 Cycles
TS 2.6 3208.00 Cycles
TS 2.7 3208.00 Cycles
TS 2.8 3208.00 Cycles
TS 2.9 3208.00 Cycles
TS 2.10 3208.00 Cycles
TS 2.11 3208.00 Cycles
TS 2.11 3208.00 Cycles
TS 2.12 3208.00 Cycles
TS 2.13 3208.00 Cycles
TS 2.14 3208.00 Cycles
TS 2.15 3208.00 Cycles
TS 2.16 3208.00 Cycles
TS 2.17 3208.00 Cycles
TS 2.18 3208.00 Cycles
TS 2.19 3208.00 Cycles
TS 2.19 3208.00 Cycles
TS 2.19 3208.00 Cycles
TS 2.21 3208.00 Cycles
TS 2.21 3208.00 Cycles
TS 2.22 3208.00 Cycles
TS 2.23 3208.00 Cycles
TS 2.24 3208.00 Cycles
TS 2.22 3208.00 Cycles
TS 2.23 3208.00 Cycles
TS 2.24 3208.00 Cycles
TS 2.22 3208.00 Cycles
TS 2.23 3208.00 Cycles
TS 2.24 3208.00 Cycles
TS 2.24 3208.00 Cycles

#### Vector Description: Description

TS 2.1All Min TS 2.2All Max TS 2.3DTC==> Min TS 2.4DTC==> Max TS 2.5DTC==> Pos TS 2.6DTCKind==> Min TS 2.7DTCKind==> Max TS 2.8DTCStatusOld==> Min TS 2.9DTCStatusOld==> Max
TS 2.10DTCStatusOld==> Pos TS 2.11DTCStatusNew==> Min TS 2.12DTCStatusNew==> Max TS 2.13DTCStatusNew==> Pos TS 2.13DTCStatusNew=> Pos
TS 2.14CTCFailedBuf\_Cnt\_M\_lgc[79]==> Min
TS 2.15CTCFailedBuf\_Cnt\_M\_lgc[79]==> Max
TS 2.16CTCFailedBuf\_Cnt\_M\_lgc[79]==> Pos
TS 2.17CTCFailed\_Cnt\_M\_lgc==> Min IS 2.1/CTCFailed\_Cnt\_M\_igc==> Min

TS 2.18CTCFailed\_Cnt\_M\_igc=> Max

TS 2.19Dem\_DTCNumberTable[79]==> Min

TS 2.20Dem\_DTCNumberTable[79]==> Max

TS 2.21Dem\_DTCNumberTable[79]==> Pos

TS 2.22Dem\_DTC\_FTB\_Table[79]==> Min

TS 2.23Dem\_DTC\_FTB\_Table[79]==> Max

TS 2.24Dem\_DTC\_FTB\_Table[79]==> Pos

Test Step 2.1 (Repeat Count = 1)	✓
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	0
CTCFailedBuf_Cnt_M_lgc[1]	0
CTCFailedBuf_Cnt_M_lgc[2]	0
CTCFailedBuf_Cnt_M_lgc[3]	0
CTCFailedBuf_Cnt_M_lgc[4]	0
CTCFailedBuf_Cnt_M_lgc[5]	0
CTCFailedBuf_Cnt_M_lgc[6]	0
CTCFailedBuf_Cnt_M_lgc[7]	0
CTCFailedBuf_Cnt_M_lgc[8]	0
CTCFailedBuf_Cnt_M_lgc[9]	0
CTCFailedBuf_Cnt_M_lgc[10]	0
CTCFailedBuf_Cnt_M_lgc[11]	0

Demlf\_DTCS

2018-04-10, 18:44:44+0530



Input Value CTCFailedBuf\_Cnt\_M\_lgc[12] 0 CTCFailedBuf\_Cnt\_M\_lgc[13] 0 CTCFailedBuf\_Cnt\_M\_lgc[14] 0 CTCFailedBuf\_Cnt\_M\_lgc[15] 0 CTCFailedBuf Cnt M lqc[16] 0 CTCFailedBuf\_Cnt\_M\_lgc[17] 0 CTCFailedBuf\_Cnt\_M\_lgc[18] 0 CTCFailedBuf\_Cnt\_M\_lgc[19] 0 CTCFailedBuf\_Cnt\_M\_lgc[20] 0 CTCFailedBuf\_Cnt\_M\_lgc[21] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[22] CTCFailedBuf\_Cnt\_M\_lgc[23] 0 CTCFailedBuf\_Cnt\_M\_lgc[24] 0 CTCFailedBuf\_Cnt\_M\_lgc[25] 0 CTCFailedBuf\_Cnt\_M\_lgc[26] 0 CTCFailedBuf\_Cnt\_M\_lgc[27] 0 CTCFailedBuf\_Cnt\_M\_lgc[28] 0 CTCFailedBuf\_Cnt\_M\_lgc[29] 0 CTCFailedBuf\_Cnt\_M\_lgc[30] 0 CTCFailedBuf\_Cnt\_M\_lgc[31] 0 CTCFailedBuf\_Cnt\_M\_lgc[32] 0 CTCFailedBuf\_Cnt\_M\_lgc[33] 0 CTCFailedBuf\_Cnt\_M\_lgc[34] 0 CTCFailedBuf\_Cnt\_M\_lgc[35] 0 CTCFailedBuf\_Cnt\_M\_lgc[36] 0 CTCFailedBuf\_Cnt\_M\_lgc[37] 0 CTCFailedBuf\_Cnt\_M\_lgc[38] 0 CTCFailedBuf\_Cnt\_M\_lgc[39] 0 CTCFailedBuf\_Cnt\_M\_lgc[40] 0 CTCFailedBuf\_Cnt\_M\_lgc[41] 0 CTCFailedBuf Cnt M Igc[42] 0 CTCFailedBuf\_Cnt\_M\_lgc[43] 0 CTCFailedBuf Cnt M Igc[44] 0 CTCFailedBuf\_Cnt\_M\_lgc[45] 0 CTCFailedBuf\_Cnt\_M\_lgc[46] 0 CTCFailedBuf\_Cnt\_M\_lgc[47] 0 CTCFailedBuf\_Cnt\_M\_lgc[48] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[49] CTCFailedBuf\_Cnt\_M\_lgc[50] 0 CTCFailedBuf\_Cnt\_M\_lgc[51] 0 CTCFailedBuf\_Cnt\_M\_lgc[52] 0 CTCFailedBuf\_Cnt\_M\_lgc[53] 0 CTCFailedBuf\_Cnt\_M\_lgc[54] 0 CTCFailedBuf\_Cnt\_M\_lgc[55] 0 CTCFailedBuf\_Cnt\_M\_lgc[56] n CTCFailedBuf\_Cnt\_M\_lgc[57] 0 CTCFailedBuf\_Cnt\_M\_lgc[58] n CTCFailedBuf\_Cnt\_M\_lgc[59] 0 CTCFailedBuf\_Cnt\_M\_lgc[60] n CTCFailedBuf\_Cnt\_M\_lgc[61] 0 CTCFailedBuf\_Cnt\_M\_lgc[62] 0 CTCFailedBuf\_Cnt\_M\_lgc[63] 0 CTCFailedBuf\_Cnt\_M\_lgc[64] 0 CTCFailedBuf\_Cnt\_M\_lgc[65] 0 CTCFailedBuf\_Cnt\_M\_lgc[66] 0 CTCFailedBuf\_Cnt\_M\_lgc[67] 0 CTCFailedBuf\_Cnt\_M\_lgc[68] 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 CTCFailedBuf\_Cnt\_M\_lgc[71] CTCFailedBuf\_Cnt\_M\_lgc[72] 0 CTCFailedBuf\_Cnt\_M\_lgc[73] 0 CTCFailedBuf\_Cnt\_M\_lgc[74] 0 CTCFailedBuf\_Cnt\_M\_lgc[75] 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 CTCFailed\_Cnt\_M\_lgc 0 DTC 0 DTCKind 1 DTCStatusNew 0 DTCStatusOld 0 Dem DTCNumberTable[0] 0 Dem\_DTCNumberTable[1] 0 Dem\_DTCNumberTable[2] 0

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Name Input Value Dem\_DTCNumberTable[3] 0 Dem\_DTCNumberTable[4] 0 Dem\_DTCNumberTable[5] 0 Dem\_DTCNumberTable[6] 0 Dem\_DTCNumberTable[7] 0 Dem\_DTCNumberTable[8] 0 Dem\_DTCNumberTable[9] 0 Dem\_DTCNumberTable[10] 0 Dem\_DTCNumberTable[11] 0 Dem DTCNumberTable[12] n Dem\_DTCNumberTable[13] 0 Dem\_DTCNumberTable[14] n Dem\_DTCNumberTable[15] 0 Dem\_DTCNumberTable[16] n Dem\_DTCNumberTable[17] 0 Dem\_DTCNumberTable[18] 0 Dem\_DTCNumberTable[19] 0 Dem\_DTCNumberTable[20] 0 Dem\_DTCNumberTable[21] 0 Dem\_DTCNumberTable[22] 0 Dem\_DTCNumberTable[23] 0 Dem\_DTCNumberTable[24] 0 Dem\_DTCNumberTable[25] 0 Dem\_DTCNumberTable[26] 0 Dem\_DTCNumberTable[27] 0 Dem\_DTCNumberTable[28] 0 Dem\_DTCNumberTable[29] 0 Dem\_DTCNumberTable[30] 0 Dem\_DTCNumberTable[31] 0 Dem\_DTCNumberTable[32] 0 Dem\_DTCNumberTable[33] 0 Dem\_DTCNumberTable[34] 0 Dem DTCNumberTable[35] 0 Dem\_DTCNumberTable[36] 0 Dem\_DTCNumberTable[37] 0 Dem DTCNumberTable[38] 0 Dem\_DTCNumberTable[39] 0 Dem\_DTCNumberTable[40] 0 Dem\_DTCNumberTable[41] 0 Dem DTCNumberTable[42] 0 Dem\_DTCNumberTable[43] 0 Dem DTCNumberTable[44] 0 Dem\_DTCNumberTable[45] 0 Dem\_DTCNumberTable[46] 0 Dem\_DTCNumberTable[47] 0 Dem\_DTCNumberTable[48] 0 0 Dem DTCNumberTable[49] Dem\_DTCNumberTable[50] 0 Dem\_DTCNumberTable[51] 0 Dem\_DTCNumberTable[52] 0 Dem\_DTCNumberTable[53] 0 Dem\_DTCNumberTable[54] 0 Dem\_DTCNumberTable[55] 0 Dem\_DTCNumberTable[56] 0 Dem\_DTCNumberTable[57] 0 Dem\_DTCNumberTable[58] 0 Dem\_DTCNumberTable[59] 0 Dem\_DTCNumberTable[60] 0 0 Dem\_DTCNumberTable[61] Dem\_DTCNumberTable[62] 0 Dem\_DTCNumberTable[63] 0 Dem DTCNumberTable[64] 0 Dem\_DTCNumberTable[65] 0 Dem DTCNumberTable[66] 0 Dem\_DTCNumberTable[67] 0 Dem DTCNumberTable[68] 0 Dem\_DTCNumberTable[69] 0 Dem DTCNumberTable[70] 0 Dem\_DTCNumberTable[71] 0 Dem\_DTCNumberTable[72] 0 Dem\_DTCNumberTable[73] 0 Dem\_DTCNumberTable[74] 0 Dem\_DTCNumberTable[75] 0

### **TEST DETAILS REPORT** Ch n e

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Name	Input Value
Dem_DTCNumberTable[76]	0
Dem_DTC_FTB_Table[0]	0
Dem_DTC_FTB_Table[1]	0
Dem_DTC_FTB_Table[2]	0
Dem_DTC_FTB_Table[3]	0
Dem_DTC_FTB_Table[4]	0
Dem_DTC_FTB_Table[5]	0
Dem_DTC_FTB_Table[6]	0
Dem_DTC_FTB_Table[7]	0
Dem_DTC_FTB_Table[8]	0
Dem_DTC_FTB_Table[9]	0
Dem_DTC_FTB_Table[10]	0
Dem_DTC_FTB_Table[11]	0
Dem_DTC_FTB_Table[12]	0
Dem_DTC_FTB_Table[13]	0
Dem_DTC_FTB_Table[14]	0
Dem_DTC_FTB_Table[15]	0
Dem_DTC_FTB_Table[16]	0
Dem_DTC_FTB_Table[17]	0
Dem_DTC_FTB_Table[18]	0
Dem_DTC_FTB_Table[19]	0
Dem_DTC_FTB_Table[19] Dem_DTC_FTB_Table[20]	0
Dem_DTC_FTB_Table[21]	0
Dem_DTC_FTB_Table[22]	0
	0
Dem_DTC_FTB_Table[23] Dem_DTC_FTB_Table[24]	0
	0
Dem_DTC_FTB_Table[25] Dem_DTC_FTB_Table[26]	0
	0
Dem_DTC_FTB_Table[27]	0
Dem_DTC_FTB_Table[28]	
Dem_DTC_FTB_Table[29]	0
Dem_DTC_FTB_Table[30]	0
Dem_DTC_FTB_Table[31]	0
Dem_DTC_FTB_Table[32]	0
Dem_DTC_FTB_Table[33]	0
Dem_DTC_FTB_Table[34]	0
Dem_DTC_FTB_Table[35]	0
Dem_DTC_FTB_Table[36]	0
Dem_DTC_FTB_Table[37]	0
Dem_DTC_FTB_Table[38]	0
Dem_DTC_FTB_Table[39]	0
Dem_DTC_FTB_Table[40]	0
Dem_DTC_FTB_Table[41]	0
Dem_DTC_FTB_Table[42]	0
Dem_DTC_FTB_Table[43]	0
Dem_DTC_FTB_Table[44]	0
Dem_DTC_FTB_Table[45]	0
Dem_DTC_FTB_Table[46]	0
Dem_DTC_FTB_Table[47]	0
Dem_DTC_FTB_Table[48]	0
Dem_DTC_FTB_Table[49]	0
Dem_DTC_FTB_Table[50]	0
Dem_DTC_FTB_Table[51]	0
Dem_DTC_FTB_Table[52]	0
Dem_DTC_FTB_Table[53]	0
Dem_DTC_FTB_Table[54]	0
Dem_DTC_FTB_Table[55]	0
Dem_DTC_FTB_Table[56]	0
Dem_DTC_FTB_Table[57]	0
Dem_DTC_FTB_Table[58]	0
Dem_DTC_FTB_Table[59]	0
Dem_DTC_FTB_Table[60]	0
Dem_DTC_FTB_Table[61]	0
Dem_DTC_FTB_Table[62]	0
Dem_DTC_FTB_Table[63]	0
Dem_DTC_FTB_Table[64]	0
Dem_DTC_FTB_Table[65]	0
Dem_DTC_FTB_Table[66]	0
Dem_DTC_FTB_Table[67]	0
Dem_DTC_FTB_Table[68]	0
Dem_DTC_FTB_Table[69]	0
Dem_DTC_FTB_Table[70]	0
Dem_DTC_FTB_Table[71]	0

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value Dem DTC FTB Table[72] 0 Dem\_DTC\_FTB\_Table[73] Dem\_DTC\_FTB\_Table[74] 0 Dem\_DTC\_FTB\_Table[75] 0 Dem\_DTC\_FTB\_Table[76] 0 **Actual Value Expected Value** Name Result CTCFailedBuf\_Cnt\_M\_lgc[0] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[1] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[2] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[3] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[4] n n CTCFailedBuf\_Cnt\_M\_lgc[5] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[6] n 0 CTCFailedBuf\_Cnt\_M\_lgc[7] 0 0 n n CTCFailedBuf Cnt M lgc[8] CTCFailedBuf\_Cnt\_M\_lgc[9] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[10] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[11] 0 0 CTCFailedBuf Cnt M lqc[12] 0 0  $CTCFailedBuf\_Cnt\_M\_lgc[13]$ 0 0 CTCFailedBuf\_Cnt\_M\_lgc[14] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[15] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[16] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[17] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[18] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[19] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[20] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[21] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[22] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[23] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[24] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[25] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[26] n n CTCFailedBuf Cnt M Igc[27] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[28] 0 0 **v** CTCFailedBuf\_Cnt\_M\_lgc[29] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[30] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[31] 0 ~ CTCFailedBuf\_Cnt\_M\_lgc[32] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[33] 0 0 CTCFailedBuf Cnt M lqc[34] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[35] 0 0 CTCFailedBuf Cnt M lqc[36] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[37] 0 0 CTCFailedBuf Cnt M lqc[38] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[39] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[40] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[41] 0 0 0 CTCFailedBuf\_Cnt\_M\_lgc[42] 0 **~** CTCFailedBuf\_Cnt\_M\_lgc[43] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[44] 0 0 **~** CTCFailedBuf\_Cnt\_M\_lgc[45] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[46] 0 0 **~** CTCFailedBuf\_Cnt\_M\_lgc[47] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[48] 0 0 **~** CTCFailedBuf\_Cnt\_M\_lgc[49] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[50] 0 0 **v** CTCFailedBuf\_Cnt\_M\_lgc[51] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[52] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[53] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[54] 0 0 0 0 CTCFailedBuf\_Cnt\_M\_lgc[55] CTCFailedBuf Cnt M Igc[56] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[57] 0 0 CTCFailedBuf Cnt M lqc[58] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[59] 0 0 0 CTCFailedBuf Cnt M lqc[60] 0 CTCFailedBuf\_Cnt\_M\_lgc[61] 0 0 CTCFailedBuf Cnt M Igc[62] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[63] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[64] 0 0  $CTCFailedBuf\_Cnt\_M\_lgc[65]$ 0 0 CTCFailedBuf\_Cnt\_M\_lgc[66] 0 0

Demlf\_DTCS

2018-04-10, 18:44:44+0530



**Actual Value Expected Value** CTCFailedBuf\_Cnt\_M\_lgc[67] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[68] 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[73] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[74] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[75] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 0 CTCFailed\_Cnt\_M\_lgc 0 0 Demlf\_DTCStatusChanged() 0 0 Rte\_Write\_Ap\_Demlf\_CTCFailed\_Cnt\_lgc(data) 0 0

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte Write Ap Demlf CTCFailed Cnt lgc	1	Rte Write Ap Demlf CTCFailed Cnt lgc	1	•

CTCPainceStur Crit. M. jpc71   1   1   1   1   1   1   1   1   1		
CTCPainedful, Cru, M, 1941    1	Test Step 2.2 (Repeat Count = 1)	
CTCFaledBuff_CTM_Mgd2  1	Name	
CTCFaledBuf_CR_M_IngS]	CTCFailedBuf_Cnt_M_lgc[0]	
CICPalestiful Cott, M. 1945  CICPalestiful Cott, M. 1941  CICPalestiful Cott, M. 1942  CICPalestiful Cott, M. 1943  CICPalestiful Cott, M. 1944  CICPalestiful Co	CTCFailedBuf_Cnt_M_lgc[1]	
CICFaiedbuf_Cn_M_lgclg) 1 CICFaiedbuf_Cn_M_l		
CTCFaiedBuf_Cnt_M_lgc[8]	CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFaiedBuf_Cnt_M_19d7	CTCFailedBuf_Cnt_M_lgc[4]	
CICFailedBuf_Crt_M_lgct0 CICFailedBuf_Crt_M_lgct0 CICFailedBuf_Crt_M_lgct0 CICFailedBuf_Crt_M_lgct10 CICFailedBuf_Crt_M_lgct10 CICFailedBuf_Crt_M_lgct11 1 CICFailedBuf_Crt_M_lgct11 1 CICFailedBuf_Crt_M_lgct12 CICFailedBuf_Crt_M_lgct13 1 CICFailedBuf_Crt_M_lgct13 1 CICFailedBuf_Crt_M_lgct16 CICFailedBuf_Crt_M_lgct16 CICFailedBuf_Crt_M_lgct17 CICFailedBuf_Crt_M_lgct18 CICFailedBuf_Crt_M_lgct18 CICFailedBuf_Crt_M_lgct18 CICFailedBuf_Crt_M_lgct10 CICFailedBuf_Crt_M_lgct10 CICFailedBuf_Crt_M_lgct10 CICFailedBuf_Crt_M_lgct10 CICFailedBuf_Crt_M_lgct20 1 CICFailedBuf_Crt_M_lgct30 1 CICFailedBuf_Crt_M_lgct30 1 CICFailedBuf_Crt_M_lgct30 1 CICFailedBuf_Crt_M_lgct30 1 CICFailedBuf_Crt_M_lgct30 1 CICFailedBuf_Crt_M_lgct40 1 CICFailed	CTCFailedBuf_Cnt_M_lgc[5]	1
CICFaiedBuf, Cnt, M, lgd?]  CI	CTCFailedBuf_Cnt_M_lgc[6]	1
CICFalesbur, Crit, M. Jog-10 CICFalesbur, Crit, M. Jog-20 CICFalesbur, Cri	CTCFailedBuf_Cnt_M_lgc[7]	1
CICFailedBuf_Cnt_M_lgc[10] 1 CICFailedBuf_Cnt_M_lgc[11] 1 CICFailedBuf_Cnt_M_lgc[13] 1 CICFailedBuf_Cnt_M_lgc[13] 1 CICFailedBuf_Cnt_M_lgc[14] 1 CICFailedBuf_Cnt_M_lgc[15] 1 CICFailedBuf_Cnt_M_lgc[15] 1 CICFailedBuf_Cnt_M_lgc[15] 1 CICFailedBuf_Cnt_M_lgc[16] 1 CICFailedBuf_Cnt_M_lgc[17] 1 CICFailedBuf_Cnt_M_lgc[18] 1 CICFailedBuf_Cnt_M_lgc[18] 1 CICFailedBuf_Cnt_M_lgc[18] 1 CICFailedBuf_Cnt_M_lgc[18] 1 CICFailedBuf_Cnt_M_lgc[20] 1 CICFailedBuf_Cnt_M_lgc[40] 1 CICFailedBuf_Cnt	CTCFailedBuf_Cnt_M_lgc[8]	1
CICFaiedBuf, Crit, M. Jog(19) CITCFaiedBuf, Crit, M. Jog(18) CITCFaiedBuf, Crit, M. Jog(18) CICFaiedBuf, Crit, M. Jog(19) CICFaiedBuf, Crit, M. Jog(19) CICFaiedBuf, Crit, M. Jog(19) CICFaiedBuf, Crit, M. Jog(19) CICFaiedBuf, Crit, M. Jog(20) CICFaiedBuf, Crit, M. Jog(40) CICF	CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc 12  1 CTCFailedBuf_Cnt_M_lgc 13  1 CTCFailedBuf_Cnt_M_lgc 14  1 CTCFailedBuf_Cnt_M_lgc 15  1 CTCFailedBuf_Cnt_M_lgc 16  1 CTCFailedBuf_Cnt_M_lgc 17  1 CTCFailedBuf_Cnt_M_lgc 17  1 CTCFailedBuf_Cnt_M_lgc 18  1 CTCFailedBuf_Cnt_M_lgc 19  1 CTCFailedBuf_Cnt_M_lgc 20  1 CTCFailedBuf_Cnt_M_lgc 20  1 CTCFailedBuf_Cnt_M_lgc 21  1 CTCFailedBuf_Cnt_M_lgc 21  1 CTCFailedBuf_Cnt_M_lgc 22  1 CTCFailedBuf_Cnt_M_lgc 23  1 CTCFailedBuf_Cnt_M_lgc 23  1 CTCFailedBuf_Cnt_M_lgc 25  1 CTCFailedBuf_Cnt_M_lgc 25  1 CTCFailedBuf_Cnt_M_lgc 26  1 CTCFailedBuf_Cnt_M_lgc 27  1 CTCFailedBuf_Cnt_M_lgc 28  1 CTCFailedBuf_Cnt_M_lgc 38  1 CTCFailedBuf_Cnt_M_lgc 48  1	CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFaiedBuf_Cnt_M_lgc[13] 1 CTCFaiedBuf_Cnt_M_lgc[15] 1 CTCFaiedBuf_Cnt_M_lgc[16] 1 CTCFaiedBuf_Cnt_M_lgc[16] 1 CTCFaiedBuf_Cnt_M_lgc[16] 1 CTCFaiedBuf_Cnt_M_lgc[18] 1 CTCFaiedBuf_Cnt_M_lgc[18] 1 CTCFaiedBuf_Cnt_M_lgc[18] 1 CTCFaiedBuf_Cnt_M_lgc[18] 1 CTCFaiedBuf_Cnt_M_lgc[20] 1 CTCFaiedBuf_Cnt_M_lgc[21] 1 CTCFaiedBuf_Cnt_M_lgc[21] 1 CTCFaiedBuf_Cnt_M_lgc[21] 1 CTCFaiedBuf_Cnt_M_lgc[23] 1 CTCFaiedBuf_Cnt_M_lgc[23] 1 CTCFaiedBuf_Cnt_M_lgc[24] 1 CTCFaiedBuf_Cnt_M_lgc[26] 1 CTCFaiedBuf_Cnt_M_lgc[26] 1 CTCFaiedBuf_Cnt_M_lgc[26] 1 CTCFaiedBuf_Cnt_M_lgc[28] 1 CTCFaiedBuf_Cnt_M_lgc[48] 1	CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc 14  1 CTCFailedBuf_Cnt_M_lgc 15  1 CTCFailedBuf_Cnt_M_lgc 16  1 CTCFailedBuf_Cnt_M_lgc 17  1 CTCFailedBuf_Cnt_M_lgc 18  1 CTCFailedBuf_Cnt_M_lgc 18  1 CTCFailedBuf_Cnt_M_lgc 19  1 CTCFailedBuf_Cnt_M_lgc 20  1 CTCFailedBuf_Cnt_M_lgc 21  1 CTCFailedBuf_Cnt_M_lgc 21  1 CTCFailedBuf_Cnt_M_lgc 22  1 CTCFailedBuf_Cnt_M_lgc 23  1 CTCFailedBuf_Cnt_M_lgc 24  1 CTCFailedBuf_Cnt_M_lgc 26  1 CTCFailedBuf_Cnt_M_lgc 28  1 CTCFailedBuf_Cnt_M_lgc 30  1 CTCFailedBuf_Cnt_M_lgc 30  1 CTCFailedBuf_Cnt_M_lgc 30  1 CTCFailedBuf_Cnt_M_lgc 35  1 CTCFailedBuf_Cnt_M_lgc 36  1 CTCFailedBuf_Cnt_M_lgc 38  1 CTCFailedBuf_Cnt_M_lgc 40  1	CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[15] 1 CTCFailedBuf_Cnt_M_lgc[16] 1 CTCFailedBuf_Cnt_M_lgc[17] 1 CTCFailedBuf_Cnt_M_lgc[18] 1 CTCFailedBuf_Cnt_M_lgc[18] 1 CTCFailedBuf_Cnt_M_lgc[18] 1 CTCFailedBuf_Cnt_M_lgc[20] 1 CTCFailedBuf_Cnt_M_lgc[21] 1 CTCFailedBuf_Cnt_M_lgc[22] 1 CTCFailedBuf_Cnt_M_lgc[23] 1 CTCFailedBuf_Cnt_M_lgc[23] 1 CTCFailedBuf_Cnt_M_lgc[24] 1 CTCFailedBuf_Cnt_M_lgc[25] 1 CTCFailedBuf_Cnt_M_lgc[26] 1 CTCFailedBuf_Cnt_M_lgc[26] 1 CTCFailedBuf_Cnt_M_lgc[26] 1 CTCFailedBuf_Cnt_M_lgc[26] 1 CTCFailedBuf_Cnt_M_lgc[26] 1 CTCFailedBuf_Cnt_M_lgc[28] 1 CTCFailedBuf_Cnt_M_lgc[28] 1 CTCFailedBuf_Cnt_M_lgc[28] 1 CTCFailedBuf_Cnt_M_lgc[28] 1 CTCFailedBuf_Cnt_M_lgc[28] 1 CTCFailedBuf_Cnt_M_lgc[28] 1 CTCFailedBuf_Cnt_M_lgc[30] 1 CTCFailedBuf_Cnt_M_lgc[40] 1 CTCFailedBuf_Cnt	CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFaledBuf_Cnt_M_lgc[16] 1 CTCFaledBuf_Cnt_M_lgc[18] 1 CTCFaledBuf_Cnt_M_lgc[18] 1 CTCFaledBuf_Cnt_M_lgc[19] 1 CTCFaledBuf_Cnt_M_lgc[20] 1 CTCFaledBuf_Cnt_M_lgc[20] 1 CTCFaledBuf_Cnt_M_lgc[21] 1 CTCFaledBuf_Cnt_M_lgc[22] 1 CTCFaledBuf_Cnt_M_lgc[23] 1 CTCFaledBuf_Cnt_M_lgc[23] 1 CTCFaledBuf_Cnt_M_lgc[23] 1 CTCFaledBuf_Cnt_M_lgc[26] 1 CTCFaledBuf_Cnt_M_lgc[26] 1 CTCFaledBuf_Cnt_M_lgc[26] 1 CTCFaledBuf_Cnt_M_lgc[26] 1 CTCFaledBuf_Cnt_M_lgc[26] 1 CTCFaledBuf_Cnt_M_lgc[26] 1 CTCFaledBuf_Cnt_M_lgc[28] 1 CTCFaledBuf_Cnt_M_lgc[48] 1	CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc 17  1 CTCFailedBuf_Cnt_M_lgc 18  1 CTCFailedBuf_Cnt_M_lgc 19  1 CTCFailedBuf_Cnt_M_lgc 20  1 CTCFailedBuf_Cnt_M_lgc 40  1	CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFaiedBuf_Cnt_M_lgct17] 1 CTCFaiedBuf_Cnt_M_lgct18] 1 CTCFaiedBuf_Cnt_M_lgct19] 1 CTCFaiedBuf_Cnt_M_lgct20] 1 CTCFaiedBuf_Cnt_M_lgct20] 1 CTCFaiedBuf_Cnt_M_lgct21] 1 CTCFaiedBuf_Cnt_M_lgct22] 1 CTCFaiedBuf_Cnt_M_lgct22] 1 CTCFaiedBuf_Cnt_M_lgct23] 1 CTCFaiedBuf_Cnt_M_lgct24] 1 CTCFaiedBuf_Cnt_M_lgct24] 1 CTCFaiedBuf_Cnt_M_lgct26] 1 CTCFaiedBuf_Cnt_M_lgct26] 1 CTCFaiedBuf_Cnt_M_lgct27] 1 CTCFaiedBuf_Cnt_M_lgct27] 1 CTCFaiedBuf_Cnt_M_lgct28] 1 CTCFaiedBuf_Cnt_M_lgct30] 1 CTCFaiedBuf_Cnt_M_lgct40] 1 CTCFaiedBuf_Cnt_M_lgct40] 1 CTCFaiedBuf_Cnt_M_lgct41] 1 CT	CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFaledBuf_Cnt_M_lgc[18]         1           CTCFaledBuf_Cnt_M_lgc[20]         1           CTCFaledBuf_Cnt_M_lgc[21]         1           CTCFaledBuf_Cnt_M_lgc[21]         1           CTCFaledBuf_Cnt_M_lgc[23]         1           CTCFaledBuf_Cnt_M_lgc[23]         1           CTCFaledBuf_Cnt_M_lgc[24]         1           CTCFaledBuf_Cnt_M_lgc[26]         1           CTCFaledBuf_Cnt_M_lgc[27]         1           CTCFaledBuf_Cnt_M_lgc[28]         1           CTCFaledBuf_Cnt_M_lgc[28]         1           CTCFaledBuf_Cnt_M_lgc[28]         1           CTCFaledBuf_Cnt_M_lgc[28]         1           CTCFaledBuf_Cnt_M_lgc[28]         1           CTCFaledBuf_Cnt_M_lgc[30]         1           CTCFaledBuf_Cnt_M_lgc[30]         1           CTCFaledBuf_Cnt_M_lgc[32]         1           CTCFaledBuf_Cnt_M_lgc[33]         1           CTCFaledBuf_Cnt_M_lgc[36]         1           CTCFaledBuf_Cnt_M_lgc[38]         1           CTCFaledBuf_Cnt_M_lgc[38]         1           CTCFaledBuf_Cnt_M_lgc[38]         1           CTCFaledBuf_Cnt_M_lgc[48]         1           CTCFaledBuf_Cnt_M_lgc[48]         1           CTCFaledBuf_Cnt_M_lgc[48]         1 <t< td=""><td></td><td>1</td></t<>		1
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CTCFailedBuf_Cnt_M_lgc[35]       1         CTCFailedBuf_Cnt_M_lgc[37]       1         CTCFailedBuf_Cnt_M_lgc[38]       1         CTCFailedBuf_Cnt_M_lgc[39]       1         CTCFailedBuf_Cnt_M_lgc[40]       1         CTCFailedBuf_Cnt_M_lgc[41]       1         CTCFailedBuf_Cnt_M_lgc[42]       1         CTCFailedBuf_Cnt_M_lgc[43]       1         CTCFailedBuf_Cnt_M_lgc[43]       1         CTCFailedBuf_Cnt_M_lgc[44]       1         CTCFailedBuf_Cnt_M_lgc[45]       1         CTCFailedBuf_Cnt_M_lgc[46]       1         CTCFailedBuf_Cnt_M_lgc[47]       1         CTCFailedBuf_Cnt_M_lgc[48]       1		
CTCFailedBuf_Cnt_M_lgc[36]       1         CTCFailedBuf_Cnt_M_lgc[37]       1         CTCFailedBuf_Cnt_M_lgc[38]       1         CTCFailedBuf_Cnt_M_lgc[39]       1         CTCFailedBuf_Cnt_M_lgc[40]       1         CTCFailedBuf_Cnt_M_lgc[41]       1         CTCFailedBuf_Cnt_M_lgc[42]       1         CTCFailedBuf_Cnt_M_lgc[43]       1         CTCFailedBuf_Cnt_M_lgc[44]       1         CTCFailedBuf_Cnt_M_lgc[45]       1         CTCFailedBuf_Cnt_M_lgc[46]       1         CTCFailedBuf_Cnt_M_lgc[47]       1         CTCFailedBuf_Cnt_M_lgc[48]       1		
CTCFailedBuf_Cnt_M_lgc[37]       1         CTCFailedBuf_Cnt_M_lgc[38]       1         CTCFailedBuf_Cnt_M_lgc[39]       1         CTCFailedBuf_Cnt_M_lgc[40]       1         CTCFailedBuf_Cnt_M_lgc[41]       1         CTCFailedBuf_Cnt_M_lgc[42]       1         CTCFailedBuf_Cnt_M_lgc[43]       1         CTCFailedBuf_Cnt_M_lgc[44]       1         CTCFailedBuf_Cnt_M_lgc[45]       1         CTCFailedBuf_Cnt_M_lgc[46]       1         CTCFailedBuf_Cnt_M_lgc[47]       1         CTCFailedBuf_Cnt_M_lgc[48]       1		
CTCFailedBuf_Cnt_M_lgc[38]       1         CTCFailedBuf_Cnt_M_lgc[39]       1         CTCFailedBuf_Cnt_M_lgc[40]       1         CTCFailedBuf_Cnt_M_lgc[41]       1         CTCFailedBuf_Cnt_M_lgc[42]       1         CTCFailedBuf_Cnt_M_lgc[43]       1         CTCFailedBuf_Cnt_M_lgc[44]       1         CTCFailedBuf_Cnt_M_lgc[45]       1         CTCFailedBuf_Cnt_M_lgc[46]       1         CTCFailedBuf_Cnt_M_lgc[47]       1         CTCFailedBuf_Cnt_M_lgc[48]       1		
CTCFailedBuf_Cnt_M_lgc[39]       1         CTCFailedBuf_Cnt_M_lgc[40]       1         CTCFailedBuf_Cnt_M_lgc[41]       1         CTCFailedBuf_Cnt_M_lgc[42]       1         CTCFailedBuf_Cnt_M_lgc[43]       1         CTCFailedBuf_Cnt_M_lgc[44]       1         CTCFailedBuf_Cnt_M_lgc[45]       1         CTCFailedBuf_Cnt_M_lgc[46]       1         CTCFailedBuf_Cnt_M_lgc[47]       1         CTCFailedBuf_Cnt_M_lgc[48]       1		
CTCFailedBuf_Cnt_M_lgc[40]       1         CTCFailedBuf_Cnt_M_lgc[41]       1         CTCFailedBuf_Cnt_M_lgc[42]       1         CTCFailedBuf_Cnt_M_lgc[43]       1         CTCFailedBuf_Cnt_M_lgc[44]       1         CTCFailedBuf_Cnt_M_lgc[45]       1         CTCFailedBuf_Cnt_M_lgc[46]       1         CTCFailedBuf_Cnt_M_lgc[47]       1         CTCFailedBuf_Cnt_M_lgc[48]       1		
CTCFailedBuf_Cnt_M_lgc[41]       1         CTCFailedBuf_Cnt_M_lgc[42]       1         CTCFailedBuf_Cnt_M_lgc[43]       1         CTCFailedBuf_Cnt_M_lgc[44]       1         CTCFailedBuf_Cnt_M_lgc[45]       1         CTCFailedBuf_Cnt_M_lgc[46]       1         CTCFailedBuf_Cnt_M_lgc[47]       1         CTCFailedBuf_Cnt_M_lgc[48]       1		
CTCFailedBuf_Cnt_M_lgc[42]       1         CTCFailedBuf_Cnt_M_lgc[43]       1         CTCFailedBuf_Cnt_M_lgc[44]       1         CTCFailedBuf_Cnt_M_lgc[45]       1         CTCFailedBuf_Cnt_M_lgc[46]       1         CTCFailedBuf_Cnt_M_lgc[47]       1         CTCFailedBuf_Cnt_M_lgc[48]       1		
CTCFailedBuf_Cnt_M_lgc[43]       1         CTCFailedBuf_Cnt_M_lgc[44]       1         CTCFailedBuf_Cnt_M_lgc[45]       1         CTCFailedBuf_Cnt_M_lgc[46]       1         CTCFailedBuf_Cnt_M_lgc[47]       1         CTCFailedBuf_Cnt_M_lgc[48]       1		
CTCFailedBuf_Cnt_M_lgc[44]       1         CTCFailedBuf_Cnt_M_lgc[45]       1         CTCFailedBuf_Cnt_M_lgc[46]       1         CTCFailedBuf_Cnt_M_lgc[47]       1         CTCFailedBuf_Cnt_M_lgc[48]       1		· · · · · · · · · · · · · · · · · · ·
CTCFailedBuf_Cnt_M_lgc[45]       1         CTCFailedBuf_Cnt_M_lgc[46]       1         CTCFailedBuf_Cnt_M_lgc[47]       1         CTCFailedBuf_Cnt_M_lgc[48]       1		
CTCFailedBuf_Cnt_M_lgc[46]       1         CTCFailedBuf_Cnt_M_lgc[47]       1         CTCFailedBuf_Cnt_M_lgc[48]       1		
CTCFailedBuf_Cnt_M_lgc[47]         1           CTCFailedBuf_Cnt_M_lgc[48]         1		
CTCFailedBuf_Cnt_M_lgc[48] 1		
OTOF-II-ID-II O-I M IIAO		
CTCFailedBuf_Cnt_M_lgc[49] 1	CTCFalledBut_Cnt_M_igc[49]	

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value CTCFailedBuf\_Cnt\_M\_lgc[50] CTCFailedBuf\_Cnt\_M\_lgc[51] CTCFailedBuf\_Cnt\_M\_lgc[52] CTCFailedBuf\_Cnt\_M\_lgc[53] CTCFailedBuf Cnt M lqc[54] CTCFailedBuf\_Cnt\_M\_lgc[55] CTCFailedBuf\_Cnt\_M\_lgc[56] 1 CTCFailedBuf\_Cnt\_M\_lgc[57] 1 CTCFailedBuf\_Cnt\_M\_lgc[58] CTCFailedBuf\_Cnt\_M\_lgc[59] 1 CTCFailedBuf\_Cnt\_M\_lgc[60] CTCFailedBuf\_Cnt\_M\_lgc[61] 1 CTCFailedBuf\_Cnt\_M\_lgc[62] CTCFailedBuf\_Cnt\_M\_lgc[63] 1 CTCFailedBuf\_Cnt\_M\_lgc[64] CTCFailedBuf\_Cnt\_M\_lgc[65] 1 CTCFailedBuf\_Cnt\_M\_lgc[66] CTCFailedBuf\_Cnt\_M\_lgc[67] 1 CTCFailedBuf\_Cnt\_M\_lgc[68] 1 CTCFailedBuf\_Cnt\_M\_lgc[69] 1 CTCFailedBuf\_Cnt\_M\_lgc[70] 1 CTCFailedBuf\_Cnt\_M\_lgc[71] 1 CTCFailedBuf\_Cnt\_M\_lgc[72] 1 CTCFailedBuf\_Cnt\_M\_lgc[73] 1 CTCFailedBuf\_Cnt\_M\_lgc[74] CTCFailedBuf\_Cnt\_M\_lgc[75] CTCFailedBuf\_Cnt\_M\_lgc[76] CTCFailed\_Cnt\_M\_lgc DTC 4294967295 **DTCKind** 2 DTCStatusNew 255 DTCStatusOld 255 Dem DTCNumberTable[0] 65535 Dem\_DTCNumberTable[1] 65535 Dem\_DTCNumberTable[2] 65535 Dem\_DTCNumberTable[3] 65535 Dem\_DTCNumberTable[4] 65535 Dem\_DTCNumberTable[5] 65535 Dem\_DTCNumberTable[6] 65535 Dem\_DTCNumberTable[7] 65535 Dem\_DTCNumberTable[8] 65535 65535 Dem\_DTCNumberTable[9] Dem\_DTCNumberTable[10] 65535 Dem\_DTCNumberTable[11] 65535 Dem\_DTCNumberTable[12] 65535 Dem\_DTCNumberTable[13] 65535 Dem DTCNumberTable[14] 65535 Dem\_DTCNumberTable[15] 65535 Dem DTCNumberTable[16] 65535 Dem\_DTCNumberTable[17] 65535 Dem\_DTCNumberTable[18] 65535 Dem\_DTCNumberTable[19] 65535 Dem\_DTCNumberTable[20] 65535 Dem\_DTCNumberTable[21] 65535 Dem\_DTCNumberTable[22] 65535 Dem\_DTCNumberTable[23] 65535 Dem\_DTCNumberTable[24] 65535 Dem\_DTCNumberTable[25] 65535 Dem\_DTCNumberTable[26] 65535 Dem\_DTCNumberTable[27] 65535 Dem\_DTCNumberTable[28] 65535 65535 Dem\_DTCNumberTable[29] Dem\_DTCNumberTable[30] 65535 Dem\_DTCNumberTable[31] 65535 Dem\_DTCNumberTable[32] 65535 Dem DTCNumberTable[33] 65535 Dem\_DTCNumberTable[34] 65535 Dem DTCNumberTable[35] 65535 Dem\_DTCNumberTable[36] 65535 Dem\_DTCNumberTable[37] 65535 Dem DTCNumberTable[38] 65535 Dem\_DTCNumberTable[39] 65535 Dem\_DTCNumberTable[40] 65535

Demlf\_DTCS

2018-04-10, 18:44:44+0530



Name Input Value Dem DTCNumberTable[41] 65535 Dem\_DTCNumberTable[42] 65535 65535 Dem DTCNumberTable[43] Dem\_DTCNumberTable[44] 65535 Dem\_DTCNumberTable[45] 65535 Dem\_DTCNumberTable[46] 65535 Dem\_DTCNumberTable[47] 65535 Dem\_DTCNumberTable[48] 65535 Dem\_DTCNumberTable[49] 65535 Dem DTCNumberTable[50] 65535 Dem\_DTCNumberTable[51] 65535 Dem\_DTCNumberTable[52] 65535 Dem\_DTCNumberTable[53] 65535 Dem DTCNumberTable[54] 65535 Dem\_DTCNumberTable[55] 65535 Dem\_DTCNumberTable[56] 65535 Dem\_DTCNumberTable[57] 65535 Dem\_DTCNumberTable[58] 65535 Dem\_DTCNumberTable[59] 65535 Dem\_DTCNumberTable[60] 65535 Dem\_DTCNumberTable[61] 65535 Dem\_DTCNumberTable[62] 65535 Dem\_DTCNumberTable[63] 65535 Dem\_DTCNumberTable[64] 65535 65535 Dem\_DTCNumberTable[65] Dem\_DTCNumberTable[66] 65535 Dem\_DTCNumberTable[67] 65535 Dem\_DTCNumberTable[68] 65535 Dem\_DTCNumberTable[69] 65535 Dem\_DTCNumberTable[70] 65535 Dem\_DTCNumberTable[71] 65535 Dem\_DTCNumberTable[72] 65535 Dem DTCNumberTable[73] 65535 Dem\_DTCNumberTable[74] 65535 Dem\_DTCNumberTable[75] 65535 Dem\_DTCNumberTable[76] 65535 Dem\_DTC\_FTB\_Table[0] 255 Dem\_DTC\_FTB\_Table[1] 255 Dem\_DTC\_FTB\_Table[2] 255 Dem DTC FTB Table[3] 255 Dem\_DTC\_FTB\_Table[4] 255 Dem DTC FTB Table[5] 255 Dem\_DTC\_FTB\_Table[6] 255 Dem\_DTC\_FTB\_Table[7] 255 Dem\_DTC\_FTB\_Table[8] 255 Dem\_DTC\_FTB\_Table[9] 255 255 Dem\_DTC\_FTB\_Table[10] Dem\_DTC\_FTB\_Table[11] 255 Dem\_DTC\_FTB\_Table[12] 255 Dem\_DTC\_FTB\_Table[13] 255 Dem DTC FTB Table[14] 255 Dem\_DTC\_FTB\_Table[15] 255 Dem\_DTC\_FTB\_Table[16] 255 Dem\_DTC\_FTB\_Table[17] 255 Dem\_DTC\_FTB\_Table[18] 255 Dem\_DTC\_FTB\_Table[19] 255 Dem\_DTC\_FTB\_Table[20] 255 Dem\_DTC\_FTB\_Table[21] 255 Dem\_DTC\_FTB\_Table[22] 255 Dem\_DTC\_FTB\_Table[23] 255 Dem\_DTC\_FTB\_Table[24] 255 Dem\_DTC\_FTB\_Table[25] 255 Dem\_DTC\_FTB\_Table[26] 255 Dem\_DTC\_FTB\_Table[27] 255 Dem\_DTC\_FTB\_Table[28] 255 Dem DTC FTB Table[29] 255 Dem\_DTC\_FTB\_Table[30] 255 Dem DTC FTB Table[31] 255 Dem\_DTC\_FTB\_Table[32] 255 Dem\_DTC\_FTB\_Table[33] 255 255 Dem\_DTC\_FTB\_Table[34] Dem\_DTC\_FTB\_Table[35] 255 Dem\_DTC\_FTB\_Table[36] 255

2018-04-10, 18:44:44+0530



Demlf\_DTCS Ch n e

Name	Input Value		
Dem_DTC_FTB_Table[37]	255		
Dem_DTC_FTB_Table[38]	255		
Dem_DTC_FTB_Table[39]	255		
Dem_DTC_FTB_Table[40] Dem_DTC_FTB_Table[41]	255 255		
Dem_DTC_FTB_Table[42]	255		
Dem_DTC_FTB_Table[43]	255		
Dem_DTC_FTB_Table[44]	255		
Dem_DTC_FTB_Table[45]	255		
Dem_DTC_FTB_Table[46]	255		
Dem_DTC_FTB_Table[47]	255		
Dem_DTC_FTB_Table[48]	255		
Dem_DTC_FTB_Table[49] Dem_DTC_FTB_Table[50]	255 255		
Dem_DTC_FTB_Table[50]	255		
Dem_DTC_FTB_Table[52]	255		
Dem_DTC_FTB_Table[53]	255		
Dem_DTC_FTB_Table[54]	255		
Dem_DTC_FTB_Table[55]	255		
Dem_DTC_FTB_Table[56]	255		
Dem_DTC_FTB_Table[57]	255		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59]	255 255		
Dem_DTC_FTB_Table[60]	255		
Dem_DTC_FTB_Table[61]	255		
Dem_DTC_FTB_Table[62]	255		
Dem_DTC_FTB_Table[63]	255		
Dem_DTC_FTB_Table[64]	255		
Dem_DTC_FTB_Table[65]	255		
Dem_DTC_FTB_Table[66]	255		
Dem_DTC_FTB_Table[67]	255 255		
Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69]	255		
Dem_DTC_FTB_Table[70]	255		
Dem_DTC_FTB_Table[71]	255		
Dem_DTC_FTB_Table[72]	255		
Dem_DTC_FTB_Table[73]	255		
Dem_DTC_FTB_Table[74]	055		
	255		
Dem_DTC_FTB_Table[75]	255		
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]	255 255	Formande al Value	Decul
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76] Name	255 255 Actual Value	Expected Value	Result
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]	255 255 Actual Value	1	~
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]	255 255 Actual Value	· ·	
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]	255 255 Actual Value 1	1	~
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]	255 255 <b>Actual Value</b> 1 1	1 1 1	· ·
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]	255 255  Actual Value  1 1 1 1 1 1	1 1 1 1 1 1	· ·
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]	255 255  Actual Value  1 1 1 1 1 1 1	1 1 1 1 1 1 1	•
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[6]	255 255  Actual Value  1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7]	255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1	•
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9]	255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10]	255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1	• • • • • • • • • • • • • • • • • • •
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9]	255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11]	255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[11]	255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15]	255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16]	255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17]	255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17]	255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19]	255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17]	255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20]	255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21]	255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24]	255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25]	255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[25]	255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27]	255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27]	255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29]	255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27]	255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	

Demlf\_DTCS

2018-04-10, 18:44:44+0530



**Actual Value Expected Value** Result CTCFailedBuf\_Cnt\_M\_lgc[32] CTCFailedBuf\_Cnt\_M\_lgc[33] CTCFailedBuf\_Cnt\_M\_lgc[34] CTCFailedBuf\_Cnt\_M\_lgc[35] CTCFailedBuf\_Cnt\_M\_lgc[36] CTCFailedBuf\_Cnt\_M\_lgc[37] CTCFailedBuf\_Cnt\_M\_lgc[38] 1 CTCFailedBuf\_Cnt\_M\_lgc[39] 1 CTCFailedBuf\_Cnt\_M\_lgc[40] CTCFailedBuf\_Cnt\_M\_lgc[41] CTCFailedBuf\_Cnt\_M\_lgc[42] CTCFailedBuf\_Cnt\_M\_lgc[43] 1 CTCFailedBuf\_Cnt\_M\_lgc[44] CTCFailedBuf\_Cnt\_M\_lgc[45] CTCFailedBuf\_Cnt\_M\_lgc[46] CTCFailedBuf\_Cnt\_M\_lgc[47] 1 CTCFailedBuf\_Cnt\_M\_lgc[48] CTCFailedBuf\_Cnt\_M\_lgc[49] 1 CTCFailedBuf\_Cnt\_M\_lgc[50] 1 CTCFailedBuf\_Cnt\_M\_lgc[51] **>** > > > 1 CTCFailedBuf\_Cnt\_M\_lgc[52] CTCFailedBuf\_Cnt\_M\_lgc[53] CTCFailedBuf\_Cnt\_M\_lgc[54] CTCFailedBuf\_Cnt\_M\_lgc[55] 1 CTCFailedBuf\_Cnt\_M\_lgc[56] CTCFailedBuf\_Cnt\_M\_lgc[57] CTCFailedBuf\_Cnt\_M\_lgc[58] CTCFailedBuf\_Cnt\_M\_lgc[59] CTCFailedBuf\_Cnt\_M\_lgc[60] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[61] CTCFailedBuf Cnt M Igc[62] CTCFailedBuf\_Cnt\_M\_lgc[63] 1 CTCFailedBuf Cnt M Igc[64] 1 ✓ ✓ CTCFailedBuf\_Cnt\_M\_lgc[65] CTCFailedBuf\_Cnt\_M\_lgc[66] CTCFailedBuf\_Cnt\_M\_lgc[67] • CTCFailedBuf\_Cnt\_M\_lgc[68] CTCFailedBuf\_Cnt\_M\_lgc[69] **~** CTCFailedBuf\_Cnt\_M\_lgc[70] CTCFailedBuf\_Cnt\_M\_lgc[71] 1 CTCFailedBuf\_Cnt\_M\_lgc[72] CTCFailedBuf\_Cnt\_M\_lgc[73] 1 CTCFailedBuf\_Cnt\_M\_lgc[74] CTCFailedBuf\_Cnt\_M\_lgc[75] CTCFailedBuf\_Cnt\_M\_lgc[76] 1 1

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte Write Ap Demlf CTCFailed Cnt lgc	1	Rte Write Ap Demlf CTCFailed Cnt lgc	1	_

1

n

1

n

Test Step 2.3 (Repeat Count = 1)	✓
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	0
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1

CTCFailed\_Cnt\_M\_lgc

Demlf DTCStatusChanged()

Rte\_Write\_Ap\_DemIf\_CTCFailed\_Cnt\_lgc(data)

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value CTCFailedBuf\_Cnt\_M\_lgc[15] 1 CTCFailedBuf\_Cnt\_M\_lgc[16] CTCFailedBuf\_Cnt\_M\_lgc[17] 1 CTCFailedBuf\_Cnt\_M\_lgc[18] CTCFailedBuf\_Cnt\_M\_lgc[19] 1 CTCFailedBuf\_Cnt\_M\_lgc[20] 0 CTCFailedBuf\_Cnt\_M\_lgc[21] 0 CTCFailedBuf\_Cnt\_M\_lgc[22] 0 CTCFailedBuf\_Cnt\_M\_lgc[23] 1 CTCFailedBuf\_Cnt\_M\_lgc[24] CTCFailedBuf\_Cnt\_M\_lgc[25] 0 CTCFailedBuf\_Cnt\_M\_lgc[26] 1 CTCFailedBuf\_Cnt\_M\_lgc[27] CTCFailedBuf\_Cnt\_M\_lgc[28] 1 CTCFailedBuf\_Cnt\_M\_lgc[29] 1 CTCFailedBuf\_Cnt\_M\_lgc[30] 1 CTCFailedBuf\_Cnt\_M\_lgc[31] 1 CTCFailedBuf\_Cnt\_M\_lgc[32] 1  $CTCFailedBuf\_Cnt\_M\_lgc[33]$ 1 CTCFailedBuf\_Cnt\_M\_lgc[34] 0 CTCFailedBuf\_Cnt\_M\_lgc[35] 0 CTCFailedBuf\_Cnt\_M\_lgc[36] 0 CTCFailedBuf\_Cnt\_M\_lgc[37] 0 CTCFailedBuf\_Cnt\_M\_lgc[38] 0 CTCFailedBuf\_Cnt\_M\_lgc[39] 0 CTCFailedBuf\_Cnt\_M\_lgc[40] 0 CTCFailedBuf\_Cnt\_M\_lgc[41] 0 CTCFailedBuf\_Cnt\_M\_lgc[42] 0 CTCFailedBuf\_Cnt\_M\_lgc[43] 0 CTCFailedBuf\_Cnt\_M\_lgc[44] 0 CTCFailedBuf Cnt M Igc[45] 0 CTCFailedBuf\_Cnt\_M\_lgc[46] n CTCFailedBuf Cnt M Igc[47] 0 CTCFailedBuf\_Cnt\_M\_lgc[48] 0 CTCFailedBuf\_Cnt\_M\_lgc[49] 0 CTCFailedBuf\_Cnt\_M\_lgc[50] 0 CTCFailedBuf\_Cnt\_M\_lgc[51] 0 CTCFailedBuf\_Cnt\_M\_lgc[52] 0 CTCFailedBuf\_Cnt\_M\_lgc[53] 1 CTCFailedBuf\_Cnt\_M\_lgc[54] 1 CTCFailedBuf\_Cnt\_M\_lgc[55] CTCFailedBuf Cnt M lqc[56] CTCFailedBuf\_Cnt\_M\_lgc[57] 1 CTCFailedBuf\_Cnt\_M\_lgc[58] 1 CTCFailedBuf\_Cnt\_M\_lgc[59] 1 CTCFailedBuf\_Cnt\_M\_lgc[60] CTCFailedBuf\_Cnt\_M\_lgc[61] 1 CTCFailedBuf\_Cnt\_M\_lgc[62] CTCFailedBuf\_Cnt\_M\_lgc[63] 0 CTCFailedBuf\_Cnt\_M\_lgc[64] CTCFailedBuf\_Cnt\_M\_lgc[65] 0 CTCFailedBuf\_Cnt\_M\_lgc[66] 0 CTCFailedBuf\_Cnt\_M\_lgc[67] 0 CTCFailedBuf\_Cnt\_M\_lgc[68] 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 CTCFailedBuf\_Cnt\_M\_lgc[73] 0 CTCFailedBuf\_Cnt\_M\_lgc[74] 0 CTCFailedBuf\_Cnt\_M\_lgc[75] 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0  $CTCFailed\_Cnt\_M\_lgc$ 0 DTC 0 **DTCKind** 1 DTCStatusNew 148 DTCStatusOld 39 Dem DTCNumberTable[0] 181 Dem\_DTCNumberTable[1] 1 Dem\_DTCNumberTable[2] 41 Dem\_DTCNumberTable[3] 22 Dem\_DTCNumberTable[4] 24 Dem\_DTCNumberTable[5] 254

Demlf\_DTCS

2018-04-10, 18:44:44+0530



Name Input Value Dem\_DTCNumberTable[6] 209 Dem\_DTCNumberTable[7] 209 Dem DTCNumberTable[8] 181 Dem\_DTCNumberTable[9] 1 Dem DTCNumberTable[10] 209 Dem\_DTCNumberTable[11] 128 Dem\_DTCNumberTable[12] 1 Dem\_DTCNumberTable[13] 209 Dem\_DTCNumberTable[14] 181 Dem\_DTCNumberTable[15] 1 Dem\_DTCNumberTable[16] Dem\_DTCNumberTable[17] 209 Dem\_DTCNumberTable[18] 33 Dem\_DTCNumberTable[19] 181 Dem\_DTCNumberTable[20] Dem\_DTCNumberTable[21] 209 Dem\_DTCNumberTable[22] 181 Dem\_DTCNumberTable[23] 41 Dem\_DTCNumberTable[24] 22 Dem\_DTCNumberTable[25] 24 Dem\_DTCNumberTable[26] 254 Dem\_DTCNumberTable[27] 1 Dem\_DTCNumberTable[28] 181 Dem\_DTCNumberTable[29] Dem\_DTCNumberTable[30] 181 Dem\_DTCNumberTable[31] 181 Dem DTCNumberTable[32] 1 Dem\_DTCNumberTable[33] Dem DTCNumberTable[34] 181 Dem\_DTCNumberTable[35] Dem DTCNumberTable[36] 181 Dem\_DTCNumberTable[37] 181 Dem DTCNumberTable[38] 181 Dem\_DTCNumberTable[39] 1 Dem\_DTCNumberTable[40] Dem\_DTCNumberTable[41] 41 Dem\_DTCNumberTable[42] 22 24 Dem\_DTCNumberTable[43] Dem\_DTCNumberTable[44] 254 Dem\_DTCNumberTable[45] 209 Dem\_DTCNumberTable[46] 181 Dem\_DTCNumberTable[47] 1 Dem\_DTCNumberTable[48] 22 Dem\_DTCNumberTable[49] 181 Dem\_DTCNumberTable[50] Dem\_DTCNumberTable[51] 181 Dem DTCNumberTable[52] 181 Dem\_DTCNumberTable[53] 1 Dem DTCNumberTable[54] 22 Dem\_DTCNumberTable[55] 209 Dem\_DTCNumberTable[56] 181 Dem\_DTCNumberTable[57] Dem\_DTCNumberTable[58] 181 Dem\_DTCNumberTable[59] 209 Dem\_DTCNumberTable[60] 181 Dem\_DTCNumberTable[61] 1 Dem\_DTCNumberTable[62] 22 41 Dem\_DTCNumberTable[63] Dem\_DTCNumberTable[64] 22 24 Dem\_DTCNumberTable[65] Dem\_DTCNumberTable[66] 254 181 Dem\_DTCNumberTable[67] Dem\_DTCNumberTable[68] 181 Dem\_DTCNumberTable[69] 1 Dem\_DTCNumberTable[70] 22 Dem\_DTCNumberTable[71] 209 Dem\_DTCNumberTable[72] 22 Dem DTCNumberTable[73] 41 Dem\_DTCNumberTable[74] 22 Dem\_DTCNumberTable[75] 24 Dem\_DTCNumberTable[76] 254 Dem\_DTC\_FTB\_Table[0] 245 Dem\_DTC\_FTB\_Table[1] 151

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Name Input Value Dem\_DTC\_FTB\_Table[2] 199 Dem\_DTC\_FTB\_Table[3] 160 Dem\_DTC\_FTB\_Table[4] 30 Dem\_DTC\_FTB\_Table[5] 136 Dem\_DTC\_FTB\_Table[6] 178 Dem\_DTC\_FTB\_Table[7] 178 Dem\_DTC\_FTB\_Table[8] 245 Dem\_DTC\_FTB\_Table[9] 151 Dem\_DTC\_FTB\_Table[10] 178 Dem\_DTC\_FTB\_Table[11] 31 Dem\_DTC\_FTB\_Table[12] 151 Dem\_DTC\_FTB\_Table[13] 178 Dem\_DTC\_FTB\_Table[14] 245 Dem DTC FTB Table[15] 151 Dem\_DTC\_FTB\_Table[16] 151 Dem\_DTC\_FTB\_Table[17] 178 Dem\_DTC\_FTB\_Table[18] 234 Dem\_DTC\_FTB\_Table[19] 245 Dem\_DTC\_FTB\_Table[20] 151 Dem\_DTC\_FTB\_Table[21] 178 Dem\_DTC\_FTB\_Table[22] 245 Dem\_DTC\_FTB\_Table[23] 199 Dem\_DTC\_FTB\_Table[24] 160 Dem\_DTC\_FTB\_Table[25] 30 Dem\_DTC\_FTB\_Table[26] 136 Dem\_DTC\_FTB\_Table[27] 151 Dem\_DTC\_FTB\_Table[28] 245 Dem\_DTC\_FTB\_Table[29] 151 Dem\_DTC\_FTB\_Table[30] 245 Dem\_DTC\_FTB\_Table[31] 245 Dem DTC FTB Table[32] 151 Dem\_DTC\_FTB\_Table[33] 151 Dem DTC FTB Table[34] 245 Dem\_DTC\_FTB\_Table[35] 151 Dem\_DTC\_FTB\_Table[36] 245 Dem DTC FTB Table[37] 245 Dem\_DTC\_FTB\_Table[38] 245 Dem\_DTC\_FTB\_Table[39] 151 Dem\_DTC\_FTB\_Table[40] 151 Dem DTC\_FTB\_Table[41] 199 Dem\_DTC\_FTB\_Table[42] 160 Dem DTC FTB Table[43] 30 Dem\_DTC\_FTB\_Table[44] 136 Dem\_DTC\_FTB\_Table[45] 178 245 Dem\_DTC\_FTB\_Table[46] Dem\_DTC\_FTB\_Table[47] 151 Dem\_DTC\_FTB\_Table[48] 160 Dem\_DTC\_FTB\_Table[49] 245 151 Dem\_DTC\_FTB\_Table[50] Dem\_DTC\_FTB\_Table[51] 245 Dem DTC FTB Table[52] 245 Dem\_DTC\_FTB\_Table[53] 151 Dem\_DTC\_FTB\_Table[54] 160 Dem\_DTC\_FTB\_Table[55] 178 Dem\_DTC\_FTB\_Table[56] 245 Dem\_DTC\_FTB\_Table[57] 151 Dem\_DTC\_FTB\_Table[58] 245 Dem\_DTC\_FTB\_Table[59] 178 Dem\_DTC\_FTB\_Table[60] 245 Dem\_DTC\_FTB\_Table[61] 151 Dem\_DTC\_FTB\_Table[62] 160 Dem DTC FTB Table[63] 199 Dem\_DTC\_FTB\_Table[64] 160 Dem\_DTC\_FTB\_Table[65] 30 Dem\_DTC\_FTB\_Table[66] 136 Dem DTC FTB Table[67] 245 Dem\_DTC\_FTB\_Table[68] 245 Dem DTC FTB Table[69] 151 Dem\_DTC\_FTB\_Table[70] 160 Dem\_DTC\_FTB\_Table[71] 178 Dem\_DTC\_FTB\_Table[72] 160 Dem\_DTC\_FTB\_Table[73] 199 Dem\_DTC\_FTB\_Table[74] 160

2018-04-10, 18:44:44+0530



Den 1016-FIR   Indextry   105	Name	Input Value		
Actual Value	Dem_DTC_FTB_Table[75]	•		
CICCINSIGNOU, CVM, Might)  I CICCINCIAN, CVM, Mi	Dem_DTC_FTB_Table[76]	136		
GCFSeinSelf, CM, M, S251  CCFSeinSelf, CM, M, S250  CCFSeinSelf, CM, M		Actual Value	Expected Value	Result
CICC-assedud: Cent M, 19020  CICC-assedud: Cent M, 19030  CICC-assedud: Ce	CTCFailedBuf_Cnt_M_Igc[0]			~
CITCHARDED, CAM, Jug Sept				
CICTORANDEL CH. M. 1954  CICTORANDEL CH. M. 1958  CICTORANDEL CH. M. 1951  CICTORANDEL CH. M. 1952  CICTORANDEL CH. M. 1953  CICTORANDEL CH. M. 19				_
CITCHARDER COLUMN   1989    1				
CICCID-ISSUED_COL_N_BERT				
CICS-anderial_Col_M_get s				-
CITCHaeldud, Cell, M, 1989  1				~
CTCFaiebdu Cot M   2010   1		1	1	~
CICTAPACED_CER_M_STEP1   CICTAPACED_CER_M_STEP2   CICTAPACED_CER_M_STEP3   CICTAPACED_CER_M_ST	CTCFailedBuf_Cnt_M_lgc[9]	1	1	~
CTCFascedud_Cot_M_det3	CTCFailedBuf_Cnt_M_Igc[10]			~
CICFairabelly Crit Muget 3				
CICFarededuct Cort M, port4				
CICFaneSettor, COLM, Judg10				
CTCFalesMart_CM_M_Set70   1				
CITC-instellation (C. M., beg17)				
CTCFaleStat Crt M, bpt18				•
CITCFaledbuf, Cm, M, Igo(2) CTCFaledbuf, Cm, M, Igo(3) CTCFaledbuf, Cm, M, Igo(4) CTCFaledbuf, Cm, M,				
SCTCFaledBuff_CRM_bg427   0		1	1	~
CTCFaledut_CTM_1g223 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	CTCFailedBuf_Cnt_M_lgc[20]			
CTCFalledut_CM_Migc23	CTCFailedBuf_Cnt_M_lgc[21]	0	0	~
CTCFaiedbut_Crd_M_logi25				
CTCFaledbuf_Cn_M_lgct26				
CTCFaledBut Cnt, M.   sqct2n    1				
CTCFaledBut Cmt M lgct27    1				
CTCFaledBut_Cnt_M_gd28				
CTCFaledBuf_Cnt_M_igq29				
CTCFaledBuf_Cnt_M_lgd30				~
CTCFaledBuf_Cnt_M_lgd31				
CTCFaiedBuf_Cnt_M_gq32] 1 1 1 1 CTCFaiedBuf_Cnt_M_gq33] 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		1	1	~
CTCFaledBuf_Cnt_M_lgct34  CTCFaledBuf_Cnt_M_lgct36  CTCFaledBuf_Cnt_M_lgct36  CTCFaledBuf_Cnt_M_lgct37  CTCFaledBuf_Cnt_M_lgct38  CTCFaledBuf_Cnt_M_lgct38  CTCFaledBuf_Cnt_M_lgct38  CTCFaledBuf_Cnt_M_lgct38  CTCFaledBuf_Cnt_M_lgct40  CTCFaledBuf_Cnt_M_lgct40  CTCFaledBuf_Cnt_M_lgct41  CTCFaledBuf_Cnt_M_lgct41  CTCFaledBuf_Cnt_M_lgct41  CTCFaledBuf_Cnt_M_lgct42  O		1	1	~
CTCFailedBuf_Crit_M_igc 35		1		~
CTCFailedBuf_Cnt_M_lgc[36] CTGFailedBuf_Cnt_M_lgc[37] 0 0 0 0 0 CTGFailedBuf_Cnt_M_lgc[38] 0 0 0 0 CTGFailedBuf_Cnt_M_lgc[40] 0 0 0 CTGFailedBuf_Cnt_M_lgc[40] 0 0 0 0 CTGFailedBuf_Cnt_M_lgc[41] 0 0 0 CTGFailedBuf_Cnt_M_lgc[51] 0 0 0 CTGFailedBuf_Cnt_M_lgc[52] 0 0 0 CTGFailedBuf_Cnt_M_lgc[52] 0 0 0 CTGFailedBuf_Cnt_M_lgc[52] 0 0 0 CTGFailedBuf_Cnt_M_lgc[53] 1 1 1 CTGFailedBuf_Cnt_M_lgc[53] 1 1 1 CTGFailedBuf_Cnt_M_lgc[54] 1 1 1 CTGFailedBuf_Cnt_M_lgc[54] 1 1 1 CTGFailedBuf_Cnt_M_lgc[56] 1 1 1 CTGFailedBuf_Cnt_M_lgc[66] 1 1 1 1 1 CTGFailedBuf_Cnt_M_lgc[66] 1 1 1 1 1 CTGFailedBuf_Cnt_M_lgc[66] 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1				-
CTCFailedBuf_Cnt_M_lgc[37]  O O O O CTCFailedBuf_Cnt_M_lgc[39]  O O O O O CTCFailedBuf_Cnt_M_lgc[40]  O O O O O CTCFailedBuf_Cnt_M_lgc[40]  O O O O O O CTCFailedBuf_Cnt_M_lgc[41]  O O O O O O O CTCFailedBuf_Cnt_M_lgc[42]  O O O O O O O O O O O O O O O O O O O				
CTCFailedBuf_Cnt_M_lgc[38] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[39] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[40] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[41] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[41] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[42] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[43] 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[43] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[44] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[44] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[46] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[46] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[47] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[47] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[48] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[49] 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[49] 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[50] 1 1 1 0 CTCFailedBuf_Cnt_M_lgc[60] 1 1 0 CTCFaile				
CTCFailedBuf_Cnt_M_lgc[43]  CTCFailedBuf_Cnt_M_lgc[41]  O  O  CTCFailedBuf_Cnt_M_lgc[41]  O  O  CTCFailedBuf_Cnt_M_lgc[42]  O  O  CTCFailedBuf_Cnt_M_lgc[42]  O  O  O  CTCFailedBuf_Cnt_M_lgc[43]  O  O  CTCFailedBuf_Cnt_M_lgc[44]  O  O  CTCFailedBuf_Cnt_M_lgc[44]  O  O  CTCFailedBuf_Cnt_M_lgc[45]  O  O  CTCFailedBuf_Cnt_M_lgc[45]  O  O  CTCFailedBuf_Cnt_M_lgc[47]  O  O  CTCFailedBuf_Cnt_M_lgc[47]  O  CTCFailedBuf_Cnt_M_lgc[48]  O  O  CTCFailedBuf_Cnt_M_lgc[48]  O  O  CTCFailedBuf_Cnt_M_lgc[50]  O  CTCFailedBuf_Cnt_M_lgc[50]  O  CTCFailedBuf_Cnt_M_lgc[50]  O  CTCFailedBuf_Cnt_M_lgc[50]  CTCFailedBuf_Cnt_M_lgc[53]  TCTCFailedBuf_Cnt_M_lgc[53]  TCTCFailedBuf_Cnt_M_lgc[53]  TCTCFailedBuf_Cnt_M_lgc[56]  TCTCFailedBuf_Cnt_M_lgc[66]  TCTCFailedBuf_Cnt_M_lgc[67]  TCTCFa				
CTCFailedBut_Cnt_M_lgc[41]  CTCFailedBut_Cnt_M_lgc[42]  CTCFailedBut_Cnt_M_lgc[43]  CTCFailedBut_Cnt_M_lgc[43]  CTCFailedBut_Cnt_M_lgc[43]  CTCFailedBut_Cnt_M_lgc[43]  CTCFailedBut_Cnt_M_lgc[45]  CTCFailedBut_Cnt_M_lgc[45]  CTCFailedBut_Cnt_M_lgc[45]  CTCFailedBut_Cnt_M_lgc[46]  CTCFailedBut_Cnt_M_lgc[46]  CTCFailedBut_Cnt_M_lgc[47]  CTCFailedBut_Cnt_M_lgc[48]  CTCFailedBut_Cnt_M_lgc[48]  CTCFailedBut_Cnt_M_lgc[48]  CTCFailedBut_Cnt_M_lgc[48]  CTCFailedBut_Cnt_M_lgc[49]  CTCFailedBut_Cnt_M_lgc[51]  CTCFailedBut_Cnt_M_lgc[51]  CTCFailedBut_Cnt_M_lgc[52]  CTCFailedBut_Cnt_M_lgc[52]  CTCFailedBut_Cnt_M_lgc[53]  TTCFailedBut_Cnt_M_lgc[54]  CTCFailedBut_Cnt_M_lgc[54]  CTCFailedBut_Cnt_M_lgc[56]  TCCFailedBut_Cnt_M_lgc[56]  TCCFailedBut_Cnt_M_lgc[56]  TCCFailedBut_Cnt_M_lgc[56]  TCCFailedBut_Cnt_M_lgc[56]  TCCFailedBut_Cnt_M_lgc[56]  TCCFailedBut_Cnt_M_lgc[58]  TCCFailedBut_Cnt_M_lgc[68]				
CTCFailedBut_Cnt_M_lgc(42)				
CTCFailedBuf_Cnt_M_lgc(42)         0         0           CTCFailedBuf_Cnt_M_lgc(44)         0         0           CTCFailedBuf_Cnt_M_lgc(44)         0         0           CTCFailedBuf_Cnt_M_lgc(45)         0         0           CTCFailedBuf_Cnt_M_lgc(47)         0         0           CTCFailedBuf_Cnt_M_lgc(48)         0         0           CTCFailedBuf_Cnt_M_lgc(50)         0         0           CTCFailedBuf_Cnt_M_lgc(50)         0         0           CTCFailedBuf_Cnt_M_lgc(51)         0         0           CTCFailedBuf_Cnt_M_lgc(52)         0         0           CTCFailedBuf_Cnt_M_lgc(52)         0         0           CTCFailedBuf_Cnt_M_lgc(53)         1         1           CTCFailedBuf_Cnt_M_lgc(54)         1         1           CTCFailedBuf_Cnt_M_lgc(55)         1         1           CTCFailedBuf_Cnt_M_lgc(55)         1         1           CTCFailedBuf_Cnt_M_lgc(57)         1         1           CTCFailedBuf_Cnt_M_lgc(58)         1         1           CTCFailedBuf_Cnt_M_lgc(60)         1         1           CTCFailedBuf_Cnt_M_lgc(60)         1         1           CTCFailedBuf_Cnt_M_lgc(68)         0         0           CTC				•
CTCFailedBuf_Cnt_M_lgc[44]  CTCFailedBuf_Cnt_M_lgc[45]  CTCFailedBuf_Cnt_M_lgc[47]  CTCFailedBuf_Cnt_M_lgc[47]  CTCFailedBuf_Cnt_M_lgc[48]  CTCFailedBuf_Cnt_M_lgc[48]  CTCFailedBuf_Cnt_M_lgc[48]  CTCFailedBuf_Cnt_M_lgc[48]  CTCFailedBuf_Cnt_M_lgc[49]  CTCFailedBuf_Cnt_M_lgc[50]  CTCFailedBuf_Cnt_M_lgc[51]  CTCFailedBuf_Cnt_M_lgc[52]  CTCFailedBuf_Cnt_M_lgc[52]  CTCFailedBuf_Cnt_M_lgc[52]  CTCFailedBuf_Cnt_M_lgc[53]  CTCFailedBuf_Cnt_M_lgc[54]  CTCFailedBuf_Cnt_M_lgc[55]  CTCFailedBuf_Cnt_M_lgc[56]  CTCFailedBuf_Cnt_M_lgc[56]  CTCFailedBuf_Cnt_M_lgc[58]  CTCFailedBuf_Cnt_M_lgc[58]  CTCFailedBuf_Cnt_M_lgc[58]  CTCFailedBuf_Cnt_M_lgc[58]  CTCFailedBuf_Cnt_M_lgc[58]  CTCFailedBuf_Cnt_M_lgc[60]  CTCFailedBuf_Cnt_M_lgc[60]  CTCFailedBuf_Cnt_M_lgc[61]  CTCFailedBuf_Cnt_M_lgc[62]  CTCFailedBuf_Cnt_M_lgc[63]  CTCFailedBuf_Cnt_M_lgc[63]  CTCFailedBuf_Cnt_M_lgc[64]  CTCFailedBuf_Cnt_M_lgc[66]  CTCFailedBuf_Cnt_M_lgc[67]  O  CTCFailedBuf_Cnt_M_lgc[68]  O  CTCFailedBuf_Cnt_M_lgc[68]				~
CTCFailedBuf_Cnt_M_lgc[45]         0 </td <td>CTCFailedBuf_Cnt_M_lgc[43]</td> <td>0</td> <td>0</td> <td>~</td>	CTCFailedBuf_Cnt_M_lgc[43]	0	0	~
CTCFailedBuf_Cnt_M_lgc[46]         0         0           CTCFailedBuf_Cnt_M_lgc[47]         0         0           CTCFailedBuf_Cnt_M_lgc[48]         0         0           CTCFailedBuf_Cnt_M_lgc[49]         0         0           CTCFailedBuf_Cnt_M_lgc[50]         0         0           CTCFailedBuf_Cnt_M_lgc[51]         0         0           CTCFailedBuf_Cnt_M_lgc[52]         0         0           CTCFailedBuf_Cnt_M_lgc[53]         1         1           CTCFailedBuf_Cnt_M_lgc[56]         1         1           CTCFailedBuf_Cnt_M_lgc[56]         1         1           CTCFailedBuf_Cnt_M_lgc[60]         1         1           CTCFailedBuf_Cnt_M_lgc[61]         1         1           CTCFailedBuf_Cnt_M_lgc[63]         0         0           CTCFailedBuf_Cnt_M_lgc[63]         0         0           CTCFailedBuf_Cnt_M_lgc[66]         0         0           CTC	CTCFailedBuf_Cnt_M_lgc[44]	0		_
CTCFailedBuf_Cnt_M_lgc[48]       0       0         CTCFailedBuf_Cnt_M_lgc[49]       0       0         CTCFailedBuf_Cnt_M_lgc[50]       0       0         CTCFailedBuf_Cnt_M_lgc[50]       0       0         CTCFailedBuf_Cnt_M_lgc[52]       0       0         CTCFailedBuf_Cnt_M_lgc[53]       1       1         CTCFailedBuf_Cnt_M_lgc[53]       1       1         CTCFailedBuf_Cnt_M_lgc[55]       1       1         CTCFailedBuf_Cnt_M_lgc[55]       1       1         CTCFailedBuf_Cnt_M_lgc[56]       1       1         CTCFailedBuf_Cnt_M_lgc[57]       1       1         CTCFailedBuf_Cnt_M_lgc[58]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       0       0         CTCFailedBuf_Cnt_M_lgc[65]       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0         CTCFailedBuf_Cnt_M_l	CTCFailedBuf_Cnt_M_lgc[45]			~
CTCFailedBuf_Cnt_M_lgc[48]       0       0         CTCFailedBuf_Cnt_M_lgc[50]       0       0         CTCFailedBuf_Cnt_M_lgc[51]       0       0         CTCFailedBuf_Cnt_M_lgc[52]       0       0         CTCFailedBuf_Cnt_M_lgc[53]       1       1         CTCFailedBuf_Cnt_M_lgc[54]       1       1         CTCFailedBuf_Cnt_M_lgc[55]       1       1         CTCFailedBuf_Cnt_M_lgc[56]       1       1         CTCFailedBuf_Cnt_M_lgc[57]       1       1         CTCFailedBuf_Cnt_M_lgc[58]       1       1         CTCFailedBuf_Cnt_M_lgc[59]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       0       0         CTCFailedBuf_Cnt_M_lgc[63]       0       0         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0         CTCFailedBuf_Cnt_M_l				
CTCFailedBuf_Cnt_M_lgc[49]       0       0         CTCFailedBuf_Cnt_M_lgc[50]       0       0         CTCFailedBuf_Cnt_M_lgc[51]       0       0         CTCFailedBuf_Cnt_M_lgc[52]       0       0         CTCFailedBuf_Cnt_M_lgc[53]       1       1         CTCFailedBuf_Cnt_M_lgc[53]       1       1         CTCFailedBuf_Cnt_M_lgc[55]       1       1         CTCFailedBuf_Cnt_M_lgc[56]       1       1         CTCFailedBuf_Cnt_M_lgc[57]       1       1         CTCFailedBuf_Cnt_M_lgc[58]       1       1         CTCFailedBuf_Cnt_M_lgc[59]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       0       0         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       0       0         CTCFailedBuf_Cnt_M_lgc[65]       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0         CTCFailedBuf_Cnt_M_l				
CTCFailedBuf_Cnt_M_lgc[51]       0       0         CTCFailedBuf_Cnt_M_lgc[52]       0       0         CTCFailedBuf_Cnt_M_lgc[53]       1       1         CTCFailedBuf_Cnt_M_lgc[53]       1       1         CTCFailedBuf_Cnt_M_lgc[54]       1       1         CTCFailedBuf_Cnt_M_lgc[55]       1       1         CTCFailedBuf_Cnt_M_lgc[56]       1       1         CTCFailedBuf_Cnt_M_lgc[57]       1       1         CTCFailedBuf_Cnt_M_lgc[58]       1       1         CTCFailedBuf_Cnt_M_lgc[59]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       0       0         CTCFailedBuf_Cnt_M_lgc[63]       0       0         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0         CTCFailedBuf_Cnt_M_l				
CTCFailedBuf_Cnt_M_lgc[51]       0       0         CTCFailedBuf_Cnt_M_lgc[52]       0       0         CTCFailedBuf_Cnt_M_lgc[53]       1       1         CTCFailedBuf_Cnt_M_lgc[54]       1       1         CTCFailedBuf_Cnt_M_lgc[55]       1       1         CTCFailedBuf_Cnt_M_lgc[56]       1       1         CTCFailedBuf_Cnt_M_lgc[57]       1       1         CTCFailedBuf_Cnt_M_lgc[58]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       0       0         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0         CTCFailedBuf_Cnt_M_lgc[68]       0       0          CTCFailedBu				
CTCFailedBuf_Cnt_M_lgc[52] 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[53] 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1				
CTCFailedBuf_Cnt_M_lgc[53]       1       1         CTCFailedBuf_Cnt_M_lgc[54]       1       1         CTCFailedBuf_Cnt_M_lgc[55]       1       1         CTCFailedBuf_Cnt_M_lgc[56]       1       1         CTCFailedBuf_Cnt_M_lgc[57]       1       1         CTCFailedBuf_Cnt_M_lgc[58]       1       1         CTCFailedBuf_Cnt_M_lgc[59]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       0       0         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0         CTCFailedBuf_Cnt_M_lgc[68]       0       0				
CTCFailedBuf_Cnt_M_lgc[54]       1       1         CTCFailedBuf_Cnt_M_lgc[55]       1       1         CTCFailedBuf_Cnt_M_lgc[56]       1       1         CTCFailedBuf_Cnt_M_lgc[57]       1       1         CTCFailedBuf_Cnt_M_lgc[58]       1       1         CTCFailedBuf_Cnt_M_lgc[59]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       0       0         CTCFailedBuf_Cnt_M_lgc[63]       0       0         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0         CTCFailedBuf_Cnt_M_lgc[68]       0       0				<b>~</b>
CTCFailedBuf_Cnt_M_lgc[56]       1       1         CTCFailedBuf_Cnt_M_lgc[57]       1       1         CTCFailedBuf_Cnt_M_lgc[58]       1       1         CTCFailedBuf_Cnt_M_lgc[59]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       0       0         CTCFailedBuf_Cnt_M_lgc[63]       0       0         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0         CTCFailedBuf_Cnt_M_lgc[68]       0       0		1	1	~
CTCFailedBuf_Cnt_M_lgc[57]       1       1         CTCFailedBuf_Cnt_M_lgc[58]       1       1         CTCFailedBuf_Cnt_M_lgc[59]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       0       0         CTCFailedBuf_Cnt_M_lgc[63]       0       0         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0         CTCFailedBuf_Cnt_M_lgc[68]       0       0	CTCFailedBuf_Cnt_M_lgc[55]	1	1	~
CTCFailedBuf_Cnt_M_lgc[58]       1       1         CTCFailedBuf_Cnt_M_lgc[59]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       0       0         CTCFailedBuf_Cnt_M_lgc[63]       0       0         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0         CTCFailedBuf_Cnt_M_lgc[68]       0       0	CTCFailedBuf_Cnt_M_lgc[56]	1	1	~
CTCFailedBuf_Cnt_M_lgc[59]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       0       0         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0         CTCFailedBuf_Cnt_M_lgc[68]       0       0				~
CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       0       0         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0         CTCFailedBuf_Cnt_M_lgc[68]       0       0				
CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       0       0         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0         CTCFailedBuf_Cnt_M_lgc[68]       0       0				
CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       0       0         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0         CTCFailedBuf_Cnt_M_lgc[68]       0       0				
CTCFailedBuf_Cnt_M_lgc[63]       0       0         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0         CTCFailedBuf_Cnt_M_lgc[68]       0       0				
CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0         CTCFailedBuf_Cnt_M_lgc[68]       0       0				~
CTCFailedBuf_Cnt_M_lgc[65]         0         0           CTCFailedBuf_Cnt_M_lgc[66]         0         0           CTCFailedBuf_Cnt_M_lgc[67]         0         0           CTCFailedBuf_Cnt_M_lgc[68]         0         0				
CTCFailedBuf_Cnt_M_lgc[66]         0         0           CTCFailedBuf_Cnt_M_lgc[67]         0         0           CTCFailedBuf_Cnt_M_lgc[68]         0         0				•
CTCFailedBuf_Cnt_M_[gc[68] 0 0		0	0	
		0	0	~
CTCFailedBuf_Cnt_M_lgc[69] 0 0				~
	CTCFailedBuf_Cnt_M_lgc[69]	0	0	~

DemIf\_DTCS



Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[70]	0	0	~
CTCFailedBuf_Cnt_M_lgc[71]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[72]	0	0	~
CTCFailedBuf_Cnt_M_lgc[73]	0	0	~
CTCFailedBuf_Cnt_M_lgc[74]	0	0	~
CTCFailedBuf_Cnt_M_lgc[75]	0	0	~
CTCFailedBuf_Cnt_M_lgc[76]	0	0	~
CTCFailed_Cnt_M_lgc	0	0	~
Demlf_DTCStatusChanged()	0	0	~
Rte Write An Demlf CTCFailed Cnt lgc(data)	0	0	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	~

Test Step 2.4 (Repeat Count = 1)	
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf Cnt M lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1.
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf Cnt M Igc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf Cnt M Igc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
TCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	0
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
TCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
TCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf Cnt M Igc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
TCFailedBuf_Cnt_M_lgc[41]	0
TCFalledBut_Crit_ivi_igc[41] TCFalledBuf_Crit_M_lgc[42]	0
TCFalledBuf_Cnt_M_lgc[42]	0
TCFalledBuf_Cnt_M_lgc[43]	0
TCFalledBuf_Cnt_M_lgc[44]	0
TCFalledBut_Cnt_M_lgc[45]	0
TCFailedBuf_Crit_M_igc[46]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFalledBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value CTCFailedBuf\_Cnt\_M\_lgc[53] 1 CTCFailedBuf\_Cnt\_M\_lgc[54] CTCFailedBuf\_Cnt\_M\_lgc[55] 1 CTCFailedBuf\_Cnt\_M\_lgc[56] CTCFailedBuf\_Cnt\_M\_lgc[57] 1 CTCFailedBuf\_Cnt\_M\_lgc[58] CTCFailedBuf\_Cnt\_M\_lgc[59] 1 CTCFailedBuf\_Cnt\_M\_lgc[60] 1 CTCFailedBuf\_Cnt\_M\_lgc[61] 1 CTCFailedBuf\_Cnt\_M\_lgc[62] CTCFailedBuf\_Cnt\_M\_lgc[63] 1 CTCFailedBuf\_Cnt\_M\_lgc[64] 1 CTCFailedBuf\_Cnt\_M\_lgc[65] 0 CTCFailedBuf\_Cnt\_M\_lgc[66] n CTCFailedBuf\_Cnt\_M\_lgc[67] 0 CTCFailedBuf\_Cnt\_M\_lgc[68] 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 CTCFailedBuf\_Cnt\_M\_lgc[73] 1 CTCFailedBuf\_Cnt\_M\_lgc[74] 0 CTCFailedBuf\_Cnt\_M\_lgc[75] 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 CTCFailed\_Cnt\_M\_lgc 1 DTC 4294967295 DTCKind 2 DTCStatusNew 126 DTCStatusOld 203 Dem\_DTCNumberTable[0] 182 Dem\_DTCNumberTable[1] 221 Dem\_DTCNumberTable[2] 159 Dem DTCNumberTable[3] 164 Dem DTCNumberTable[4] 34 Dem\_DTCNumberTable[5] 166 Dem DTCNumberTable[6] 237 Dem\_DTCNumberTable[7] 237 Dem\_DTCNumberTable[8] 182 Dem\_DTCNumberTable[9] 221 Dem DTCNumberTable[10] 237 Dem\_DTCNumberTable[11] 123 Dem DTCNumberTable[12] 221 Dem\_DTCNumberTable[13] 237 Dem\_DTCNumberTable[14] 182 221 Dem\_DTCNumberTable[15] Dem\_DTCNumberTable[16] 221 237 Dem\_DTCNumberTable[17] Dem\_DTCNumberTable[18] 239 Dem\_DTCNumberTable[19] 182 Dem\_DTCNumberTable[20] 221 Dem\_DTCNumberTable[21] 237 Dem\_DTCNumberTable[22] 182 Dem\_DTCNumberTable[23] 159 Dem\_DTCNumberTable[24] 164 Dem\_DTCNumberTable[25] 34 Dem\_DTCNumberTable[26] 166 Dem\_DTCNumberTable[27] 221 Dem\_DTCNumberTable[28] 182 Dem\_DTCNumberTable[29] 221 Dem\_DTCNumberTable[30] 182 Dem\_DTCNumberTable[31] 182 Dem DTCNumberTable[32] 221 Dem\_DTCNumberTable[33] 221 Dem DTCNumberTable[34] 182 Dem\_DTCNumberTable[35] 221 Dem DTCNumberTable[36] 182 Dem\_DTCNumberTable[37] 182 Dem DTCNumberTable[38] 182 Dem\_DTCNumberTable[39] 221 Dem\_DTCNumberTable[40] 221 Dem\_DTCNumberTable[41] 159 Dem\_DTCNumberTable[42] 164 Dem\_DTCNumberTable[43] 34

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Name Input Value Dem\_DTCNumberTable[44] 166 Dem\_DTCNumberTable[45] 237 Dem DTCNumberTable[46] 182 Dem\_DTCNumberTable[47] 221 Dem DTCNumberTable[48] 164 Dem\_DTCNumberTable[49] 182 Dem\_DTCNumberTable[50] 221 Dem\_DTCNumberTable[51] 182 Dem\_DTCNumberTable[52] 182 Dem\_DTCNumberTable[53] 221 Dem\_DTCNumberTable[54] 164 Dem\_DTCNumberTable[55] 237 Dem\_DTCNumberTable[56] 182 Dem\_DTCNumberTable[57] 221 Dem\_DTCNumberTable[58] 182 237 Dem\_DTCNumberTable[59] Dem\_DTCNumberTable[60] 182 Dem\_DTCNumberTable[61] 221 Dem\_DTCNumberTable[62] 164 Dem\_DTCNumberTable[63] 159 Dem\_DTCNumberTable[64] 164 Dem\_DTCNumberTable[65] 34 Dem\_DTCNumberTable[66] 166 Dem\_DTCNumberTable[67] 182 Dem\_DTCNumberTable[68] 182 Dem\_DTCNumberTable[69] 221 Dem\_DTCNumberTable[70] 164 Dem\_DTCNumberTable[71] 237 Dem DTCNumberTable[72] 164 Dem\_DTCNumberTable[73] 159 Dem DTCNumberTable[74] 164 Dem\_DTCNumberTable[75] 34 Dem DTCNumberTable[76] 166 Dem\_DTC\_FTB\_Table[0] 100 Dem\_DTC\_FTB\_Table[1] 77 Dem\_DTC\_FTB\_Table[2] 185 Dem\_DTC\_FTB\_Table[3] 93 72 Dem\_DTC\_FTB\_Table[4] Dem\_DTC\_FTB\_Table[5] 20 Dem\_DTC\_FTB\_Table[6] 13 Dem\_DTC\_FTB\_Table[7] 13 Dem\_DTC\_FTB\_Table[8] 100 Dem\_DTC\_FTB\_Table[9] 77 Dem\_DTC\_FTB\_Table[10] 13 Dem\_DTC\_FTB\_Table[11] 191 Dem\_DTC\_FTB\_Table[12] 77 Dem\_DTC\_FTB\_Table[13] 13 Dem\_DTC\_FTB\_Table[14] 100 Dem\_DTC\_FTB\_Table[15] 77 Dem\_DTC\_FTB\_Table[16] 77 Dem\_DTC\_FTB\_Table[17] 13 Dem\_DTC\_FTB\_Table[18] 69 Dem\_DTC\_FTB\_Table[19] 100 Dem\_DTC\_FTB\_Table[20] 77 Dem\_DTC\_FTB\_Table[21] 13 Dem\_DTC\_FTB\_Table[22] 100 Dem\_DTC\_FTB\_Table[23] 185 Dem\_DTC\_FTB\_Table[24] 93 Dem\_DTC\_FTB\_Table[25] 72 20 Dem\_DTC\_FTB\_Table[26] Dem\_DTC\_FTB\_Table[27] 77 Dem\_DTC\_FTB\_Table[28] 100 Dem\_DTC\_FTB\_Table[29] 77 Dem\_DTC\_FTB\_Table[30] 100 Dem\_DTC\_FTB\_Table[31] 100 Dem DTC FTB Table[32] 77 Dem\_DTC\_FTB\_Table[33] 77 Dem DTC FTB Table[34] 100 Dem\_DTC\_FTB\_Table[35] 77 Dem\_DTC\_FTB\_Table[36] 100 Dem\_DTC\_FTB\_Table[37] 100 Dem\_DTC\_FTB\_Table[38] 100 Dem\_DTC\_FTB\_Table[39] 77

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value Dem\_DTC\_FTB\_Table[40] Dem\_DTC\_FTB\_Table[41] 185 Dem\_DTC\_FTB\_Table[42] 93 Dem\_DTC\_FTB\_Table[43] 72 Dem\_DTC\_FTB\_Table[44] 20 Dem\_DTC\_FTB\_Table[45] 13 Dem\_DTC\_FTB\_Table[46] 100 Dem\_DTC\_FTB\_Table[47] 77 Dem\_DTC\_FTB\_Table[48] 93 Dem\_DTC\_FTB\_Table[49] 100 Dem\_DTC\_FTB\_Table[50] 77 Dem\_DTC\_FTB\_Table[51] 100 Dem\_DTC\_FTB\_Table[52] 100 Dem DTC FTB Table[53] 77 Dem\_DTC\_FTB\_Table[54] 93 Dem\_DTC\_FTB\_Table[55] 13 Dem\_DTC\_FTB\_Table[56] 100 Dem\_DTC\_FTB\_Table[57] 77 Dem\_DTC\_FTB\_Table[58] 100 Dem\_DTC\_FTB\_Table[59] 13 Dem\_DTC\_FTB\_Table[60] 100 Dem\_DTC\_FTB\_Table[61] 77 Dem\_DTC\_FTB\_Table[62] 93 Dem\_DTC\_FTB\_Table[63] 185 Dem\_DTC\_FTB\_Table[64] 93 Dem\_DTC\_FTB\_Table[65] 72 Dem\_DTC\_FTB\_Table[66] 20 Dem\_DTC\_FTB\_Table[67] 100 Dem\_DTC\_FTB\_Table[68] 100 Dem\_DTC\_FTB\_Table[69] 77 93 Dem\_DTC\_FTB\_Table[70] Dem\_DTC\_FTB\_Table[71] 13 Dem DTC FTB Table[72] 93 Dem\_DTC\_FTB\_Table[73] 185 93 Dem\_DTC\_FTB\_Table[74] Dem DTC FTB Table[75] 72 Dem\_DTC\_FTB\_Table[76] 20 **Actual Value Expected Value** Result CTCFailedBuf\_Cnt\_M\_lgc[0] 1 CTCFailedBuf\_Cnt\_M\_lgc[1] CTCFailedBuf\_Cnt\_M\_lgc[2] CTCFailedBuf\_Cnt\_M\_lgc[3] CTCFailedBuf Cnt M lqc[4] CTCFailedBuf\_Cnt\_M\_lgc[5] CTCFailedBuf\_Cnt\_M\_lgc[6] 1 CTCFailedBuf\_Cnt\_M\_lgc[7] 1 CTCFailedBuf\_Cnt\_M\_lgc[8] 1 CTCFailedBuf\_Cnt\_M\_lgc[9] 1 CTCFailedBuf\_Cnt\_M\_lgc[10] **~** CTCFailedBuf\_Cnt\_M\_lgc[11] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[12] CTCFailedBuf\_Cnt\_M\_lgc[13] 1 CTCFailedBuf\_Cnt\_M\_lgc[14] CTCFailedBuf\_Cnt\_M\_lgc[15] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[16] **~** CTCFailedBuf\_Cnt\_M\_lgc[17] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[18] CTCFailedBuf\_Cnt\_M\_lgc[19] 1 CTCFailedBuf\_Cnt\_M\_lgc[20] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[21] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[22] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[23] 1 1 CTCFailedBuf Cnt M Igc[24] CTCFailedBuf\_Cnt\_M\_lgc[25] CTCFailedBuf\_Cnt\_M\_lgc[26] 1 CTCFailedBuf\_Cnt\_M\_lgc[27] 1 CTCFailedBuf Cnt M Igc[28] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[29] 1 1 CTCFailedBuf Cnt M Igc[30] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[31] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[32] 1 1  $CTCFailedBuf\_Cnt\_M\_lgc[33]$ 1 1 CTCFailedBuf\_Cnt\_M\_lgc[34] 0 0

2018-04-10, 18:44:44+0530



Name	Actual Value	Expected Value	Resul
CTCFailedBuf_Cnt_M_lgc[35]	0	0	
CTCFailedBuf_Cnt_M_lgc[36]	0	0	•
CTCFailedBuf_Cnt_M_lgc[37]	0	0	
CTCFailedBuf_Cnt_M_lgc[38]	0	0	
CTCFailedBuf_Cnt_M_lgc[39]	0	0	
CTCFailedBuf_Cnt_M_lgc[40]	0	0	
CTCFailedBuf_Cnt_M_lgc[41]	0	0	
CTCFailedBuf_Cnt_M_lgc[42]	0	0	•
CTCFailedBuf_Cnt_M_lgc[43]	0	0	
CTCFailedBuf_Cnt_M_lgc[44]	0	0	
CTCFailedBuf_Cnt_M_lgc[45]	0	0	
CTCFailedBuf_Cnt_M_lgc[46]	0	0	
CTCFailedBuf_Cnt_M_lgc[47]	0	0	
CTCFailedBuf_Cnt_M_lgc[48]	0	0	
CTCFailedBuf_Cnt_M_lgc[49]	0	0	
CTCFailedBuf Cnt M Igc[50]	0	0	
CTCFailedBuf_Cnt_M_lgc[51]	0	0	
CTCFailedBuf_Cnt_M_lgc[52]	0	0	
CTCFailedBuf_Cnt_M_lgc[53]	1	1	
CTCFailedBuf_Cnt_M_lgc[54]	1	1	
CTCFailedBuf_Cnt_M_lgc[55]	1	1	
CTCFailedBuf_Cnt_M_lgc[56]	1	1	
CTCFailedBuf_Cnt_M_lgc[57]	1	1	
CTCFailedBuf_Cnt_M_lgc[58]	1	1	
CTCFailedBuf Cnt M Igc[59]	1	1	
CTCFailedBuf_Cnt_M_lgc[60]	1	1	
CTCFailedBuf_Cnt_M_lgc[61]	1	1	
CTCFailedBuf_Cnt_M_lgc[62]	1	1	
CTCFailedBuf_Cnt_M_lgc[63]	1	1	
CTCFailedBuf_Cnt_M_lgc[64]	1	1	
CTCFailedBuf_Cnt_M_lgc[65]	0	0	
CTCFailedBuf_Cnt_M_lgc[66]	0	0	
CTCFailedBuf_Cnt_M_lgc[67]	0	0	
CTCFailedBuf_Cnt_M_lgc[68]	0	0	
CTCFailedBuf_Cnt_M_lgc[69]	0	0	
CTCFailedBuf_Cnt_M_lgc[70]	0	0	
CTCFailedBuf_Cnt_M_lgc[71]	0	0	
CTCFailedBuf_Cnt_M_lgc[72]	0	0	
CTCFailedBuf_Cnt_M_lgc[73]	1	1	
CTCFailedBuf_Cnt_M_lgc[74]	0	0	
CTCFailedBuf_Cnt_M_lgc[75]	0	0	
CTCFailedBuf_Cnt_M_lgc[76]	0	0	
CTCFailed Cnt M Igc	1	1	
Demlf_DTCStatusChanged()	0	0	
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc(data)	1	1	

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	~

Test Step 2.5 (Repeat Count = 1)		
Name	Input Value	
CTCFailedBuf_Cnt_M_lgc[0]	1	
CTCFailedBuf_Cnt_M_lgc[1]	1	
CTCFailedBuf_Cnt_M_lgc[2]	1	
CTCFailedBuf_Cnt_M_lgc[3]	1	
CTCFailedBuf_Cnt_M_lgc[4]	1	
CTCFailedBuf_Cnt_M_lgc[5]	1	
CTCFailedBuf_Cnt_M_lgc[6]	1	
CTCFailedBuf_Cnt_M_lgc[7]	0	
CTCFailedBuf_Cnt_M_lgc[8]	1	
CTCFailedBuf_Cnt_M_lgc[9]	1	
CTCFailedBuf_Cnt_M_lgc[10]	1	
CTCFailedBuf_Cnt_M_lgc[11]	1	
CTCFailedBuf_Cnt_M_lgc[12]	0	
CTCFailedBuf_Cnt_M_lgc[13]	1	
CTCFailedBuf_Cnt_M_lgc[14]	1	
CTCFailedBuf_Cnt_M_lgc[15]	0	
CTCFailedBuf_Cnt_M_lgc[16]	1	
CTCFailedBuf_Cnt_M_lgc[17]	1	

DemIf\_DTCS



Name	Input Value
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf Cnt M Igc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf Cnt M Igc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	1
	0
CTCFailedBuf_Cnt_M_lgc[36]	
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_Igc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	0
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1
CTCFailedBuf_Cnt_M_lgc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_lgc[66]	0
CTCFailedBuf_Cnt_M_lgc[67]	0
CTCFailedBuf_Cnt_M_lgc[68]	0
CTCFailedBuf_Cnt_M_lgc[69]	0
CTCFailedBuf_Cnt_M_lgc[70]	0
CTCFailedBuf_Cnt_M_lgc[71]	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	0
CTCFailedBuf_Cnt_M_lgc[74]	0
CTCFailedBuf_Cnt_M_lgc[75]	0
CTCFailedBuf_Cnt_M_lgc[76]	0
CTCFailed_Cnt_M_lgc	1
DTC	256327693
DTCKind	1
DTCStatusNew	30
DTCStatusOld	178
Dem_DTCNumberTable[0]	99
Dem_DTCNumberTable[1]	143
Dem_DTCNumberTable[2]	36
Dem_DTCNumberTable[3]	85
Dem_DTCNumberTable[4]	238
Dem_DTCNumberTable[5]	62
Dem_DTCNumberTable[6]	217
Dem_DTCNumberTable[7]	217
Dem_DTCNumberTable[8]	99

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Name Input Value Dem\_DTCNumberTable[9] 143 Dem\_DTCNumberTable[10] 217 Dem\_DTCNumberTable[11] 101 Dem\_DTCNumberTable[12] 143 Dem\_DTCNumberTable[13] 217 Dem\_DTCNumberTable[14] 99 Dem\_DTCNumberTable[15] 143 Dem\_DTCNumberTable[16] 143 Dem\_DTCNumberTable[17] 217 Dem DTCNumberTable[18] 236 Dem\_DTCNumberTable[19] 99 Dem\_DTCNumberTable[20] 143 Dem\_DTCNumberTable[21] 217 Dem DTCNumberTable[22] 99 Dem\_DTCNumberTable[23] 36 Dem\_DTCNumberTable[24] 85 Dem\_DTCNumberTable[25] 238 Dem\_DTCNumberTable[26] 62 Dem\_DTCNumberTable[27] 143 Dem\_DTCNumberTable[28] 99 Dem\_DTCNumberTable[29] 143 Dem\_DTCNumberTable[30] 99 Dem\_DTCNumberTable[31] 99 Dem\_DTCNumberTable[32] 143 143 Dem\_DTCNumberTable[33] Dem\_DTCNumberTable[34] 99 Dem\_DTCNumberTable[35] 143 Dem\_DTCNumberTable[36] 99 Dem\_DTCNumberTable[37] 99 Dem\_DTCNumberTable[38] 99 Dem DTCNumberTable[39] 143 Dem\_DTCNumberTable[40] 143 Dem DTCNumberTable[41] 36 Dem\_DTCNumberTable[42] 85 Dem\_DTCNumberTable[43] 238 Dem DTCNumberTable[44] 62 Dem\_DTCNumberTable[45] 217 Dem\_DTCNumberTable[46] 99 Dem\_DTCNumberTable[47] 143 Dem DTCNumberTable[48] 85 Dem\_DTCNumberTable[49] 99 Dem DTCNumberTable[50] 143 Dem\_DTCNumberTable[51] 99 Dem\_DTCNumberTable[52] 99 143 Dem\_DTCNumberTable[53] Dem\_DTCNumberTable[54] 85 217 Dem DTCNumberTable[55] Dem\_DTCNumberTable[56] 99 Dem\_DTCNumberTable[57] 143 Dem\_DTCNumberTable[58] 99 Dem\_DTCNumberTable[59] 217 Dem\_DTCNumberTable[60] 99 Dem\_DTCNumberTable[61] 143 Dem\_DTCNumberTable[62] 85 Dem\_DTCNumberTable[63] 36 Dem\_DTCNumberTable[64] 85 Dem\_DTCNumberTable[65] 238 Dem DTCNumberTable[66] 62 Dem\_DTCNumberTable[67] 99 Dem\_DTCNumberTable[68] 99 Dem\_DTCNumberTable[69] 143 Dem\_DTCNumberTable[70] 85 Dem\_DTCNumberTable[71] 217 Dem DTCNumberTable[72] 85 Dem\_DTCNumberTable[73] 36 Dem DTCNumberTable[74] 85 Dem\_DTCNumberTable[75] 238 Dem DTCNumberTable[76] 62 Dem\_DTC\_FTB\_Table[0] 161 Dem\_DTC\_FTB\_Table[1] 211 Dem\_DTC\_FTB\_Table[2] 7 Dem\_DTC\_FTB\_Table[3] 239 Dem\_DTC\_FTB\_Table[4] 206

Demlf\_DTCS



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Name	Input Value
Dem_DTC_FTB_Table[5]	70
Dem_DTC_FTB_Table[6]	84
Dem_DTC_FTB_Table[7]	84
Dem_DTC_FTB_Table[8]	161
Dem_DTC_FTB_Table[9]	211
Dem_DTC_FTB_Table[10]	84
Dem_DTC_FTB_Table[11]	193
Dem_DTC_FTB_Table[12]	211
Dem_DTC_FTB_Table[13]	84
Dem_DTC_FTB_Table[14]	161
Dem_DTC_FTB_Table[15]	211
Dem_DTC_FTB_Table[16]	211
Dem_DTC_FTB_Table[17]	84
Dem_DTC_FTB_Table[18]	108
Dem_DTC_FTB_Table[19]	161
Dem_DTC_FTB_Table[20]	211
Dem_DTC_FTB_Table[21]	84
Dem_DTC_FTB_Table[22]	161
Dem_DTC_FTB_Table[23]	7
Dem_DTC_FTB_Table[24]	239
Dem_DTC_FTB_Table[25]	206
Dem_DTC_FTB_Table[26]	70
Dem_DTC_FTB_Table[27] Dem DTC FTB Table[28]	211 161
Dem_DTC_FTB_Table[29]	211 161
Dem_DTC_FTB_Table[30]	161
Dem_DTC_FTB_Table[31] Dem_DTC_FTB_Table[32]	211
Dem_DTC_FTB_Table[32]	211
Dem_DTC_FTB_Table[34]	161
Dem_DTC_FTB_Table[35]	211
Dem_DTC_FTB_Table[36]	161
Dem_DTC_FTB_Table[37]	161
Dem_DTC_FTB_Table[38]	161
Dem_DTC_FTB_Table[39]	211
Dem_DTC_FTB_Table[40]	211
Dem_DTC_FTB_Table[41]	7
Dem_DTC_FTB_Table[42]	239
Dem_DTC_FTB_Table[43]	206
Dem_DTC_FTB_Table[44]	70
Dem_DTC_FTB_Table[45]	84
Dem_DTC_FTB_Table[46]	161
Dem_DTC_FTB_Table[47]	211
Dem_DTC_FTB_Table[48]	239
Dem_DTC_FTB_Table[49]	161
Dem_DTC_FTB_Table[50]	211
Dem_DTC_FTB_Table[51]	161
Dem_DTC_FTB_Table[52]	161
Dem_DTC_FTB_Table[53]	211
Dem_DTC_FTB_Table[54]	239
Dem_DTC_FTB_Table[55]	84
Dem_DTC_FTB_Table[56]	161
Dem_DTC_FTB_Table[57]	211
Dem_DTC_FTB_Table[58]	161
Dem_DTC_FTB_Table[59]	84
Dem_DTC_FTB_Table[60]	161
Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62]	211 239
	7
Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64]	239
Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65]	206
Dem_DTC_FTB_Table[66]	70
Dem_DTC_FTB_Table[67]	161
Dem_DTC_FTB_Table[68]	161
Dem_DTC_FTB_Table[69]	211
Dem_DTC_FTB_Table[09]	239
Dem_DTC_FTB_Table[70]	84
Dem_DTC_FTB_Table[71]	239
Dem DTC FTB Table[73]	7
	7 239
Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75]	

2018-04-10, 18:44:44+0530



Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[2]	1	1	
CTCFailedBuf_Cnt_M_lgc[3]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[4]	1	1	~
CTCFailedBuf_Cnt_M_lgc[5]	1	1	~
CTCFailedBuf_Cnt_M_lgc[6]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[7]	0	0	~
CTCFailedBuf_Cnt_M_lgc[8]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10]	1	1	
CTCFailedBuf_Cnt_M_lgc[11]	1	1	<u> </u>
CTCFailedBuf_Cnt_M_lgc[12]	0	0	~
CTCFailedBuf_Cnt_M_lgc[13]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[14]	1	1	~
CTCFailedBuf_Cnt_M_lgc[15]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[16]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[17]	1	1	
CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19]	1	1	-
CTCFailedBuf_Cnt_M_lgc[20]	0	0	
CTCFailedBuf_Cnt_M_lgc[21]	0	0	~
CTCFailedBuf_Cnt_M_lgc[22]	0	0	~
CTCFailedBuf_Cnt_M_lgc[23]	1	1	~
CTCFailedBuf_Cnt_M_Igc[24]	1	1	~
CTCFailedBuf_Cnt_M_lgc[25]	1	1	~
CTCFailedBuf_Cnt_M_lgc[26]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28]	1	1	
CTCFailedBuf_Cnt_M_lgc[29]	1	1	·
CTCFailedBuf_Cnt_M_lgc[30]	1	1	
CTCFailedBuf_Cnt_M_lgc[31]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[32]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[33]	1	1	~
CTCFailedBuf_Cnt_M_lgc[34]	0	0	~
CTCFailedBuf_Cnt_M_lgc[35]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[36] CTCFailedBuf_Cnt_M_lgc[37]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[38]	0	0	
CTCFailedBuf_Cnt_M_lgc[39]	0	0	•
CTCFailedBuf_Cnt_M_lgc[40]	0	0	~
CTCFailedBuf_Cnt_M_lgc[41]	0	0	~
CTCFailedBuf_Cnt_M_lgc[42]	0	0	~
CTCFailedBuf_Cnt_M_lgc[43]	0	0	~
CTCFailedBuf_Cnt_M_lgc[44]	0	0	~
CTCFailedBuf_Cnt_M_lgc[45] CTCFailedBuf_Cnt_M_lgc[46]	0	0	
CTCFailedBuf_Cnt_M_lgc[47]	0	0	·
CTCFailedBuf Cnt M lgc[48]	0	0	-
CTCFailedBuf_Cnt_M_lgc[49]	0	0	~
CTCFailedBuf_Cnt_M_lgc[50]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_Igc[51]	0	0	~
CTCFailedBuf_Cnt_M_lgc[52]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[53]	1	1	•
CTCFailedBuf_Cnt_M_lgc[54] CTCFailedBuf_Cnt_M_lgc[55]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[56]	1	1	
CTCFailedBuf_Cnt_M_lgc[57]	0	0	<u> </u>
CTCFailedBuf_Cnt_M_lgc[58]	1	1	-
CTCFailedBuf_Cnt_M_lgc[59]	1	1	~
CTCFailedBuf_Cnt_M_lgc[60]	1	1	~
CTCFailedBuf_Cnt_M_lgc[61]	1	1	•
CTCFailedBuf_Cnt_M_lgc[62]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[63]	1	1	· ·
CTCFailedBuf_Cnt_M_lgc[64]	0	0	~
CTCFailedBuf_Cnt_M_lgc[65] CTCFailedBuf_Cnt_M_lgc[66]	0	0	
CTCFailedBuf_Cnt_M_lgc[67]	0	0	-
CTCFailedBuf_Cnt_M_lgc[68]	0	0	~
CTCFailedBuf_Cnt_M_lgc[69]	0	0	~
CTCFailedBuf_Cnt_M_lgc[70]	0	0	~
CTCFailedBuf_Cnt_M_lgc[71]	0	0	~
CTCFailedBuf_Cnt_M_lgc[72]	0	0	<b>✓</b>

Demlf\_DTCS



Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[73]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[74]	0	0	~
CTCFailedBuf_Cnt_M_lgc[75]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[76]	0	0	<b>✓</b>
CTCFailed_Cnt_M_lgc	1	1	<b>✓</b>
Demlf_DTCStatusChanged()	0	0	~
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc(data)	1	1	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte Write Ap Demlf CTCFailed Cnt lgc	1	Rte Write Ap Demlf CTCFailed Cnt lgc	1	

Test Step 2.6 (Repeat Count = 1)	
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf Cnt M lgc[2]	0
CTCFailedBuf_Cnt_M_lgc[3]	1
	1
CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
	1
CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8]	1
	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1.
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_Igc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_Igc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	1
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1

DemIf\_DTCS



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Name	Input Value
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1
CTCFailedBuf_Cnt_M_lgc[64]	1
CTCFailedBuf_Cnt_M_lgc[65]	0
CTCFailedBuf_Cnt_M_lgc[66]	0
CTCFailedBuf_Cnt_M_lgc[67]	0
CTCFailedBuf_Cnt_M_lgc[68]	0
CTCFailedBuf_Cnt_M_lgc[69]	0
CTCFailedBuf_Cnt_M_lgc[70]	0
CTCFailedBuf_Cnt_M_lgc[71]	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	0
CTCFailedBuf_Cnt_M_lgc[74]	0
CTCFailedBuf_Cnt_M_lgc[75]	0
CTCFailedBuf_Cnt_M_lgc[76]	0
CTCFailed_Cnt_M_lgc	1
DTC	3061213468
DTCKind DTCStatusNavi	1
DTCStatusNew	72
DTCStatusOld	13
Dem_DTCNumberTable[0]	31
Dem_DTCNumberTable[1]	227
Dem_DTCNumberTable[2]	66
Dem_DTCNumberTable[3]	96
Dem_DTCNumberTable[4]	130
Dem_DTCNumberTable[5]	24
Dem_DTCNumberTable[6]	240 240
Dem_DTCNumberTable[7] Dem_DTCNumberTable[8]	31
Dem_DTCNumberTable[9]	227
Dem_DTCNumberTable[10]	240
Dem DTCNumberTable[11]	151
Dem_DTCNumberTable[12]	227
Dem_DTCNumberTable[13]	240
Dem_DTCNumberTable[14]	31
Dem_DTCNumberTable[15]	227
Dem_DTCNumberTable[16]	227
Dem_DTCNumberTable[17]	240
Dem_DTCNumberTable[18]	241
Dem_DTCNumberTable[19]	31
Dem_DTCNumberTable[20]	227
Dem_DTCNumberTable[21]	240
Dem_DTCNumberTable[22]	31
Dem_DTCNumberTable[23]	66
Dem_DTCNumberTable[24]	96
Dem_DTCNumberTable[25]	130
Dem_DTCNumberTable[26]	24
Dem_DTCNumberTable[27]	227
Dem_DTCNumberTable[28]	31
Dem_DTCNumberTable[29]	227
Dem_DTCNumberTable[30]	31
Dem_DTCNumberTable[31]	31
Dem_DTCNumberTable[32]	227
Dem_DTCNumberTable[33]	227
Dem_DTCNumberTable[34]	31
Dem_DTCNumberTable[35]	227
Dem_DTCNumberTable[36]	31
Dem_DTCNumberTable[37]	31
Dem_DTCNumberTable[38]	31
Dem_DTCNumberTable[39]	227
Dem_DTCNumberTable[40]	227
Dem_DTCNumberTable[41]	66
Dem_DTCNumberTable[42]	96
Dem_DTCNumberTable[43]	130
Dem_DTCNumberTable[44]	24
	240
Dem_DTCNumberTable[45] Dem_DTCNumberTable[46]	31

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Name Input Value Dem DTCNumberTable[47] 227 Dem\_DTCNumberTable[48] Dem\_DTCNumberTable[49] 31 Dem\_DTCNumberTable[50] 227 Dem\_DTCNumberTable[51] 31 Dem\_DTCNumberTable[52] 31 Dem\_DTCNumberTable[53] 227 Dem\_DTCNumberTable[54] 96 Dem\_DTCNumberTable[55] 240 Dem DTCNumberTable[56] 31 Dem\_DTCNumberTable[57] 227 Dem\_DTCNumberTable[58] 31 Dem\_DTCNumberTable[59] 240 Dem DTCNumberTable[60] 31 Dem\_DTCNumberTable[61] 227 Dem\_DTCNumberTable[62] 96 Dem\_DTCNumberTable[63] 66 Dem\_DTCNumberTable[64] 96 Dem\_DTCNumberTable[65] 130 Dem\_DTCNumberTable[66] 24 Dem\_DTCNumberTable[67] 31 Dem\_DTCNumberTable[68] 31 Dem\_DTCNumberTable[69] 227 Dem\_DTCNumberTable[70] 96 Dem\_DTCNumberTable[71] 240 Dem\_DTCNumberTable[72] 96 Dem\_DTCNumberTable[73] 66 Dem\_DTCNumberTable[74] 96 Dem\_DTCNumberTable[75] 130 Dem\_DTCNumberTable[76] 24 Dem DTC FTB Table[0] 181 Dem\_DTC\_FTB\_Table[1] Dem DTC FTB Table[2] 41 Dem\_DTC\_FTB\_Table[3] 22 Dem\_DTC\_FTB\_Table[4] 24 Dem\_DTC\_FTB\_Table[5] 254 Dem\_DTC\_FTB\_Table[6] 209 Dem\_DTC\_FTB\_Table[7] 209 Dem\_DTC\_FTB\_Table[8] 181 Dem DTC FTB Table[9] Dem\_DTC\_FTB\_Table[10] 209 Dem DTC FTB Table[11] 128 Dem\_DTC\_FTB\_Table[12] 1 Dem\_DTC\_FTB\_Table[13] 209 181 Dem\_DTC\_FTB\_Table[14] Dem\_DTC\_FTB\_Table[15] Dem\_DTC\_FTB\_Table[16] 1 Dem\_DTC\_FTB\_Table[17] 209 Dem\_DTC\_FTB\_Table[18] 33 Dem\_DTC\_FTB\_Table[19] 181 Dem\_DTC\_FTB\_Table[20] 1 Dem\_DTC\_FTB\_Table[21] 209 Dem\_DTC\_FTB\_Table[22] 181 Dem\_DTC\_FTB\_Table[23] 41 Dem\_DTC\_FTB\_Table[24] 22 Dem\_DTC\_FTB\_Table[25] 24 Dem\_DTC\_FTB\_Table[26] 254 Dem\_DTC\_FTB\_Table[27] Dem\_DTC\_FTB\_Table[28] 181 Dem\_DTC\_FTB\_Table[29] Dem\_DTC\_FTB\_Table[30] 181 Dem\_DTC\_FTB\_Table[31] 181 Dem\_DTC\_FTB\_Table[32] 1 Dem\_DTC\_FTB\_Table[33] Dem\_DTC\_FTB\_Table[34] 181 Dem DTC FTB Table[35] 1 Dem\_DTC\_FTB\_Table[36] 181 Dem DTC FTB Table[37] 181 Dem\_DTC\_FTB\_Table[38] 181 Dem\_DTC\_FTB\_Table[39] Dem\_DTC\_FTB\_Table[40] 1 Dem\_DTC\_FTB\_Table[41] 41 Dem\_DTC\_FTB\_Table[42] 22

2018-04-10, 18:44:44+0530



Name	Input Value		
Dem_DTC_FTB_Table[43]	24		
Dem_DTC_FTB_Table[44]	254		
Dem_DTC_FTB_Table[45]	209		
Dem_DTC_FTB_Table[46]	181		
Dem_DTC_FTB_Table[47]	1		
Dem_DTC_FTB_Table[48]	22		
Dem_DTC_FTB_Table[49]	181		
Dem_DTC_FTB_Table[50]	1		
Dem_DTC_FTB_Table[51]	181		
Dem_DTC_FTB_Table[52]	181		
Dem_DTC_FTB_Table[53]	1		
Dem_DTC_FTB_Table[54]	22		
Dem_DTC_FTB_Table[55]	209		
Dem_DTC_FTB_Table[56]	181		
Dem_DTC_FTB_Table[57]	1		
Dem_DTC_FTB_Table[58]	181		
Dem_DTC_FTB_Table[59]	209		
Dem_DTC_FTB_Table[60]	181		
Dem_DTC_FTB_Table[61]	1		
Dem_DTC_FTB_Table[62]	22		
Dem_DTC_FTB_Table[63]	41		
Dem_DTC_FTB_Table[64]	22		
Dem_DTC_FTB_Table[65]	24		
Dem_DTC_FTB_Table[66]	254 181		
Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68]	181		
	181		
Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70]	22		
	209		
	209		
Dem_DTC_FTB_Table[71]	22		
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72]	22		
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73]	41		
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74]	41 22		
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75]	41 22 24		
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]	41 22 24 254	Evpected Value	Popul
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76] Name	41 22 24 254 Actual Value	Expected Value	Resul
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76] Name CTCFailedBuf_Cnt_M_lgc[0]	41 22 24 254 <b>Actual Value</b> 1	1	•
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1]	41 22 24 254 <b>Actual Value</b> 1	1	•
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2]	41 22 24 254 <b>Actual Value</b> 1 1	1 1 0	•
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3]	41 22 24 254  Actual Value  1 1 0 1	1 1 0 1	
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4]	41 22 24 254  Actual Value  1 1 0 1	1 1 0 1 1	
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[4]	41 22 24 254  Actual Value  1 1 0 1 1 1	1 1 0 1	
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6]	41 22 24 254  Actual Value  1 1 0 1	1 1 0 1 1 1	
Dem_DTC_FTB_Table[71]  Dem_DTC_FTB_Table[72]  Dem_DTC_FTB_Table[73]  Dem_DTC_FTB_Table[74]  Dem_DTC_FTB_Table[75]  Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[6]	41 22 24 254  Actual Value  1 1 0 1 1 1 1	1 1 0 1 1 1	
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6]	41 22 24 254  Actual Value  1 1 0 1 1 1 1 1	1 1 0 1 1 1 1	
Dem_DTC_FTB_Table[71]  Dem_DTC_FTB_Table[72]  Dem_DTC_FTB_Table[73]  Dem_DTC_FTB_Table[74]  Dem_DTC_FTB_Table[75]  Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[7]	41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1	1 1 0 1 1 1 1 1	
Dem_DTC_FTB_Table[71]  Dem_DTC_FTB_Table[72]  Dem_DTC_FTB_Table[73]  Dem_DTC_FTB_Table[74]  Dem_DTC_FTB_Table[75]  Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[8]	41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1	1 1 0 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[9]	41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1 1 1 1	1 1 0 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[10]	41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 0 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[11]	41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 0 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[11]	41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 0 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13]	41 22 24 254  Actual Value  1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15]	41 22 24 254  Actual Value  1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15]	41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[16]	41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[71]  Dem_DTC_FTB_Table[72]  Dem_DTC_FTB_Table[73]  Dem_DTC_FTB_Table[74]  Dem_DTC_FTB_Table[75]  Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[17]	41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[18]	41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
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Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29]	41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
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Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[30]	41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[30]	41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[31] CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[34] CTCFailedBuf_Cnt_M_lgc[35]	41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[30]	41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	

Demlf\_DTCS

CTCFailedBuf\_Cnt\_M\_lgc[74]

CTCFailedBuf\_Cnt\_M\_lgc[75]

CTCFailedBuf\_Cnt\_M\_lgc[76]

Demlf\_DTCStatusChanged()

Rte\_Write\_Ap\_Demlf\_CTCFailed\_Cnt\_lgc(data)

CTCFailed\_Cnt\_M\_lgc

2018-04-10, 18:44:44+0530



**Actual Value Expected Value** CTCFailedBuf\_Cnt\_M\_lgc[38] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[39] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[40] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[41] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[42] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[43] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[44] 0 0  $CTCFailedBuf\_Cnt\_M\_lgc[45]$ 0 0 CTCFailedBuf\_Cnt\_M\_lgc[46] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[47] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[48] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[49] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[50] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[51] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[52] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[53] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[54] ソソソソソソソ CTCFailedBuf\_Cnt\_M\_lgc[55] 1 1  $CTCFailedBuf\_Cnt\_M\_lgc[56]$ 1 1 CTCFailedBuf\_Cnt\_M\_lgc[57] 1 CTCFailedBuf\_Cnt\_M\_lgc[58] CTCFailedBuf\_Cnt\_M\_lgc[59] CTCFailedBuf\_Cnt\_M\_lgc[60] CTCFailedBuf\_Cnt\_M\_lgc[61] 1 CTCFailedBuf\_Cnt\_M\_lgc[62] CTCFailedBuf\_Cnt\_M\_lgc[63] CTCFailedBuf\_Cnt\_M\_lgc[64] CTCFailedBuf\_Cnt\_M\_lgc[65] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[66] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[67] 0 0 CTCFailedBuf Cnt M Igc[68] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 0 **y y y** CTCFailedBuf Cnt M Igc[70] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 0 **V** CTCFailedBuf\_Cnt\_M\_lgc[73] 0 0

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	~

0

0

0

1

0

0

0

0

1

0

Test Step 2.7 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value CTCFailedBuf\_Cnt\_M\_lgc[21] 0 CTCFailedBuf\_Cnt\_M\_lgc[22] 0 CTCFailedBuf\_Cnt\_M\_lgc[23] 1 CTCFailedBuf\_Cnt\_M\_lgc[24] CTCFailedBuf\_Cnt\_M\_lgc[25] 1 CTCFailedBuf\_Cnt\_M\_lgc[26] CTCFailedBuf\_Cnt\_M\_lgc[27] 1 CTCFailedBuf\_Cnt\_M\_lgc[28] CTCFailedBuf\_Cnt\_M\_lgc[29] 0 CTCFailedBuf\_Cnt\_M\_lgc[30] CTCFailedBuf\_Cnt\_M\_lgc[31] 1 CTCFailedBuf\_Cnt\_M\_lgc[32] 1 CTCFailedBuf\_Cnt\_M\_lgc[33] CTCFailedBuf\_Cnt\_M\_lgc[34] n CTCFailedBuf\_Cnt\_M\_lgc[35] 0 CTCFailedBuf\_Cnt\_M\_lgc[36] 0 CTCFailedBuf\_Cnt\_M\_lgc[37] 0 CTCFailedBuf\_Cnt\_M\_lgc[38] 0  $CTCFailedBuf\_Cnt\_M\_lgc[39]$ 0 CTCFailedBuf\_Cnt\_M\_lgc[40] 0 CTCFailedBuf\_Cnt\_M\_lgc[41] 0 CTCFailedBuf\_Cnt\_M\_lgc[42] 0 CTCFailedBuf\_Cnt\_M\_lgc[43] 0 CTCFailedBuf\_Cnt\_M\_lgc[44] 0 CTCFailedBuf\_Cnt\_M\_lgc[45] 0 CTCFailedBuf\_Cnt\_M\_lgc[46] 0 CTCFailedBuf\_Cnt\_M\_lgc[47] 0 CTCFailedBuf\_Cnt\_M\_lgc[48] 0 CTCFailedBuf\_Cnt\_M\_lgc[49] 0 CTCFailedBuf\_Cnt\_M\_lgc[50] 0 CTCFailedBuf Cnt M Igc[51] 0 CTCFailedBuf\_Cnt\_M\_lgc[52] n CTCFailedBuf Cnt M Igc[53] 1 CTCFailedBuf\_Cnt\_M\_lgc[54] 1 CTCFailedBuf\_Cnt\_M\_lgc[55] CTCFailedBuf\_Cnt\_M\_lgc[56] 1 CTCFailedBuf\_Cnt\_M\_lgc[57] 1 CTCFailedBuf\_Cnt\_M\_lgc[58] CTCFailedBuf\_Cnt\_M\_lgc[59] CTCFailedBuf\_Cnt\_M\_lgc[60] 1 CTCFailedBuf\_Cnt\_M\_lgc[61] CTCFailedBuf Cnt M lqc[62] CTCFailedBuf\_Cnt\_M\_lgc[63] 1 CTCFailedBuf\_Cnt\_M\_lgc[64] 1 CTCFailedBuf\_Cnt\_M\_lgc[65] 0 CTCFailedBuf\_Cnt\_M\_lgc[66] 0 CTCFailedBuf\_Cnt\_M\_lgc[67] 0 CTCFailedBuf\_Cnt\_M\_lgc[68] 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 CTCFailedBuf\_Cnt\_M\_lgc[73] 0 CTCFailedBuf\_Cnt\_M\_lgc[74] CTCFailedBuf\_Cnt\_M\_lgc[75] 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 CTCFailed\_Cnt\_M\_lgc 0 3405792142 DTC DTCKind 2 DTCStatusNew 206 DTCStatusOld 84 Dem DTCNumberTable[0] 83 Dem\_DTCNumberTable[1] 99 Dem DTCNumberTable[2] 240 Dem\_DTCNumberTable[3] 233 Dem DTCNumberTable[4] 31 Dem\_DTCNumberTable[5] 75 Dem DTCNumberTable[6] 164 Dem\_DTCNumberTable[7] 164 Dem\_DTCNumberTable[8] 83 Dem\_DTCNumberTable[9] 99 Dem\_DTCNumberTable[10] 164 Dem\_DTCNumberTable[11] 40

DemIf\_DTCS



Name	Input Value
Dem_DTCNumberTable[12]	99
Dem_DTCNumberTable[13]	164
Dem_DTCNumberTable[14]	83
Dem_DTCNumberTable[15]	99
Dem_DTCNumberTable[16]	99
Dem_DTCNumberTable[17]	164
Dem_DTCNumberTable[18]	74
Dem_DTCNumberTable[19]	83
Dem_DTCNumberTable[20]	99
Dem_DTCNumberTable[21]	164
Dem_DTCNumberTable[22]	83
Dem_DTCNumberTable[23]	240
Dem_DTCNumberTable[24]	233
Dem_DTCNumberTable[25]	31
Dem_DTCNumberTable[26]	75
Dem_DTCNumberTable[27]	99
Dem_DTCNumberTable[28]	83
Dem_DTCNumberTable[29]	99
Dem_DTCNumberTable[30]	83
Dem_DTCNumberTable[31]	83
Dem_DTCNumberTable[32]	99
Dem_DTCNumberTable[33]	99
Dem_DTCNumberTable[34]	83
Dem_DTCNumberTable[35]	99
Dem_DTCNumberTable[36]	83
Dem_DTCNumberTable[37]	83
Dem_DTCNumberTable[38]	83
Dem_DTCNumberTable[39]	99
Dem_DTCNumberTable[40]	99
	240
Dem_DTCNumberTable[41]	
Dem_DTCNumberTable[42]	233
Dem_DTCNumberTable[43]	31
Dem_DTCNumberTable[44]	75
Dem_DTCNumberTable[45]	164
Dem_DTCNumberTable[46]	83
Dem_DTCNumberTable[47]	99
Dem_DTCNumberTable[48]	233
Dem_DTCNumberTable[49]	83
Dem_DTCNumberTable[50]	99
Dem_DTCNumberTable[51]	83
Dem_DTCNumberTable[52]	83
Dem_DTCNumberTable[53]	99
Dem_DTCNumberTable[54]	233
Dem_DTCNumberTable[55]	164
Dem_DTCNumberTable[56]	83
Dem_DTCNumberTable[57]	99
Dem_DTCNumberTable[58]	83
Dem_DTCNumberTable[59]	164
Dem_DTCNumberTable[60]	83
Dem_DTCNumberTable[61]	99
Dem_DTCNumberTable[62]	233
Dem_DTCNumberTable[63]	240
Dem_DTCNumberTable[64]	233
Dem_DTCNumberTable[65]	31
Dem_DTCNumberTable[66]	75
Dem_DTCNumberTable[67]	83
Dem_DTCNumberTable[68]	83
Dem_DTCNumberTable[69]	99
Dem_DTCNumberTable[70]	233
Dem_DTCNumberTable[71]	164
Dem_DTCNumberTable[72]	233
Dem_DTCNumberTable[73]	240
Dem_DTCNumberTable[74]	233
Dem_DTCNumberTable[75]	31
Dem_DTCNumberTable[76]	75
Dem_DTC_FTB_Table[0]	182
Dem_DTC_FTB_Table[1]	221
Dem_DTC_FTB_Table[2]	159
Dem_DTC_FTB_Table[3]	164
Dem_DTC_FTB_Table[4]	34
Dem_DTC_FTB_Table[5]	166
Dem_DTC_FTB_Table[6]	237
Dem_DTC_FTB_Table[7]	237

2018-04-10, 18:44:44+0530



Name	Input Value		
Dem_DTC_FTB_Table[8]	182		
Dem_DTC_FTB_Table[9]	221		
Dem_DTC_FTB_Table[10]	237		
Dem_DTC_FTB_Table[11]	123		
Dem_DTC_FTB_Table[12]	221		
Dem_DTC_FTB_Table[13]	237		
Dem_DTC_FTB_Table[14]	182		
Dem_DTC_FTB_Table[15]	221		
Dem_DTC_FTB_Table[16]	221		
Dem_DTC_FTB_Table[17]	237		
Dem DTC FTB Table[18]	239		
Dem_DTC_FTB_Table[19]	182		
Dem_DTC_FTB_Table[20]	221		
Dem_DTC_FTB_Table[21]	237		
Dem_DTC_FTB_Table[22]	182		
Dem_DTC_FTB_Table[23]	159		
Dem_DTC_FTB_Table[23]	164		
Dem_DTC_FTB_Table[25]	34		
	166		
Dem_DTC_FTB_Table[26]			
Dem_DTC_FTB_Table[27]	221		
Dem_DTC_FTB_Table[28]	182		
Dem_DTC_FTB_Table[29]	221		
Dem_DTC_FTB_Table[30]	182		
Dem_DTC_FTB_Table[31]	182		
Dem_DTC_FTB_Table[32]	221		
Dem_DTC_FTB_Table[33]	221		
Dem_DTC_FTB_Table[34]	182		
Dem_DTC_FTB_Table[35]	221		
Dem_DTC_FTB_Table[36]	182		
Dem_DTC_FTB_Table[37]	182		
Dem_DTC_FTB_Table[38]	182		
Dem_DTC_FTB_Table[39]	221		
Dem_DTC_FTB_Table[40]	221		
Dem_DTC_FTB_Table[41]	159		
Dem_DTC_FTB_Table[42]	164		
Dem_DTC_FTB_Table[43]	34		
Dem_DTC_FTB_Table[44]	166		
Dem_DTC_FTB_Table[45]	237		
Dem_DTC_FTB_Table[46]	182		
Dem_DTC_FTB_Table[47]	221		
Dem_DTC_FTB_Table[48]	164		
Dem_DTC_FTB_Table[49]	182		
Dem_DTC_FTB_Table[50]	221		
Dem_DTC_FTB_Table[51]	182		
Dem_DTC_FTB_Table[52]	182		
Dem_DTC_FTB_Table[53]	221		
Dem_DTC_FTB_Table[54]	164		
Dem_DTC_FTB_Table[55]	237		
Dem_DTC_FTB_Table[56]	182		
Dem_DTC_FTB_Table[57]	221		
Dem_DTC_FTB_Table[58]	182		
Dem_DTC_FTB_Table[59]	237		
Dem_DTC_FTB_Table[60]	182		
Dem_DTC_FTB_Table[61]	221		
Dem_DTC_FTB_Table[62]	164		
Dem DTC FTB Table[63]	159		
Dem_DTC_FTB_Table[64]	164		
Dem_DTC_FTB_Table[65]	34		
Dem_DTC_FTB_Table[66]	166		
Dem_DTC_FTB_Table[67]	182		
Dem_DTC_FTB_Table[68]	182		
Dem_DTC_FTB_Table[69]	221		
Dem_DTC_FTB_Table[09] Dem_DTC_FTB_Table[70]	164		
	237		
Dem_DTC_FTB_Table[71]			
Dem_DTC_FTB_Table[72]	164		
Dem_DTC_FTB_Table[73]	159		
Dem_DTC_FTB_Table[74]	164		
Dem_DTC_FTB_Table[75]	34		
Dem_DTC_FTB_Table[76]	166		1_
Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[0]	1	1	~
CTCFailedBuf_Cnt_M_lgc[1]	1	1	~
CTCFailedBuf_Cnt_M_lgc[2]	1	1	<b>✓</b>

2018-04-10, 18:44:44+0530



Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf Cnt M lgc[4]	1	1	
CTCFailedBuf_Cnt_M_lgc[5]	1	1	
CTCFailedBuf_Cnt_M_lgc[6]	1	1	-
CTCFailedBuf_Cnt_M_lgc[7]	1	1	~
CTCFailedBuf_Cnt_M_lgc[8]	1	1	~
CTCFailedBuf_Cnt_M_lgc[9]	1	1	~
CTCFailedBuf_Cnt_M_lgc[10]	1	1	~
CTCFailedBuf_Cnt_M_lgc[11]	1	1	~
CTCFailedBuf_Cnt_M_lgc[12]	1	1	~
CTCFailedBuf_Cnt_M_lgc[13]	1	1	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf Cnt M lgc[15]	1	1	· ·
CTCFailedBuf_Cnt_M_lgc[16]	1	1	
CTCFailedBuf_Cnt_M_lgc[17]	1	1	~
CTCFailedBuf_Cnt_M_lgc[18]	1	1	~
CTCFailedBuf_Cnt_M_lgc[19]	1	1	~
CTCFailedBuf_Cnt_M_lgc[20]	0	0	~
CTCFailedBuf_Cnt_M_lgc[21]	0	0	~
CTCFailedBuf_Cnt_M_lgc[22]	0	0	~
CTCFailedBuf_Cnt_M_lgc[23]	1	1	~
CTCFailedBuf_Cnt_M_lgc[24]	1	1	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26]	1	1	-
CTCFailedBuf_Cnt_M_lgc[27]	1	1	~
CTCFailedBuf_Cnt_M_lgc[28]	1	1	-
CTCFailedBuf_Cnt_M_lgc[29]	0	0	~
CTCFailedBuf_Cnt_M_lgc[30]	1	1	~
CTCFailedBuf_Cnt_M_lgc[31]	1	1	~
CTCFailedBuf_Cnt_M_lgc[32]	1	1	~
CTCFailedBuf_Cnt_M_lgc[33]	1	1	~
CTCFailedBuf_Cnt_M_lgc[34]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[35]	0	0	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[36] CTCFailedBuf_Cnt_M_lgc[37]	0	0	~
CTCFailedBuf_Cnt_M_lgc[38]	0	0	-
CTCFailedBuf_Cnt_M_lgc[39]	0	0	~
CTCFailedBuf_Cnt_M_lgc[40]	0	0	~
CTCFailedBuf_Cnt_M_lgc[41]	0	0	~
CTCFailedBuf_Cnt_M_lgc[42]	0	0	~
CTCFailedBuf_Cnt_M_lgc[43]	0	0	~
CTCFailedBuf_Cnt_M_lgc[44]	0	0	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[45] CTCFailedBuf_Cnt_M_lgc[46]	0	0	
CTCFailedBuf_Cnt_M_lgc[47]	0	0	~
CTCFailedBuf_Cnt_M_lgc[48]	0	0	~
CTCFailedBuf_Cnt_M_lgc[49]	0	0	~
CTCFailedBuf_Cnt_M_lgc[50]	0	0	~
CTCFailedBuf_Cnt_M_lgc[51]	0	0	~
CTCFailedBuf_Cnt_M_lgc[52]	0	0	~
CTCFailedBuf_Cnt_M_lgc[53]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[54]	1	1	~
CTCFailedBuf_Cnt_M_lgc[55] CTCFailedBuf_Cnt_M_lgc[56]	1	1	J
CTCFailedBuf Cnt M lgc[57]	1	1	<b>V</b>
CTCFailedBuf Cnt M Igc[58]	1	1	~
CTCFailedBuf_Cnt_M_lgc[59]	1	1	~
CTCFailedBuf_Cnt_M_lgc[60]	1	1	~
CTCFailedBuf_Cnt_M_lgc[61]	1	1	~
CTCFailedBuf_Cnt_M_lgc[62]	1	1	~
CTCFailedBuf_Cnt_M_lgc[63]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[64]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[65] CTCFailedBuf_Cnt_M_lgc[66]	0	0	
CTCFailedBuf_Cnt_M_lgc[67]	0	0	V
CTCFailedBuf_Cnt_M_lgc[68]	0	0	~
CTCFailedBuf_Cnt_M_lgc[69]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[70]	0	0	~
CTCFailedBuf_Cnt_M_lgc[71]	0	0	~
CTCFailedBuf_Cnt_M_lgc[72]	0	0	~
OTOF-11-4D-4 O-4 M 11701	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[73]			-
CTCFailedBuf_Cnt_M_lgc[73] CTCFailedBuf_Cnt_M_lgc[74] CTCFailedBuf_Cnt_M_lgc[75]	1 0	1 0	<b>V</b>

2018-04-10, 18:44:44+0530



Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[76]	0	0	~
CTCFailed_Cnt_M_lgc	0	0	<b>✓</b>
Demlf_DTCStatusChanged()	0	0	<b>✓</b>
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	0	0	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	~

Test Stan 2.9 (Beneat Count = 4)	
Test Step 2.8 (Repeat Count = 1) Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	0
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	0
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_igc[17] CTCFailedBuf_Cnt_M_igc[18]	0
CTCFailedBuf Cnt M Igc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
	1
CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25]	1
	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	0
CTCFailedBuf_Cnt_M_lgc[34]	
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0 0
CTCFailedBuf_Cnt_M_lgc[37]	
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value CTCFailedBuf\_Cnt\_M\_lgc[59] 1 CTCFailedBuf\_Cnt\_M\_lgc[60] CTCFailedBuf\_Cnt\_M\_lgc[61] 1 CTCFailedBuf\_Cnt\_M\_lgc[62] CTCFailedBuf\_Cnt\_M\_lgc[63] 1 CTCFailedBuf\_Cnt\_M\_lgc[64] CTCFailedBuf\_Cnt\_M\_lgc[65] 0 CTCFailedBuf\_Cnt\_M\_lgc[66] 0 CTCFailedBuf\_Cnt\_M\_lgc[67] 0 CTCFailedBuf\_Cnt\_M\_lgc[68] n CTCFailedBuf\_Cnt\_M\_lgc[69] 0 CTCFailedBuf\_Cnt\_M\_lgc[70] n CTCFailedBuf\_Cnt\_M\_lgc[71] 0 CTCFailedBuf\_Cnt\_M\_lgc[72] n CTCFailedBuf\_Cnt\_M\_lgc[73] 0 CTCFailedBuf\_Cnt\_M\_lgc[74] 0 CTCFailedBuf\_Cnt\_M\_lgc[75] 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 CTCFailed\_Cnt\_M\_lgc 1 DTC 20 DTCKind 1 DTCStatusNew 24 DTCStatusOld 0 Dem\_DTCNumberTable[0] 67 Dem\_DTCNumberTable[1] 177 Dem\_DTCNumberTable[2] 247 Dem\_DTCNumberTable[3] 156 Dem\_DTCNumberTable[4] 178 Dem\_DTCNumberTable[5] 171 Dem\_DTCNumberTable[6] 176 Dem DTCNumberTable[7] 176 Dem\_DTCNumberTable[8] 67 Dem DTCNumberTable[9] 177 Dem\_DTCNumberTable[10] 176 Dem\_DTCNumberTable[11] 116 Dem DTCNumberTable[12] 177 Dem\_DTCNumberTable[13] 176 Dem\_DTCNumberTable[14] 67 Dem\_DTCNumberTable[15] 177 Dem DTCNumberTable[16] 177 Dem\_DTCNumberTable[17] 176 Dem DTCNumberTable[18] 171 Dem\_DTCNumberTable[19] 67 Dem\_DTCNumberTable[20] 177 176 Dem\_DTCNumberTable[21] Dem\_DTCNumberTable[22] 67 247 Dem DTCNumberTable[23] Dem\_DTCNumberTable[24] Dem\_DTCNumberTable[25] 178 Dem\_DTCNumberTable[26] 171 Dem\_DTCNumberTable[27] 177 Dem\_DTCNumberTable[28] 67 Dem\_DTCNumberTable[29] 177 Dem\_DTCNumberTable[30] 67 Dem\_DTCNumberTable[31] 67 Dem\_DTCNumberTable[32] 177 Dem\_DTCNumberTable[33] 177 Dem\_DTCNumberTable[34] 67 Dem\_DTCNumberTable[35] 177 Dem\_DTCNumberTable[36] 67 Dem\_DTCNumberTable[37] 67 Dem DTCNumberTable[38] 67 Dem\_DTCNumberTable[39] 177 Dem DTCNumberTable[40] 177 Dem\_DTCNumberTable[41] 247 Dem DTCNumberTable[42] 156 Dem\_DTCNumberTable[43] 178 Dem DTCNumberTable[44] 171 Dem\_DTCNumberTable[45] 176 Dem\_DTCNumberTable[46] 67 Dem\_DTCNumberTable[47] 177 Dem\_DTCNumberTable[48] 156 Dem\_DTCNumberTable[49] 67

DemIf\_DTCS



Name	Input Value
Dem_DTCNumberTable[50]	177
Dem_DTCNumberTable[51]	67
Dem_DTCNumberTable[52]	67
Dem_DTCNumberTable[53]	177
Dem_DTCNumberTable[54]	156
Dem_DTCNumberTable[55]	176
Dem_DTCNumberTable[56]	67
Dem_DTCNumberTable[57]	177
Dem_DTCNumberTable[58]	67
Dem_DTCNumberTable[59]	176
Dem_DTCNumberTable[60]	67
Dem_DTCNumberTable[61]	177
Dem_DTCNumberTable[62]	156
	247
Dem_DTCNumberTable[63]	
Dem_DTCNumberTable[64]	156
Dem_DTCNumberTable[65]	178
Dem_DTCNumberTable[66]	171
Dem_DTCNumberTable[67]	67
Dem_DTCNumberTable[68]	67
Dem_DTCNumberTable[69]	177
Dem_DTCNumberTable[70]	156
Dem_DTCNumberTable[71]	176
Dem_DTCNumberTable[72]	156
Dem_DTCNumberTable[73]	247
Dem_DTCNumberTable[74]	156
Dem_DTCNumberTable[75]	178
Dem_DTCNumberTable[76]	171
Dem_DTC_FTB_Table[0]	99
Dem_DTC_FTB_Table[1]	143
Dem_DTC_FTB_Table[2]	36
Dem_DTC_FTB_Table[3]	85
Dem_DTC_FTB_Table[4]	238
Dem_DTC_FTB_Table[5]	62
Dem_DTC_FTB_Table[6]	217
Dem_DTC_FTB_Table[7]	217
Dem_DTC_FTB_Table[8]	99
Dem_DTC_FTB_Table[9]	143
	217
Dem_DTC_FTB_Table[10] Dem_DTC_FTB_Table[11]	101
	143
Dem_DTC_FTB_Table[12]	
Dem_DTC_FTB_Table[13]	217
Dem_DTC_FTB_Table[14]	99
Dem_DTC_FTB_Table[15]	143
Dem_DTC_FTB_Table[16]	143
Dem_DTC_FTB_Table[17]	217
Dem_DTC_FTB_Table[18]	236
Dem_DTC_FTB_Table[19]	99
Dem_DTC_FTB_Table[20]	143
Dem_DTC_FTB_Table[21]	217
Dem_DTC_FTB_Table[22]	99
Dem_DTC_FTB_Table[23]	36
Dem_DTC_FTB_Table[24]	85
Dem_DTC_FTB_Table[25]	238
Dem_DTC_FTB_Table[26]	62
Dem_DTC_FTB_Table[27]	143
Dem_DTC_FTB_Table[28]	99
Dem_DTC_FTB_Table[29]	143
Dem_DTC_FTB_Table[30]	99
Dem_DTC_FTB_Table[31]	99
Dem_DTC_FTB_Table[32]	143
Dem_DTC_FTB_Table[33]	143
Dem_DTC_FTB_Table[34]	99
Dem_DTC_FTB_Table[35]	143
Dem_DTC_FTB_Table[36]	99
Dem_DTC_FTB_Table[37]	99
Dem_DTC_FTB_Table[38]	99
Dem_DTC_FTB_Table[39]	143
Dem_DTC_FTB_Table[40]	143
Dem_DTC_FTB_Table[40] Dem_DTC_FTB_Table[41]	36
Dem_DTC_FTB_Table[41] Dem_DTC_FTB_Table[42]	85
	238
Dem_DTC_FTB_Table[43] Dem_DTC_FTB_Table[44]	62
	217
Dem_DTC_FTB_Table[45]	411

2018-04-10, 18:44:44+0530



Dem_DTC_FTB_Table[46]   99     Dem_DTC_FTB_Table[47]   143     Dem_DTC_FTB_Table[48]   86     Dem_DTC_FTB_Table[49]   99     Dem_DTC_FTB_Table[50]   143     Dem_DTC_FTB_Table[51]   99     Dem_DTC_FTB_Table[51]   99     Dem_DTC_FTB_Table[51]   99     Dem_DTC_FTB_Table[52]   99     Dem_DTC_FTB_Table[54]   86     Dem_DTC_FTB_Table[54]   86     Dem_DTC_FTB_Table[55]   217     Dem_DTC_FTB_Table[56]   99     Dem_DTC_FTB_Table[57]   143     Dem_DTC_FTB_Table[57]   143     Dem_DTC_FTB_Table[58]   99     Dem_DTC_FTB_Table[58]   99     Dem_DTC_FTB_Table[58]   99     Dem_DTC_FTB_Table[58]   99     Dem_DTC_FTB_Table[68]   99     Dem_DTC_FTB_Table[68]   99     Dem_DTC_FTB_Table[68]   99     Dem_DTC_FTB_Table[68]   99     Dem_DTC_FTB_Table[68]   86     Dem_DTC_FTB_Table[68]   86     Dem_DTC_FTB_Table[68]   86     Dem_DTC_FTB_Table[68]   99     Dem_DTC_FTB_Table[69]   143     Dem_DTC_FTB_Table[69]   144     Dem_DTC_FTB_Table[69]   145     Dem_DTC_FTB_Table[69]   145     Dem_DTC_FTB_Table[69]   145     Dem_DTC_FTB_Table[69]	Name	Input Value		
Des.   DO   To   Taskel   S   Des.	Dem_DTC_FTB_Table[46]	-		
Descriptor	Dem_DTC_FTB_Table[47]			
Den   DEL   FIR   Jacks   Color   Del				
Des. DTC_FER_1046(51)   99   99   99   99   99   99   99				
Des. DTC_FTR_TealS13   143				
Den DTC_FTR_Table[5]   145				
Dem DTC_FTR_Table[5]   ST				
Dear DIC_FER_Table[9]				
Dem DTC_FTB_Take[97]  Dem DTC_FTB_Take[98]	Dem_DTC_FTB_Table[55]	217		
Dem. DTC_FTB_Table(9)	Dem_DTC_FTB_Table[56]	99		
Dem. DTC_FTR_Table(9) Dem. DTC_FTR_Table(1)				
Dem. DTC-FIR   Table(1)   143   14				
Den.   DEC.   PET.   Table   S				
Den. DTC_FTE_Table(S)   36   10   10   10   10   10   10   10   1				
Dem_DTC_FTR_Table(S)				
Dem. DTC_FTR_Table(5)   238				
Dem, DTC FTE Tabelet9   528				
Den. DTC. FTB. Table(RF)   99   Den. DTC. FTB. Table(RF)   99   Den. DTC. FTB. Table(RF)   85   Den. DTC. FTB. Table(RF)   82   Den. DTC. FTB. Table(RF)   92   Den. DTC. FTB. Table(RF)   92   Den. DTC. FTB. Table(RF)   93   Den. DTC. FTB. Table(RF)   94   Den. DTC. FTB. Table(RF)   9		238		
Dem. DTC FTE_Table(R)	Dem_DTC_FTB_Table[66]	62		
Dem. DTC, FTB. Table(P0)   85				
Dem. DTC, FTB. Table(PT)   217				
Dem. DTC_FTB_Tabel(PT)				
Dem DTC, FTB_Table(FZ)   85				
Dem_DTC_FTB_Table/74				
Dem_DTC_FTB_Table[74]   85   Dem_DTC_FTB_Table[75]   82   Dem_DTC_FTB_Table[76]   82   Name				
Dem_DTC_FTB_Table/T6    62				
Name		238		
CTCFaledBut_Cnt_M_lgct	Dem_DTC_FTB_Table[76]	62		
CTCFaledBuf_Cnt_M_lgc[1]	Name		-	Result
CTCFaledBuf_Cnt_M_lgq2]				~
CTCFaledBut_Cnt_M_lgc 3				•
CTCFaledBuf_Cnt_M_lgc[4]				•
CTCFailedBuf_Cnt_M_lgd[5]				
CTCFailedBuf_Cnt_M_lgcf6    1				
CTCFailedBuf_Cnt_M_lgcf8] 1 1 1 1 1 CTCFailedBuf_Cnt_M_lgcf8] 1 1 1 1 1 1 CTCFailedBuf_Cnt_M_lgcf8] 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1				-
CTCFailedBuf_Cnt_M_lgd]9		1	1	•
CTCFailedBuf_Cnt_M_lgc[10]	0705 1 10 ( 0 ) 14   155			<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[11]	CTCFalledBut_Cnt_M_lgc[8]	1	1	•
CTCFailedBuf_Cnt_M_lgc[12] 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	CTCFailedBuf_Cnt_M_lgc[9]	1	1	•
CTCFailedBuf_Cnt_M_lgc[13] 1 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[15] 1 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[15] 1 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[16] 1 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[17] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[17] 1 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[18] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[19] 1 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[20] 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[20] 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[21] 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[23] 1 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[23] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[23] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[24] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[25] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[26] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[26] 1 1 1 CTCFailedBuf_Cnt_M_lgc[27] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[28] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[38] 1 1 1 CTCFailedBuf_Cnt_M_lgc[38] 1 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[38] 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10]	1	1	•
CTCFailedBuf_Cnt_M_lgc[14] 1 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[16] 1 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[16] 1 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[17] 1 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[17] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[18] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[18] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[20] 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[20] 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[21] 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[23] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[23] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[23] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[24] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[25] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[26] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[26] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[27] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[28] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[31] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[34] 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[35] 0 0 0 CTCFailedBuf_Cnt_M_lgc[35] 0 0 0 CTCFailedBuf_Cnt_M_lgc[35] 0 0 CTCFailedBuf_Cnt_M_lgc[38] 0 0 CTCFailedBuf_Cnt_M_lgc[38] 0 0 CTCFailedBuf_Cnt_M_lgc[38] 0 0 CTCFailedBuf_Cnt_M_lgc[38] 0 C	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11]	1 1 1	1 1 1	•
CTCFailedBuf_Cnt_M_lgc[15] 1 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[17] 1 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[17] 1 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[18] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[18] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[18] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[20] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[20] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[21] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[22] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[23] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[23] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[25] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[26] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[27] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[28] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[28] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[28] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[30] 1 1 1 CTCFailedBuf_Cnt_M_lgc[30] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[30] 1 1 1 1 CTCFailedBuf_Cnt_M_lgc[30] 1 1 1 CTCFailedBuf_Cnt_M_lgc[30] 1 1 1 CTCFailedBuf_Cnt_M_lgc[30] 1 1 1 CTCFailedBuf_Cnt_M_lgc[30] 1 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[30] 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[30] 0 0 CTCFailedBuf_Cnt_M_lgc[30] 0 0 CTCFailedBuf_Cnt_M_lgc[30] 0 0 CTCFailedBuf_Cnt_M_lgc[30] 0 CTCFailedBuf_Cnt_M_lgc[30] 0 CTCFaile	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12]	1 1 1 0	1 1 1 0	
CTCFailedBuf_Cnt_M_lgc[16]       1       1         CTCFailedBuf_Cnt_M_lgc[17]       1       1         CTCFailedBuf_Cnt_M_lgc[18]       0       0         CTCFailedBuf_Cnt_M_lgc[19]       1       1         CTCFailedBuf_Cnt_M_lgc[20]       0       0         CTCFailedBuf_Cnt_M_lgc[21]       0       0         CTCFailedBuf_Cnt_M_lgc[22]       0       0         CTCFailedBuf_Cnt_M_lgc[23]       1       1         CTCFailedBuf_Cnt_M_lgc[24]       1       1         CTCFailedBuf_Cnt_M_lgc[25]       1       1         CTCFailedBuf_Cnt_M_lgc[26]       1       1         CTCFailedBuf_Cnt_M_lgc[27]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[30]       1       1         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_l	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13]	1 1 1 0	1 1 1 0	
CTCFailedBuf_Cnt_M_lgc[18]       0       0         CTCFailedBuf_Cnt_M_lgc[20]       0       0         CTCFailedBuf_Cnt_M_lgc[21]       0       0         CTCFailedBuf_Cnt_M_lgc[21]       0       0         CTCFailedBuf_Cnt_M_lgc[22]       0       0         CTCFailedBuf_Cnt_M_lgc[23]       1       1         CTCFailedBuf_Cnt_M_lgc[24]       1       1         CTCFailedBuf_Cnt_M_lgc[25]       1       1         CTCFailedBuf_Cnt_M_lgc[26]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[29]       1       1         CTCFailedBuf_Cnt_M_lgc[30]       1       1         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_l	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14]	1 1 1 0 1	1 1 1 0 1	
CTCFailedBuf_Cnt_M_lgc[20]	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15]	1 1 1 0 1 1	1 1 1 0 1 1 1	
CTCFailedBuf_Cnt_M_lgc[21]       0       0         CTCFailedBuf_Cnt_M_lgc[22]       0       0         CTCFailedBuf_Cnt_M_lgc[23]       1       1         CTCFailedBuf_Cnt_M_lgc[24]       1       1         CTCFailedBuf_Cnt_M_lgc[24]       1       1         CTCFailedBuf_Cnt_M_lgc[26]       1       1         CTCFailedBuf_Cnt_M_lgc[26]       1       1         CTCFailedBuf_Cnt_M_lgc[27]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[30]       1       1         CTCFailedBuf_Cnt_M_lgc[30]       1       1         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[32]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_l	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15]	1 1 0 1 1 1 1	1 1 0 1 1 1 1	
CTCFailedBuf_Cnt_M_lgc[21]       0       0         CTCFailedBuf_Cnt_M_lgc[22]       0       0         CTCFailedBuf_Cnt_M_lgc[23]       1       1         CTCFailedBuf_Cnt_M_lgc[24]       1       1         CTCFailedBuf_Cnt_M_lgc[25]       1       1         CTCFailedBuf_Cnt_M_lgc[26]       1       1         CTCFailedBuf_Cnt_M_lgc[27]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[30]       1       1         CTCFailedBuf_Cnt_M_lgc[30]       1       1         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[32]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_l	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[16]	1 1 0 1 1 1 1 1 1	1 1 0 1 1 1 1 1 1 0	
CTCFailedBuf_Cnt_M_lgc[22]       0       0         CTCFailedBuf_Cnt_M_lgc[23]       1       1         CTCFailedBuf_Cnt_M_lgc[24]       1       1         CTCFailedBuf_Cnt_M_lgc[25]       1       1         CTCFailedBuf_Cnt_M_lgc[26]       1       1         CTCFailedBuf_Cnt_M_lgc[27]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[29]       1       1         CTCFailedBuf_Cnt_M_lgc[30]       1       1         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[32]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0          CTCFailedBu	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[18]	1 1 0 1 1 1 1 1 1 0	1 1 0 1 1 1 1 1 1 0 1	
CTCFailedBuf_Cnt_M_igc[23]       1       1         CTCFailedBuf_Cnt_M_igc[24]       1       1         CTCFailedBuf_Cnt_M_igc[25]       1       1         CTCFailedBuf_Cnt_M_igc[26]       1       1         CTCFailedBuf_Cnt_M_igc[27]       1       1         CTCFailedBuf_Cnt_M_igc[28]       1       1         CTCFailedBuf_Cnt_M_igc[29]       1       1         CTCFailedBuf_Cnt_M_igc[30]       1       1         CTCFailedBuf_Cnt_M_igc[31]       1       1         CTCFailedBuf_Cnt_M_igc[32]       1       1         CTCFailedBuf_Cnt_M_igc[33]       1       1         CTCFailedBuf_Cnt_M_igc[34]       0       0         CTCFailedBuf_Cnt_M_igc[35]       0       0         CTCFailedBuf_Cnt_M_igc[36]       0       0         CTCFailedBuf_Cnt_M_igc[37]       0       0         CTCFailedBuf_Cnt_M_igc[38]       0       0         CTCFailedBuf_Cnt_M_igc[38]       0       0         CTCFailedBuf_Cnt_M_igc[39]       0       0	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[19]	1 1 0 1 1 1 1 1 1 0 1	1 1 0 1 1 1 1 1 1 0 1	
CTCFailedBuf_Cnt_M_lgc[24]       1       1         CTCFailedBuf_Cnt_M_lgc[25]       1       1         CTCFailedBuf_Cnt_M_lgc[26]       1       1         CTCFailedBuf_Cnt_M_lgc[27]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[29]       1       1         CTCFailedBuf_Cnt_M_lgc[30]       1       1         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[32]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21]	1 1 0 1 1 1 1 1 1 0 1 0	1 1 1 0 1 1 1 1 1 1 0 1 0	
CTCFailedBuf_Cnt_M_lgc[25]       1       1         CTCFailedBuf_Cnt_M_lgc[26]       1       1         CTCFailedBuf_Cnt_M_lgc[27]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[29]       1       1         CTCFailedBuf_Cnt_M_lgc[30]       1       1         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[32]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[21]	1 1 0 1 1 1 1 1 1 0 1 0 0	1 1 1 0 1 1 1 1 1 1 0 1 0 0 0	
CTCFailedBuf_Cnt_M_lgc[26]       1       1         CTCFailedBuf_Cnt_M_lgc[27]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[29]       1       1         CTCFailedBuf_Cnt_M_lgc[30]       1       1         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[32]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23]	1 1 0 1 1 1 1 1 1 0 1 0 0 0 0	1 1 1 0 1 1 1 1 1 1 0 1 0 0 1	
CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[29]       1       1         CTCFailedBuf_Cnt_M_lgc[30]       1       1         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[32]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24]	1 1 1 0 1 1 1 1 1 0 1 0 0 0 0 0	1 1 1 0 1 1 1 1 1 1 0 1 0 0 0 0 0	
CTCFailedBuf_Cnt_M_lgc[29]       1       1         CTCFailedBuf_Cnt_M_lgc[30]       1       1         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[32]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25]	1 1 1 0 1 1 1 1 1 1 1 0 1 1 0 0 1 1 1 1	1 1 1 0 1 1 1 1 1 1 1 1 0 1 1 0 0 1	
CTCFailedBuf_Cnt_M_lgc[30]       1       1         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[32]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26]	1 1 1 0 1 1 1 1 1 1 1 1 0 0 1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 0 1 1 1 1 1 1 1 1 0 0 1 1 0 0 0 0	
CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[32]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28]	1 1 1 0 1 1 1 1 1 1 1 1 0 1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 0 1 1 1 1 1 1 1 1 0 0 1 1 0 0 0 0	
CTCFailedBuf_Cnt_M_lgc[32]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28]	1 1 1 0 1 1 1 1 1 1 1 1 0 1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 0 1 1 1 1 1 1 1 1 1 0 0 1 1 0 0 1	
CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29]	1 1 1 1 0 1 1 1 1 1 1 1 0 0 1 1 0 0 0 1	1 1 1 0 1 1 1 1 1 1 1 1 1 0 0 1 1 1 0 0 0 0 1	
CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[31]	1 1 1 1 0 1 1 1 1 1 1 1 0 0 1 1 0 0 0 1	1 1 1 1 0 1 1 1 1 1 1 1 1 0 0 1 1 1 1 1	
CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[31] CTCFailedBuf_Cnt_M_lgc[31]	1 1 1 1 0 1 1 1 1 1 1 1 0 0 1 1 0 0 0 1	1 1 1 1 0 1 1 1 1 1 1 1 1 0 0 1 1 0 0 0 0 1	
CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[31] CTCFailedBuf_Cnt_M_lgc[32] CTCFailedBuf_Cnt_M_lgc[32] CTCFailedBuf_Cnt_M_lgc[33]	1 1 1 1 0 1 1 1 1 1 1 1 0 0 1 1 0 0 0 1	1 1 1 1 0 1 1 1 1 1 1 1 1 0 0 1 1 1 1 1	
CTCFailedBuf_Cnt_M_lgc[37]         0         0           CTCFailedBuf_Cnt_M_lgc[38]         0         0           CTCFailedBuf_Cnt_M_lgc[39]         0         0	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[31] CTCFailedBuf_Cnt_M_lgc[32] CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[34]	1 1 1 1 0 1 1 1 1 1 1 1 0 0 1 1 0 0 0 1	1 1 1 1 0 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0	
CTCFailedBuf_Cnt_M_[gc[39] 0 0	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[31] CTCFailedBuf_Cnt_M_lgc[32] CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[34] CTCFailedBuf_Cnt_M_lgc[34] CTCFailedBuf_Cnt_M_lgc[35]	1 1 1 1 0 1 1 1 1 1 1 1 1 0 0 1 1 1 1 1	1 1 1 1 0 1 1 1 1 1 1 1 1 0 0 1 1 1 1 1	
	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[31] CTCFailedBuf_Cnt_M_lgc[32] CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[34] CTCFailedBuf_Cnt_M_lgc[35] CTCFailedBuf_Cnt_M_lgc[35]	1 1 1 1 0 1 1 1 1 1 1 1 1 0 0 1 1 1 1 1	1 1 1 1 0 1 1 1 1 1 1 1 1 1 0 0 1 1 1 1	
CTCFailedBuf Cnt M Inc[40]	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[31] CTCFailedBuf_Cnt_M_lgc[32] CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[34] CTCFailedBuf_Cnt_M_lgc[35] CTCFailedBuf_Cnt_M_lgc[36] CTCFailedBuf_Cnt_M_lgc[37]	1 1 1 1 0 1 1 1 1 1 1 1 1 0 0 1 1 1 1 1	1 1 1 1 0 0 1 1 1 1 1 1 1 1 0 0 1 1 1 1	
5.6. alloasa_5.im_go(10)	CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[31] CTCFailedBuf_Cnt_M_lgc[32] CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[34] CTCFailedBuf_Cnt_M_lgc[35] CTCFailedBuf_Cnt_M_lgc[37] CTCFailedBuf_Cnt_M_lgc[37] CTCFailedBuf_Cnt_M_lgc[38] CTCFailedBuf_Cnt_M_lgc[38] CTCFailedBuf_Cnt_M_lgc[38] CTCFailedBuf_Cnt_M_lgc[39]	1 1 1 1 0 1 1 1 1 1 1 1 1 0 0 1 1 1 1 1	1 1 1 1 0 0 1 1 1 1 1 1 1 1 0 0 1 1 1 1	

Demlf\_DTCS



Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[41]	0	0	~
CTCFailedBuf_Cnt_M_lgc[42]	0	0	~
CTCFailedBuf_Cnt_M_lgc[43]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[44]	0	0	~
CTCFailedBuf_Cnt_M_lgc[45]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[46]	0	0	~
CTCFailedBuf_Cnt_M_lgc[47]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[48]	0	0	~
CTCFailedBuf_Cnt_M_lgc[49]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[50]	0	0	~
CTCFailedBuf_Cnt_M_lgc[51]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[52]	0	0	~
CTCFailedBuf_Cnt_M_lgc[53]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[54]	1	1	~
CTCFailedBuf_Cnt_M_lgc[55]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[56]	1	1	~
CTCFailedBuf_Cnt_M_lgc[57]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[58]	1	1	~
CTCFailedBuf_Cnt_M_lgc[59]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[60]	1	1	~
CTCFailedBuf_Cnt_M_lgc[61]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[62]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[63]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[64]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[65]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[66]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[67]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[68]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[69]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[70]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[71]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[72]	0	0	~
CTCFailedBuf_Cnt_M_lgc[73]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[74]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[75]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[76]	0	0	~
CTCFailed_Cnt_M_lgc	1	1	<b>✓</b>
Demlf_DTCStatusChanged()	0	0	<b>✓</b>
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	1	1	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	~

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1

DemIf\_DTCS



Name	Input Value
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	0
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf Cnt M lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	0
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1
CTCFailedBuf_Cnt_M_lgc[64]	1 0
CTCFailedBuf_Cnt_M_lgc[65]	0
CTCFailedBuf_Cnt_M_lgc[66] CTCFailedBuf_Cnt_M_lgc[67]	1
CTCFailedBuf_Cnt_M_lgc[68]	0
CTCFailedBuf_Cnt_M_lgc[69]	0
CTCFailedBuf_Cnt_M_lgc[70]	0
CTCFailedBuf_Cnt_M_lgc[71]	0
CTCFailedBuf Cnt M lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	0
CTCFailedBuf_Cnt_M_lgc[74]	0
CTCFailedBuf_Cnt_M_lgc[75]	0
CTCFailedBuf_Cnt_M_lgc[76]	0
CTCFailed Cnt M Igc	0
DTC	1692840925
DTCKind	1
DTCStatusNew	34
DTCStatusOld	255
Dem_DTCNumberTable[0]	89
Dem_DTCNumberTable[1]	78
Dem_DTCNumberTable[2]	204
Dem_DTCNumberTable[3]	103
Dem_DTCNumberTable[4]	238
Dem_DTCNumberTable[5]	77
Dem_DTCNumberTable[6]	228
Dem_DTCNumberTable[7]	228
Dem_DTCNumberTable[8]	89
Dem_DTCNumberTable[9]	78
Dem_DTCNumberTable[10]	228
Dem_DTCNumberTable[11]	90
Dem_DTCNumberTable[12]	78
Dem_DTCNumberTable[13]	228
Dem_DTCNumberTable[14]	89

Demlf\_DTCS

2018-04-10, 18:44:44+0530



Name Input Value Dem\_DTCNumberTable[15] 78 Dem\_DTCNumberTable[16] Dem\_DTCNumberTable[17] 228 Dem\_DTCNumberTable[18] 228 Dem\_DTCNumberTable[19] 89 Dem\_DTCNumberTable[20] 78 Dem\_DTCNumberTable[21] 228 Dem\_DTCNumberTable[22] 89 Dem\_DTCNumberTable[23] 204 Dem DTCNumberTable[24] 103 Dem\_DTCNumberTable[25] 238 Dem\_DTCNumberTable[26] 77 Dem\_DTCNumberTable[27] 78 Dem DTCNumberTable[28] 89 Dem\_DTCNumberTable[29] 78 Dem\_DTCNumberTable[30] 89 Dem\_DTCNumberTable[31] 89 Dem\_DTCNumberTable[32] 78 Dem\_DTCNumberTable[33] 78 Dem\_DTCNumberTable[34] 89 Dem\_DTCNumberTable[35] 78 Dem\_DTCNumberTable[36] 89 Dem\_DTCNumberTable[37] 89 Dem\_DTCNumberTable[38] 89 78 Dem\_DTCNumberTable[39] Dem\_DTCNumberTable[40] 78 Dem\_DTCNumberTable[41] 204 Dem\_DTCNumberTable[42] 103 Dem\_DTCNumberTable[43] 238 Dem\_DTCNumberTable[44] 77 Dem\_DTCNumberTable[45] 228 Dem\_DTCNumberTable[46] 89 Dem DTCNumberTable[47] 78 Dem\_DTCNumberTable[48] 103 Dem\_DTCNumberTable[49] 89 Dem DTCNumberTable[50] 78 Dem\_DTCNumberTable[51] 89 Dem\_DTCNumberTable[52] 89 Dem\_DTCNumberTable[53] 78 Dem DTCNumberTable[54] 103 Dem\_DTCNumberTable[55] 228 Dem DTCNumberTable[56] 89 Dem\_DTCNumberTable[57] 78 Dem\_DTCNumberTable[58] 89 228 Dem\_DTCNumberTable[59] Dem\_DTCNumberTable[60] 89 78 Dem\_DTCNumberTable[61] Dem\_DTCNumberTable[62] Dem\_DTCNumberTable[63] 204 Dem\_DTCNumberTable[64] 103 Dem\_DTCNumberTable[65] 238 Dem\_DTCNumberTable[66] 77 Dem\_DTCNumberTable[67] 89 Dem\_DTCNumberTable[68] 89 Dem\_DTCNumberTable[69] 78 Dem\_DTCNumberTable[70] 103 Dem\_DTCNumberTable[71] 228 Dem DTCNumberTable[72] 103 Dem\_DTCNumberTable[73] 204 Dem\_DTCNumberTable[74] 103 Dem\_DTCNumberTable[75] 238 Dem\_DTCNumberTable[76] 77 Dem\_DTC\_FTB\_Table[0] 31 Dem\_DTC\_FTB\_Table[1] 227 Dem\_DTC\_FTB\_Table[2] 66 Dem DTC FTB Table[3] 96 Dem\_DTC\_FTB\_Table[4] 130 Dem DTC FTB Table[5] 24 Dem\_DTC\_FTB\_Table[6] 240 Dem\_DTC\_FTB\_Table[7] 240 31 Dem\_DTC\_FTB\_Table[8] Dem\_DTC\_FTB\_Table[9] 227 Dem\_DTC\_FTB\_Table[10] 240

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Name Input Value Dem\_DTC\_FTB\_Table[11] 151 Dem\_DTC\_FTB\_Table[12] 227 Dem DTC\_FTB\_Table[13] 240 Dem\_DTC\_FTB\_Table[14] 31 Dem\_DTC\_FTB\_Table[15] 227 Dem\_DTC\_FTB\_Table[16] 227 Dem\_DTC\_FTB\_Table[17] 240 Dem\_DTC\_FTB\_Table[18] 241 Dem\_DTC\_FTB\_Table[19] 31 Dem\_DTC\_FTB\_Table[20] 227 Dem\_DTC\_FTB\_Table[21] 240 Dem\_DTC\_FTB\_Table[22] 31 Dem\_DTC\_FTB\_Table[23] 66 Dem\_DTC\_FTB\_Table[24] 96 Dem\_DTC\_FTB\_Table[25] 130 Dem\_DTC\_FTB\_Table[26] 24 Dem\_DTC\_FTB\_Table[27] 227 Dem\_DTC\_FTB\_Table[28] 31 Dem\_DTC\_FTB\_Table[29] 227 Dem\_DTC\_FTB\_Table[30] 31 Dem\_DTC\_FTB\_Table[31] 31 Dem\_DTC\_FTB\_Table[32] 227 Dem\_DTC\_FTB\_Table[33] 227 Dem\_DTC\_FTB\_Table[34] 31 Dem\_DTC\_FTB\_Table[35] 227 Dem\_DTC\_FTB\_Table[36] 31 Dem\_DTC\_FTB\_Table[37] 31 Dem\_DTC\_FTB\_Table[38] 31 Dem DTC FTB Table[39] 227 Dem\_DTC\_FTB\_Table[40] 227 Dem DTC FTB Table[41] 66 Dem\_DTC\_FTB\_Table[42] 96 Dem DTC FTB Table[43] 130 Dem\_DTC\_FTB\_Table[44] 24 Dem\_DTC\_FTB\_Table[45] 240 Dem\_DTC\_FTB\_Table[46] 31 Dem\_DTC\_FTB\_Table[47] 227 Dem\_DTC\_FTB\_Table[48] 96 Dem\_DTC\_FTB\_Table[49] 31 Dem\_DTC\_FTB\_Table[50] 227 Dem\_DTC\_FTB\_Table[51] 31 Dem\_DTC\_FTB\_Table[52] 31 Dem\_DTC\_FTB\_Table[53] 227 Dem\_DTC\_FTB\_Table[54] 96 Dem\_DTC\_FTB\_Table[55] 240 Dem\_DTC\_FTB\_Table[56] 31 Dem\_DTC\_FTB\_Table[57] 227 Dem\_DTC\_FTB\_Table[58] 31 Dem\_DTC\_FTB\_Table[59] 240 Dem\_DTC\_FTB\_Table[60] 31 Dem DTC FTB Table[61] 227 Dem\_DTC\_FTB\_Table[62] 96 Dem\_DTC\_FTB\_Table[63] 66 Dem\_DTC\_FTB\_Table[64] 96 Dem\_DTC\_FTB\_Table[65] 130 Dem\_DTC\_FTB\_Table[66] 24 Dem\_DTC\_FTB\_Table[67] 31 Dem\_DTC\_FTB\_Table[68] 31 Dem\_DTC\_FTB\_Table[69] 227 Dem\_DTC\_FTB\_Table[70] 96 Dem\_DTC\_FTB\_Table[71] 240 Dem\_DTC\_FTB\_Table[72] 96 Dem\_DTC\_FTB\_Table[73] 66 Dem\_DTC\_FTB\_Table[74] 96 Dem\_DTC\_FTB\_Table[75] 130 Dem\_DTC\_FTB\_Table[76] 24 **Actual Value Expected Value** Result CTCFailedBuf\_Cnt\_M\_lgc[0] 1 1 CTCFailedBuf Cnt M lgc[1] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[2] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[3] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[4] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[5]

2018-04-10, 18:44:44+0530



Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[8]	1	1	
CTCFailedBuf_Cnt_M_lgc[9]	1	1	~
CTCFailedBuf_Cnt_M_lgc[10]	1	1	~
CTCFailedBuf_Cnt_M_lgc[11]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[12]	1	1	~
CTCFailedBuf_Cnt_M_lgc[13]	1	1	~
CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15]	1	1	~
CTCFailedBuf Cnt M Igc[16]	1	1	~
CTCFailedBuf_Cnt_M_lgc[17]	1	1	~
CTCFailedBuf_Cnt_M_lgc[18]	1	1	~
CTCFailedBuf_Cnt_M_lgc[19]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[20]	0	0	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22]	0	0	
CTCFailedBuf_Cnt_M_lgc[23]	1	1	~
CTCFailedBuf_Cnt_M_lgc[24]	1	1	~
CTCFailedBuf_Cnt_M_lgc[25]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[26]	1	1	~
CTCFailedBuf_Cnt_M_lgc[27]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[28]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[30]	1	1	
CTCFailedBuf Cnt M Igc[31]	1	1	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[32]	1	1	~
CTCFailedBuf_Cnt_M_lgc[33]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[34]	0	0	~
CTCFailedBuf_Cnt_M_lgc[35]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[36]	0	0	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[37] CTCFailedBuf_Cnt_M_lgc[38]	0	0	Ž
CTCFailedBuf_Cnt_M_lgc[39]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[40]	0	0	~
CTCFailedBuf_Cnt_M_lgc[41]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[42]	0	0	~
CTCFailedBuf_Cnt_M_lgc[43]	0	0	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[44] CTCFailedBuf_Cnt_M_lgc[45]	0	0	~
CTCFailedBuf Cnt M Igc[46]	0	0	_
CTCFailedBuf_Cnt_M_lgc[47]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[48]	0	0	~
CTCFailedBuf_Cnt_M_lgc[49]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[50]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[51] CTCFailedBuf_Cnt_M_lgc[52]	0	0	~
CTCFailedBuf_Cnt_M_lgc[53]	0	0	~
CTCFailedBuf_Cnt_M_lgc[54]	1	1	~
CTCFailedBuf_Cnt_M_lgc[55]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[56]	1	1	~
CTCFailedBuf_Cnt_M_lgc[57]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[58] CTCFailedBuf_Cnt_M_lgc[59]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[60]	1	1	Ž
CTCFailedBuf Cnt M Igc[61]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[62]	1	1	~
CTCFailedBuf_Cnt_M_lgc[63]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[64]	1	1	~
CTCFailedBuf_Cnt_M_lgc[65]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[66]	0	0	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[67] CTCFailedBuf_Cnt_M_lgc[68]	0	0	Ž
CTCFailedBuf_Cnt_M_lgc[69]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[70]	0	0	~
CTCFailedBuf_Cnt_M_lgc[71]	0	0	~
CTCFailedBuf_Cnt_M_lgc[72]	0	0	~
CTCFailedBuf_Cnt_M_lgc[73]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[74] CTCFailedBuf_Cnt_M_lgc[75]	0	0	- v
CTCFailedBuf_Cnt_M_lgc[76]	0	0	~
CTCFailed_Cnt_M_lgc	0	0	~
Demlf_DTCStatusChanged()	0	0	~

Demlf\_DTCS



Name	Actual Value	Expected Value	Result
Rte Write Ap Demlf CTCFailed Cnt loc(data)	0	0	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	~

Test Stan 2.10 (Penest Count = 1)	ني ا
Test Step 2.10 (Repeat Count = 1)	Innuit Value
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	0
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	0
CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf Cnt M Igc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_Igc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf Cnt M Igc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	1
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51] CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_[gc[52] CTCFailedBuf_Cnt_M_[gc[53]	1
CTCFailedBuf Cnt M lgc[54]	1
CTCFailedBuf Cnt M Igc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1

DemIf\_DTCS



Name	Input Value
CTCFailedBuf_Cnt_M_lgc[62]	0
CTCFailedBuf_Cnt_M_lgc[63]	1
CTCFailedBuf_Cnt_M_lgc[64]	1
CTCFailedBuf_Cnt_M_lgc[65]	0 0
CTCFailedBuf_Cnt_M_lgc[66] CTCFailedBuf_Cnt_M_lgc[67]	0
CTCFailedBuf_Cnt_M_lgc[68]	0
CTCFailedBuf_Cnt_M_lgc[69]	0
CTCFailedBuf_Cnt_M_lgc[70]	0
CTCFailedBuf_Cnt_M_lgc[71]	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	0
CTCFailedBuf_Cnt_M_lgc[74]	0
CTCFailedBuf_Cnt_M_lgc[75] CTCFailedBuf_Cnt_M_lgc[76]	0 0
CTCFailed_Cnt_M_lgc	1
DTC	1392997139
DTCKind	2
DTCStatusNew	238
DTCStatusOld	217
Dem_DTCNumberTable[0]	170
Dem_DTCNumberTable[1]	194
Dem_DTCNumberTable[2]	13
Dem_DTCNumberTable[3] Dem_DTCNumberTable[4]	32 172
Dem_DTCNumberTable[4] Dem_DTCNumberTable[5]	241
Dem_DTCNumberTable[6]	91
Dem_DTCNumberTable[7]	91
Dem_DTCNumberTable[8]	170
Dem_DTCNumberTable[9]	194
Dem_DTCNumberTable[10]	91
Dem_DTCNumberTable[11]	82
Dem_DTCNumberTable[12] Dem_DTCNumberTable[13]	194 91
Dem_DTCNumberTable[14]	170
Dem_DTCNumberTable[15]	194
Dem_DTCNumberTable[16]	194
Dem_DTCNumberTable[17]	91
Dem_DTCNumberTable[18]	55
Dem_DTCNumberTable[19]	170
Dem_DTCNumberTable[20]	194
Dem_DTCNumberTable[21]	91
Dem_DTCNumberTable[22] Dem_DTCNumberTable[23]	170 13
Dem_DTCNumberTable[24]	32
Dem_DTCNumberTable[25]	172
Dem_DTCNumberTable[26]	241
Dem_DTCNumberTable[27]	194
Dem_DTCNumberTable[28]	170
Dem_DTCNumberTable[29]	194
Dem_DTCNumberTable[30]	170
Dem_DTCNumberTable[31] Dem_DTCNumberTable[32]	170 194
Dem_DTCNumberTable[32] Dem_DTCNumberTable[33]	194
Dem DTCNumberTable[34]	170
Dem_DTCNumberTable[35]	194
Dem_DTCNumberTable[36]	170
Dem_DTCNumberTable[37]	170
Dem_DTCNumberTable[38]	170
Dem_DTCNumberTable[39]	194
Dem_DTCNumberTable[40]	194
Dem_DTCNumberTable[41] Dem_DTCNumberTable[42]	13 32
Dem_DTCNumberTable[42] Dem_DTCNumberTable[43]	172
Dem_DTCNumberTable[44]	241
Dem_DTCNumberTable[45]	91
Dem_DTCNumberTable[46]	170
Dem_DTCNumberTable[47]	194
Dem_DTCNumberTable[48]	32
Dem_DTCNumberTable[49]	170
Dem_DTCNumberTable[50]	194
Dem_DTCNumberTable[51]	170
Dem_DTCNumberTable[52]	170

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Name Input Value Dem DTCNumberTable[53] 194 Dem\_DTCNumberTable[54] 32 Dem\_DTCNumberTable[55] 91 Dem\_DTCNumberTable[56] 170 Dem\_DTCNumberTable[57] 194 Dem\_DTCNumberTable[58] 170 Dem\_DTCNumberTable[59] 91 Dem\_DTCNumberTable[60] 170 Dem\_DTCNumberTable[61] 194 Dem DTCNumberTable[62] 32 Dem\_DTCNumberTable[63] 13 Dem\_DTCNumberTable[64] 32 Dem\_DTCNumberTable[65] 172 Dem DTCNumberTable[66] 241 Dem\_DTCNumberTable[67] 170 Dem\_DTCNumberTable[68] 170 Dem\_DTCNumberTable[69] 194 Dem\_DTCNumberTable[70] 32 Dem\_DTCNumberTable[71] 91 Dem\_DTCNumberTable[72] 32 Dem\_DTCNumberTable[73] 13 Dem\_DTCNumberTable[74] 32 Dem\_DTCNumberTable[75] 172 Dem\_DTCNumberTable[76] 241 Dem\_DTC\_FTB\_Table[0] 83 Dem\_DTC\_FTB\_Table[1] 99 Dem\_DTC\_FTB\_Table[2] 240 Dem\_DTC\_FTB\_Table[3] 233 Dem\_DTC\_FTB\_Table[4] 31 Dem\_DTC\_FTB\_Table[5] 75 Dem\_DTC\_FTB\_Table[6] 164 Dem\_DTC\_FTB\_Table[7] 164 Dem DTC FTB Table[8] 83 Dem\_DTC\_FTB\_Table[9] 99 Dem\_DTC\_FTB\_Table[10] 164 Dem DTC FTB Table[11] 40 Dem\_DTC\_FTB\_Table[12] 99 Dem\_DTC\_FTB\_Table[13] 164 Dem\_DTC\_FTB\_Table[14] 83 Dem DTC\_FTB\_Table[15] 99 Dem\_DTC\_FTB\_Table[16] 99 Dem DTC FTB Table[17] 164 Dem\_DTC\_FTB\_Table[18] 74 Dem\_DTC\_FTB\_Table[19] 83 99 Dem\_DTC\_FTB\_Table[20] Dem\_DTC\_FTB\_Table[21] 164 83 Dem\_DTC\_FTB\_Table[22] Dem\_DTC\_FTB\_Table[23] 240 Dem\_DTC\_FTB\_Table[24] 233 Dem\_DTC\_FTB\_Table[25] 31 Dem\_DTC\_FTB\_Table[26] 75 Dem\_DTC\_FTB\_Table[27] 99 Dem\_DTC\_FTB\_Table[28] 83 Dem\_DTC\_FTB\_Table[29] 99 Dem\_DTC\_FTB\_Table[30] 83 Dem\_DTC\_FTB\_Table[31] 83 Dem\_DTC\_FTB\_Table[32] 99 Dem\_DTC\_FTB\_Table[33] 99 Dem\_DTC\_FTB\_Table[34] 83 Dem\_DTC\_FTB\_Table[35] 99 Dem\_DTC\_FTB\_Table[36] 83 Dem\_DTC\_FTB\_Table[37] 83 Dem\_DTC\_FTB\_Table[38] 83 Dem\_DTC\_FTB\_Table[39] 99 Dem\_DTC\_FTB\_Table[40] 99 Dem DTC FTB Table[41] 240 Dem\_DTC\_FTB\_Table[42] 233 Dem DTC FTB Table[43] 31 Dem\_DTC\_FTB\_Table[44] 75 Dem\_DTC\_FTB\_Table[45] 164 Dem\_DTC\_FTB\_Table[46] 83 Dem\_DTC\_FTB\_Table[47] 99 Dem\_DTC\_FTB\_Table[48] 233

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value Dem\_DTC\_FTB\_Table[49] 83 Dem\_DTC\_FTB\_Table[50] 99 Dem DTC\_FTB\_Table[51] 83 Dem\_DTC\_FTB\_Table[52] 83 Dem\_DTC\_FTB\_Table[53] 99 Dem\_DTC\_FTB\_Table[54] 233 Dem\_DTC\_FTB\_Table[55] 164 Dem\_DTC\_FTB\_Table[56] 83 Dem\_DTC\_FTB\_Table[57] 99 Dem\_DTC\_FTB\_Table[58] 83 Dem\_DTC\_FTB\_Table[59] 164 83 Dem\_DTC\_FTB\_Table[60] Dem\_DTC\_FTB\_Table[61] 99 Dem\_DTC\_FTB\_Table[62] 233 Dem\_DTC\_FTB\_Table[63] 240 233 Dem DTC FTB Table[64] Dem\_DTC\_FTB\_Table[65] 31 Dem\_DTC\_FTB\_Table[66] 75 Dem\_DTC\_FTB\_Table[67] 83 Dem\_DTC\_FTB\_Table[68] 83 Dem\_DTC\_FTB\_Table[69] qq Dem\_DTC\_FTB\_Table[70] 233 Dem\_DTC\_FTB\_Table[71] 164 Dem\_DTC\_FTB\_Table[72] 233 Dem\_DTC\_FTB\_Table[73] 240 Dem\_DTC\_FTB\_Table[74] 233 Dem\_DTC\_FTB\_Table[75] 31 Dem\_DTC\_FTB\_Table[76] 75 **Actual Value Expected Value** Result CTCFailedBuf\_Cnt\_M\_lgc[0] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[1] 1 CTCFailedBuf Cnt M Igc[2] CTCFailedBuf\_Cnt\_M\_lgc[3] 1 1 CTCFailedBuf Cnt M Igc[4] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[5] 1 CTCFailedBuf\_Cnt\_M\_lgc[6] CTCFailedBuf\_Cnt\_M\_lgc[7] CTCFailedBuf\_Cnt\_M\_lgc[8]  $CTCFailedBuf\_Cnt\_M\_lgc[9]$ 1 1 CTCFailedBuf\_Cnt\_M\_lgc[10] CTCFailedBuf\_Cnt\_M\_lgc[11] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[12] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[13] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[14] **~** CTCFailedBuf\_Cnt\_M\_lgc[15] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[16] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[17] 1 1 ~ CTCFailedBuf\_Cnt\_M\_lgc[18] CTCFailedBuf\_Cnt\_M\_lgc[19] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[20] n 0 CTCFailedBuf\_Cnt\_M\_lgc[21] 0 0 CTCFailedBuf Cnt M Igc[22] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[23] CTCFailedBuf\_Cnt\_M\_lgc[24] CTCFailedBuf\_Cnt\_M\_lgc[25] 1 CTCFailedBuf\_Cnt\_M\_lgc[26] 1 CTCFailedBuf\_Cnt\_M\_lgc[27] 1 CTCFailedBuf\_Cnt\_M\_lgc[28] CTCFailedBuf\_Cnt\_M\_lgc[29] CTCFailedBuf\_Cnt\_M\_lgc[30] 1 CTCFailedBuf\_Cnt\_M\_lgc[31] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[32] CTCFailedBuf\_Cnt\_M\_lgc[33] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[34] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[35] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[36] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[37] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[38] 0 0 CTCFailedBuf Cnt M Igc[39] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[40] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[41] 1 1 ~ CTCFailedBuf\_Cnt\_M\_lgc[42] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[43] 0 0

2018-04-10, 18:44:44+0530



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Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[44]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[45]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[46]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[47]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[48]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[49]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[50]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[51]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[52]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[53]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[54]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[55]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[56]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[57]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[58]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[59]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[60]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[61]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[62]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[63]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[64]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[65]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[66]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[67]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[68]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[69]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[70]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[71]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[72]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[73]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[74]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[75]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[76]	0	0	✓
CTCFailed_Cnt_M_lgc	1	1	✓
DemIf_DTCStatusChanged()	0	0	✓
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc(data)	1	1	✓

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value CTCFailedBuf\_Cnt\_M\_lgc[27] 1 CTCFailedBuf\_Cnt\_M\_lgc[28] CTCFailedBuf\_Cnt\_M\_lgc[29] 1 CTCFailedBuf\_Cnt\_M\_lgc[30] CTCFailedBuf\_Cnt\_M\_lgc[31] 1 CTCFailedBuf\_Cnt\_M\_lgc[32] CTCFailedBuf\_Cnt\_M\_lgc[33] 1 CTCFailedBuf\_Cnt\_M\_lgc[34] 1 CTCFailedBuf\_Cnt\_M\_lgc[35] 0 CTCFailedBuf\_Cnt\_M\_lgc[36] n CTCFailedBuf\_Cnt\_M\_lgc[37] 0 CTCFailedBuf\_Cnt\_M\_lgc[38] n CTCFailedBuf\_Cnt\_M\_lgc[39] 0 CTCFailedBuf\_Cnt\_M\_lgc[40] n CTCFailedBuf\_Cnt\_M\_lgc[41] 0 CTCFailedBuf\_Cnt\_M\_lgc[42] 0 CTCFailedBuf\_Cnt\_M\_lgc[43] 0 CTCFailedBuf\_Cnt\_M\_lgc[44] 0  $CTCFailedBuf\_Cnt\_M\_lgc[45]$ 0 CTCFailedBuf\_Cnt\_M\_lgc[46] 0 CTCFailedBuf\_Cnt\_M\_lgc[47] 0 CTCFailedBuf\_Cnt\_M\_lgc[48] 0 CTCFailedBuf\_Cnt\_M\_lgc[49] 0 CTCFailedBuf\_Cnt\_M\_lgc[50] 0 CTCFailedBuf\_Cnt\_M\_lgc[51] 0 CTCFailedBuf\_Cnt\_M\_lgc[52] 0 CTCFailedBuf\_Cnt\_M\_lgc[53] 1 CTCFailedBuf\_Cnt\_M\_lgc[54] CTCFailedBuf\_Cnt\_M\_lgc[55] 1 CTCFailedBuf\_Cnt\_M\_lgc[56] 1 CTCFailedBuf Cnt M Igc[57] 1 CTCFailedBuf\_Cnt\_M\_lgc[58] CTCFailedBuf Cnt M Igc[59] 1 CTCFailedBuf\_Cnt\_M\_lgc[60] 1 CTCFailedBuf\_Cnt\_M\_lgc[61] CTCFailedBuf\_Cnt\_M\_lgc[62] 1 CTCFailedBuf\_Cnt\_M\_lgc[63] 1 CTCFailedBuf\_Cnt\_M\_lgc[64] CTCFailedBuf\_Cnt\_M\_lgc[65] 0 CTCFailedBuf\_Cnt\_M\_lgc[66] 0 CTCFailedBuf\_Cnt\_M\_lgc[67] 0 CTCFailedBuf Cnt M lqc[68] 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 CTCFailedBuf\_Cnt\_M\_lgc[73] 0 CTCFailedBuf\_Cnt\_M\_lgc[74] 0 CTCFailedBuf\_Cnt\_M\_lgc[75] 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 CTCFailed Cnt M Igc 0 DTC 983749041 DTCKind 2 DTCStatusNew 0 DTCStatusOld 240 Dem\_DTCNumberTable[0] 161 Dem\_DTCNumberTable[1] 211 Dem DTCNumberTable[2] Dem\_DTCNumberTable[3] 239 Dem\_DTCNumberTable[4] 206 Dem\_DTCNumberTable[5] 70 Dem DTCNumberTable[6] 84 Dem\_DTCNumberTable[7] 84 Dem DTCNumberTable[8] 161 Dem\_DTCNumberTable[9] 211 Dem DTCNumberTable[10] 84 Dem\_DTCNumberTable[11] 193 Dem DTCNumberTable[12] 211 Dem\_DTCNumberTable[13] 84 Dem\_DTCNumberTable[14] 161 Dem\_DTCNumberTable[15] 211 Dem\_DTCNumberTable[16] 211 Dem\_DTCNumberTable[17] 84

## **TEST DETAILS REPORT** Ch n e

Demlf\_DTCS



	( -4 - 10-10
Name	Input Value
Dem_DTCNumberTable[18]	108
Dem_DTCNumberTable[19]	161
Dem_DTCNumberTable[20]	211
Dem_DTCNumberTable[21]	84
Dem_DTCNumberTable[22]	161
Dem_DTCNumberTable[23]	7
Dem_DTCNumberTable[24]	239
Dem_DTCNumberTable[25]	206
Dem_DTCNumberTable[26]	70
Dem_DTCNumberTable[27]	211
Dem_DTCNumberTable[28]	161
Dem_DTCNumberTable[29]	211
Dem_DTCNumberTable[30]	161
Dem_DTCNumberTable[31]	161
Dem_DTCNumberTable[32]	211
Dem_DTCNumberTable[33]	211
Dem_DTCNumberTable[34]	161
Dem_DTCNumberTable[35]	211
Dem_DTCNumberTable[36]	161
Dem_DTCNumberTable[37]	161
Dem_DTCNumberTable[38]	161
Dem_DTCNumberTable[39]	211
Dem_DTCNumberTable[40]	211
Dem_DTCNumberTable[41]	7
Dem_DTCNumberTable[42]	239
Dem_DTCNumberTable[43] Dem DTCNumberTable[44]	206 70
Dem DTCNumberTable[45]	84
	161
Dem_DTCNumberTable[46]	211
Dem_DTCNumberTable[47] Dem_DTCNumberTable[48]	239
Dem_DTCNumberTable[49]	161
Dem_DTCNumberTable[49] Dem_DTCNumberTable[50]	211
Dem_DTCNumberTable[50]	161
Dem_DTCNumberTable[51] Dem_DTCNumberTable[52]	161
Dem_DTCNumberTable[53]	211
Dem_DTCNumberTable[54]	239
Dem_DTCNumberTable[55]	84
Dem_DTCNumberTable[56]	161
Dem_DTCNumberTable[57]	211
Dem_DTCNumberTable[58]	161
Dem DTCNumberTable[59]	84
Dem_DTCNumberTable[60]	161
Dem_DTCNumberTable[61]	211
Dem_DTCNumberTable[62]	239
Dem_DTCNumberTable[63]	7
Dem_DTCNumberTable[64]	239
Dem_DTCNumberTable[65]	206
Dem_DTCNumberTable[66]	70
Dem_DTCNumberTable[67]	161
Dem_DTCNumberTable[68]	161
Dem_DTCNumberTable[69]	211
Dem_DTCNumberTable[70]	239
Dem_DTCNumberTable[71]	84
Dem_DTCNumberTable[72]	239
Dem_DTCNumberTable[73]	7
Dem_DTCNumberTable[74]	239
Dem_DTCNumberTable[75]	206
Dem_DTCNumberTable[76]	70
Dem_DTC_FTB_Table[0]	46
Dem_DTC_FTB_Table[1]	245
Dem_DTC_FTB_Table[2]	24
Dem_DTC_FTB_Table[3]	143
Dem_DTC_FTB_Table[4]	13
Dem_DTC_FTB_Table[5]	12
Dem_DTC_FTB_Table[6]	209
Dem_DTC_FTB_Table[7]	209
Dem_DTC_FTB_Table[8]	46
Dem_DTC_FTB_Table[9]	245
Dem_DTC_FTB_Table[10]	209
Dem_DTC_FTB_Table[11]	145
Dem_DTC_FTB_Table[12] Dem_DTC_FTB_Table[13]	245 209

2018-04-10, 18:44:44+0530



Name	Input Value		
Dem_DTC_FTB_Table[14]	46		
Dem_DTC_FTB_Table[15]	245		
Dem_DTC_FTB_Table[16]	245		
Dem_DTC_FTB_Table[17]	209		
Dem_DTC_FTB_Table[18]	239		
Dem_DTC_FTB_Table[19]	46		
Dem_DTC_FTB_Table[20]	245		
Dem_DTC_FTB_Table[21]	209		
Dem_DTC_FTB_Table[22]	46		
	24		
Dem_DTC_FTB_Table[23]	143		
Dem_DTC_FTB_Table[24]			
Dem_DTC_FTB_Table[25]	13		
Dem_DTC_FTB_Table[26]	12		
Dem_DTC_FTB_Table[27]	245		
Dem_DTC_FTB_Table[28]	46		
Dem_DTC_FTB_Table[29]	245		
Dem_DTC_FTB_Table[30]	46		
Dem_DTC_FTB_Table[31]	46		
Dem_DTC_FTB_Table[32]	245		
Dem_DTC_FTB_Table[33]	245		
Dem_DTC_FTB_Table[34]	46		
Dem_DTC_FTB_Table[35]	245		
Dem_DTC_FTB_Table[36]	46		
Dem_DTC_FTB_Table[37]	46		
Dem_DTC_FTB_Table[38]	46		
Dem_DTC_FTB_Table[39]	245		
Dem_DTC_FTB_Table[40]	245		
Dem_DTC_FTB_Table[41]	24		
Dem_DTC_FTB_Table[42]	143		
Dem_DTC_FTB_Table[43]	13		
Dem_DTC_FTB_Table[44]	12		
Dem_DTC_FTB_Table[45]	209		
Dem_DTC_FTB_Table[46]	46		
Dem_DTC_FTB_Table[47]	245		
Dem_DTC_FTB_Table[48]	143		
Dem_DTC_FTB_Table[49]	46		
Dem_DTC_FTB_Table[50]	245		
Dem_DTC_FTB_Table[51]	46		
Dem_DTC_FTB_Table[52]	46		
Dem_DTC_FTB_Table[53]	245		
Dem_DTC_FTB_Table[54]	143		
Dem_DTC_FTB_Table[55]	209		
Dem_DTC_FTB_Table[56]	46		
Dem_DTC_FTB_Table[50]	245		
Dem_DTC_FTB_Table[58]	46		
Dem_DTC_FTB_Table[59]			
	209		
Dem_DTC_FTB_Table[60]	46		
Dem_DTC_FTB_Table[61]	245		
Dem_DTC_FTB_Table[62]	143		
Dem_DTC_FTB_Table[63]	24		
Dem_DTC_FTB_Table[64]	143		
Dem_DTC_FTB_Table[65]	13		
Dem_DTC_FTB_Table[66]	12		
Dem_DTC_FTB_Table[67]	46		
Dem_DTC_FTB_Table[68]	46		
Dem_DTC_FTB_Table[69]	245		
Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70]			
	245		
Dem_DTC_FTB_Table[70]	245 143		
Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71]	245 143 209		
Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72]	245 143 209 143		
Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73]	245 143 209 143 24		
Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74]	245 143 209 143 24 143		
Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75]	245 143 209 143 24 143 13	Expected Value	Result
Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76] Name	245 143 209 143 24 143 13	Expected Value	Result
Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]	245 143 209 143 24 143 13 12  Actual Value 1	-	
Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1]	245 143 209 143 24 143 13 12  Actual Value 1	1	~
Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2]	245 143 209 143 24 143 13 12  Actual Value 1 1	1 1 1	<b>*</b> * * * * * * * * * * * * * * * * * *
Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3]	245 143 209 143 24 143 13 12  Actual Value 1 1 1	1 1 1 1	· · · · · ·
Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4]	245 143 209 143 24 143 13 12  Actual Value 1 1 1 1	1 1 1 1	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[4]	245 143 209 143 24 143 13 12  Actual Value 1 1 1 1 1	1 1 1 1 1 1	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6]	245 143 209 143 24 143 13 12  Actual Value 1 1 1 1 1 1	1 1 1 1 1 1	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[4]	245 143 209 143 24 143 13 12  Actual Value 1 1 1 1 1	1 1 1 1 1 1	· · · · · · · · · · · · · · · · · · ·

2018-04-10, 18:44:44+0530



Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[9]	1	1	~
CTCFailedBuf_Cnt_M_lgc[10]	1	1	~
CTCFailedBuf_Cnt_M_lgc[11]	1	1	~
CTCFailedBuf_Cnt_M_lgc[12]	1	1	~
CTCFailedBuf_Cnt_M_lgc[13]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[14]	1	1	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16]	1	1	
CTCFailedBuf_Cnt_M_lgc[17]	1	1	~
CTCFailedBuf_Cnt_M_lgc[18]	1	1	
CTCFailedBuf_Cnt_M_lgc[19]	1	1	~
CTCFailedBuf_Cnt_M_lgc[20]	0	0	~
CTCFailedBuf_Cnt_M_lgc[21]	0	0	~
CTCFailedBuf_Cnt_M_lgc[22]	0	0	~
CTCFailedBuf_Cnt_M_lgc[23]	1	1	~
CTCFailedBuf_Cnt_M_lgc[24]	1	1	~
CTCFailedBuf_Cnt_M_lgc[25]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[26]	1	1	~
CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28]	1	1	Ž
CTCFailedBuf Cnt M lgc[29]	1	1	· ·
CTCFailedBuf Cnt M Igc[30]	1	1	_
CTCFailedBuf_Cnt_M_lgc[31]	1	1	~
CTCFailedBuf_Cnt_M_lgc[32]	1	1	~
CTCFailedBuf_Cnt_M_lgc[33]	1	1	~
CTCFailedBuf_Cnt_M_lgc[34]	1	1	~
CTCFailedBuf_Cnt_M_lgc[35]	0	0	~
CTCFailedBuf_Cnt_M_lgc[36]	0	0	~
CTCFailedBuf_Cnt_M_lgc[37]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[38]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[39]	0	0	~
CTCFailedBuf_Cnt_M_lgc[40] CTCFailedBuf_Cnt_M_lgc[41]	0	0	· ·
CTCFailedBuf_Cnt_M_lgc[42]	0	0	
CTCFailedBuf_Cnt_M_lgc[43]	0	0	~
CTCFailedBuf_Cnt_M_lgc[44]	0	0	~
CTCFailedBuf_Cnt_M_lgc[45]	0	0	~
CTCFailedBuf_Cnt_M_lgc[46]	0	0	~
CTCFailedBuf_Cnt_M_lgc[47]	0	0	~
CTCFailedBuf_Cnt_M_lgc[48]	0	0	~
CTCFailedBuf_Cnt_M_lgc[49]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[50]	0	0	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[51] CTCFailedBuf_Cnt_M_lgc[52]	0	0	Ž
CTCFailedBuf_Cnt_M_lgc[53]	1	1	
CTCFailedBuf Cnt M Igc[54]	1	1	-
CTCFailedBuf_Cnt_M_lgc[55]	1	1	~
CTCFailedBuf_Cnt_M_lgc[56]	1	1	~
CTCFailedBuf_Cnt_M_lgc[57]	1	1	~
CTCFailedBuf_Cnt_M_lgc[58]	1	1	~
CTCFailedBuf_Cnt_M_Igc[59]	1	1	~
CTCFailedBuf_Cnt_M_lgc[60]	1	1	~
CTCFailedBuf_Cnt_M_lgc[61]	1	1	~
CTCFailedBuf_Cnt_M_lgc[62]	1	1	· ·
CTCFailedBuf_Cnt_M_lgc[63]	1	1	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[64] CTCFailedBuf_Cnt_M_lgc[65]	0	0	~
CTCFailedBuf Cnt M lgc[66]	0	0	-
CTCFailedBuf_Cnt_M_lgc[67]	0	0	~
CTCFailedBuf_Cnt_M_lgc[68]	0	0	~
CTCFailedBuf_Cnt_M_Igc[69]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[70]	0	0	~
CTCFailedBuf_Cnt_M_lgc[71]	0	0	~
CTCFailedBuf_Cnt_M_lgc[72]	0	0	~
CTCFailedBuf_Cnt_M_Igc[73]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[74]	0	0	~
CTCFailedBuf_Cnt_M_lgc[75]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[76]	0	0	<b>V</b>
CTCFailed_Cnt_M_lgc Demlf_DTCStatusChanged()	0	0	<b>*</b>
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc(data)	0	0	· ·
Tito_Titito_Ap_bollili_o Foi alleu_olit_igo(uata)	·	,	

Demlf\_DTCS



Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte Write An Demlf CTCFailed Cnt loc	1	Rte Write An Demlf CTCFailed Cnt loc	1	_

Test Step 2.12 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1.
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1 0
CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf Cnt M Igc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf Cnt M lgc[20]	0
CTCFailedBuf Cnt M Igc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	0
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_Igc[27] CTCFailedBuf_Cnt_M_Igc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36] CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_gc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45] CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55] CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1

Demlf\_DTCS

2018-04-10, 18:44:44+0530



Input Value CTCFailedBuf\_Cnt\_M\_lgc[64] CTCFailedBuf\_Cnt\_M\_lgc[65] 0 CTCFailedBuf\_Cnt\_M\_lgc[66] 0 CTCFailedBuf\_Cnt\_M\_lgc[67] 0 CTCFailedBuf Cnt M lqc[68] 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 CTCFailedBuf\_Cnt\_M\_lgc[73] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[74] CTCFailedBuf\_Cnt\_M\_lgc[75] 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 CTCFailed\_Cnt\_M\_lgc 0 DTC 56 DTCKind 1 DTCStatusNew 255 DTCStatusOld 164 Dem\_DTCNumberTable[0] 181 Dem\_DTCNumberTable[1] 1 Dem\_DTCNumberTable[2] 41 Dem\_DTCNumberTable[3] 22 Dem\_DTCNumberTable[4] 24 Dem\_DTCNumberTable[5] 254 Dem\_DTCNumberTable[6] 209 Dem\_DTCNumberTable[7] 209 Dem DTCNumberTable[8] 181 Dem\_DTCNumberTable[9] 1 Dem DTCNumberTable[10] 209 Dem\_DTCNumberTable[11] 128 Dem DTCNumberTable[12] Dem\_DTCNumberTable[13] 209 Dem DTCNumberTable[14] 181 Dem\_DTCNumberTable[15] 1 Dem\_DTCNumberTable[16] Dem\_DTCNumberTable[17] 209 Dem\_DTCNumberTable[18] 33 Dem\_DTCNumberTable[19] 181 Dem\_DTCNumberTable[20] Dem\_DTCNumberTable[21] 209 Dem\_DTCNumberTable[22] 181 41 Dem\_DTCNumberTable[23] Dem\_DTCNumberTable[24] 22 Dem\_DTCNumberTable[25] 24 Dem\_DTCNumberTable[26] 254 Dem\_DTCNumberTable[27] 1 Dem\_DTCNumberTable[28] 181 Dem\_DTCNumberTable[29] 1 Dem DTCNumberTable[30] 181 Dem\_DTCNumberTable[31] 181 Dem DTCNumberTable[32] 1 Dem\_DTCNumberTable[33] Dem\_DTCNumberTable[34] 181 Dem\_DTCNumberTable[35] 1 Dem\_DTCNumberTable[36] 181 Dem\_DTCNumberTable[37] 181 Dem\_DTCNumberTable[38] 181 Dem\_DTCNumberTable[39] 1 Dem\_DTCNumberTable[40] Dem\_DTCNumberTable[41] 41 Dem\_DTCNumberTable[42] 22 24 Dem\_DTCNumberTable[43] Dem\_DTCNumberTable[44] 254 Dem\_DTCNumberTable[45] 209 Dem\_DTCNumberTable[46] 181 Dem DTCNumberTable[47] 1 Dem\_DTCNumberTable[48] 22 Dem DTCNumberTable[49] 181 Dem\_DTCNumberTable[50] Dem\_DTCNumberTable[51] 181 Dem DTCNumberTable[52] 181 Dem\_DTCNumberTable[53] 1 22 Dem\_DTCNumberTable[54]

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Name Input Value Dem DTCNumberTable[55] 209 Dem\_DTCNumberTable[56] 181 Dem\_DTCNumberTable[57] 1 Dem\_DTCNumberTable[58] 181 Dem\_DTCNumberTable[59] 209 Dem\_DTCNumberTable[60] 181 Dem\_DTCNumberTable[61] 1 Dem\_DTCNumberTable[62] 22 Dem\_DTCNumberTable[63] 41 Dem DTCNumberTable[64] 22 Dem\_DTCNumberTable[65] 24 Dem\_DTCNumberTable[66] 254 Dem\_DTCNumberTable[67] 181 Dem DTCNumberTable[68] 181 Dem\_DTCNumberTable[69] 1 Dem\_DTCNumberTable[70] 22 Dem\_DTCNumberTable[71] 209 Dem\_DTCNumberTable[72] 22 Dem\_DTCNumberTable[73] 41 Dem\_DTCNumberTable[74] 22 Dem\_DTCNumberTable[75] 24 Dem\_DTCNumberTable[76] 254 Dem\_DTC\_FTB\_Table[0] 112 Dem\_DTC\_FTB\_Table[1] 227 Dem\_DTC\_FTB\_Table[2] 76 Dem\_DTC\_FTB\_Table[3] 252 Dem\_DTC\_FTB\_Table[4] 240 Dem\_DTC\_FTB\_Table[5] 206 Dem\_DTC\_FTB\_Table[6] 62 Dem\_DTC\_FTB\_Table[7] 62 Dem\_DTC\_FTB\_Table[8] 112 Dem\_DTC\_FTB\_Table[9] 227 Dem DTC FTB Table[10] 62 Dem\_DTC\_FTB\_Table[11] 80 Dem\_DTC\_FTB\_Table[12] 227 Dem DTC FTB Table[13] 62 Dem\_DTC\_FTB\_Table[14] 112 Dem\_DTC\_FTB\_Table[15] 227 Dem\_DTC\_FTB\_Table[16] 227 Dem DTC\_FTB\_Table[17] 62 Dem\_DTC\_FTB\_Table[18] 57 Dem DTC FTB Table[19] 112 Dem\_DTC\_FTB\_Table[20] 227 Dem\_DTC\_FTB\_Table[21] 62 112 Dem\_DTC\_FTB\_Table[22] Dem\_DTC\_FTB\_Table[23] 76 252 Dem\_DTC\_FTB\_Table[24] Dem\_DTC\_FTB\_Table[25] 240 Dem\_DTC\_FTB\_Table[26] 206 Dem\_DTC\_FTB\_Table[27] 227 Dem\_DTC\_FTB\_Table[28] 112 Dem\_DTC\_FTB\_Table[29] 227 Dem\_DTC\_FTB\_Table[30] 112 Dem\_DTC\_FTB\_Table[31] 112 Dem\_DTC\_FTB\_Table[32] 227 Dem\_DTC\_FTB\_Table[33] 227 Dem\_DTC\_FTB\_Table[34] 112 Dem\_DTC\_FTB\_Table[35] 227 Dem\_DTC\_FTB\_Table[36] 112 Dem\_DTC\_FTB\_Table[37] 112 Dem\_DTC\_FTB\_Table[38] 112 Dem\_DTC\_FTB\_Table[39] 227 Dem\_DTC\_FTB\_Table[40] 227 Dem\_DTC\_FTB\_Table[41] 76 Dem\_DTC\_FTB\_Table[42] 252 Dem DTC FTB Table[43] 240 Dem\_DTC\_FTB\_Table[44] 206 Dem DTC FTB Table[45] 62 Dem\_DTC\_FTB\_Table[46] 112 Dem\_DTC\_FTB\_Table[47] 227 Dem\_DTC\_FTB\_Table[48] 252 Dem\_DTC\_FTB\_Table[49] 112 Dem\_DTC\_FTB\_Table[50] 227

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value Dem\_DTC\_FTB\_Table[51] 112 Dem\_DTC\_FTB\_Table[52] 112 Dem DTC\_FTB\_Table[53] 227 Dem\_DTC\_FTB\_Table[54] 252 Dem\_DTC\_FTB\_Table[55] 62 Dem\_DTC\_FTB\_Table[56] 112 Dem\_DTC\_FTB\_Table[57] 227 Dem\_DTC\_FTB\_Table[58] 112 Dem\_DTC\_FTB\_Table[59] 62 Dem\_DTC\_FTB\_Table[60] 112 Dem\_DTC\_FTB\_Table[61] 227 252 Dem\_DTC\_FTB\_Table[62] Dem\_DTC\_FTB\_Table[63] 76 Dem\_DTC\_FTB\_Table[64] 252 Dem\_DTC\_FTB\_Table[65] 240 206 Dem DTC FTB Table[66] Dem\_DTC\_FTB\_Table[67] 112 Dem\_DTC\_FTB\_Table[68] 112 Dem\_DTC\_FTB\_Table[69] 227 Dem\_DTC\_FTB\_Table[70] 252 Dem\_DTC\_FTB\_Table[71] 62 Dem\_DTC\_FTB\_Table[72] 252 Dem\_DTC\_FTB\_Table[73] 76 Dem\_DTC\_FTB\_Table[74] 252 Dem\_DTC\_FTB\_Table[75] 240 Dem\_DTC\_FTB\_Table[76] 206 Name **Actual Value Expected Value** Result CTCFailedBuf Cnt M Igc[0] 1 CTCFailedBuf\_Cnt\_M\_lgc[1] CTCFailedBuf\_Cnt\_M\_lgc[2] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[3] 1 CTCFailedBuf Cnt M lgc[4] CTCFailedBuf\_Cnt\_M\_lgc[5] 1 1 CTCFailedBuf Cnt M Igc[6] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[7] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[8] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[9] 1 CTCFailedBuf\_Cnt\_M\_lgc[10] CTCFailedBuf\_Cnt\_M\_lgc[11] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[12] CTCFailedBuf Cnt M lqc[13] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[14] CTCFailedBuf\_Cnt\_M\_lgc[15] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[16] **~** CTCFailedBuf\_Cnt\_M\_lgc[17] 1 CTCFailedBuf\_Cnt\_M\_lgc[18] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[19] 1 1 ~ CTCFailedBuf\_Cnt\_M\_lgc[20] n 0 CTCFailedBuf\_Cnt\_M\_lgc[21] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[22] n n CTCFailedBuf\_Cnt\_M\_lgc[23] 1 1 CTCFailedBuf Cnt M lqc[24] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[25] CTCFailedBuf\_Cnt\_M\_lgc[26] CTCFailedBuf\_Cnt\_M\_lgc[27] 1 CTCFailedBuf\_Cnt\_M\_lgc[28] 1  $CTCFailedBuf\_Cnt\_M\_lgc[29]$ 1 CTCFailedBuf\_Cnt\_M\_lgc[30] CTCFailedBuf\_Cnt\_M\_lgc[31] 1 CTCFailedBuf\_Cnt\_M\_lgc[32] 1 CTCFailedBuf\_Cnt\_M\_lgc[33] 1 1 0 CTCFailedBuf\_Cnt\_M\_lgc[34] 0 CTCFailedBuf\_Cnt\_M\_lgc[35] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[36] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[37] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[38] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[39] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[40] 0 0 CTCFailedBuf Cnt M Igc[41] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[42] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[43] 0 0 ~ CTCFailedBuf\_Cnt\_M\_lgc[44] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[45] 0 0

Rte\_Write\_Ap\_DemIf\_CTCFailed\_Cnt\_lgc(data)

DemIf\_DTCS

2018-04-10, 18:44:44+0530



**Actual Value Expected Value** CTCFailedBuf\_Cnt\_M\_lgc[46] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[47] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[48] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[49] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[50] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[51] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[52] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[53] 1 CTCFailedBuf\_Cnt\_M\_lgc[54] CTCFailedBuf\_Cnt\_M\_lgc[55] CTCFailedBuf\_Cnt\_M\_lgc[56] CTCFailedBuf\_Cnt\_M\_lgc[57] 1 CTCFailedBuf\_Cnt\_M\_lgc[58] CTCFailedBuf\_Cnt\_M\_lgc[59] CTCFailedBuf\_Cnt\_M\_lgc[60] CTCFailedBuf\_Cnt\_M\_lgc[61] 1 CTCFailedBuf\_Cnt\_M\_lgc[62] CTCFailedBuf\_Cnt\_M\_lgc[63] 1  $CTCFailedBuf\_Cnt\_M\_lgc[64]$ ソソソソソ CTCFailedBuf\_Cnt\_M\_lgc[65] 0 0  $CTCFailedBuf\_Cnt\_M\_lgc[66]$ 0 0 CTCFailedBuf\_Cnt\_M\_lgc[67] 0 0  $CTCFailedBuf\_Cnt\_M\_lgc[68]$ 0 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[73] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[74] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[75] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 0 CTCFailed\_Cnt\_M\_lgc 0 0 Demlf DTCStatusChanged() 0 0

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte Write Ap Demlf CTCFailed Cnt lgc	1	Rte Write Ap Demlf CTCFailed Cnt lgc	1	~

0

0

Test Step 2.13 (Repeat Count = 1)	v v v v v v v v v v v v v v v v v v v
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	0
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	0
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	0
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1

2018-04-10, 18:44:44+0530



	<u> </u>	
Name		Input Value
CTCFailedBuf_Cnt_M	lac[29]	1
CTCFailedBuf_Cnt_M		0
CTCFailedBuf_Cnt_M		0
CTCFailedBuf_Cnt_M		0
		0
CTCFailedBuf_Cnt_M		
CTCFailedBuf_Cnt_M		0
CTCFailedBuf_Cnt_M	_lgc[47]	0
CTCFailedBuf_Cnt_M	_lgc[48]	0
CTCFailedBuf_Cnt_M	_lgc[49]	1
CTCFailedBuf_Cnt_M	_lgc[50]	0
CTCFailedBuf_Cnt_M	_lgc[51]	0
CTCFailedBuf_Cnt_M	_lgc[52]	0
CTCFailedBuf_Cnt_M	_lgc[53]	1
CTCFailedBuf_Cnt_M	_lgc[54]	1
CTCFailedBuf_Cnt_M	_lgc[55]	1
CTCFailedBuf_Cnt_M	_lgc[56]	1
CTCFailedBuf_Cnt_M	_lgc[57]	1.
CTCFailedBuf_Cnt_M	_lgc[58]	0
CTCFailedBuf_Cnt_M	Igc[59]	1
CTCFailedBuf_Cnt_M		0
CTCFailedBuf Cnt M		0
		1
CTCFailedBuf_Cnt_M		0
CTCFailedBuf_Cnt_M		0
CTCFailedBuf_Cnt_M		
CTCFailedBuf_Cnt_M		0
CTCFailed_Cnt_M_lgc	3	0
DTC		180560374
DTCKind		1
DTCStatusNew		13
DTCStatusOld		209
Dem_DTCNumberTab		182
Dem_DTCNumberTab	• •	221
Dem_DTCNumberTab	ple[2]	159
Dem_DTCNumberTab	ple[3]	164
Dem_DTCNumberTab	ple[4]	34
Dem_DTCNumberTab	ple[5]	166
Dem_DTCNumberTab	ple[6]	237
Dem_DTCNumberTab	ple[7]	237
Dem_DTCNumberTab	ple[8]	182
Dem_DTCNumberTab		221
Dem_DTCNumberTab		237
Dem_DTCNumberTab		123
Dem_DTCNumberTab		221
Dem_DTCNumberTab		237
_ 3D . 314d11156714b		182
Dem DTCNumherTah		221
Dem_DTCNumberTab		1441
Dem_DTCNumberTab		
Dem_DTCNumberTab	ole[16]	221
Dem_DTCNumberTab Dem_DTCNumberTab Dem_DTCNumberTab	ole[16] ole[17]	221 237
Dem_DTCNumberTab	ole[16] ole[17] ole[18]	221

## **TEST DETAILS REPORT** Ch n e

Demlf\_DTCS



Name	Input Value
Dem_DTCNumberTable[20]	221
Dem DTCNumberTable[21]	237
Dem_DTCNumberTable[22]	182
Dem_DTCNumberTable[23]	159
Dem DTCNumberTable[24]	164
Dem_DTCNumberTable[25]	34
	166
Dem_DTCNumberTable[26]	221
Dem_DTCNumberTable[27]	
Dem_DTCNumberTable[28]	182
Dem_DTCNumberTable[29]	221
Dem_DTCNumberTable[30]	182
Dem_DTCNumberTable[31]	182
Dem_DTCNumberTable[32]	221
Dem_DTCNumberTable[33]	221
Dem_DTCNumberTable[34]	182
Dem_DTCNumberTable[35]	221
Dem_DTCNumberTable[36]	182
Dem_DTCNumberTable[37]	182
Dem_DTCNumberTable[38]	182
Dem_DTCNumberTable[39]	221
Dem_DTCNumberTable[40]	221
Dem_DTCNumberTable[41]	159
Dem_DTCNumberTable[42]	164
Dem_DTCNumberTable[43]	34
Dem_DTCNumberTable[44]	166
Dem_DTCNumberTable[45]	237
Dem_DTCNumberTable[46]	182
Dem DTCNumberTable[47]	221
Dem_DTCNumberTable[48]	164
Dem_DTCNumberTable[49]	182
Dem_DTCNumberTable[50]	221
	182
Dem_DTCNumberTable[51]	
Dem_DTCNumberTable[52]	182
Dem_DTCNumberTable[53]	221
Dem_DTCNumberTable[54]	164
Dem_DTCNumberTable[55]	237
Dem_DTCNumberTable[56]	182
Dem_DTCNumberTable[57]	221
Dem_DTCNumberTable[58]	182
Dem_DTCNumberTable[59]	237
Dem_DTCNumberTable[60]	182
Dem_DTCNumberTable[61]	221
Dem_DTCNumberTable[62]	164
Dem_DTCNumberTable[63]	159
Dem_DTCNumberTable[64]	164
Dem_DTCNumberTable[65]	34
Dem_DTCNumberTable[66]	166
Dem_DTCNumberTable[67]	182
Dem_DTCNumberTable[68]	182
Dem_DTCNumberTable[69]	221
Dem_DTCNumberTable[70]	164
Dem_DTCNumberTable[71]	237
Dem_DTCNumberTable[72]	164
Dem DTCNumberTable[73]	159
Dem_DTCNumberTable[73] Dem_DTCNumberTable[74]	164
Dem_DTCNumberTable[74] Dem_DTCNumberTable[75]	34
Dem_DTC. FTP, Table[0]	166
Dem_DTC_FTB_Table[0]	252
Dem_DTC_FTB_Table[1]	122
Dem_DTC_FTB_Table[2]	173
Dem_DTC_FTB_Table[3]	253
Dem_DTC_FTB_Table[4]	78
Dem_DTC_FTB_Table[5]	251
Dem_DTC_FTB_Table[6]	172
Dem_DTC_FTB_Table[7]	172
Dem_DTC_FTB_Table[8]	252
Dem_DTC_FTB_Table[9]	122
Dem_DTC_FTB_Table[10]	172
Dem_DTC_FTB_Table[11]	225
Dem_DTC_FTB_Table[12]	122
Dem_DTC_FTB_Table[13]	172
Dem_DTC_FTB_Table[14]	252
Dem_DTC_FTB_Table[15]	122

2018-04-10, 18:44:44+0530



Bonni_B100 On n c			
Name	Input Value		
Dem_DTC_FTB_Table[16]	122		
Dem_DTC_FTB_Table[17]	172		
Dem_DTC_FTB_Table[18]	117		
Dem_DTC_FTB_Table[19]	252 122		
Dem_DTC_FTB_Table[20] Dem_DTC_FTB_Table[21]	172		
Dem_DTC_FTB_Table[22]	252		
Dem_DTC_FTB_Table[23]	173		
Dem_DTC_FTB_Table[24]	253		
Dem_DTC_FTB_Table[25]	78		
Dem_DTC_FTB_Table[26]	251		
Dem_DTC_FTB_Table[27]	122 252		
Dem_DTC_FTB_Table[28] Dem_DTC_FTB_Table[29]	122		
Dem_DTC_FTB_Table[30]	252		
Dem_DTC_FTB_Table[31]	252		
Dem_DTC_FTB_Table[32]	122		
Dem_DTC_FTB_Table[33]	122		
Dem_DTC_FTB_Table[34]	252		
Dem_DTC_FTB_Table[35]	122		
Dem_DTC_FTB_Table[36] Dem_DTC_FTB_Table[37]	252 252		
Dem_DTC_FTB_Table[38]	252		
Dem_DTC_FTB_Table[39]	122		
Dem_DTC_FTB_Table[40]	122		
Dem_DTC_FTB_Table[41]	173		
Dem_DTC_FTB_Table[42]	253		
Dem_DTC_FTB_Table[43]	78		
Dem_DTC_FTB_Table[44] Dem_DTC_FTB_Table[45]	251 172		
Dem_DTC_FTB_Table[46]	252		
Dem_DTC_FTB_Table[47]	122		
Dem_DTC_FTB_Table[48]	253		
Dem_DTC_FTB_Table[49]	252		
Dem_DTC_FTB_Table[50]	122		
Dem_DTC_FTB_Table[51] Dem_DTC_FTB_Table[52]	252 252		
Dem_DTC_FTB_Table[52]	122		
Dem_DTC_FTB_Table[54]	253		
Dem_DTC_FTB_Table[55]	172		
Dem_DTC_FTB_Table[56]	252		
Dem_DTC_FTB_Table[57]	122		
Dem_DTC_FTB_Table[58]	252		
Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60]	172 252		
Dem_DTC_FTB_Table[61]	122		
Dem_DTC_FTB_Table[62]	253		
Dem_DTC_FTB_Table[63]	173		
Dem_DTC_FTB_Table[64]	253		
Dem_DTC_FTB_Table[65]	78		
Dem_DTC_FTB_Table[66]	251		
Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68]	252 252		
Dem DTC FTB Table[69]	122		
Dem_DTC_FTB_Table[70]	253		
Dem_DTC_FTB_Table[71]	172		
Dem_DTC_FTB_Table[72]	253		
Dem_DTC_FTB_Table[73]	173		
Dem_DTC_FTB_Table[74]	253		
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]	78 251		
Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[0]	0	0	Kesuit
CTCFailedBuf_Cnt_M_lgc[1]	1	1	
CTCFailedBuf_Cnt_M_lgc[2]	1	1	-
CTCFailedBuf_Cnt_M_lgc[3]	0	0	•
CTCFailedBuf_Cnt_M_lgc[4]	1	1	~
CTCFailedBuf_Cnt_M_lgc[5]	1	1	
CTCFailedBuf_Cnt_M_lgc[6]	1	1	
CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8]	1	1	- J
CTCFailedBuf_Cnt_M_lgc[9]	1	1	
CTCFailedBuf_Cnt_M_lgc[10]	1	1	-
·			

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COTO-Belled On M pd 12  COTO-Belled On M pd 12  COTO-Belled On M pd 14  COTO-B	Name	Actual Value	Expected Value	Result
CICR-Seaded, One, Mage13 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1			•	
CICParlandid Cort, Myspeta		1	1	~
CICCHardball, Cott, M. 19979   1				
CICTORISIDED, COLM, 19(19)  CI				-
CICFanisella, Cim, Muject 19 CICFanisella, Ci				
CCT-Gradebid, Crit. M, 19219 1 1 1 1 CT-Gradebid, Crit. M, 19220 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0				
CFCSaccidati Cent M, 19678				~
CET-Based Cett M   9621   0		1	1	
COF Griedold Cot M 1922  O COF Griedold Cot M 1924  O COF Griedold Cot M 1			*	
CICFaleagud Call, M. 9623 1 1 1 1				
CICFaired Col. Col. N. 19624    1				
CICCRain-Bull, Cort, My, 19629				
CICFaiesBull, City, M. Jug28]	CTCFailedBuf_Cnt_M_lgc[25]	1	1	~
CICFailed Control   March   March   CICFailed Control   CICFailed   CICFailed Control   CICFailed   CICF				
CICFaleaded Cet. M. Jag-29    1				
CICFaledral, Cort, M. (pd.30)  1				
CCFCaledBuf Cnt M lpd33				
CCFGaledBut_CR, M_1gq349				~
CCFGaiedBuf, Crit, M. 1gq439  CTCFGaiedBuf, Crit, M. 1gq449  CTCFGaiedBuf, Crit, M. 1gq459  C	CTCFailedBuf_Cnt_M_lgc[32]	1	1	
CICFaledBuf, Crit, M. Jagd38]				
CICFalesbul, Cm, M, 19437  O O O O O O O O O O O O O O O O O O O				
CICFaiedBuf, Cnt, M, 19ct38				
CTCFaledBuf_Cnt_Migd59				
CICFailedful, Cit, M. Jog(43) CICFailedful, Cit, M. Jog(41) CICFailedful, Cit, M. Jog(41) CICFailedful, Cit, M. Jog(42) CICFailedful, Cit, M. Jog(43) CICFailedful, Cit, M. Jog(44) CICFailedful, Cit, M. Jog(44) CICFailedful, Cit, M. Jog(44) CICFailedful, Cit, M. Jog(45) CICFailedful, Cit, M. Jog(46) CICFailedful, Cit, M. Jog(47) CICFailedful, Cit, M. Jog(48) CICFailedful, Cit, M. Jog(48) CICFailedful, Cit, M. Jog(49) CICFailedful, Cit, M. Jog(50) CICFailedful, Cit, M. Jog(51) CICFailedful, Cit, M. Jog(61) CICFailedful, Cit, M. Jog(61) CICFailedful, Cit, M. Jog(62) CICFailedful, Cit, M. Jog(63) CICFailedful, Cit, M. Jog(64) CICFailedful, Cit, M. Jog(64) CICFailedful, Cit, M. Jog(67) CICFailedful, Cit, M. Jog(64) CICFailedful, Cit, M. Jog(64) CICFai				
CTCFailedBuf_Cnt_M_lgct41  CTCFailedBuf_Cnt_M_lgct42  CTCFailedBuf_Cnt_M_lgct43  CTCFailedBuf_Cnt_M_lgct44  CTCFailedBuf_Cnt_M_lgct45  CTCFailedBuf_Cnt_M_lgct45  CTCFailedBuf_Cnt_M_lgct47  CTCFailedBuf_Cnt_M_lgct47  CTCFailedBuf_Cnt_M_lgct47  CTCFailedBuf_Cnt_M_lgct48  CTCFailedBuf_Cnt_M_lgct49  CTCFailedBuf_Cnt_M_lgct51  CTCFailedBuf_Cnt_M_lgct61  CTCFailedBuf_Cnt_M_lgct71  O O O O O O O O O O O O O O O O O O O		0	0	~
CTCFailedBuf, Cnt, M, Jgc(42)  CTCFailedBuf, Cnt, M, Jgc(44)  CTCFailedBuf, Cnt, M, Jgc(45)  CTCFailedBuf, Cnt, M, Jgc(46)  CTCFailedBuf, Cnt, M, Jgc(46)  CTCFailedBuf, Cnt, M, Jgc(47)  CTCFailedBuf, Cnt, M, Jgc(48)  CTCFailedBuf, Cnt, M, Jgc(49)  CTCFailedBuf, Cnt, M, Jgc(49)  CTCFailedBuf, Cnt, M, Jgc(50)  CTCFailedBuf, Cnt, M, Jgc(50)  CTCFailedBuf, Cnt, M, Jgc(50)  CTCFailedBuf, Cnt, M, Jgc(50)  CTCFailedBuf, Cnt, M, Jgc(53)  CTCFailedBuf, Cnt, M, Jgc(53)  CTCFailedBuf, Cnt, M, Jgc(53)  CTCFailedBuf, Cnt, M, Jgc(58)	CTCFailedBuf_Cnt_M_lgc[40]			
CTCFailedBuf_Cnt_M_lgc[43]  O O O O O O O O O O O O O O O O O O O				
CTCFailedBuf_Cnt_M_lgc[44]  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0				
CTCFaiedBuf_Cnt_M_lgc[45]				
CTCFalledBuf_Cnt_M_lgc[46] CTCFalledBuf_Cnt_M_lgc[47] O O O O O CTCFalledBuf_Cnt_M_lgc[48] O O O O O CTCFalledBuf_Cnt_M_lgc[48] O O O O O O O O O O O O O O O O O O O				•
CTCFailedBuf_Cnt_M_lgc[48]  1 1 1 1 1		0	0	
CTCFaledBuf_Cnf_M_lgcj49         1         1         V           CTCFaledBuf_Cnf_M_lgcj50         0         0         V           CTCFaledBuf_Cnf_M_lgcj51         0         0         V           CTCFaledBuf_Cnf_M_lgcj52         0         0         V           CTCFaledBuf_Cnf_M_lgcj53         1         1         1         V           CTCFaledBuf_Cnf_M_lgcj54         1         1         1         V         CTCFaledBuf_Cnf_M_lgcj55         1         1         1         V         CTCFaledBuf_Cnf_M_lgcj55         1         1         1         V         CTCFaledBuf_Cnf_M_lgcj57         1         1         1         V         CTCFaledBuf_Cnf_M_lgcj57         1         1         1         V         CTCFaledBuf_Cnf_M_lgcj58         0         0         0         V         CTCFaledBuf_Cnf_M_lgcj69         1         1         1         V         CTCFaledBuf_Cnf_M_lgcj60         1         1         1         V         CTCFaledBuf_Cnf_M_lgcj60         1         1         1         V         CTCFaledBuf_Cnf_M_lgcj63         1         1         1         V         CTCFaledBuf_Cnf_M_lgcj63         1         1         1         V         CTCFaledBuf_Cnf_M_lgcj63         0         0         V         CTCFaledBuf_Cnf_M				
CTCFailedBuf_Cnt_M_lgd[51]         0         0         0           CTCFailedBuf_Cnt_M_lgd[52]         0         0         0           CTCFailedBuf_Cnt_M_lgd[52]         0         0         0           CTCFailedBuf_Cnt_M_lgd[53]         1         1         1           CTCFailedBuf_Cnt_M_lgd[55]         1         1         1           CTCFailedBuf_Cnt_M_lgd[56]         1         1         1           CTCFailedBuf_Cnt_M_lgd[58]         1         1         1           CTCFailedBuf_Cnt_M_lgd[58]         1         1         1           CTCFailedBuf_Cnt_M_lgd[58]         1         1         1           CTCFailedBuf_Cnt_M_lgd[59]         1         1         1           CTCFailedBuf_Cnt_M_lgd[69]         1         1         1           CTCFailedBuf_Cnt_M_lgd[61]         1         1         1           CTCFailedBuf_Cnt_M_lgd[62]         1         1         1           CTCFailedBuf_Cnt_M_lgd[63]         1         1         1           CTCFailedBuf_Cnt_M_lgd[64]         1         1         1           CTCFailedBuf_Cnt_M_lgd[65]         0         0         0           CTCFailedBuf_Cnt_M_lgd[67]         0         0         0				-
CTCFailedBuf_Cnl_M]gc[51]         0         0         0           CTCFailedBuf_Cnl_M]gc[52]         0         0         0           CTCFailedBuf_Cnl_M]gc[53]         1         1         1           CTCFailedBuf_Cnl_M]gc[54]         1         1         1           CTCFailedBuf_Cnl_M]gc[56]         1         1         1           CTCFailedBuf_Cnl_M]gc[57]         1         1         1           CTCFailedBuf_Cnl_M]gc[58]         0         0         0           CTCFailedBuf_Cnl_M]gc[58]         1         1         1           CTCFailedBuf_Cnl_M]gc[69]         1         1         1           CTCFailedBuf_Cnl_M]gc[60]         1         1         1           CTCFailedBuf_Cnl_M]gc[61]         1         1         1           CTCFailedBuf_Cnl_M]gc[63]         1         1         1           CTCFailedBuf_Cnl_M_[gc[63]         1         1         1           CTCFailedBuf_Cnl_M_[gc[64]         1         1         1           CTCFailedBuf_Cnl_M_[gc[65]         0         0         0           CTCFailedBuf_Cnl_M_[gc[66]         0         0         0           CTCFailedBuf_Cnl_M_[gc[67]         0         0         0				
CTCFailedBuf_Cnt_M_lgc[52]         0         0         V           CTCFailedBuf_Cnt_M_lgc[53]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[54]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[55]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[57]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[58]         0         0         0         V           CTCFailedBuf_Cnt_M_lgc[58]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[69]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[60]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[62]         1         1         1         V         CTCFailedBuf_Cnt_M_lgc[62]         1         1         1         V         CTCFailedBuf_Cnt_M_lgc[63]         1         1         1         V         CTCFailedBuf_Cnt_M_lgc[64]         1         1         1         V         CTCFailedBuf_Cnt_M_lgc[65]         0         0         0         V         CTCFailedBuf_Cnt_M_lgc[67]         0         0         V         CTCFailedBuf_Cnt_M_lgc[67]         0         0         V				
CTCFailedBuf_Cnt_M_lgc[54]         1         1         1           CTCFailedBuf_Cnt_M_lgc[56]         1         1         1           CTCFailedBuf_Cnt_M_lgc[56]         1         1         2           CTCFailedBuf_Cnt_M_lgc[57]         1         1         1           CTCFailedBuf_Cnt_M_lgc[58]         0         0         0           CTCFailedBuf_Cnt_M_lgc[60]         1         1         1           CTCFailedBuf_Cnt_M_lgc[61]         1         1         2           CTCFailedBuf_Cnt_M_lgc[62]         1         1         1         2           CTCFailedBuf_Cnt_M_lgc[62]         1         1         1         2         4         1         1         2         4         1         1         2         4         1         1         2         4         1         1         2         4         1         1         2         4         1         1         2         4         1         1         2         4         1         1         2         4         1         1         2         4         1         2         4         1         2         4         4         4         4         4         4         4			0	•
CTCFailedBuf_Cnt_M_lgc[55]         1         1         4           CTCFailedBuf_Cnt_M_lgc[57]         1         1         4           CTCFailedBuf_Cnt_M_lgc[58]         0         0         0           CTCFailedBuf_Cnt_M_lgc[58]         0         0         0           CTCFailedBuf_Cnt_M_lgc[69]         1         1         1           CTCFailedBuf_Cnt_M_lgc[61]         1         1         1           CTCFailedBuf_Cnt_M_lgc[62]         1         1         1           CTCFailedBuf_Cnt_M_lgc[63]         1         1         1           CTCFailedBuf_Cnt_M_lgc[63]         1         1         1           CTCFailedBuf_Cnt_M_lgc[65]         0         0         0           CTCFailedBuf_Cnt_M_lgc[66]         0         0         0           CTCFailedBuf_Cnt_M_lgc[67]         0         0         0           CTCFailedBuf_Cnt_M_lgc[69]         0         0         0				
CTCFailedBuf_Cnt_M_lgc[56]         1         1         1         4           CTCFailedBuf_Cnt_M_lgc[57]         1         1         1         2           CTCFailedBuf_Cnt_M_lgc[58]         0         0         0         2           CTCFailedBuf_Cnt_M_lgc[69]         1         1         1         2           CTCFailedBuf_Cnt_M_lgc[60]         1         1         1         2           CTCFailedBuf_Cnt_M_lgc[61]         1         1         1         2           CTCFailedBuf_Cnt_M_lgc[62]         1         1         1         4         2           CTCFailedBuf_Cnt_M_lgc[63]         1         1         1         4 <td< td=""><td></td><td></td><td></td><td>~</td></td<>				~
CTCFailedBuf_Cnt_M_lgc[57]         1         1         •           CTCFailedBuf_Cnt_M_lgc[58]         0         0         •           CTCFailedBuf_Cnt_M_lgc[60]         1         1         •           CTCFailedBuf_Cnt_M_lgc[61]         1         1         •           CTCFailedBuf_Cnt_M_lgc[62]         1         1         •           CTCFailedBuf_Cnt_M_lgc[63]         1         1         •           CTCFailedBuf_Cnt_M_lgc[64]         1         1         •           CTCFailedBuf_Cnt_M_lgc[65]         0         0         •           CTCFailedBuf_Cnt_M_lgc[66]         0         0         •           CTCFailedBuf_Cnt_M_lgc[67]         0         0         •           CTCFailedBuf_Cnt_M_lgc[68]         0         0         •           CTCFailedBuf_Cnt_M_lgc[68]         0         0         •           CTCFailedBuf_Cnt_M_lgc[68]         0         0         •           CTCFailedBuf_Cnt_M_lgc[68]         0         0         •           CTCFailedBuf_Cnt_M_lgc[70]         1         1         1         •           CTCFailedBuf_Cnt_M_lgc[71]         0         0         •           CTCFailedBuf_Cnt_M_lgc[73]         0         0         •<				-
CTCFailedBuf_Cnt_M_lgc[58]         0         0         ✓           CTCFailedBuf_Cnt_M_lgc[59]         1         1         1         ✓           CTCFailedBuf_Cnt_M_lgc[60]         1         1         1         ✓           CTCFailedBuf_Cnt_M_lgc[61]         1         1         1         ✓           CTCFailedBuf_Cnt_M_lgc[62]         1         1         1         ✓           CTCFailedBuf_Cnt_M_lgc[63]         1         1         1         ✓           CTCFailedBuf_Cnt_M_lgc[64]         1         1         ✓         ✓           CTCFailedBuf_Cnt_M_lgc[65]         0         0         0         ✓ <td< td=""><td></td><td></td><td></td><td>-</td></td<>				-
CTCFailedBuf_Cnt_M_lgc[61]       1       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1       1         CTCFailedBuf_Cnt_M_lgc[63]       0       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0       0         CTCFailedBuf_Cnt_M_lgc[68]       0       0       0         CTCFailedBuf_Cnt_M_lgc[69]       0       0       0         CTCFailedBuf_Cnt_M_lgc[70]       1       1       1         CTCFailedBuf_Cnt_M_lgc[71]       0       0       0         CTCFailedBuf_Cnt_M_lgc[72]       0       0       0         CTCFailedBuf_Cnt_M_lgc[73]       0       0       0         CTCFailedBuf_Cnt_M_lgc[74]       0       0       0         CTCFailedBuf_Cnt_M_lgc[75]       0       0       0         CTCFailedBuf_Cnt_M_lgc[76]       0       0       0         CTCFailedBuf_Cnt_M_lgc[76]       0       0       0         CTCFailedBuf_Cnt_M_lgc[76]       0       0       0 <td< td=""><td></td><td></td><td></td><td>~</td></td<>				~
CTCFailedBut_Cnt_M_lgc[61]         1         1         4           CTCFailedBuf_Cnt_M_lgc[62]         1         1         4           CTCFailedBuf_Cnt_M_lgc[63]         1         1         1           CTCFailedBuf_Cnt_M_lgc[63]         1         1         1           CTCFailedBuf_Cnt_M_lgc[65]         0         0         0           CTCFailedBuf_Cnt_M_lgc[66]         0         0         0           CTCFailedBuf_Cnt_M_lgc[67]         0         0         0           CTCFailedBuf_Cnt_M_lgc[68]         0         0         0           CTCFailedBuf_Cnt_M_lgc[69]         0         0         0           CTCFailedBuf_Cnt_M_lgc[70]         1         1         1           CTCFailedBuf_Cnt_M_lgc[71]         0         0         0           CTCFailedBuf_Cnt_M_lgc[73]         0         0         0           CTCFailedBuf_Cnt_M_lgc[74]         0         0         0           CTCFailedBuf_Cnt_M_lgc[75]         0         0         0           CTCFailedBuf_Cnt_M_lgc[76]         0         0         0           CTCFailedBuf_Cnt_M_lgc[76]         0         0         0           CTCFailedBuf_Cnt_M_lgc[76]         0         0         0			1	~
CTCFailedBuf_Cnt_M_lgc[62]       1       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1       4         CTCFailedBuf_Cnt_M_lgc[65]       0       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0       0         CTCFailedBuf_Cnt_M_lgc[68]       0       0       0         CTCFailedBuf_Cnt_M_lgc[70]       1       1       1         CTCFailedBuf_Cnt_M_lgc[71]       0       0       0         CTCFailedBuf_Cnt_M_lgc[72]       0       0       0         CTCFailedBuf_Cnt_M_lgc[73]       0       0       0         CTCFailedBuf_Cnt_M_lgc[74]       0       0       0         CTCFailedBuf_Cnt_M_lgc[75]       0       0       0         CTCFailedBuf_Cnt_M_lgc[76]       0       0       0 <td< td=""><td></td><td></td><td></td><td></td></td<>				
CTCFailedBuf_Cnt_M_lgc[63]       1       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1       1         CTCFailedBuf_Cnt_M_lgc[65]       0       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0       0         CTCFailedBuf_Cnt_M_lgc[68]       0       0       0         CTCFailedBuf_Cnt_M_lgc[70]       1       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1       1       4         CTCFailedBuf_Cnt_M_lgc[71]       0       0       0       0         CTCFailedBuf_Cnt_M_lgc[72]       0       0       0       0         CTCFailedBuf_Cnt_M_lgc[73]       0       0       0       0         CTCFailedBuf_Cnt_M_lgc[74]       0       0       0       0         CTCFailedBuf_Cnt_M_lgc[75]       0       0       0       0         CTCFailedBuf_Cnt_M_lgc[76]       0       0       0       0         CTCFailedBuf_Cnt_M_lgc       0       0       0       0         CTCFailedBuf_Cnt_M_lgc       0       0       0       0         CTCFailedBuf_Cnt_M_lgc       0       0       0				
CTCFailedBuf_Cnt_M_lgc[64]       1       1       4         CTCFailedBuf_Cnt_M_lgc[65]       0       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0       0         CTCFailedBuf_Cnt_M_lgc[68]       0       0       0         CTCFailedBuf_Cnt_M_lgc[69]       0       0       0         CTCFailedBuf_Cnt_M_lgc[70]       1       1       1         CTCFailedBuf_Cnt_M_lgc[71]       0       0       0         CTCFailedBuf_Cnt_M_lgc[72]       0       0       0         CTCFailedBuf_Cnt_M_lgc[73]       0       0       0         CTCFailedBuf_Cnt_M_lgc[74]       0       0       0         CTCFailedBuf_Cnt_M_lgc[75]       0       0       0         CTCFailedBuf_Cnt_M_lgc[76]       0       0       0         CTCFailed_Cnt_M_lgc       0       0       0         CTCFailed_Cnt_M_lgc       0       0       0         CTCFailed_Cnt_M_lgc       0       0       0         CTCFailed_Cnt_M_lgc       0       0       0				
CTCFailedBuf_Cnt_M_lgc[65]       0       0       •         CTCFailedBuf_Cnt_M_lgc[66]       0       0       •         CTCFailedBuf_Cnt_M_lgc[67]       0       0       •         CTCFailedBuf_Cnt_M_lgc[68]       0       0       •         CTCFailedBuf_Cnt_M_lgc[69]       0       0       •         CTCFailedBuf_Cnt_M_lgc[70]       1       1       1       •         CTCFailedBuf_Cnt_M_lgc[71]       0       0       •       •         CTCFailedBuf_Cnt_M_lgc[72]       0       0       •       •         CTCFailedBuf_Cnt_M_lgc[73]       0       0       •       •         CTCFailedBuf_Cnt_M_lgc[74]       0       0       •       •         CTCFailedBuf_Cnt_M_lgc[75]       0       0       •       •         CTCFailedBuf_Cnt_M_lgc[76]       0       0       •       •         CTCFailed_Cnt_M_lgc       0       0       •       •         Demif_DTCStatusChanged()       0       0       •       •				
CTCFailedBuf_Cnt_M_lgc[67]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[68]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[69]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[70]       1       1       1       ✓         CTCFailedBuf_Cnt_M_lgc[71]       0       0       ✓       ✓         CTCFailedBuf_Cnt_M_lgc[72]       0       0       ✓       ✓         CTCFailedBuf_Cnt_M_lgc[73]       0       0       ✓       ✓         CTCFailedBuf_Cnt_M_lgc[74]       0       0       ✓       ✓         CTCFailedBuf_Cnt_M_lgc[75]       0       0       ✓       ✓         CTCFailedBuf_Cnt_M_lgc[76]       0       0       ✓       ✓         CTCFailed_Cnt_M_lgc       0       0       ✓       ✓         Demlf_DTCStatusChanged()       0       0       ✓       ✓			0	~
CTCFailedBuf_Cnt_M_lgc[68]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[69]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[70]       1       1       1         CTCFailedBuf_Cnt_M_lgc[71]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[72]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[73]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[74]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[75]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[76]       0       0       ✓         CTCFailed_Cnt_M_lgc       0       0       ✓         Demlf_DTCStatusChanged()       0       0       ✓				
CTCFailedBuf_Cnt_M_lgc[69]       0       0         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       0       0         CTCFailedBuf_Cnt_M_lgc[72]       0       0         CTCFailedBuf_Cnt_M_lgc[73]       0       0         CTCFailedBuf_Cnt_M_lgc[74]       0       0         CTCFailedBuf_Cnt_M_lgc[75]       0       0         CTCFailedBuf_Cnt_M_lgc[76]       0       0         CTCFailed_Cnt_M_lgc       0       0         Demlf_DTCStatusChanged()       0       0				
CTCFailedBuf_Cnt_M_lgc[70]       1       1          CTCFailedBuf_Cnt_M_lgc[71]       0       0          CTCFailedBuf_Cnt_M_lgc[72]       0       0          CTCFailedBuf_Cnt_M_lgc[73]       0       0          CTCFailedBuf_Cnt_M_lgc[74]       0       0          CTCFailedBuf_Cnt_M_lgc[75]       0       0          CTCFailedBuf_Cnt_M_lgc[76]       0       0          CTCFailed_Cnt_M_lgc       0       0          Demlf_DTCStatusChanged()       0       0				
CTCFailedBuf_Cnt_M_lgc[71]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[72]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[73]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[74]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[75]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[76]       0       0       ✓         CTCFailed_Cnt_M_lgc       0       0       ✓         Demlf_DTCStatusChanged()       0       0       ✓				
CTCFailedBuf_Cnt_M_lgc[72]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[73]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[74]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[75]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[76]       0       0       ✓         CTCFailed_Cnt_M_lgc       0       0       ✓         Demlf_DTCStatusChanged()       0       0       ✓				
CTCFailedBuf_Cnt_M_lgc[73]       0       0         CTCFailedBuf_Cnt_M_lgc[74]       0       0         CTCFailedBuf_Cnt_M_lgc[75]       0       0         CTCFailedBuf_Cnt_M_lgc[76]       0       0         CTCFailed_Cnt_M_lgc       0       0         Demlf_DTCStatusChanged()       0       0			0	
CTCFailedBuf_Cnt_M_lgc[75]         0         0         ✓           CTCFailedBuf_Cnt_M_lgc[76]         0         0         ✓           CTCFailed_Cnt_M_lgc         0         0         ✓           Demlf_DTCStatusChanged()         0         0         ✓				
CTCFailedBuf_Cnt_M_lgc[76]         0         0         ✓           CTCFailed_Cnt_M_lgc         0         0         ✓           Demlf_DTCStatusChanged()         0         0         ✓				
CTCFailed_Cnt_M_lgc         0         0         ✓           Demlf_DTCStatusChanged()         0         0         ✓				
Demlf_DTCStatusChanged() 0				
	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	0	0	~

Demlf\_DTCS



Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte Write An Demlf CTCFailed Cnt loc	1	Rte Write An Demlf CTCFailed Cnt loc	1	_

Test Step 2.14 (Repeat Count = 1)	V
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	0
CTCFailedBuf_Cnt_M_Igc[1]	0
CTCFailedBuf_Cnt_M_lgc[2]	0
CTCFailedBuf_Cnt_M_lgc[3]	0
CTCFailedBuf_Cnt_M_lgc[4]	0
CTCFailedBuf_Cnt_M_lgc[5]	0
CTCFailedBuf_Cnt_M_lgc[6]	0
CTCFailedBuf_Cnt_M_lgc[7]	0
CTCFailedBuf_Cnt_M_lgc[8]	0
CTCFailedBuf_Cnt_M_Igc[9] CTCFailedBuf_Cnt_M_Igc[10]	0
CTCFailedBuf_Cnt_M_lgc[10]	0
CTCFailedBuf_Cnt_M_lgc[12]	0
CTCFailedBuf_Cnt_M_lgc[13]	0
CTCFailedBuf_Cnt_M_lgc[14]	0
CTCFailedBuf_Cnt_M_lgc[15]	0
CTCFailedBuf_Cnt_M_lgc[16]	0
CTCFailedBuf_Cnt_M_lgc[17]	0
CTCFailedBuf_Cnt_M_lgc[18]	0
CTCFailedBuf_Cnt_M_lgc[19]	0
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	0
CTCFailedBuf_Cnt_M_lgc[24]	0
CTCFailedBuf_Cnt_M_lgc[25]	0
CTCFailedBuf_Cnt_M_lgc[26]	0
CTCFailedBuf_Cnt_M_lgc[27]	0
CTCFailedBuf_Cnt_M_lgc[28]	0
CTCFailedBuf_Cnt_M_Igc[29]	0
CTCFailedBuf_Cnt_M_lgc[30]	0
CTCFailedBuf_Cnt_M_lgc[31]	0
CTCFailedBuf_Cnt_M_lgc[32]	0
CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_Igc[44] CTCFailedBuf_Cnt_M_Igc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	0
CTCFailedBuf_Cnt_M_lgc[54]	0
CTCFailedBuf_Cnt_M_lgc[55]	0
CTCFailedBuf_Cnt_M_lgc[56]	0
CTCFailedBuf_Cnt_M_lgc[57] CTCFailedBuf_Cnt_M_lgc[58]	0
CTCFailedBuf_Cnt_M_lgc[59]	0
CTCFailedBuf_Cnt_M_lgc[60]	0
CTCFailedBuf_Cnt_M_lgc[61]	0
CTCFailedBuf_Cnt_M_lgc[62]	0
CTCFailedBuf_Cnt_M_lgc[63]	0

Demlf\_DTCS

2018-04-10, 18:44:44+0530



Input Value CTCFailedBuf\_Cnt\_M\_lgc[64] 0 CTCFailedBuf\_Cnt\_M\_lgc[65] 0 CTCFailedBuf\_Cnt\_M\_lgc[66] 0 CTCFailedBuf\_Cnt\_M\_lgc[67] 0 CTCFailedBuf Cnt M lqc[68] 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 CTCFailedBuf\_Cnt\_M\_lgc[73] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[74] CTCFailedBuf\_Cnt\_M\_lgc[75] 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 CTCFailed\_Cnt\_M\_lgc 1 DTC 2534667367 DTCKind 2 DTCStatusNew 240 DTCStatusOld 62 Dem\_DTCNumberTable[0] 99 Dem\_DTCNumberTable[1] 143 Dem\_DTCNumberTable[2] 36 Dem\_DTCNumberTable[3] 85 Dem\_DTCNumberTable[4] 238 Dem\_DTCNumberTable[5] 62 Dem\_DTCNumberTable[6] 217 Dem\_DTCNumberTable[7] 217 Dem DTCNumberTable[8] 99 Dem\_DTCNumberTable[9] 143 Dem DTCNumberTable[10] 217 Dem\_DTCNumberTable[11] 101 Dem DTCNumberTable[12] 143 Dem\_DTCNumberTable[13] 217 Dem DTCNumberTable[14] 99 Dem\_DTCNumberTable[15] 143 Dem\_DTCNumberTable[16] 143 Dem\_DTCNumberTable[17] 217 Dem\_DTCNumberTable[18] 236 Dem\_DTCNumberTable[19] 99 Dem\_DTCNumberTable[20] 143 Dem\_DTCNumberTable[21] 217 Dem\_DTCNumberTable[22] 99 36 Dem\_DTCNumberTable[23] Dem\_DTCNumberTable[24] 85 Dem\_DTCNumberTable[25] 238 Dem\_DTCNumberTable[26] 62 Dem\_DTCNumberTable[27] 143 Dem\_DTCNumberTable[28] 99 Dem\_DTCNumberTable[29] 143 Dem DTCNumberTable[30] 99 Dem\_DTCNumberTable[31] 99 Dem DTCNumberTable[32] 143 Dem\_DTCNumberTable[33] 143 Dem\_DTCNumberTable[34] 99 Dem\_DTCNumberTable[35] 143 Dem\_DTCNumberTable[36] 99 Dem\_DTCNumberTable[37] 99 Dem\_DTCNumberTable[38] 99 Dem\_DTCNumberTable[39] 143 Dem\_DTCNumberTable[40] 143 36 Dem\_DTCNumberTable[41] Dem\_DTCNumberTable[42] 85 Dem\_DTCNumberTable[43] 238 Dem\_DTCNumberTable[44] 62 Dem\_DTCNumberTable[45] 217 Dem\_DTCNumberTable[46] 99 Dem DTCNumberTable[47] 143 Dem\_DTCNumberTable[48] 85 Dem DTCNumberTable[49] 99 Dem\_DTCNumberTable[50] 143 Dem\_DTCNumberTable[51] 99 Dem DTCNumberTable[52] 99 Dem\_DTCNumberTable[53] 143 Dem\_DTCNumberTable[54] 85

2018-04-10, 18:44:44+0530



Demii_DTC3 Cit ii e	TOPO (MV
Name	Input Value
Dem_DTCNumberTable[55]	217
Dem_DTCNumberTable[56]	99
Dem_DTCNumberTable[57]	143
Dem_DTCNumberTable[58]	99
Dem_DTCNumberTable[59]	217
Dem_DTCNumberTable[60]	99
Dem_DTCNumberTable[61]	143
Dem_DTCNumberTable[62]	85
Dem_DTCNumberTable[63]	36
Dem_DTCNumberTable[64]	85
Dem_DTCNumberTable[65]	238
Dem_DTCNumberTable[66]	62
Dem_DTCNumberTable[67]	99
Dem_DTCNumberTable[68]	99
Dem_DTCNumberTable[69]	143
Dem_DTCNumberTable[70]	85 217
Dem_DTCNumberTable[71]	
Dem_DTCNumberTable[72] Dem_DTCNumberTable[73]	85 36
Dem DTCNumberTable[74]	85
Dem_DTCNumberTable[74] Dem_DTCNumberTable[75]	238
Dem_DTCNumberTable[75] Dem_DTCNumberTable[76]	62
Dem_DTC_FTB_Table[0]	67
Dem DTC FTB Table[1]	177
Dem DTC FTB Table[2]	247
Dem_DTC_FTB_Table[3]	156
Dem_DTC_FTB_Table[4]	178
Dem_DTC_FTB_Table[5]	171
Dem_DTC_FTB_Table[6]	176
Dem_DTC_FTB_Table[7]	176
Dem_DTC_FTB_Table[8]	67
Dem_DTC_FTB_Table[9]	177
Dem_DTC_FTB_Table[10]	176
Dem_DTC_FTB_Table[11]	116
Dem_DTC_FTB_Table[12]	177
Dem_DTC_FTB_Table[13]	176
Dem_DTC_FTB_Table[14]	67
Dem_DTC_FTB_Table[15]	177
Dem_DTC_FTB_Table[16]	177
Dem_DTC_FTB_Table[17]	176
Dem_DTC_FTB_Table[18]	171
Dem_DTC_FTB_Table[19]	67
Dem_DTC_FTB_Table[20]	177
Dem_DTC_FTB_Table[21] Dem_DTC_FTB_Table[22]	176
Dem_DTC_FTB_Table[22]	67 247
Dem_DTC_FTB_Table[23]	156
Dem_DTC_FTB_Table[24]	178
Dem_DTC_FTB_Table[26]	171
Dem_DTC_FTB_Table[27]	177
Dem DTC FTB Table[28]	67
Dem_DTC_FTB_Table[29]	177
Dem_DTC_FTB_Table[30]	67
Dem_DTC_FTB_Table[31]	67
Dem_DTC_FTB_Table[32]	177
Dem_DTC_FTB_Table[33]	177
Dem_DTC_FTB_Table[34]	67
Dem_DTC_FTB_Table[35]	177
Dem_DTC_FTB_Table[36]	67
Dem_DTC_FTB_Table[37]	67
Dem_DTC_FTB_Table[38]	67
Dem_DTC_FTB_Table[39]	177
Dem_DTC_FTB_Table[40]	177
Dem_DTC_FTB_Table[41]	247
Dem_DTC_FTB_Table[42]	156
Dem_DTC_FTB_Table[43]	178
Dem_DTC_FTB_Table[44]	171
Dem_DTC_FTB_Table[45]	
	176
Dem_DTC_FTB_Table[46]	176 67
Dem_DTC_FTB_Table[46] Dem_DTC_FTB_Table[47]	176 67 177
Dem_DTC_FTB_Table[46] Dem_DTC_FTB_Table[47] Dem_DTC_FTB_Table[48]	176 67 177 156
Dem_DTC_FTB_Table[46] Dem_DTC_FTB_Table[47]	176 67 177

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value Dem\_DTC\_FTB\_Table[51] 67 Dem\_DTC\_FTB\_Table[52] 67 Dem DTC\_FTB\_Table[53] 177 Dem\_DTC\_FTB\_Table[54] 156 Dem\_DTC\_FTB\_Table[55] 176 Dem\_DTC\_FTB\_Table[56] 67 Dem\_DTC\_FTB\_Table[57] 177 Dem\_DTC\_FTB\_Table[58] 67 Dem\_DTC\_FTB\_Table[59] 176 Dem\_DTC\_FTB\_Table[60] 67 Dem\_DTC\_FTB\_Table[61] 177 Dem\_DTC\_FTB\_Table[62] 156 247 Dem\_DTC\_FTB\_Table[63] Dem\_DTC\_FTB\_Table[64] 156 Dem\_DTC\_FTB\_Table[65] 178 Dem DTC FTB Table[66] 171 Dem\_DTC\_FTB\_Table[67] 67 Dem\_DTC\_FTB\_Table[68] 67 Dem\_DTC\_FTB\_Table[69] 177 Dem\_DTC\_FTB\_Table[70] 156 Dem\_DTC\_FTB\_Table[71] 176 Dem\_DTC\_FTB\_Table[72] 156 Dem\_DTC\_FTB\_Table[73] 247 Dem\_DTC\_FTB\_Table[74] 156 Dem\_DTC\_FTB\_Table[75] 178 Dem\_DTC\_FTB\_Table[76] 171 Name **Actual Value Expected Value** Result CTCFailedBuf Cnt M Igc[0] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[1] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[2] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[3] 0 0 CTCFailedBuf Cnt M lgc[4] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[5] 0 0 CTCFailedBuf Cnt M Igc[6] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[7] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[8] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[9] 0 0 0 0 CTCFailedBuf\_Cnt\_M\_lgc[10] CTCFailedBuf\_Cnt\_M\_lgc[11] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[12] 0 0 CTCFailedBuf Cnt M lqc[13] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[14] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[15] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[16] 0 0 **~** CTCFailedBuf\_Cnt\_M\_lgc[17] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[18] n n CTCFailedBuf\_Cnt\_M\_lgc[19] 0 0 ~ CTCFailedBuf\_Cnt\_M\_lgc[20] n 0 CTCFailedBuf\_Cnt\_M\_lgc[21] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[22] n 0 CTCFailedBuf\_Cnt\_M\_lgc[23] 0 0 CTCFailedBuf Cnt M Igc[24] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[25] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[26] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[27] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[28] 0 0  $CTCFailedBuf\_Cnt\_M\_lgc[29]$ 0 0 CTCFailedBuf\_Cnt\_M\_lgc[30] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[31] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[32] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[33] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[34] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[35] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[36] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[37] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[38] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[39] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[40] 0 0 CTCFailedBuf Cnt M Igc[41] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[42] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[43] 0 0 ~ CTCFailedBuf\_Cnt\_M\_lgc[44] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[45] 0 0

Rte\_Write\_Ap\_DemIf\_CTCFailed\_Cnt\_lgc(data)

Demlf\_DTCS

2018-04-10, 18:44:44+0530



**Actual Value Expected Value** CTCFailedBuf\_Cnt\_M\_lgc[46] CTCFailedBuf\_Cnt\_M\_lgc[47] CTCFailedBuf\_Cnt\_M\_lgc[48] CTCFailedBuf\_Cnt\_M\_lgc[49] CTCFailedBuf\_Cnt\_M\_lgc[50] CTCFailedBuf\_Cnt\_M\_lgc[51] CTCFailedBuf\_Cnt\_M\_lgc[52] CTCFailedBuf\_Cnt\_M\_lgc[53] CTCFailedBuf\_Cnt\_M\_lgc[54] CTCFailedBuf\_Cnt\_M\_lgc[55] CTCFailedBuf\_Cnt\_M\_lgc[56] CTCFailedBuf\_Cnt\_M\_lgc[57] CTCFailedBuf\_Cnt\_M\_lgc[58] CTCFailedBuf\_Cnt\_M\_lgc[59] CTCFailedBuf\_Cnt\_M\_lgc[60] CTCFailedBuf\_Cnt\_M\_lgc[61] CTCFailedBuf\_Cnt\_M\_lgc[62] CTCFailedBuf\_Cnt\_M\_lgc[63]  $CTCFailedBuf\_Cnt\_M\_lgc[64]$ CTCFailedBuf\_Cnt\_M\_lgc[65] CTCFailedBuf\_Cnt\_M\_lgc[66] CTCFailedBuf\_Cnt\_M\_lgc[67]  $CTCFailedBuf\_Cnt\_M\_lgc[68]$ CTCFailedBuf\_Cnt\_M\_lgc[69] CTCFailedBuf\_Cnt\_M\_lgc[70] CTCFailedBuf\_Cnt\_M\_lgc[71] CTCFailedBuf\_Cnt\_M\_lgc[72] CTCFailedBuf\_Cnt\_M\_lgc[73] CTCFailedBuf\_Cnt\_M\_lgc[74] CTCFailedBuf\_Cnt\_M\_lgc[75] CTCFailedBuf\_Cnt\_M\_lgc[76] CTCFailed\_Cnt\_M\_lgc Demlf DTCStatusChanged() 

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte Write Ap Demlf CTCFailed Cnt lgc	1	Rte Write Ap Demlf CTCFailed Cnt lgc	1	~

Test Step 2.15 (Repeat Count = 1)	✓
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_Igc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_Igc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_Igc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_Igc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	1
CTCFailedBuf_Cnt_M_Igc[21]	1
CTCFailedBuf_Cnt_M_lgc[22]	1
CTCFailedBuf_Cnt_M_Igc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1

2018-04-10, 18:44:44+0530



Demit_DTCS Ch n e	TAACILAU
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	1
CTCFailedBuf_Cnt_M_lgc[35]	1
CTCFailedBuf_Cnt_M_lgc[36]	1
CTCFailedBuf_Cnt_M_lgc[37]	1
CTCFailedBuf_Cnt_M_lgc[38] CTCFailedBuf_Cnt_M_lgc[39]	1
CTCFailedBuf_Cnt_M_lgc[40]	1
CTCFailedBuf_Cnt_M_lgc[41]	1
CTCFailedBuf_Cnt_M_lgc[42]	1
CTCFailedBuf_Cnt_M_lgc[43]	1
CTCFailedBuf_Cnt_M_lgc[44]	1
CTCFailedBuf_Cnt_M_lgc[45]	1
CTCFailedBuf_Cnt_M_lgc[46]	1
CTCFailedBuf_Cnt_M_lgc[47]	1
CTCFailedBuf_Cnt_M_lgc[48]	1
CTCFailedBuf_Cnt_M_lgc[49]	1
CTCFailedBuf_Cnt_M_lgc[50]	1
CTCFailedBuf_Cnt_M_lgc[51]	1
CTCFailedBuf_Cnt_M_lgc[52]	1.
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58] CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1
CTCFailedBuf_Cnt_M_lgc[64]	1
CTCFailedBuf_Cnt_M_lgc[65]	1
CTCFailedBuf_Cnt_M_lgc[66]	1
CTCFailedBuf_Cnt_M_lgc[67]	1
CTCFailedBuf_Cnt_M_lgc[68]	1
CTCFailedBuf_Cnt_M_lgc[69]	1
CTCFailedBuf_Cnt_M_lgc[70]	1
CTCFailedBuf_Cnt_M_lgc[71]	1
CTCFailedBuf_Cnt_M_lgc[72]	1
CTCFailedBuf_Cnt_M_lgc[73]	1
CTCFailedBuf_Cnt_M_lgc[74]	1
CTCFailedBuf_Cnt_M_lgc[75]	1
CTCFailedBuf_Cnt_M_lgc[76] CTCFailed_Cnt_M_lgc	0
DTC	3261627242
DTCKind	1
DTCStatusNew	78
DTCStatusOld	172
Dem_DTCNumberTable[0]	31
Dem_DTCNumberTable[1]	227
Dem_DTCNumberTable[2]	66
Dem_DTCNumberTable[3]	96
Dem_DTCNumberTable[4]	130
Dem_DTCNumberTable[5]	24
Dem_DTCNumberTable[6]	240
Dem_DTCNumberTable[7]	240
Dem_DTCNumberTable[8]	31
	227
	240
Dem_DTCNumberTable[10]	
Dem_DTCNumberTable[10] Dem_DTCNumberTable[11]	151
Dem_DTCNumberTable[10] Dem_DTCNumberTable[11] Dem_DTCNumberTable[12]	151 227
Dem_DTCNumberTable[10] Dem_DTCNumberTable[11] Dem_DTCNumberTable[12] Dem_DTCNumberTable[13]	151 227 240
Dem_DTCNumberTable[10] Dem_DTCNumberTable[11] Dem_DTCNumberTable[12] Dem_DTCNumberTable[13] Dem_DTCNumberTable[13] Dem_DTCNumberTable[14]	151 227 240 31
Dem_DTCNumberTable[10]  Dem_DTCNumberTable[11]  Dem_DTCNumberTable[12]  Dem_DTCNumberTable[13]  Dem_DTCNumberTable[14]  Dem_DTCNumberTable[15]	151 227 240 31 227
Dem_DTCNumberTable[10]  Dem_DTCNumberTable[11]  Dem_DTCNumberTable[12]  Dem_DTCNumberTable[13]  Dem_DTCNumberTable[14]  Dem_DTCNumberTable[15]  Dem_DTCNumberTable[16]	151 227 240 31 227 227
Dem_DTCNumberTable[9] Dem_DTCNumberTable[10] Dem_DTCNumberTable[11] Dem_DTCNumberTable[12] Dem_DTCNumberTable[13] Dem_DTCNumberTable[14] Dem_DTCNumberTable[15] Dem_DTCNumberTable[16] Dem_DTCNumberTable[17] Dem_DTCNumberTable[17]	151 227 240 31 227

Demlf\_DTCS

2018-04-10, 18:44:44+0530



Name Input Value Dem\_DTCNumberTable[20] 227 Dem\_DTCNumberTable[21] 240 Dem DTCNumberTable[22] 31 Dem\_DTCNumberTable[23] 66 Dem DTCNumberTable[24] 96 Dem\_DTCNumberTable[25] 130 Dem\_DTCNumberTable[26] 24 Dem\_DTCNumberTable[27] 227 Dem\_DTCNumberTable[28] 31 Dem\_DTCNumberTable[29] 227 Dem\_DTCNumberTable[30] 31 Dem\_DTCNumberTable[31] 31 Dem\_DTCNumberTable[32] 227 Dem\_DTCNumberTable[33] 227 Dem\_DTCNumberTable[34] 31 Dem\_DTCNumberTable[35] 227 Dem\_DTCNumberTable[36] 31 Dem\_DTCNumberTable[37] 31 Dem\_DTCNumberTable[38] 31 Dem\_DTCNumberTable[39] 227 Dem\_DTCNumberTable[40] 227 Dem\_DTCNumberTable[41] 66 Dem\_DTCNumberTable[42] 96 Dem\_DTCNumberTable[43] 130 Dem\_DTCNumberTable[44] 24 Dem\_DTCNumberTable[45] 240 Dem DTCNumberTable[46] 31 Dem\_DTCNumberTable[47] 227 Dem DTCNumberTable[48] 96 Dem\_DTCNumberTable[49] 31 Dem DTCNumberTable[50] 227 Dem\_DTCNumberTable[51] 31 Dem DTCNumberTable[52] 31 Dem\_DTCNumberTable[53] 227 Dem\_DTCNumberTable[54] 96 Dem\_DTCNumberTable[55] 240 Dem\_DTCNumberTable[56] 31 Dem\_DTCNumberTable[57] 227 Dem\_DTCNumberTable[58] Dem\_DTCNumberTable[59] 240 Dem\_DTCNumberTable[60] 31 Dem\_DTCNumberTable[61] 227 Dem\_DTCNumberTable[62] 96 Dem\_DTCNumberTable[63] 66 Dem\_DTCNumberTable[64] 96 Dem\_DTCNumberTable[65] 130 Dem DTCNumberTable[66] 24 Dem\_DTCNumberTable[67] 31 Dem DTCNumberTable[68] 31 Dem\_DTCNumberTable[69] 227 Dem\_DTCNumberTable[70] 96 Dem\_DTCNumberTable[71] 240 Dem\_DTCNumberTable[72] 96 Dem\_DTCNumberTable[73] 66 Dem\_DTCNumberTable[74] 96 Dem\_DTCNumberTable[75] 130 Dem\_DTCNumberTable[76] 24 Dem\_DTC\_FTB\_Table[0] 89 Dem\_DTC\_FTB\_Table[1] 78 Dem\_DTC\_FTB\_Table[2] 204 Dem\_DTC\_FTB\_Table[3] 103 238 Dem\_DTC\_FTB\_Table[4] Dem\_DTC\_FTB\_Table[5] 77 Dem\_DTC\_FTB\_Table[6] 228 Dem\_DTC\_FTB\_Table[7] 228 Dem DTC FTB Table[8] 89 Dem\_DTC\_FTB\_Table[9] 78 Dem DTC FTB Table[10] 228 Dem\_DTC\_FTB\_Table[11] 90 Dem\_DTC\_FTB\_Table[12] 78 Dem\_DTC\_FTB\_Table[13] 228 Dem\_DTC\_FTB\_Table[14] 89 Dem\_DTC\_FTB\_Table[15] 78

2018-04-10, 18:44:44+0530

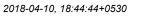


DemIf\_DTCS Name Input Value Dem\_DTC\_FTB\_Table[16] 78 Dem\_DTC\_FTB\_Table[17] 228 Dem\_DTC\_FTB\_Table[18] 228 Dem\_DTC\_FTB\_Table[19] 89 78 Dem\_DTC\_FTB\_Table[20] Dem\_DTC\_FTB\_Table[21] 228 Dem\_DTC\_FTB\_Table[22] 89 Dem\_DTC\_FTB\_Table[23] 204 Dem\_DTC\_FTB\_Table[24] 103 Dem\_DTC\_FTB\_Table[25] 238 Dem\_DTC\_FTB\_Table[26] 77 Dem\_DTC\_FTB\_Table[27] 78 Dem\_DTC\_FTB\_Table[28] 89 Dem DTC FTB Table[29] 78 Dem\_DTC\_FTB\_Table[30] 89 Dem\_DTC\_FTB\_Table[31] 89 Dem\_DTC\_FTB\_Table[32] 78 Dem\_DTC\_FTB\_Table[33] 78 Dem\_DTC\_FTB\_Table[34] 89 Dem\_DTC\_FTB\_Table[35] 78 Dem\_DTC\_FTB\_Table[36] 89 Dem\_DTC\_FTB\_Table[37] 89 Dem\_DTC\_FTB\_Table[38] 89 Dem\_DTC\_FTB\_Table[39] 78 Dem\_DTC\_FTB\_Table[40] 78 Dem\_DTC\_FTB\_Table[41] 204 Dem\_DTC\_FTB\_Table[42] 103 Dem\_DTC\_FTB\_Table[43] 238 Dem\_DTC\_FTB\_Table[44] 77 Dem\_DTC\_FTB\_Table[45] 228 Dem\_DTC\_FTB\_Table[46] 89 Dem\_DTC\_FTB\_Table[47] 78 Dem DTC FTB Table[48] 103 Dem\_DTC\_FTB\_Table[49] 89 Dem\_DTC\_FTB\_Table[50] 78 Dem\_DTC\_FTB\_Table[51] 89 Dem\_DTC\_FTB\_Table[52] 89 Dem\_DTC\_FTB\_Table[53] 78 Dem\_DTC\_FTB\_Table[54] 103 Dem DTC\_FTB\_Table[55] 228 Dem\_DTC\_FTB\_Table[56] 89 Dem\_DTC\_FTB\_Table[57] 78 Dem\_DTC\_FTB\_Table[58] 89 Dem\_DTC\_FTB\_Table[59] 228 89 Dem\_DTC\_FTB\_Table[60] Dem\_DTC\_FTB\_Table[61] 78 Dem\_DTC\_FTB\_Table[62] 103 Dem\_DTC\_FTB\_Table[63] 204 Dem\_DTC\_FTB\_Table[64] 103 Dem\_DTC\_FTB\_Table[65] 238 Dem\_DTC\_FTB\_Table[66] 77 Dem\_DTC\_FTB\_Table[67] 89 Dem\_DTC\_FTB\_Table[68] 89 Dem\_DTC\_FTB\_Table[69] 78 Dem\_DTC\_FTB\_Table[70] 103 Dem\_DTC\_FTB\_Table[71] 228 Dem\_DTC\_FTB\_Table[72] 103 Dem\_DTC\_FTB\_Table[73] 204 Dem\_DTC\_FTB\_Table[74] 103 Dem\_DTC\_FTB\_Table[75] 238

Dem_DTC_FTB_Table[76]	77		
Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[0]	1	1	~
CTCFailedBuf_Cnt_M_lgc[1]	1	1	~
CTCFailedBuf_Cnt_M_lgc[2]	1	1	~
CTCFailedBuf_Cnt_M_lgc[3]	1	1	~
CTCFailedBuf_Cnt_M_lgc[4]	1	1	~
CTCFailedBuf_Cnt_M_lgc[5]	1	1	•
CTCFailedBuf_Cnt_M_lgc[6]	1	1	~
CTCFailedBuf_Cnt_M_lgc[7]	1	1	~
CTCFailedBuf_Cnt_M_lgc[8]	1	1	~
CTCFailedBuf_Cnt_M_lgc[9]	1	1	~
CTCFailedBuf_Cnt_M_lgc[10]	1	1	~

## **TEST DETAILS REPORT** Ch n e

DemIf\_DTCS





CICCHARDS CALL N. 19613	Name	Actual Value	Expected Value	Result
CTCFaedBull Col. M. 19513	CTCFailedBuf_Cnt_M_lgc[11]	1		~
CTCFMacRadu Colt W, 30(14)  1				~
CICHARDBL_COV_LU_SCIP	CTCFailedBuf_Cnt_M_lgc[13]		1	~
CTCFaledbull, Cott, M., 19879   1				~
STCF/SeeSell_CER_M_pdf4    1				~
CTCFaieddd, Cot M, Jog50				<b>✓</b>
CitCrianded, Citch, Mig (20)   1   1   1   1   1   1   1   1   1				<b>*</b>
CTCFailedBull Cort M. Jug270    1				
CTCFalestand CM, M   plo22				
CTCFaneStuff_CTLM_bgt22  1				<b>*</b>
CTCFailedton_CTM_M_5023  1				
CITCFacebated, CTM, Mpd289 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		1	1	<b>✓</b>
CTCFaledbuf, CM, Migo2P)		1	1	<b>✓</b>
CTCFalestudy_CTM_Mgc(28)	CTCFailedBuf_Cnt_M_lgc[25]	1	1	~
CITCFalebord, CM, Mg(20)  1	CTCFailedBuf_Cnt_M_lgc[26]			~
CTCFaledbuf_CM_Mgc(3)				<b>✓</b>
CTCFaledBuf, CM, Mgc30				~
CTCFaledBut, Cot, M, Ugd31				~
CTCFaledud_CM_Migd3    CTCFaledud_CM_Migd4    CTCFaledud_CM_Migd5				<b>✓</b>
CTCFaledBuf_Cnt_M_get33				- J
CTCFaleeBuf_Cnt_M_lgct30]  CTCFaleeBuf_Cnt_M_lgct30]  1				- V
CTCFaledBul_Cnt_M_gqt35				
CTCFaledBuf_Cnt_M_lgq39] 1				<u> </u>
CTCFaiesdBuf_Cnt, M_1gct37  CTCFaiesdBuf_Cnt, M_1gct38  1				
CTCFaledBuf_Cnt_M_lgq(38) 1 CTCFaledBuf_Cnt_M_lgq(39) 1 CTCFaledBuf_Cnt_M_lgq(41) 1 1 CTCFaledBuf_Cnt_M_lgq(41) 1 1 CTCFaledBuf_Cnt_M_lgq(42) 1 1 1 1 CTCFaledBuf_Cnt_M_lgq(42) 1 1 1 1 CTCFaledBuf_Cnt_M_lgq(43) 1 1 CTCFaledBuf_Cnt_M_lgq(44) 1 CTCFaledBuf_Cnt_M_lgq(44) 1 CTCFaledBuf_Cnt_M_lgq(44) 1 CTCFaledBuf_Cnt_M_lgq(48) 1 CTCFaledBuf_Cnt_M_lgq(58) 1 CTCFaledBuf_		1	1	<b>✓</b>
CTCFaiedBuf_Cnt_M_logd9  1		1	1	~
CTCFailedBuf_Cnt_M_logic41		1	1	~
CTCFaledBuf_Cnt_M_lgc[42]	CTCFailedBuf_Cnt_M_lgc[40]	1	1	~
CTCFaledBuf_Cnt_M_lgc[43]   1	CTCFailedBuf_Cnt_M_Igc[41]	1	1	<b>✓</b>
CTCFaledBuf, Cnt, M, Igq449 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	CTCFailedBuf_Cnt_M_lgc[42]			~
CTCFalledBuf_Cnt_M_lgc[45]				~
CTCFailedBut_Cnt_M_lgcl49  CTCFailedBut_Cnt_M_lgcl48  1  CTCFailedBut_Cnt_M_lgcl49  1  CTCFailedBut_Cnt_M_lgcl49  1  CTCFailedBut_Cnt_M_lgcl51  1  1  CTCFailedBut_Cnt_M_lgcl51  1  1  CTCFailedBut_Cnt_M_lgcl51  1  CTCFailedBut_Cnt_M_lgcl52  1  CTCFailedBut_Cnt_M_lgcl52  1  CTCFailedBut_Cnt_M_lgcl54  1  CTCFailedBut_Cnt_M_lgcl54  1  CTCFailedBut_Cnt_M_lgcl54  1  CTCFailedBut_Cnt_M_lgcl56  CTCFailedBut_Cnt_M_lgcl56  CTCFailedBut_Cnt_M_lgcl57  TCTCFailedBut_Cnt_M_lgcl58  1  CTCFailedBut_Cnt_M_lgcl59  CTCFailedBut_Cnt_M_lgcl59  CTCFailedBut_Cnt_M_lgcl59  CTCFailedBut_Cnt_M_lgcl59  CTCFailedBut_Cnt_M_lgcl59  CTCFailedBut_Cnt_M_lgcl60  CTCFailedBut_Cnt_M_lgcl60  CTCFailedBut_Cnt_M_lgcl60  CTCFailedBut_Cnt_M_lgcl60  CTCFailedBut_Cnt_M_lgcl60  TCTCFailedBut_Cnt_M_lgcl60  TCTCFailedBut_Cnt_M_lgcl70  TCTCFailedBut				<b>Y</b>
CTCFailedBuf_Cnt_M_lgcl48				<b>*</b>
CTCFailedBuf_Cnt_M_lgc[48] 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1				· ·
CTCFailedBuf_Cnt_M_lgc[49]				
CTCFailedBuf_Cnt_M_lgc[50] 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1				·
CTCFailedBuf_Cnt_M_lgc[51]				_
CTCFailedBuf_Cnt_M_lgc[53]				~
CTCFailedBuf_Cnt_M_lgc[54]         1         1           CTCFailedBuf_Cnt_M_lgc[55]         1         1           CTCFailedBuf_Cnt_M_lgc[56]         1         1           CTCFailedBuf_Cnt_M_lgc[57]         1         1           CTCFailedBuf_Cnt_M_lgc[58]         1         1           CTCFailedBuf_Cnt_M_lgc[59]         1         1           CTCFailedBuf_Cnt_M_lgc[60]         1         1           CTCFailedBuf_Cnt_M_lgc[61]         1         1           CTCFailedBuf_Cnt_M_lgc[63]         1         1           CTCFailedBuf_Cnt_M_lgc[63]         1         1           CTCFailedBuf_Cnt_M_lgc[64]         1         1           CTCFailedBuf_Cnt_M_lgc[65]         1         1           CTCFailedBuf_Cnt_M_lgc[66]         1         1           CTCFailedBuf_Cnt_M_lgc[68]         1         1           CTCFailedBuf_Cnt_M_lgc[68]         1         1           CTCFailedBuf_Cnt_M_lgc[68]         1         1           CTCFailedBuf_Cnt_M_lgc[70]         1         1           CTCFailedBuf_Cnt_M_lgc[70]         1         1           CTCFailedBuf_Cnt_M_lgc[72]         1         1           CTCFailedBuf_Cnt_M_lgc[72]         1         1           CTC	CTCFailedBuf_Cnt_M_lgc[52]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[55]       1       1         CTCFailedBuf_Cnt_M_lgc[56]       1       1         CTCFailedBuf_Cnt_M_lgc[58]       1       1         CTCFailedBuf_Cnt_M_lgc[58]       1       1         CTCFailedBuf_Cnt_M_lgc[50]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1         CTCFailedBuf_Cnt_M_lgc[72]       1       1         CTCFailedBuf_Cnt_M_lgc[73]       1       1         CTCFailedBuf_Cnt_M_lgc[75]       1       1         CTCFailedBuf_Cnt_M_l	CTCFailedBuf_Cnt_M_lgc[53]	1	1	~
CTCFailedBuf_Cnt_M_lgc[56]       1       1         CTCFailedBuf_Cnt_M_lgc[57]       1       1         CTCFailedBuf_Cnt_M_lgc[58]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1         CTCFailedBuf_Cnt_M_lgc[72]       1       1         CTCFailedBuf_Cnt_M_lgc[73]       1       1         CTCFailedBuf_Cnt_M_lgc[73]       1       1         CTCFailedBuf_Cnt_M_lgc[75]       1       1         CTCFailedBuf_Cnt_M_lgc[75]       1       1         CTCFailedBuf_Cnt_M_l	CTCFailedBuf_Cnt_M_lgc[54]	1	1	~
CTCFailedBuf_Cnt_M_lgc[57]       1       1         CTCFailedBuf_Cnt_M_lgc[58]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1         CTCFailedBuf_Cnt_M_lgc[72]       1       1         CTCFailedBuf_Cnt_M_lgc[73]       1       1         CTCFailedBuf_Cnt_M_lgc[74]       1       1         CTCFailedBuf_Cnt_M_lgc[74]       1       1         CTCFailedBuf_Cnt_M_lgc[75]       1       1         CTCFailedBuf_Cnt_M_lgc[75]       1       1         CTCFailedBuf_Cnt_M_l		1	1	~
CTCFailedBuf_Cnt_M_lgc[58]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1         CTCFailedBuf_Cnt_M_lgc[73]       1       1         CTCFailedBuf_Cnt_M_lgc[73]       1       1         CTCFailedBuf_Cnt_M_lgc[74]       1       1         CTCFailedBuf_Cnt_M_lgc[75]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       0       0				~
CTCFailedBuf_Cnt_M_lgc[59]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1         CTCFailedBuf_Cnt_M_lgc[72]       1       1         CTCFailedBuf_Cnt_M_lgc[73]       1       1         CTCFailedBuf_Cnt_M_lgc[74]       1       1         CTCFailedBuf_Cnt_M_lgc[75]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       0       0				~
CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1         CTCFailedBuf_Cnt_M_lgc[72]       1       1         CTCFailedBuf_Cnt_M_lgc[73]       1       1         CTCFailedBuf_Cnt_M_lgc[73]       1       1         CTCFailedBuf_Cnt_M_lgc[75]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       0       0				<b>V</b>
CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1         CTCFailedBuf_Cnt_M_lgc[72]       1       1         CTCFailedBuf_Cnt_M_lgc[73]       1       1         CTCFailedBuf_Cnt_M_lgc[74]       1       1         CTCFailedBuf_Cnt_M_lgc[75]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       0       0				<b>V</b>
CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1         CTCFailedBuf_Cnt_M_lgc[72]       1       1         CTCFailedBuf_Cnt_M_lgc[73]       1       1         CTCFailedBuf_Cnt_M_lgc[74]       1       1         CTCFailedBuf_Cnt_M_lgc[75]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       0       0				<b>~</b>
CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1         CTCFailedBuf_Cnt_M_lgc[72]       1       1         CTCFailedBuf_Cnt_M_lgc[73]       1       1         CTCFailedBuf_Cnt_M_lgc[74]       1       1         CTCFailedBuf_Cnt_M_lgc[75]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       0       0				
CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1         CTCFailedBuf_Cnt_M_lgc[72]       1       1         CTCFailedBuf_Cnt_M_lgc[73]       1       1         CTCFailedBuf_Cnt_M_lgc[74]       1       1         CTCFailedBuf_Cnt_M_lgc[75]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       0       0				~
CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1         CTCFailedBuf_Cnt_M_lgc[72]       1       1         CTCFailedBuf_Cnt_M_lgc[73]       1       1         CTCFailedBuf_Cnt_M_lgc[74]       1       1         CTCFailedBuf_Cnt_M_lgc[75]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       1       1         CTCFailed_Cnt_M_lgc       0       0				
CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1         CTCFailedBuf_Cnt_M_lgc[72]       1       1         CTCFailedBuf_Cnt_M_lgc[73]       1       1         CTCFailedBuf_Cnt_M_lgc[74]       1       1         CTCFailedBuf_Cnt_M_lgc[75]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       1       1         CTCFailed_Cnt_M_lgc       0       0				<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1         CTCFailedBuf_Cnt_M_lgc[72]       1       1         CTCFailedBuf_Cnt_M_lgc[73]       1       1         CTCFailedBuf_Cnt_M_lgc[74]       1       1         CTCFailedBuf_Cnt_M_lgc[75]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       1       1         CTCFailed_Cnt_M_lgc       0       0				~
CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1         CTCFailedBuf_Cnt_M_lgc[72]       1       1         CTCFailedBuf_Cnt_M_lgc[73]       1       1         CTCFailedBuf_Cnt_M_lgc[74]       1       1         CTCFailedBuf_Cnt_M_lgc[75]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       1       1         CTCFailed_Cnt_M_lgc       0       0		1	1	~
CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1         CTCFailedBuf_Cnt_M_lgc[72]       1       1         CTCFailedBuf_Cnt_M_lgc[73]       1       1         CTCFailedBuf_Cnt_M_lgc[74]       1       1         CTCFailedBuf_Cnt_M_lgc[75]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       1       1         CTCFailed_Cnt_M_lgc       0       0		1	1	~
CTCFailedBuf_Cnt_M_lgc[71]       1       1         CTCFailedBuf_Cnt_M_lgc[72]       1       1         CTCFailedBuf_Cnt_M_lgc[73]       1       1         CTCFailedBuf_Cnt_M_lgc[74]       1       1         CTCFailedBuf_Cnt_M_lgc[75]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       1       1         CTCFailed_Cnt_M_lgc       0       0	CTCFailedBuf_Cnt_M_lgc[69]			<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[72]       1       1         CTCFailedBuf_Cnt_M_lgc[73]       1       1         CTCFailedBuf_Cnt_M_lgc[74]       1       1         CTCFailedBuf_Cnt_M_lgc[75]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       1       1         CTCFailed_Cnt_M_lgc       0       0				•
CTCFailedBuf_Cnt_M_lgc[73]       1       1         CTCFailedBuf_Cnt_M_lgc[74]       1       1         CTCFailedBuf_Cnt_M_lgc[75]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       1       1         CTCFailed_Cnt_M_lgc       0       0				~
CTCFailedBuf_Cnt_M_lgc[74]       1       1         CTCFailedBuf_Cnt_M_lgc[75]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       1       1         CTCFailed_Cnt_M_lgc       0       0				<b>V</b>
CTCFailedBuf_Cnt_M_lgc[75]       1       1         CTCFailedBuf_Cnt_M_lgc[76]       1       1         CTCFailed_Cnt_M_lgc       0       0				v
CTCFailedBuf_Cnt_M_lgc[76]         1         1           CTCFailed_Cnt_M_lgc         0         0				<b>✓</b>
CTCFailed_Cnt_M_lgc 0 0				
				-
	Demlf_DTCStatusChanged()	0	0	
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc(data) 0 0				_

Demlf\_DTCS



Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte Write An Demlf CTCFailed Cnt loc	1	Rte Write An Demlf CTCFailed Cnt loc	1	_

Test Step 2.16 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf Cnt M Igc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf Cnt M lgc[20]	0
CTCFailedBuf Cnt M Igc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_Igc[27] CTCFailedBuf_Cnt_M_Igc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36] CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_gc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45] CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55] CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1.
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1

## **TEST DETAILS REPORT** Ch n e

DemIf\_DTCS



Denni_DTC3 Ch h e	(WAC)
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[64]	1
CTCFailedBuf_Cnt_M_lgc[65]	0
CTCFailedBuf_Cnt_M_lgc[66]	1
CTCFailedBuf_Cnt_M_lgc[67]	0
CTCFailedBuf_Cnt_M_lgc[68]	0
CTCFailedBuf_Cnt_M_lgc[69]	0
CTCFailedBuf_Cnt_M_lgc[70]	0
CTCFailedBuf_Cnt_M_lgc[71]	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	0
CTCFailedBuf_Cnt_M_lgc[74]	0
	0
CTCFailedBuf_Cnt_M_lgc[75]	
CTCFailedBuf_Cnt_M_lgc[76]	0
CTCFailed_Cnt_M_lgc	1
OTC	4231674622
OTCKind	2
DTCStatusNew	178
OTCStatusOld	176
Dem_DTCNumberTable[0]	83
Dem_DTCNumberTable[1]	99
Dem_DTCNumberTable[2]	240
Dem_DTCNumberTable[3]	233
Dem_DTCNumberTable[4]	31
Dem_DTCNumberTable[5]	75
Dem_DTCNumberTable[6]	164
Dem_DTCNumberTable[7]	164
Dem_DTCNumberTable[8]	83
Dem_DTCNumberTable[9]	99
Dem_DTCNumberTable[10]	164
Dem_DTCNumberTable[11]	40
Dem_DTCNumberTable[12]	99
Dem_DTCNumberTable[13]	164
Dem_DTCNumberTable[14]	83
	99
Dem_DTCNumberTable[15]	99
Dem_DTCNumberTable[16]	164
Dem_DTCNumberTable[17]	
Dem_DTCNumberTable[18]	74
Dem_DTCNumberTable[19]	83
Dem_DTCNumberTable[20]	99
Dem_DTCNumberTable[21]	164
Dem_DTCNumberTable[22]	83
Dem_DTCNumberTable[23]	240
Dem_DTCNumberTable[24]	233
Dem_DTCNumberTable[25]	31
Dem_DTCNumberTable[26]	75
Dem_DTCNumberTable[27]	99
Dem_DTCNumberTable[28]	83
Dem_DTCNumberTable[29]	99
Dem_DTCNumberTable[30]	83
Dem_DTCNumberTable[31]	83
DTCNumberTable[32]	99
Dem_DTCNumberTable[33]	99
Dem_DTCNumberTable[34]	83
em_DTCNumberTable[35]	99
em_DTCNumberTable[36]	83
	83
em_DTCNumberTable[37]	
em_DTCNumberTable[38]	83
em_DTCNumberTable[39]	99
em_DTCNumberTable[40]	99
em_DTCNumberTable[41]	240
em_DTCNumberTable[42]	233
em_DTCNumberTable[43]	31
em_DTCNumberTable[44]	75
em_DTCNumberTable[45]	164
em_DTCNumberTable[46]	83
em_DTCNumberTable[47]	99
DTCNumberTable[48]	233
Dem_DTCNumberTable[49]	83
em_DTCNumberTable[50]	99
pem_DTCNumberTable[50]	83
Dem_DTCNumberTable[51]	83
Dem_DTCNumberTable[52]	99
	233
Dem_DTCNumberTable[54]	

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Name Input Value Dem DTCNumberTable[55] 164 Dem\_DTCNumberTable[56] 83 Dem\_DTCNumberTable[57] 99 Dem\_DTCNumberTable[58] 83 Dem\_DTCNumberTable[59] 164 Dem\_DTCNumberTable[60] 83 Dem\_DTCNumberTable[61] 99 Dem\_DTCNumberTable[62] 233 Dem\_DTCNumberTable[63] 240 Dem DTCNumberTable[64] 233 Dem\_DTCNumberTable[65] 31 Dem\_DTCNumberTable[66] 75 Dem\_DTCNumberTable[67] 83 Dem DTCNumberTable[68] 83 Dem\_DTCNumberTable[69] 99 Dem\_DTCNumberTable[70] 233 Dem\_DTCNumberTable[71] 164 Dem\_DTCNumberTable[72] 233 Dem\_DTCNumberTable[73] 240 Dem\_DTCNumberTable[74] 233 Dem\_DTCNumberTable[75] 31 Dem\_DTCNumberTable[76] 75 Dem\_DTC\_FTB\_Table[0] 170 Dem\_DTC\_FTB\_Table[1] 194 Dem\_DTC\_FTB\_Table[2] 13 Dem\_DTC\_FTB\_Table[3] 32 Dem\_DTC\_FTB\_Table[4] 172 Dem\_DTC\_FTB\_Table[5] 241 Dem\_DTC\_FTB\_Table[6] 91 Dem\_DTC\_FTB\_Table[7] 91 Dem\_DTC\_FTB\_Table[8] 170 Dem\_DTC\_FTB\_Table[9] 194 Dem DTC FTB Table[10] 91 Dem\_DTC\_FTB\_Table[11] 82 Dem\_DTC\_FTB\_Table[12] 194 Dem DTC FTB Table[13] 91 Dem\_DTC\_FTB\_Table[14] 170 Dem\_DTC\_FTB\_Table[15] 194 Dem\_DTC\_FTB\_Table[16] 194 Dem DTC\_FTB\_Table[17] 91 Dem\_DTC\_FTB\_Table[18] 55 Dem DTC FTB Table[19] 170 Dem\_DTC\_FTB\_Table[20] 194 Dem\_DTC\_FTB\_Table[21] 91 170 Dem\_DTC\_FTB\_Table[22] Dem\_DTC\_FTB\_Table[23] 13 32 Dem\_DTC\_FTB\_Table[24] Dem\_DTC\_FTB\_Table[25] 172 Dem\_DTC\_FTB\_Table[26] 241 Dem\_DTC\_FTB\_Table[27] 194 Dem\_DTC\_FTB\_Table[28] 170 Dem\_DTC\_FTB\_Table[29] 194 Dem\_DTC\_FTB\_Table[30] 170 Dem\_DTC\_FTB\_Table[31] 170 Dem\_DTC\_FTB\_Table[32] 194 Dem\_DTC\_FTB\_Table[33] 194 Dem\_DTC\_FTB\_Table[34] 170 Dem\_DTC\_FTB\_Table[35] 194 Dem\_DTC\_FTB\_Table[36] 170 Dem\_DTC\_FTB\_Table[37] 170 Dem\_DTC\_FTB\_Table[38] 170 Dem\_DTC\_FTB\_Table[39] 194 Dem\_DTC\_FTB\_Table[40] 194 Dem\_DTC\_FTB\_Table[41] 13 Dem\_DTC\_FTB\_Table[42] 32 Dem DTC FTB Table[43] 172 Dem\_DTC\_FTB\_Table[44] 241 Dem DTC FTB Table[45] 91 Dem\_DTC\_FTB\_Table[46] 170 Dem\_DTC\_FTB\_Table[47] 194 Dem\_DTC\_FTB\_Table[48] 32 Dem\_DTC\_FTB\_Table[49] 170 Dem\_DTC\_FTB\_Table[50] 194

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value Dem\_DTC\_FTB\_Table[51] 170 Dem\_DTC\_FTB\_Table[52] 170 Dem DTC\_FTB\_Table[53] 194 Dem\_DTC\_FTB\_Table[54] 32 Dem\_DTC\_FTB\_Table[55] 91 Dem\_DTC\_FTB\_Table[56] 170 Dem\_DTC\_FTB\_Table[57] 194 Dem\_DTC\_FTB\_Table[58] 170 Dem\_DTC\_FTB\_Table[59] 91 Dem\_DTC\_FTB\_Table[60] 170 Dem\_DTC\_FTB\_Table[61] 194 32 Dem\_DTC\_FTB\_Table[62] Dem\_DTC\_FTB\_Table[63] 13 Dem\_DTC\_FTB\_Table[64] 32 Dem\_DTC\_FTB\_Table[65] 172 241 Dem DTC FTB Table[66] Dem\_DTC\_FTB\_Table[67] 170 Dem\_DTC\_FTB\_Table[68] 170 Dem\_DTC\_FTB\_Table[69] 194 Dem\_DTC\_FTB\_Table[70] 32 Dem\_DTC\_FTB\_Table[71] 91 Dem\_DTC\_FTB\_Table[72] 32 Dem\_DTC\_FTB\_Table[73] 13 Dem\_DTC\_FTB\_Table[74] 32 Dem\_DTC\_FTB\_Table[75] 172 Dem\_DTC\_FTB\_Table[76] 241 Name **Actual Value Expected Value** Result CTCFailedBuf Cnt M Igc[0] 1 CTCFailedBuf\_Cnt\_M\_lgc[1] CTCFailedBuf\_Cnt\_M\_lgc[2] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[3] 1 CTCFailedBuf Cnt M lgc[4] CTCFailedBuf\_Cnt\_M\_lgc[5] 1 1 CTCFailedBuf Cnt M Igc[6] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[7] 1 CTCFailedBuf\_Cnt\_M\_lgc[8] CTCFailedBuf\_Cnt\_M\_lgc[9] CTCFailedBuf\_Cnt\_M\_lgc[10] CTCFailedBuf\_Cnt\_M\_lgc[11] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[12] CTCFailedBuf Cnt M lqc[13] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[14] CTCFailedBuf\_Cnt\_M\_lgc[15] 1 CTCFailedBuf\_Cnt\_M\_lgc[16] **~** CTCFailedBuf\_Cnt\_M\_lgc[17] 1 CTCFailedBuf\_Cnt\_M\_lgc[18] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[19] 1 1 V CTCFailedBuf\_Cnt\_M\_lgc[20] n 0 CTCFailedBuf\_Cnt\_M\_lgc[21] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[22] n n CTCFailedBuf\_Cnt\_M\_lgc[23] 1 CTCFailedBuf Cnt M lqc[24] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[25] CTCFailedBuf\_Cnt\_M\_lgc[26] CTCFailedBuf\_Cnt\_M\_lgc[27] 1 CTCFailedBuf\_Cnt\_M\_lgc[28] 1  $CTCFailedBuf\_Cnt\_M\_lgc[29]$ 1 CTCFailedBuf\_Cnt\_M\_lgc[30] CTCFailedBuf\_Cnt\_M\_lgc[31] CTCFailedBuf\_Cnt\_M\_lgc[32] 1 CTCFailedBuf\_Cnt\_M\_lgc[33] 1 1 0 CTCFailedBuf\_Cnt\_M\_lgc[34] 0 CTCFailedBuf\_Cnt\_M\_lgc[35] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[36] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[37] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[38] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[39] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[40] 0 0 CTCFailedBuf Cnt M Igc[41] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[42] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[43] 0 0 ~ CTCFailedBuf\_Cnt\_M\_lgc[44] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[45] 0 0

Rte\_Write\_Ap\_DemIf\_CTCFailed\_Cnt\_lgc(data)

DemIf\_DTCS

2018-04-10, 18:44:44+0530



**Actual Value Expected Value** CTCFailedBuf\_Cnt\_M\_lgc[46] CTCFailedBuf\_Cnt\_M\_lgc[47] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[48] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[49] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[50] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[51] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[52] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[53] 1 CTCFailedBuf\_Cnt\_M\_lgc[54] CTCFailedBuf\_Cnt\_M\_lgc[55] CTCFailedBuf\_Cnt\_M\_lgc[56] CTCFailedBuf\_Cnt\_M\_lgc[57] 1 CTCFailedBuf\_Cnt\_M\_lgc[58] CTCFailedBuf\_Cnt\_M\_lgc[59] CTCFailedBuf\_Cnt\_M\_lgc[60] CTCFailedBuf\_Cnt\_M\_lgc[61] 1 CTCFailedBuf\_Cnt\_M\_lgc[62] ソソソソソソソ CTCFailedBuf\_Cnt\_M\_lgc[63] 1  $CTCFailedBuf\_Cnt\_M\_lgc[64]$ CTCFailedBuf\_Cnt\_M\_lgc[65] 0 0  $CTCFailedBuf\_Cnt\_M\_lgc[66]$ CTCFailedBuf\_Cnt\_M\_lgc[67] 0 0  $CTCFailedBuf\_Cnt\_M\_lgc[68]$ 0 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[73] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[74] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[75] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 0 CTCFailed\_Cnt\_M\_lgc 1 1 Demlf DTCStatusChanged() 0 0

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte Write Ap Demlf CTCFailed Cnt lgc	1	Rte Write Ap Demlf CTCFailed Cnt lgc	1	~

Name         Input Value           CTCFailedBuf_Cnt_M_lgc[0]         1           CTCFailedBuf_Cnt_M_lgc[1]         1           CTCFailedBuf_Cnt_M_lgc[2]         1           CTCFailedBuf_Cnt_M_lgc[3]         1           CTCFailedBuf_Cnt_M_lgc[4]         1           CTCFailedBuf_Cnt_M_lgc[6]         1           CTCFailedBuf_Cnt_M_lgc[6]         1           CTCFailedBuf_Cnt_M_lgc[7]         0           CTCFailedBuf_Cnt_M_lgc[8]         1           CTCFailedBuf_Cnt_M_lgc[10]         1           CTCFailedBuf_Cnt_M_lgc[10]         1           CTCFailedBuf_Cnt_M_lgc[11]         1           CTCFailedBuf_Cnt_M_lgc[12]         1           CTCFailedBuf_Cnt_M_lgc[13]         1
CTCFailedBuf_Cnt_M_lgc[1]       1         CTCFailedBuf_Cnt_M_lgc[2]       1         CTCFailedBuf_Cnt_M_lgc[3]       1         CTCFailedBuf_Cnt_M_lgc[4]       1         CTCFailedBuf_Cnt_M_lgc[5]       1         CTCFailedBuf_Cnt_M_lgc[6]       1         CTCFailedBuf_Cnt_M_lgc[7]       0         CTCFailedBuf_Cnt_M_lgc[8]       1         CTCFailedBuf_Cnt_M_lgc[9]       1         CTCFailedBuf_Cnt_M_lgc[10]       1         CTCFailedBuf_Cnt_M_lgc[11]       1         CTCFailedBuf_Cnt_M_lgc[12]       1
CTCFailedBuf_Cnt_M_lgc[2]       1         CTCFailedBuf_Cnt_M_lgc[3]       1         CTCFailedBuf_Cnt_M_lgc[4]       1         CTCFailedBuf_Cnt_M_lgc[5]       1         CTCFailedBuf_Cnt_M_lgc[6]       1         CTCFailedBuf_Cnt_M_lgc[7]       0         CTCFailedBuf_Cnt_M_lgc[8]       1         CTCFailedBuf_Cnt_M_lgc[9]       1         CTCFailedBuf_Cnt_M_lgc[10]       1         CTCFailedBuf_Cnt_M_lgc[11]       1         CTCFailedBuf_Cnt_M_lgc[12]       1
CTCFailedBuf_Cnt_M_lgc[3]       1         CTCFailedBuf_Cnt_M_lgc[4]       1         CTCFailedBuf_Cnt_M_lgc[5]       1         CTCFailedBuf_Cnt_M_lgc[6]       1         CTCFailedBuf_Cnt_M_lgc[7]       0         CTCFailedBuf_Cnt_M_lgc[8]       1         CTCFailedBuf_Cnt_M_lgc[9]       1         CTCFailedBuf_Cnt_M_lgc[10]       1         CTCFailedBuf_Cnt_M_lgc[11]       1         CTCFailedBuf_Cnt_M_lgc[12]       1
CTCFailedBuf_Cnt_M_lgc[4]       1         CTCFailedBuf_Cnt_M_lgc[5]       1         CTCFailedBuf_Cnt_M_lgc[6]       1         CTCFailedBuf_Cnt_M_lgc[7]       0         CTCFailedBuf_Cnt_M_lgc[8]       1         CTCFailedBuf_Cnt_M_lgc[9]       1         CTCFailedBuf_Cnt_M_lgc[10]       1         CTCFailedBuf_Cnt_M_lgc[11]       1         CTCFailedBuf_Cnt_M_lgc[12]       1
CTCFailedBuf_Cnt_M_lgc[5]       1         CTCFailedBuf_Cnt_M_lgc[6]       1         CTCFailedBuf_Cnt_M_lgc[7]       0         CTCFailedBuf_Cnt_M_lgc[8]       1         CTCFailedBuf_Cnt_M_lgc[9]       1         CTCFailedBuf_Cnt_M_lgc[10]       1         CTCFailedBuf_Cnt_M_lgc[11]       1         CTCFailedBuf_Cnt_M_lgc[12]       1
CTCFailedBuf_Cnt_M_lgc[6]       1         CTCFailedBuf_Cnt_M_lgc[7]       0         CTCFailedBuf_Cnt_M_lgc[8]       1         CTCFailedBuf_Cnt_M_lgc[9]       1         CTCFailedBuf_Cnt_M_lgc[10]       1         CTCFailedBuf_Cnt_M_lgc[11]       1         CTCFailedBuf_Cnt_M_lgc[12]       1
CTCFailedBuf_Cnt_M_lgc[7]       0         CTCFailedBuf_Cnt_M_lgc[8]       1         CTCFailedBuf_Cnt_M_lgc[9]       1         CTCFailedBuf_Cnt_M_lgc[10]       1         CTCFailedBuf_Cnt_M_lgc[11]       1         CTCFailedBuf_Cnt_M_lgc[12]       1
CTCFailedBuf_Cnt_M_lgc[8]       1         CTCFailedBuf_Cnt_M_lgc[9]       1         CTCFailedBuf_Cnt_M_lgc[10]       1         CTCFailedBuf_Cnt_M_lgc[11]       1         CTCFailedBuf_Cnt_M_lgc[12]       1
CTCFailedBuf_Cnt_M_lgc[9]       1         CTCFailedBuf_Cnt_M_lgc[10]       1         CTCFailedBuf_Cnt_M_lgc[11]       1         CTCFailedBuf_Cnt_M_lgc[12]       1
CTCFailedBuf_Cnt_M_lgc[10]       1         CTCFailedBuf_Cnt_M_lgc[11]       1         CTCFailedBuf_Cnt_M_lgc[12]       1
CTCFailedBuf_Cnt_M_lgc[11]         1           CTCFailedBuf_Cnt_M_lgc[12]         1
CTCFailedBuf_Cnt_M_lgc[12] 1
CTCEgilodPuf Cnt M Igg[12]
CTCFailedBuf_Cnt_M_lgc[14] 1
CTCFailedBuf_Cnt_M_lgc[15] 1
CTCFailedBuf_Cnt_M_lgc[16] 1
CTCFailedBuf_Cnt_M_lgc[17] 1
CTCFailedBuf_Cnt_M_lgc[18]
CTCFailedBuf_Cnt_M_lgc[19] 1
CTCFailedBuf_Cnt_M_lgc[20] 0
CTCFailedBuf_Cnt_M_lgc[21] 0
CTCFailedBuf_Cnt_M_lgc[22] 0
CTCFailedBuf_Cnt_M_lgc[23] 1
CTCFailedBuf_Cnt_M_lgc[24] 1
CTCFailedBuf_Cnt_M_lgc[25] 1
CTCFailedBuf_Cnt_M_lgc[26] 1
CTCFailedBuf_Cnt_M_lgc[27] 1
CTCFailedBuf_Cnt_M_lgc[28] 1

2018-04-10, 18:44:44+0530



DemIt_DTCS	Ch n e	TAZOICAL
Name		Input Value
CTCFailedBuf_Cnt_M	1 lgc[29]	1
CTCFailedBuf_Cnt_M		1
CTCFailedBuf_Cnt_M		1
CTCFailedBuf_Cnt_M		1
CTCFailedBuf_Cnt_M	1_lgc[33]	1.
CTCFailedBuf_Cnt_M	1_lgc[34]	0
CTCFailedBuf_Cnt_M	1_lgc[35]	0
CTCFailedBuf_Cnt_M	1_lgc[36]	0
CTCFailedBuf_Cnt_M	1_lgc[37]	0
CTCFailedBuf_Cnt_M	1_lgc[38]	0
CTCFailedBuf_Cnt_M	1_lgc[39]	0
CTCFailedBuf_Cnt_M	1_lgc[40]	0
CTCFailedBuf_Cnt_M	1_lgc[41]	0
CTCFailedBuf_Cnt_N	1_lgc[42]	0
CTCFailedBuf_Cnt_M	1_lgc[43]	0
CTCFailedBuf_Cnt_M	1_lgc[44]	0
CTCFailedBuf_Cnt_M		0
CTCFailedBuf_Cnt_M	1_lgc[46]	0
CTCFailedBuf_Cnt_M		1
CTCFailedBuf_Cnt_M		1
CTCFailedBuf_Cnt_M		1
CTCFailedBuf_Cnt_M		0
CTCFailedBuf_Cnt_M		1
CTCFailedBuf_Cnt_N		1
CTCFailedBuf_Cnt_M		1
CTCFailedBuf_Cnt_N		1
CTCFailedBuf_Cnt_N		1
CTCFailedBuf_Cnt_N		1
CTCFailedBuf_Cnt_M		1
CTCFailedBuf_Cnt_M		1
CTCFailedBuf_Cnt_M		0
CTCFailedBuf_Cnt_M CTCFailedBuf Cnt M		0
		0
CTCFailedBuf_Cnt_M		0
CTCFailedBuf_Cnt_M CTCFailed_Cnt_M_lg		0
DTC	6	1673189688
DTCKind		1
DTCStatusNew		238
DTCStatusOld		228
Dem_DTCNumberTal	ble[0]	46
Dem_DTCNumberTal		245
Dem_DTCNumberTal		24
Dem_DTCNumberTal		143
Dem_DTCNumberTal		13
Dem_DTCNumberTal		12
Dem_DTCNumberTal		209
Dem_DTCNumberTal		209
Dem_DTCNumberTal		46
Dem_DTCNumberTal		245
Dem_DTCNumberTal		209
Dem_DTCNumberTal		145
Dem_DTCNumberTal		245
Dem_DTCNumberTal		209
_		46
Dem DICNumberial		245
	DIE[15]	
Dem_DTCNumberTal		245
Dem_DTCNumberTal Dem_DTCNumberTal Dem_DTCNumberTal Dem_DTCNumberTal	ble[16]	245 209
Dem_DTCNumberTal	ble[16] ble[17]	

## **TEST DETAILS REPORT** Ch n e

DemIf\_DTCS



Denni_DTC3 Ch n e		i
Name	Input Value	
Dem_DTCNumberTable[20]	245	
Dem_DTCNumberTable[21]	209	
Dem_DTCNumberTable[22]	46	
Dem_DTCNumberTable[23]	24	
Dem_DTCNumberTable[24]	143	
Dem_DTCNumberTable[25]	13	
Dem_DTCNumberTable[26]	12	
Dem_DTCNumberTable[27]	245	
Dem_DTCNumberTable[28]	46	
Dem_DTCNumberTable[29]	245	
Dem_DTCNumberTable[30]	46	
Dem_DTCNumberTable[31]	46	
Dem_DTCNumberTable[32]	245	
em_DTCNumberTable[33]	245	
em_DTCNumberTable[34]	46	
lem_DTCNumberTable[35] lem_DTCNumberTable[36]	245 46	
em_DTCNumberTable[37]	46	
em_DTCNumberTable[38]	46	
Dem DTCNumberTable[39]	245	
em DTCNumberTable[40]	245	
em_DTCNumberTable[41]	24	
Dem_DTCNumberTable[42]	143	
Dem_DTCNumberTable[42]	13	
Dem_DTCNumberTable[44]	12	
Dem_DTCNumberTable[45]	209	
em_DTCNumberTable[46]	46	
em_DTCNumberTable[47]	245	
em_DTCNumberTable[48]	143	
em_DTCNumberTable[49]	46	
em_DTCNumberTable[50]	245	
em_DTCNumberTable[51]	46	
em_DTCNumberTable[52]	46	
em_DTCNumberTable[53]	245	
Dem_DTCNumberTable[54]	143	
em_DTCNumberTable[55]	209	
Dem_DTCNumberTable[56]	46	
Dem_DTCNumberTable[57]	245	
Dem_DTCNumberTable[58]	46	
Dem_DTCNumberTable[59]	209	
Dem_DTCNumberTable[60]	46	
dem_DTCNumberTable[61]	245	
em_DTCNumberTable[62]	143	
em_DTCNumberTable[63]	24 143	
em_DTCNumberTable[64] em_DTCNumberTable[65]	13	
	13	
Dem_DTCNumberTable[66] Dem_DTCNumberTable[67]	46	
em_DTCNumberTable[67] em_DTCNumberTable[68]	46	
em DTCNumberTable[69]	245	
em_DTCNumberTable[70]	143	
em_DTCNumberTable[71]	209	
em_DTCNumberTable[72]	143	
em_DTCNumberTable[73]	24	
em_DTCNumberTable[74]	143	
em DTCNumberTable[75]	13	
em_DTCNumberTable[76]	12	
em_DTC_FTB_Table[0]	107	
em_DTC_FTB_Table[1]	156	
em_DTC_FTB_Table[2]	5	
em_DTC_FTB_Table[3]	166	
em_DTC_FTB_Table[4]	182	
em_DTC_FTB_Table[5]	118	
em_DTC_FTB_Table[6]	237	
em_DTC_FTB_Table[7]	237	
em_DTC_FTB_Table[8]	107	
em_DTC_FTB_Table[9]	156	
em_DTC_FTB_Table[10]	237	
em_DTC_FTB_Table[11]	66	
em_DTC_FTB_Table[12]	156	
em_DTC_FTB_Table[13]	237	
em_DTC_FTB_Table[14]	107	
,	156	

2018-04-10, 18:44:44+0530



DemIf\_DTCS Input Value Dem\_DTC\_FTB\_Table[16] 156 Dem\_DTC\_FTB\_Table[17] 237 Dem\_DTC\_FTB\_Table[18] 106 Dem\_DTC\_FTB\_Table[19] 107 Dem\_DTC\_FTB\_Table[20] 156 Dem\_DTC\_FTB\_Table[21] 237 Dem\_DTC\_FTB\_Table[22] 107 Dem\_DTC\_FTB\_Table[23] 5 Dem\_DTC\_FTB\_Table[24] 166 Dem\_DTC\_FTB\_Table[25] 182 Dem\_DTC\_FTB\_Table[26] 118 Dem\_DTC\_FTB\_Table[27] 156 Dem\_DTC\_FTB\_Table[28] 107 Dem DTC FTB Table[29] 156 Dem\_DTC\_FTB\_Table[30] 107 Dem\_DTC\_FTB\_Table[31] 107 Dem\_DTC\_FTB\_Table[32] 156 Dem\_DTC\_FTB\_Table[33] 156 Dem\_DTC\_FTB\_Table[34] 107 Dem\_DTC\_FTB\_Table[35] 156 Dem\_DTC\_FTB\_Table[36] 107 Dem\_DTC\_FTB\_Table[37] 107 Dem\_DTC\_FTB\_Table[38] 107 Dem\_DTC\_FTB\_Table[39] 156 Dem\_DTC\_FTB\_Table[40] 156 Dem\_DTC\_FTB\_Table[41] 5 Dem\_DTC\_FTB\_Table[42] 166 Dem\_DTC\_FTB\_Table[43] 182 Dem\_DTC\_FTB\_Table[44] 118 Dem\_DTC\_FTB\_Table[45] 237 Dem DTC FTB Table[46] 107 Dem\_DTC\_FTB\_Table[47] 156 Dem DTC FTB Table[48] 166 Dem\_DTC\_FTB\_Table[49] 107 Dem\_DTC\_FTB\_Table[50] 156 Dem DTC FTB Table[51] 107 Dem\_DTC\_FTB\_Table[52] 107 Dem\_DTC\_FTB\_Table[53] 156 Dem\_DTC\_FTB\_Table[54] 166 Dem DTC FTB Table[55] 237 Dem\_DTC\_FTB\_Table[56] 107 Dem DTC FTB Table[57] 156 Dem\_DTC\_FTB\_Table[58] 107 Dem\_DTC\_FTB\_Table[59] 237 Dem\_DTC\_FTB\_Table[60] 107 Dem\_DTC\_FTB\_Table[61] 156 166 Dem\_DTC\_FTB\_Table[62] Dem\_DTC\_FTB\_Table[63] 5 Dem\_DTC\_FTB\_Table[64] 166 Dem\_DTC\_FTB\_Table[65] 182 Dem\_DTC\_FTB\_Table[66] 118 Dem\_DTC\_FTB\_Table[67] 107 Dem\_DTC\_FTB\_Table[68] 107 Dem\_DTC\_FTB\_Table[69] 156 Dem\_DTC\_FTB\_Table[70] 166 Dem\_DTC\_FTB\_Table[71] 237 Dem\_DTC\_FTB\_Table[72] 166 Dem\_DTC\_FTB\_Table[73] 5 Dem\_DTC\_FTB\_Table[74] 166 Dem\_DTC\_FTB\_Table[75] 182 Dem\_DTC\_FTB\_Table[76] 118 **Actual Value Expected Value** Result CTCFailedBuf\_Cnt\_M\_lgc[0] CTCFailedBuf\_Cnt\_M\_lgc[1] CTCFailedBuf\_Cnt\_M\_lgc[2] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[3] 1 CTCFailedBuf\_Cnt\_M\_lgc[4] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[5] 1 1 CTCFailedBuf Cnt M Igc[6] 1 CTCFailedBuf\_Cnt\_M\_lgc[7] 0 0

1

1

1

1

CTCFailedBuf\_Cnt\_M\_lgc[8]

CTCFailedBuf\_Cnt\_M\_lgc[9]

CTCFailedBuf\_Cnt\_M\_lgc[10]

**~** 

## **TEST DETAILS REPORT** Ch n e

Demlf\_DTCS





Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[11]	1	1	~
CTCFailedBuf_Cnt_M_lgc[12]	1	1	~
CTCFailedBuf_Cnt_M_lgc[13]	1	1	~
CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15]	1	1	~
CTCFailedBuf_Cnt_M_lgc[16]	1	1	-
CTCFailedBuf_Cnt_M_lgc[17]	1	1	~
CTCFailedBuf_Cnt_M_lgc[18]	1	1	~
CTCFailedBuf_Cnt_M_lgc[19]	1	1	~
CTCFailedBuf_Cnt_M_lgc[20]	0	0	~
CTCFailedBuf_Cnt_M_lgc[21]	0	0	~
CTCFailedBuf_Cnt_M_lgc[22]	0	0	~
CTCFailedBuf_Cnt_M_lgc[23]	1	1	~
CTCFailedBuf_Cnt_M_lgc[24]	1	1	~
CTCFailedBuf_Cnt_M_lgc[25]	1	1	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[26]	1	1	~
CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28]	1	1	
CTCFailedBuf_Cnt_M_lgc[29]	1	1	~
CTCFailedBuf_Cnt_M_lgc[30]	1	1	-
CTCFailedBuf_Cnt_M_lgc[31]	1	1	~
CTCFailedBuf_Cnt_M_lgc[32]	1	1	~
CTCFailedBuf_Cnt_M_lgc[33]	1	1	~
CTCFailedBuf_Cnt_M_lgc[34]	0	0	~
CTCFailedBuf_Cnt_M_lgc[35]	0	0	~
CTCFailedBuf_Cnt_M_lgc[36]	0	0	~
CTCFailedBuf_Cnt_M_lgc[37]	0	0	~
CTCFailedBuf_Cnt_M_lgc[38]	0	0	~
CTCFailedBuf_Cnt_M_lgc[39]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[40]	0	0	~
CTCFailedBuf_Cnt_M_lgc[41] CTCFailedBuf_Cnt_M_lgc[42]	0	0	
CTCFailedBuf_Cnt_M_lgc[43]	0	0	~
CTCFailedBuf_Cnt_M_lgc[44]	0	0	•
CTCFailedBuf_Cnt_M_lgc[45]	0	0	•
CTCFailedBuf_Cnt_M_lgc[46]	0	0	~
CTCFailedBuf_Cnt_M_lgc[47]	0	0	~
CTCFailedBuf_Cnt_M_lgc[48]	0	0	~
CTCFailedBuf_Cnt_M_lgc[49]	0	0	•
CTCFailedBuf_Cnt_M_lgc[50]	0	0	~
CTCFailedBuf_Cnt_M_lgc[51]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[52]	0	0	~
CTCFailedBuf_Cnt_M_Igc[53] CTCFailedBuf_Cnt_M_Igc[54]	1	1	
CTCFailedBuf_Cnt_M_lgc[55]	1	1	~
CTCFailedBuf Cnt M lgc[56]	0	0	~
CTCFailedBuf_Cnt_M_lgc[57]	1	1	~
CTCFailedBuf_Cnt_M_lgc[58]	1	1	~
CTCFailedBuf_Cnt_M_lgc[59]	1	1	~
CTCFailedBuf_Cnt_M_lgc[60]	1	1	~
CTCFailedBuf_Cnt_M_lgc[61]	1	1	~
CTCFailedBuf_Cnt_M_lgc[62]	1	1	~
CTCFailedBuf_Cnt_M_lgc[63]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[64]	0	1	~
CTCFailedBuf_Cnt_M_lgc[65] CTCFailedBuf_Cnt_M_lgc[66]	0	0	
CTCFailedBuf_Cnt_M_lgc[67]	0	0	~
CTCFailedBuf_Cnt_M_lgc[68]	0	0	-
CTCFailedBuf_Cnt_M_lgc[69]	0	0	~
CTCFailedBuf_Cnt_M_lgc[70]	0	0	~
CTCFailedBuf_Cnt_M_lgc[71]	0	0	~
CTCFailedBuf_Cnt_M_lgc[72]	0	0	~
CTCFailedBuf_Cnt_M_lgc[73]	0	0	~
CTCFailedBuf_Cnt_M_lgc[74]	0	0	~
CTCFailedBuf_Cnt_M_lgc[75]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[76]	0	0	~
CTCFailed_Cnt_M_lgc	0	0	<b>V</b>
Demlf_DTCStatusChanged()	0	0	<b>✓</b>
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	U	,	

Demlf\_DTCS



Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte Write An Demlf CTCFailed Cnt loc	1	Rte Write An Demlf CTCFailed Cnt loc	1	_

Test Step 2.18 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	0
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_Igc[9] CTCFailedBuf_Cnt_M_Igc[10]	1
CTCFailedBuf Cnt M lgc[11]	0
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	0
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	0
CTCFailedBuf_Cnt_M_lgc[34] CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf Cnt M Igc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45] CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_igc[47]	0
CTCFailedBuf_Cnt_M_gc[47] CTCFailedBuf Cnt M lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1.
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58] CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1.

## **TEST DETAILS REPORT** Ch n e

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Name	Input Value
CTCFailedBuf_Cnt_M_lgc[64]	1
CTCFailedBuf_Cnt_M_lgc[65]	0
CTCFailedBuf_Cnt_M_lgc[66]	0
CTCFailedBuf_Cnt_M_lgc[67]	0
CTCFailedBuf Cnt M lgc[68]	0
CTCFailedBuf_Cnt_M_lgc[69]	0
CTCFailedBuf_Cnt_M_lgc[70]	0
CTCFailedBuf_Cnt_M_lgc[71]	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	0
CTCFailedBuf_Cnt_M_lgc[74]	1
	0
CTCFailedBuf_Cnt_M_lgc[75]	0
CTCFailedBuf_Cnt_M_lgc[76]	1
CTCFailed_Cnt_M_lgc	
DTC	3302797192
DTCKind	1
DTCStatusNew	172
DTCStatusOld	91
Dem_DTCNumberTable[0]	112
Dem_DTCNumberTable[1]	227
Dem_DTCNumberTable[2]	76
Dem_DTCNumberTable[3]	252
Dem_DTCNumberTable[4]	240
Dem_DTCNumberTable[5]	206
Dem_DTCNumberTable[6]	62
Dem_DTCNumberTable[7]	62
Dem_DTCNumberTable[8]	112
Dem_DTCNumberTable[9]	227
Dem_DTCNumberTable[10]	62
Dem_DTCNumberTable[11]	80
Dem_DTCNumberTable[12]	227
Dem_DTCNumberTable[13]	62
Dem_DTCNumberTable[14]	112
Dem_DTCNumberTable[15]	227
Dem_DTCNumberTable[16]	227
Dem_DTCNumberTable[17]	62
Dem_DTCNumberTable[18]	57
Dem DTCNumberTable[19]	112
Dem_DTCNumberTable[20]	227
Dem_DTCNumberTable[21]	62
Dem_DTCNumberTable[22]	112
Dem DTCNumberTable[23]	76
Dem_DTCNumberTable[24]	252
Dem_DTCNumberTable[24] Dem_DTCNumberTable[25]	240
Dem DTCNumberTable[25]	
	206
Dem_DTCNumberTable[27]	227
Dem_DTCNumberTable[28]	112
Dem_DTCNumberTable[29]	227
Dem_DTCNumberTable[30]	112
Dem_DTCNumberTable[31]	112
Dem_DTCNumberTable[32]	227
Dem_DTCNumberTable[33]	227
Dem_DTCNumberTable[34]	112
Dem_DTCNumberTable[35]	227
Dem_DTCNumberTable[36]	112
Dem_DTCNumberTable[37]	112
Dem_DTCNumberTable[38]	112
Dem_DTCNumberTable[39]	227
Dem_DTCNumberTable[40]	227
Dem_DTCNumberTable[41]	76
Dem_DTCNumberTable[42]	252
Dem_DTCNumberTable[43]	240
Dem_DTCNumberTable[44]	206
Dem_DTCNumberTable[45]	62
Dem_DTCNumberTable[46]	112
Dem_DTCNumberTable[47]	227
Dem_DTCNumberTable[47] Dem_DTCNumberTable[48]	252
Dem_DTCNumberTable[49]	112
Dem_DTCNumberTable[50]	227
	112
	110
Dem_DTCNumberTable[52]	112
Dem_DTCNumberTable[51]  Dem_DTCNumberTable[52]  Dem_DTCNumberTable[53]  Dem_DTCNumberTable[54]	112 227 252

2018-04-10, 18:44:44+0530



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Name	Input Value	
Dem_DTCNumberTable[55]	62	
Dem_DTCNumberTable[56]	112	
Dem_DTCNumberTable[57]	227	
Dem_DTCNumberTable[58]	112	
Dem_DTCNumberTable[59]	62	
Dem_DTCNumberTable[60]	112	
Dem_DTCNumberTable[61]	227	
Dem_DTCNumberTable[62]	252	
Dem_DTCNumberTable[63]	76	
Dem_DTCNumberTable[64]	252	
Dem_DTCNumberTable[65]	240	
Dem_DTCNumberTable[66]	206	
Dem_DTCNumberTable[67]	112	
Dem_DTCNumberTable[68]	112	
Dem_DTCNumberTable[69]	227	
Dem_DTCNumberTable[70]	252	
Dem_DTCNumberTable[71]	62	
Dem_DTCNumberTable[72]	252	
Dem_DTCNumberTable[73]	76	
Dem_DTCNumberTable[74]	252	
Dem_DTCNumberTable[75]	240	
Dem_DTCNumberTable[76]	206	
Dem_DTC_FTB_Table[0]	219	
Dem_DTC_FTB_Table[1]	237	
Dem_DTC_FTB_Table[2]	46	
Dem_DTC_FTB_Table[3]	187	
Dem_DTC_FTB_Table[4]	250	
Dem_DTC_FTB_Table[5]	36	
Dem_DTC_FTB_Table[6]	202	
Dem_DTC_FTB_Table[7]	202	
Dem_DTC_FTB_Table[8]	219	
Dem_DTC_FTB_Table[9]	237	
Dem_DTC_FTB_Table[10]	202	
Dem_DTC_FTB_Table[11]	126	
Dem_DTC_FTB_Table[12]	237	
Dem_DTC_FTB_Table[13]	202	
Dem_DTC_FTB_Table[14]	219	
Dem_DTC_FTB_Table[15]	237	
Dem DTC FTB Table[16]	237	
Dem_DTC_FTB_Table[17]	202	
Dem_DTC_FTB_Table[18]	86	
Dem_DTC_FTB_Table[19]	219	
Dem_DTC_FTB_Table[20]	237	
Dem_DTC_FTB_Table[21]	202	
Dem_DTC_FTB_Table[22]	219	
Dem_DTC_FTB_Table[23]	46	
Dem_DTC_FTB_Table[24]	187	
Dem_DTC_FTB_Table[25]	250	
Dem_DTC_FTB_Table[25]	36	
	237	
Dem_DTC_FTB_Table[27] Dem DTC FTB Table[28]	219	
Dem_DTC_FTB_Table[28]  Dem_DTC_FTB_Table[29]	237	
Dem_DTC_FTB_Table[29]	219	
Dem_DTC_FTB_Table[30]	219	
Dem_DTC_FTB_Table[31]	219	
	237	
Dem_DTC_FTB_Table[33]	237	
Dem_DTC_FTB_Table[34]		
Dem_DTC_FTB_Table[35]	237	
Dem_DTC_FTB_Table[36]	219	
Dem_DTC_FTB_Table[37]	219	
Dem_DTC_FTB_Table[38]	219	
Dem_DTC_FTB_Table[39]	237	
Dem_DTC_FTB_Table[40]	237	
Dem_DTC_FTB_Table[41]	46	
Dem_DTC_FTB_Table[42]	187	
Dem_DTC_FTB_Table[43]	250	
Dem_DTC_FTB_Table[44]	36	
Dem_DTC_FTB_Table[45]	202	
Dem_DTC_FTB_Table[46]	219	
Dem_DTC_FTB_Table[47]	237	
Dem_DTC_FTB_Table[48]	187	
Dem_DTC_FTB_Table[49]	219	
Dem_DTC_FTB_Table[50]	237	

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value Dem\_DTC\_FTB\_Table[51] 219 Dem\_DTC\_FTB\_Table[52] 219 Dem DTC\_FTB\_Table[53] 237 Dem\_DTC\_FTB\_Table[54] 187 Dem\_DTC\_FTB\_Table[55] 202 Dem\_DTC\_FTB\_Table[56] 219 Dem\_DTC\_FTB\_Table[57] 237 Dem\_DTC\_FTB\_Table[58] 219 Dem\_DTC\_FTB\_Table[59] 202 Dem\_DTC\_FTB\_Table[60] 219 Dem\_DTC\_FTB\_Table[61] 237 Dem\_DTC\_FTB\_Table[62] 187 Dem\_DTC\_FTB\_Table[63] 46 Dem\_DTC\_FTB\_Table[64] 187 Dem\_DTC\_FTB\_Table[65] 250 Dem DTC FTB Table[66] 36 Dem\_DTC\_FTB\_Table[67] 219 Dem\_DTC\_FTB\_Table[68] 219 Dem\_DTC\_FTB\_Table[69] 237 Dem\_DTC\_FTB\_Table[70] 187 Dem\_DTC\_FTB\_Table[71] 202 Dem\_DTC\_FTB\_Table[72] 187 Dem\_DTC\_FTB\_Table[73] 46 Dem\_DTC\_FTB\_Table[74] 187 Dem\_DTC\_FTB\_Table[75] 250 Dem\_DTC\_FTB\_Table[76] 36 Name **Actual Value Expected Value** Result CTCFailedBuf Cnt M Igc[0] 1 CTCFailedBuf\_Cnt\_M\_lgc[1] CTCFailedBuf\_Cnt\_M\_lgc[2] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[3] 0 0 CTCFailedBuf Cnt M lgc[4] 1 CTCFailedBuf\_Cnt\_M\_lgc[5] 1 1 CTCFailedBuf Cnt M Igc[6] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[7] 1 CTCFailedBuf\_Cnt\_M\_lgc[8] CTCFailedBuf\_Cnt\_M\_lgc[9] CTCFailedBuf\_Cnt\_M\_lgc[10] CTCFailedBuf\_Cnt\_M\_lgc[11] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[12] CTCFailedBuf Cnt M lqc[13] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[14] CTCFailedBuf\_Cnt\_M\_lgc[15] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[16] **~** CTCFailedBuf\_Cnt\_M\_lgc[17] 1 CTCFailedBuf\_Cnt\_M\_lgc[18] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[19] 1 1 V CTCFailedBuf\_Cnt\_M\_lgc[20] n 0 CTCFailedBuf\_Cnt\_M\_lgc[21] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[22] n n CTCFailedBuf\_Cnt\_M\_lgc[23] 1 CTCFailedBuf Cnt M lqc[24] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[25] CTCFailedBuf\_Cnt\_M\_lgc[26] CTCFailedBuf\_Cnt\_M\_lgc[27] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[28] 1  $CTCFailedBuf\_Cnt\_M\_lgc[29]$ 1 CTCFailedBuf\_Cnt\_M\_lgc[30] CTCFailedBuf\_Cnt\_M\_lgc[31] 1 CTCFailedBuf\_Cnt\_M\_lgc[32] 1 CTCFailedBuf\_Cnt\_M\_lgc[33] 1 1 0 CTCFailedBuf\_Cnt\_M\_lgc[34] 0 CTCFailedBuf\_Cnt\_M\_lgc[35] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[36] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[37] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[38] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[39] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[40] 0 0 CTCFailedBuf Cnt M Igc[41] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[42] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[43] 0 0 ~ CTCFailedBuf\_Cnt\_M\_lgc[44] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[45] 0 0

Rte\_Write\_Ap\_DemIf\_CTCFailed\_Cnt\_lgc(data)

DemIf\_DTCS

2018-04-10, 18:44:44+0530



**Actual Value Expected Value** CTCFailedBuf\_Cnt\_M\_lgc[46] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[47] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[48] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[49] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[50] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[51] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[52] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[53] 1 CTCFailedBuf\_Cnt\_M\_lgc[54] CTCFailedBuf\_Cnt\_M\_lgc[55] CTCFailedBuf\_Cnt\_M\_lgc[56] CTCFailedBuf\_Cnt\_M\_lgc[57] 1 CTCFailedBuf\_Cnt\_M\_lgc[58] CTCFailedBuf\_Cnt\_M\_lgc[59] CTCFailedBuf\_Cnt\_M\_lgc[60] CTCFailedBuf\_Cnt\_M\_lgc[61] 1 CTCFailedBuf\_Cnt\_M\_lgc[62] CTCFailedBuf\_Cnt\_M\_lgc[63] 1  $CTCFailedBuf\_Cnt\_M\_lgc[64]$ CTCFailedBuf\_Cnt\_M\_lgc[65] 0 0  $CTCFailedBuf\_Cnt\_M\_lgc[66]$ 0 0 CTCFailedBuf\_Cnt\_M\_lgc[67] 0 0  $CTCFailedBuf\_Cnt\_M\_lgc[68]$ 0 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[73] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[74] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[75] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 0 CTCFailed\_Cnt\_M\_lgc 1 1 Demlf DTCStatusChanged() 0 0

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	~

Test Step 2.19 (Repeat Count = 1)	🗸
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_Igc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_Igc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_Igc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value CTCFailedBuf\_Cnt\_M\_lgc[29] 1 CTCFailedBuf\_Cnt\_M\_lgc[30] CTCFailedBuf\_Cnt\_M\_lgc[31] 1 CTCFailedBuf\_Cnt\_M\_lgc[32] CTCFailedBuf\_Cnt\_M\_lgc[33] 1 CTCFailedBuf\_Cnt\_M\_lgc[34] 0 CTCFailedBuf\_Cnt\_M\_lgc[35] 0 CTCFailedBuf\_Cnt\_M\_lgc[36] 0 CTCFailedBuf\_Cnt\_M\_lgc[37] 0 CTCFailedBuf\_Cnt\_M\_lgc[38] n CTCFailedBuf\_Cnt\_M\_lgc[39] 0 CTCFailedBuf\_Cnt\_M\_lgc[40] n CTCFailedBuf\_Cnt\_M\_lgc[41] 0 CTCFailedBuf\_Cnt\_M\_lgc[42] n CTCFailedBuf\_Cnt\_M\_lgc[43] 0 CTCFailedBuf\_Cnt\_M\_lgc[44] 0 CTCFailedBuf\_Cnt\_M\_lgc[45] 0 CTCFailedBuf\_Cnt\_M\_lgc[46] 0  $CTCFailedBuf\_Cnt\_M\_lgc[47]$ 0 CTCFailedBuf\_Cnt\_M\_lgc[48] 0 CTCFailedBuf\_Cnt\_M\_lgc[49] 0 CTCFailedBuf\_Cnt\_M\_lgc[50] 0 CTCFailedBuf\_Cnt\_M\_lgc[51] 0 CTCFailedBuf\_Cnt\_M\_lgc[52] 0 CTCFailedBuf\_Cnt\_M\_lgc[53] 1 CTCFailedBuf\_Cnt\_M\_lgc[54] CTCFailedBuf\_Cnt\_M\_lgc[55] 1 CTCFailedBuf\_Cnt\_M\_lgc[56] CTCFailedBuf\_Cnt\_M\_lgc[57] 1 CTCFailedBuf\_Cnt\_M\_lgc[58] 1 CTCFailedBuf\_Cnt\_M\_lgc[59] 1 CTCFailedBuf\_Cnt\_M\_lgc[60] n CTCFailedBuf Cnt M Igc[61] 1 CTCFailedBuf\_Cnt\_M\_lgc[62] 1 CTCFailedBuf\_Cnt\_M\_lgc[63] CTCFailedBuf\_Cnt\_M\_lgc[64] 1 CTCFailedBuf\_Cnt\_M\_lgc[65] 0 CTCFailedBuf\_Cnt\_M\_lgc[66] 0 CTCFailedBuf\_Cnt\_M\_lgc[67] 0 CTCFailedBuf\_Cnt\_M\_lgc[68] 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 CTCFailedBuf Cnt M lqc[70] 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[73] CTCFailedBuf\_Cnt\_M\_lgc[74] 0 CTCFailedBuf\_Cnt\_M\_lgc[75] 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 CTCFailed\_Cnt\_M\_lgc 0 DTC 3645660753 DTCKind 1 DTCStatusNew 182 DTCStatusOld 237 Dem\_DTCNumberTable[0] 0 Dem\_DTCNumberTable[1] 0 Dem\_DTCNumberTable[2] 0 0 Dem\_DTCNumberTable[3] Dem DTCNumberTable[4] 0 0 Dem\_DTCNumberTable[5] Dem\_DTCNumberTable[6] 0 Dem\_DTCNumberTable[7] 0 Dem DTCNumberTable[8] 0 Dem\_DTCNumberTable[9] 0 Dem DTCNumberTable[10] 0 Dem\_DTCNumberTable[11] 0 Dem DTCNumberTable[12] 0 Dem\_DTCNumberTable[13] 0 Dem DTCNumberTable[14] 0 Dem\_DTCNumberTable[15] 0 Dem\_DTCNumberTable[16] 0 Dem\_DTCNumberTable[17] 0 Dem\_DTCNumberTable[18] 0 Dem\_DTCNumberTable[19] 0

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2018-04-10, 18:44:44+0530



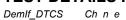
Name	Input Value
Dem_DTCNumberTable[20]	0
Dem DTCNumberTable[21]	0
Dem_DTCNumberTable[22]	0
Dem_DTCNumberTable[23]	0
Dem DTCNumberTable[24]	0
Dem DTCNumberTable[25]	0
Dem_DTCNumberTable[26]	0
Dem_DTCNumberTable[27]	0
Dem_DTCNumberTable[28]	0
Dem DTCNumberTable[29]	0
Dem_DTCNumberTable[30]	0
Dem DTCNumberTable[31]	0
Dem DTCNumberTable[32]	0
Dem_DTCNumberTable[33]	0
Dem_DTCNumberTable[34]	0
Dem_DTCNumberTable[35]	0
Dem_DTCNumberTable[36]	0
	0
Dem_DTCNumberTable[37]	0
Dem_DTCNumberTable[38]	0
Dem_DTCNumberTable[39]	
Dem_DTCNumberTable[40]	0
Dem_DTCNumberTable[41]	0
Dem_DTCNumberTable[42]	0
Dem_DTCNumberTable[43]	0
Dem_DTCNumberTable[44]	0
Dem_DTCNumberTable[45]	0
Dem_DTCNumberTable[46]	0
Dem_DTCNumberTable[47]	0
Dem_DTCNumberTable[48]	0
Dem_DTCNumberTable[49]	0
Dem_DTCNumberTable[50]	0
Dem_DTCNumberTable[51]	0
Dem_DTCNumberTable[52]	0
Dem_DTCNumberTable[53]	0
Dem_DTCNumberTable[54]	0
Dem_DTCNumberTable[55]	0
Dem_DTCNumberTable[56]	0
Dem_DTCNumberTable[57]	0
Dem_DTCNumberTable[58]	0
Dem_DTCNumberTable[59]	0
Dem_DTCNumberTable[60]	0
Dem_DTCNumberTable[61]	0
Dem_DTCNumberTable[62]	0
Dem_DTCNumberTable[63]	0
Dem_DTCNumberTable[64]	0
Dem_DTCNumberTable[65]	0
Dem_DTCNumberTable[66]	0
Dem_DTCNumberTable[67]	0
Dem_DTCNumberTable[68]	0
Dem_DTCNumberTable[69]	0
Dem_DTCNumberTable[70]	0
Dem_DTCNumberTable[71]	0
Dem_DTCNumberTable[72]	0
Dem_DTCNumberTable[73]	0
Dem_DTCNumberTable[74]	0
Dem_DTCNumberTable[75]	0
Dem_DTCNumberTable[76]	0
Dem_DTC_FTB_Table[0]	69
Dem_DTC_FTB_Table[1]	30
Dem_DTC_FTB_Table[2]	148
Dem_DTC_FTB_Table[3]	120
Dem_DTC_FTB_Table[4]	135
Dem_DTC_FTB_Table[5]	193
Dem_DTC_FTB_Table[6]	53
Dem_DTC_FTB_Table[7]	53
Dem_DTC_FTB_Table[8]	69
Dem_DTC_FTB_Table[9]	30
Dem_DTC_FTB_Table[10]	53
Dem_DTC_FTB_Table[11]	189
Dem_DTC_FTB_Table[12]	30
Dem_DTC_FTB_Table[13]	53
Dem_DTC_FTB_Table[14]	69
Dem_DTC_FTB_Table[15]	30

2018-04-10, 18:44:44+0530



Name	Input Value		
Dem_DTC_FTB_Table[16]	30		
Dem_DTC_FTB_Table[17]	53		
Dem_DTC_FTB_Table[18]	127		
Dem_DTC_FTB_Table[19]	69		
Dem_DTC_FTB_Table[20]	30		
Dem_DTC_FTB_Table[21]	53		
Dem_DTC_FTB_Table[22]	69		
Dem_DTC_FTB_Table[23] Dem_DTC_FTB_Table[24]	148 120		
Dem_DTC_FTB_Table[25]	135		
Dem_DTC_FTB_Table[26]	193		
Dem_DTC_FTB_Table[27]	30		
Dem_DTC_FTB_Table[28]	69		
Dem_DTC_FTB_Table[29]	30		
Dem_DTC_FTB_Table[30]	69		
Dem_DTC_FTB_Table[31]	69		
Dem_DTC_FTB_Table[32]	30		
Dem_DTC_FTB_Table[33]	30 69		
Dem_DTC_FTB_Table[34] Dem_DTC_FTB_Table[35]	30		
Dem_DTC_FTB_Table[36]	69		
Dem_DTC_FTB_Table[37]	69		
Dem_DTC_FTB_Table[38]	69		
Dem_DTC_FTB_Table[39]	30		
Dem_DTC_FTB_Table[40]	30		
Dem_DTC_FTB_Table[41]	148		
Dem_DTC_FTB_Table[42]	120		
Dem_DTC_FTB_Table[43]	135		
Dem_DTC_FTB_Table[44]	193 53		
Dem_DTC_FTB_Table[45] Dem_DTC_FTB_Table[46]	69		
Dem_DTC_FTB_Table[47]	30		
Dem_DTC_FTB_Table[48]	120		
Dem_DTC_FTB_Table[49]	69		
Dem_DTC_FTB_Table[50]	30		
Dem_DTC_FTB_Table[51]	69		
Dem_DTC_FTB_Table[52]	69		
Dem_DTC_FTB_Table[53]	30		
Dem_DTC_FTB_Table[54] Dem_DTC_FTB_Table[55]	120 53		
Dem_DTC_FTB_Table[56]	69		
Dem_DTC_FTB_Table[57]	30		
Dem_DTC_FTB_Table[58]	69		
Dem_DTC_FTB_Table[59]	53		
Dem_DTC_FTB_Table[60]	69		
Dem_DTC_FTB_Table[61]	30		
Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63]	120 148		
Dem DTC FTB Table[63]	120		
Dem DTC FTB Table[65]	135		
Dem_DTC_FTB_Table[66]	193		
Dem_DTC_FTB_Table[67]	69		
Dem_DTC_FTB_Table[68]	69		
Dem_DTC_FTB_Table[69]	30		
Dem_DTC_FTB_Table[70]	120		
Dem_DTC_FTB_Table[71]	53		
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73]	120 148		
Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74]	120		
Dem_DTC_FTB_Table[75]	135		
Dem_DTC_FTB_Table[76]	193		
Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[0]	1	1	~
CTCFailedBuf_Cnt_M_lgc[1]	1	1	•
CTCFailedBuf_Cnt_M_lgc[2]	1	1	~
CTCFailedBuf_Cnt_M_lgc[3]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[4]	1	1	<b>Y</b>
CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6]	1	1	,
CTCFailedBuf_Cnt_M_lgc[7]	1	1	·
CTCFailedBuf_Cnt_M_lgc[8]	1	1	~
CTCFailedBuf_Cnt_M_lgc[9]	1	1	•
CTCFailedBuf_Cnt_M_lgc[10]	1	1	~

2018-04-10, 18:44:44+0530





Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[11]	1	1	✓ ✓
CTCFailedBuf_Cnt_M_lgc[12]	1	1	~
CTCFailedBuf_Cnt_M_lgc[13]	1	1	~
CTCFailedBuf_Cnt_M_lgc[14]	1	1	~
CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16]	1	1	
CTCFailedBuf_Cnt_M_lgc[17]	1	1	•
CTCFailedBuf_Cnt_M_lgc[18]	1	1	~
CTCFailedBuf_Cnt_M_lgc[19]	1	1	~
CTCFailedBuf_Cnt_M_lgc[20]	0	0	~
CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22]	0	0	~
CTCFailedBuf_Cnt_M_lgc[23]	1	1	~
CTCFailedBuf_Cnt_M_lgc[24]	1	1	~
CTCFailedBuf_Cnt_M_lgc[25]	1	1	•
CTCFailedBuf_Cnt_M_lgc[26]	1	1	~
CTCFailedBuf_Cnt_M_lgc[27]	1	1	~
CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29]	1	1	~
CTCFailedBuf_Cnt_M_Igc[30]	1	1	~
CTCFailedBuf_Cnt_M_lgc[31]	1	1	•
CTCFailedBuf_Cnt_M_lgc[32]	1	1	~
CTCFailedBuf_Cnt_M_lgc[33]	1	1	•
CTCFailedBuf_Cnt_M_lgc[34] CTCFailedBuf Cnt M lgc[35]	0	0	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[36]	0	0	
CTCFailedBuf_Cnt_M_lgc[37]	0	0	•
CTCFailedBuf_Cnt_M_lgc[38]	0	0	•
CTCFailedBuf_Cnt_M_lgc[39]	0	0	•
CTCFailedBuf_Cnt_M_lgc[40]	0	0	~
CTCFailedBuf_Cnt_M_lgc[41] CTCFailedBuf_Cnt_M_lgc[42]	0	0	
CTCFailedBuf_Cnt_M_lgc[43]	0	0	~
CTCFailedBuf_Cnt_M_lgc[44]	0	0	•
CTCFailedBuf_Cnt_M_lgc[45]	0	0	•
CTCFailedBuf_Cnt_M_lgc[46]	0	0	~
CTCFailedBuf_Cnt_M_lgc[47] CTCFailedBuf_Cnt_M_lgc[48]	0	0	
CTCFailedBuf_Cnt_M_lgc[49]	0	0	•
CTCFailedBuf_Cnt_M_lgc[50]	0	0	•
CTCFailedBuf_Cnt_M_lgc[51]	0	0	•
CTCFailedBuf_Cnt_M_lgc[52]	0	0	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[53] CTCFailedBuf Cnt M lgc[54]	1	1	
CTCFailedBuf_Cnt_M_lgc[55]	1	1	•
CTCFailedBuf_Cnt_M_lgc[56]	1	1	•
CTCFailedBuf_Cnt_M_lgc[57]	1	1	~
CTCFailedBuf_Cnt_M_lgc[58]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[59] CTCFailedBuf_Cnt_M_lgc[60]	1	0	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[61]	1	1	~
CTCFailedBuf_Cnt_M_lgc[62]	1	1	•
CTCFailedBuf_Cnt_M_lgc[63]	1	1	~
CTCFailedBuf_Cnt_M_lgc[64]	1	1	~
CTCFailedBuf_Cnt_M_lgc[65]	0	0	~
CTCFailedBuf_Cnt_M_lgc[66] CTCFailedBuf_Cnt_M_lgc[67]	0	0	~
CTCFailedBuf_Cnt_M_lgc[68]	0	0	-
CTCFailedBuf_Cnt_M_lgc[69]	0	0	•
CTCFailedBuf_Cnt_M_lgc[70]	0	0	•
CTCFailedBuf_Cnt_M_lgc[71]	0	0	~
CTCFailedBuf_Cnt_M_lgc[72] CTCFailedBuf_Cnt_M_lgc[73]	0	0	-
CTCFailedBuf_Cnt_M_lgc[74]	0	0	-
CTCFailedBuf_Cnt_M_lgc[75]	0	0	~
CTCFailedBuf_Cnt_M_lgc[76]	0	0	•
CTCFailed_Cnt_M_lgc Demlf_DTCStatusChanged()	0	0	<b>*</b>
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc(data)	0	0	~

Demlf\_DTCS

2018-04-10, 18:44:44+0530



Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte Write An Demlf CTCFailed Cnt loc	1	Rte Write An Demlf CTCFailed Cnt loc	1	_

Test Step 2.20 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf Cnt M Igc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	
CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18]	0
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf Cnt M lgc[20]	0
CTCFailedBuf Cnt M Igc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_Igc[27] CTCFailedBuf_Cnt_M_Igc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36] CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[37] CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45] CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55] CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1.
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value CTCFailedBuf\_Cnt\_M\_lgc[64] CTCFailedBuf\_Cnt\_M\_lgc[65] 0 CTCFailedBuf\_Cnt\_M\_lgc[66] 0 CTCFailedBuf\_Cnt\_M\_lgc[67] 1 CTCFailedBuf Cnt M lqc[68] 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 CTCFailedBuf\_Cnt\_M\_lgc[73] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[74] CTCFailedBuf\_Cnt\_M\_lgc[75] 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 CTCFailed\_Cnt\_M\_lgc 1 DTC 4137755052 DTCKind 2 DTCStatusNew 250 DTCStatusOld 202 Dem\_DTCNumberTable[0] 65535 Dem\_DTCNumberTable[1] 65535 Dem\_DTCNumberTable[2] 65535 Dem\_DTCNumberTable[3] 65535 Dem\_DTCNumberTable[4] 65535 Dem\_DTCNumberTable[5] 65535 Dem DTCNumberTable[6] 65535 Dem\_DTCNumberTable[7] 65535 Dem DTCNumberTable[8] 65535 Dem\_DTCNumberTable[9] 65535 Dem DTCNumberTable[10] 65535 Dem\_DTCNumberTable[11] 65535 Dem DTCNumberTable[12] 65535 Dem\_DTCNumberTable[13] 65535 Dem DTCNumberTable[14] 65535 Dem\_DTCNumberTable[15] 65535 Dem\_DTCNumberTable[16] 65535 Dem\_DTCNumberTable[17] 65535 Dem\_DTCNumberTable[18] 65535 Dem\_DTCNumberTable[19] 65535 Dem\_DTCNumberTable[20] 65535 Dem\_DTCNumberTable[21] 65535 Dem\_DTCNumberTable[22] 65535 Dem\_DTCNumberTable[23] 65535 Dem\_DTCNumberTable[24] 65535 Dem\_DTCNumberTable[25] 65535 Dem\_DTCNumberTable[26] 65535 Dem\_DTCNumberTable[27] 65535 Dem DTCNumberTable[28] 65535 Dem\_DTCNumberTable[29] 65535 Dem DTCNumberTable[30] 65535 Dem\_DTCNumberTable[31] 65535 Dem DTCNumberTable[32] 65535 Dem\_DTCNumberTable[33] 65535 Dem\_DTCNumberTable[34] 65535 Dem\_DTCNumberTable[35] 65535 Dem\_DTCNumberTable[36] 65535 Dem\_DTCNumberTable[37] 65535 Dem\_DTCNumberTable[38] 65535 Dem\_DTCNumberTable[39] 65535 Dem\_DTCNumberTable[40] 65535 Dem\_DTCNumberTable[41] 65535 Dem\_DTCNumberTable[42] 65535 65535 Dem\_DTCNumberTable[43] Dem\_DTCNumberTable[44] 65535 Dem\_DTCNumberTable[45] 65535 Dem\_DTCNumberTable[46] 65535 Dem DTCNumberTable[47] 65535 Dem\_DTCNumberTable[48] 65535 Dem DTCNumberTable[49] 65535 Dem DTCNumberTable[50] 65535 Dem\_DTCNumberTable[51] 65535 Dem DTCNumberTable[52] 65535 Dem\_DTCNumberTable[53] 65535 Dem\_DTCNumberTable[54] 65535

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Name Input Value Dem DTCNumberTable[55] 65535 Dem\_DTCNumberTable[56] 65535 Dem\_DTCNumberTable[57] 65535 Dem\_DTCNumberTable[58] 65535 65535 Dem\_DTCNumberTable[59] Dem\_DTCNumberTable[60] 65535 Dem\_DTCNumberTable[61] 65535 Dem\_DTCNumberTable[62] 65535 Dem\_DTCNumberTable[63] 65535 Dem DTCNumberTable[64] 65535 Dem\_DTCNumberTable[65] 65535 Dem\_DTCNumberTable[66] 65535 Dem\_DTCNumberTable[67] 65535 Dem DTCNumberTable[68] 65535 Dem\_DTCNumberTable[69] 65535 Dem\_DTCNumberTable[70] 65535 Dem\_DTCNumberTable[71] 65535 Dem\_DTCNumberTable[72] 65535 Dem\_DTCNumberTable[73] 65535 Dem\_DTCNumberTable[74] 65535 Dem\_DTCNumberTable[75] 65535 Dem\_DTCNumberTable[76] 65535 Dem\_DTC\_FTB\_Table[0] 254 Dem\_DTC\_FTB\_Table[1] 153 Dem\_DTC\_FTB\_Table[2] 91 Dem\_DTC\_FTB\_Table[3] 138 Dem\_DTC\_FTB\_Table[4] 54 Dem\_DTC\_FTB\_Table[5] 108 Dem\_DTC\_FTB\_Table[6] 239 Dem\_DTC\_FTB\_Table[7] 239 Dem DTC FTB Table[8] 254 Dem\_DTC\_FTB\_Table[9] 153 Dem DTC FTB Table[10] 239 Dem\_DTC\_FTB\_Table[11] 200 Dem\_DTC\_FTB\_Table[12] 153 Dem DTC FTB Table[13] 239 Dem\_DTC\_FTB\_Table[14] 254 Dem\_DTC\_FTB\_Table[15] 153 Dem\_DTC\_FTB\_Table[16] 153 Dem DTC FTB Table[17] 239 Dem\_DTC\_FTB\_Table[18] 33 Dem DTC FTB Table[19] 254 Dem\_DTC\_FTB\_Table[20] 153 Dem\_DTC\_FTB\_Table[21] 239 254 Dem\_DTC\_FTB\_Table[22] Dem\_DTC\_FTB\_Table[23] 91 138 Dem\_DTC\_FTB\_Table[24] Dem\_DTC\_FTB\_Table[25] 108 Dem\_DTC\_FTB\_Table[26] Dem\_DTC\_FTB\_Table[27] 153 Dem\_DTC\_FTB\_Table[28] 254 Dem\_DTC\_FTB\_Table[29] 153 Dem\_DTC\_FTB\_Table[30] 254 Dem\_DTC\_FTB\_Table[31] 254 Dem\_DTC\_FTB\_Table[32] 153 Dem\_DTC\_FTB\_Table[33] 153 Dem\_DTC\_FTB\_Table[34] 254 Dem\_DTC\_FTB\_Table[35] 153 Dem\_DTC\_FTB\_Table[36] 254 Dem\_DTC\_FTB\_Table[37] 254 Dem\_DTC\_FTB\_Table[38] 254 Dem DTC FTB Table[39] 153 Dem\_DTC\_FTB\_Table[40] 153 Dem\_DTC\_FTB\_Table[41] 91 Dem\_DTC\_FTB\_Table[42] 138 Dem DTC FTB Table[43] 54 Dem\_DTC\_FTB\_Table[44] 108 Dem DTC FTB Table[45] 239 Dem\_DTC\_FTB\_Table[46] 254 Dem\_DTC\_FTB\_Table[47] 153 Dem\_DTC\_FTB\_Table[48] 138 Dem\_DTC\_FTB\_Table[49] 254 Dem\_DTC\_FTB\_Table[50] 153

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value Dem\_DTC\_FTB\_Table[51] 254 Dem\_DTC\_FTB\_Table[52] 254 Dem DTC\_FTB\_Table[53] 153 Dem\_DTC\_FTB\_Table[54] 138 Dem\_DTC\_FTB\_Table[55] 239 Dem\_DTC\_FTB\_Table[56] 254 Dem\_DTC\_FTB\_Table[57] 153 Dem\_DTC\_FTB\_Table[58] 254 Dem\_DTC\_FTB\_Table[59] 239 Dem\_DTC\_FTB\_Table[60] 254 Dem\_DTC\_FTB\_Table[61] 153 138 Dem\_DTC\_FTB\_Table[62] Dem\_DTC\_FTB\_Table[63] 91 Dem\_DTC\_FTB\_Table[64] 138 Dem\_DTC\_FTB\_Table[65] 54 108 Dem DTC FTB Table[66] Dem\_DTC\_FTB\_Table[67] 254 Dem\_DTC\_FTB\_Table[68] 254 Dem\_DTC\_FTB\_Table[69] 153 Dem\_DTC\_FTB\_Table[70] 138 Dem\_DTC\_FTB\_Table[71] 239 Dem\_DTC\_FTB\_Table[72] 138 Dem\_DTC\_FTB\_Table[73] 91 Dem\_DTC\_FTB\_Table[74] 138 Dem\_DTC\_FTB\_Table[75] 54 Dem\_DTC\_FTB\_Table[76] 108 Name **Actual Value Expected Value** Result CTCFailedBuf Cnt M Igc[0] 1 CTCFailedBuf\_Cnt\_M\_lgc[1] CTCFailedBuf\_Cnt\_M\_lgc[2] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[3] 1 CTCFailedBuf Cnt M lgc[4] CTCFailedBuf\_Cnt\_M\_lgc[5] 1 1 CTCFailedBuf Cnt M Igc[6] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[7] 1 CTCFailedBuf\_Cnt\_M\_lgc[8] CTCFailedBuf\_Cnt\_M\_lgc[9] CTCFailedBuf\_Cnt\_M\_lgc[10] CTCFailedBuf\_Cnt\_M\_lgc[11] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[12] CTCFailedBuf Cnt M lqc[13] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[14] CTCFailedBuf\_Cnt\_M\_lgc[15] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[16] **~** CTCFailedBuf\_Cnt\_M\_lgc[17] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[18] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[19] 1 1 ~ CTCFailedBuf\_Cnt\_M\_lgc[20] n 0 CTCFailedBuf\_Cnt\_M\_lgc[21] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[22] n n CTCFailedBuf\_Cnt\_M\_lgc[23] 1 CTCFailedBuf Cnt M lqc[24] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[25] CTCFailedBuf\_Cnt\_M\_lgc[26] CTCFailedBuf\_Cnt\_M\_lgc[27] 1 CTCFailedBuf\_Cnt\_M\_lgc[28] 1  $CTCFailedBuf\_Cnt\_M\_lgc[29]$ 1 CTCFailedBuf\_Cnt\_M\_lgc[30] CTCFailedBuf\_Cnt\_M\_lgc[31] CTCFailedBuf\_Cnt\_M\_lgc[32] 1 CTCFailedBuf\_Cnt\_M\_lgc[33] 1 1 0 CTCFailedBuf\_Cnt\_M\_lgc[34] 0 CTCFailedBuf\_Cnt\_M\_lgc[35] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[36] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[37] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[38] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[39] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[40] 0 0 CTCFailedBuf Cnt M Igc[41] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[42] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[43] 0 0 V CTCFailedBuf\_Cnt\_M\_lgc[44] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[45] 0 0

DemIf\_DTCS

2018-04-10, 18:44:44+0530



**Actual Value Expected Value** CTCFailedBuf\_Cnt\_M\_lgc[46] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[47] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[48] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[49] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[50] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[51] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[52] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[53] 1 CTCFailedBuf\_Cnt\_M\_lgc[54] CTCFailedBuf\_Cnt\_M\_lgc[55] 1 CTCFailedBuf\_Cnt\_M\_lgc[56] CTCFailedBuf\_Cnt\_M\_lgc[57] 1 CTCFailedBuf\_Cnt\_M\_lgc[58] CTCFailedBuf\_Cnt\_M\_lgc[59] CTCFailedBuf\_Cnt\_M\_lgc[60] CTCFailedBuf\_Cnt\_M\_lgc[61] 1 CTCFailedBuf\_Cnt\_M\_lgc[62] CTCFailedBuf\_Cnt\_M\_lgc[63] 1 1  $CTCFailedBuf\_Cnt\_M\_lgc[64]$ 1 CTCFailedBuf\_Cnt\_M\_lgc[65] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[66] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[67] 1 1  $CTCFailedBuf\_Cnt\_M\_lgc[68]$ 0 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[73] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[74] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[75] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 0 CTCFailed\_Cnt\_M\_lgc 1 1 Demlf DTCStatusChanged() 0 0 Rte\_Write\_Ap\_DemIf\_CTCFailed\_Cnt\_lgc(data)

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte Write Ap Demlf CTCFailed Cnt lgc	1	Rte Write Ap Demlf CTCFailed Cnt lgc	1	~

Test Step 2.21 (Repeat Count = 1)	🗸
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	0
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	0
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	0
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_Igc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_Igc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_Igc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1

2018-04-10, 18:44:44+0530



Demlf_DTCS Ch n e	TOLO (AU
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	0
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_Igc[32]	1
CTCFailedBuf_Cnt_M_Igc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	1 0
CTCFailedBuf_Cnt_M_lgc[38] CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCF alledbut_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[42]	1
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	1
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	0
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58] CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFalledBuf_Cnt_M_lgc[59] CTCFalledBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1
CTCFailedBuf_Cnt_M_lgc[64]	1
CTCFailedBuf_Cnt_M_lgc[65]	0
CTCFailedBuf_Cnt_M_lgc[66]	0
CTCFailedBuf_Cnt_M_lgc[67]	0
CTCFailedBuf_Cnt_M_lgc[68]	0
CTCFailedBuf_Cnt_M_lgc[69]	0
CTCFailedBuf_Cnt_M_lgc[70]	0
CTCFailedBuf_Cnt_M_lgc[71]	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	0
CTCFailedBuf_Cnt_M_lgc[74] CTCFailedBuf_Cnt_M_lgc[75]	0
CTCFalledBuf_Cnt_M_lgc[76] CTCFalledBuf_Cnt_M_lgc[76]	0
CTCFalledBut_Cftt_M_lgc CTCFalled_Cnt_M_lgc	0
DTC	2969842604
DTCKind	1
DTCStatusNew	135
DTCStatusOld	53
Dem_DTCNumberTable[0]	219
Dem_DTCNumberTable[1]	237
Dem_DTCNumberTable[2]	46
Dem_DTCNumberTable[3]	187
Dem_DTCNumberTable[4]	250
Dem_DTCNumberTable[5]	36
Dem_DTCNumberTable[6]	202
Dem_DTCNumberTable[7]	202
Dem_DTCNumberTable[8]	219
Dem_DTCNumberTable[9]	237
Dem_DTCNumberTable[10]	202
Dem_DTCNumberTable[11]	126
Dem_DTCNumberTable[12]	237
Dem_DTCNumberTable[13]	202
Dem_DTCNumberTable[14]	219
Dem_DTCNumberTable[15]	237
Dem_DTCNumberTable[16]	237
Dem_DTCNumberTable[17]	202
Dem_DTCNumberTable[18] Dem_DTCNumberTable[19]	86 219
	413

Demlf\_DTCS

2018-04-10, 18:44:44+0530



Name Input Value Dem\_DTCNumberTable[20] 237 Dem\_DTCNumberTable[21] 202 Dem DTCNumberTable[22] 219 Dem\_DTCNumberTable[23] 46 Dem DTCNumberTable[24] 187 Dem\_DTCNumberTable[25] 250 Dem\_DTCNumberTable[26] 36 Dem\_DTCNumberTable[27] 237 Dem\_DTCNumberTable[28] 219 Dem\_DTCNumberTable[29] 237 Dem\_DTCNumberTable[30] 219 Dem\_DTCNumberTable[31] 219 Dem\_DTCNumberTable[32] 237 Dem\_DTCNumberTable[33] 237 Dem\_DTCNumberTable[34] 219 Dem\_DTCNumberTable[35] 237 Dem\_DTCNumberTable[36] 219 Dem\_DTCNumberTable[37] 219 Dem\_DTCNumberTable[38] 219 Dem\_DTCNumberTable[39] 237 Dem\_DTCNumberTable[40] 237 Dem\_DTCNumberTable[41] 46 Dem\_DTCNumberTable[42] 187 Dem\_DTCNumberTable[43] 250 Dem\_DTCNumberTable[44] 36 Dem\_DTCNumberTable[45] 202 Dem DTCNumberTable[46] 219 Dem\_DTCNumberTable[47] 237 Dem DTCNumberTable[48] 187 Dem\_DTCNumberTable[49] 219 Dem DTCNumberTable[50] 237 Dem\_DTCNumberTable[51] 219 Dem DTCNumberTable[52] 219 Dem\_DTCNumberTable[53] 237 Dem\_DTCNumberTable[54] 187 Dem\_DTCNumberTable[55] 202 Dem\_DTCNumberTable[56] 219 Dem\_DTCNumberTable[57] 237 Dem\_DTCNumberTable[58] 219 Dem\_DTCNumberTable[59] 202 Dem\_DTCNumberTable[60] 219 Dem\_DTCNumberTable[61] 237 Dem\_DTCNumberTable[62] 187 Dem\_DTCNumberTable[63] 46 Dem\_DTCNumberTable[64] 187 Dem\_DTCNumberTable[65] 250 Dem DTCNumberTable[66] 36 Dem\_DTCNumberTable[67] 219 Dem DTCNumberTable[68] 219 Dem\_DTCNumberTable[69] 237 Dem\_DTCNumberTable[70] 187 Dem\_DTCNumberTable[71] 202 Dem\_DTCNumberTable[72] 187 Dem\_DTCNumberTable[73] 46 Dem\_DTCNumberTable[74] 187 Dem\_DTCNumberTable[75] 250 Dem\_DTCNumberTable[76] 36 Dem\_DTC\_FTB\_Table[0] 157 Dem\_DTC\_FTB\_Table[1] 112 Dem\_DTC\_FTB\_Table[2] Dem\_DTC\_FTB\_Table[3] 195 200 Dem\_DTC\_FTB\_Table[4] Dem\_DTC\_FTB\_Table[5] 99 Dem\_DTC\_FTB\_Table[6] 203 Dem\_DTC\_FTB\_Table[7] 203 Dem DTC FTB Table[8] 157 Dem\_DTC\_FTB\_Table[9] Dem DTC FTB Table[10] 203 Dem\_DTC\_FTB\_Table[11] 201 Dem\_DTC\_FTB\_Table[12] 1 Dem\_DTC\_FTB\_Table[13] 203 Dem\_DTC\_FTB\_Table[14] 157 Dem\_DTC\_FTB\_Table[15] 1

2018-04-10, 18:44:44+0530



Name	In and Walter		
Name Dem_DTC_FTB_Table[16]	Input Value		
Dem_DTC_FTB_Table[17]	203		
Dem_DTC_FTB_Table[18]	101		
Dem_DTC_FTB_Table[19]	157		
Dem_DTC_FTB_Table[20]	1		
Dem_DTC_FTB_Table[21]	203		
Dem_DTC_FTB_Table[22]	157		
Dem_DTC_FTB_Table[23] Dem_DTC_FTB_Table[24]	112 195		
Dem_DTC_FTB_Table[24]	200		
Dem_DTC_FTB_Table[26]	99		
Dem_DTC_FTB_Table[27]	1		
Dem_DTC_FTB_Table[28]	157		
Dem_DTC_FTB_Table[29]	1		
Dem_DTC_FTB_Table[30] Dem_DTC_FTB_Table[31]	157 157		
Dem_DTC_FTB_Table[31]	1		
Dem_DTC_FTB_Table[33]	1		
Dem_DTC_FTB_Table[34]	157		
Dem_DTC_FTB_Table[35]	1		
Dem_DTC_FTB_Table[36]	157		
Dem_DTC_FTB_Table[37]	157 157		
Dem_DTC_FTB_Table[38] Dem_DTC_FTB_Table[39]	1		
Dem_DTC_FTB_Table[40]	1		
Dem_DTC_FTB_Table[41]	112		
Dem_DTC_FTB_Table[42]	195		
Dem_DTC_FTB_Table[43]	200		
Dem_DTC_FTB_Table[44] Dem_DTC_FTB_Table[45]	99 203		
Dem_DTC_FTB_Table[46]	157		
Dem_DTC_FTB_Table[47]	1		
Dem_DTC_FTB_Table[48]	195		
Dem_DTC_FTB_Table[49]	157		
Dem_DTC_FTB_Table[50]	1		
Dem_DTC_FTB_Table[51] Dem_DTC_FTB_Table[52]	157 157		
Dem_DTC_FTB_Table[52]	1		
Dem_DTC_FTB_Table[54]	195		
Dem_DTC_FTB_Table[55]	203		
Dem_DTC_FTB_Table[56]	157		
Dem_DTC_FTB_Table[57]	1		
	157		
Dem_DTC_FTB_Table[58]			
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59]	203		
Dem_DTC_FTB_Table[58]			
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62]	203 157 1 1		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63]	203 157 1 195 112		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64]	203 157 1 195 112		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65]	203 157 1 195 112 195 200		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66]	203 157 1 195 112		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65]	203 157 1 195 112 195 200 99		
Dem_DTC_FTB_Table[58]  Dem_DTC_FTB_Table[59]  Dem_DTC_FTB_Table[60]  Dem_DTC_FTB_Table[61]  Dem_DTC_FTB_Table[62]  Dem_DTC_FTB_Table[63]  Dem_DTC_FTB_Table[64]  Dem_DTC_FTB_Table[65]  Dem_DTC_FTB_Table[66]  Dem_DTC_FTB_Table[67]  Dem_DTC_FTB_Table[68]  Dem_DTC_FTB_Table[69]	203 157 1 195 112 195 200 99 157 157		
Dem_DTC_FTB_Table[58]  Dem_DTC_FTB_Table[59]  Dem_DTC_FTB_Table[60]  Dem_DTC_FTB_Table[61]  Dem_DTC_FTB_Table[62]  Dem_DTC_FTB_Table[63]  Dem_DTC_FTB_Table[64]  Dem_DTC_FTB_Table[65]  Dem_DTC_FTB_Table[66]  Dem_DTC_FTB_Table[67]  Dem_DTC_FTB_Table[68]  Dem_DTC_FTB_Table[69]  Dem_DTC_FTB_Table[69]	203 157 1 195 112 195 200 99 157 157 1		
Dem_DTC_FTB_Table[58]  Dem_DTC_FTB_Table[59]  Dem_DTC_FTB_Table[60]  Dem_DTC_FTB_Table[61]  Dem_DTC_FTB_Table[62]  Dem_DTC_FTB_Table[63]  Dem_DTC_FTB_Table[64]  Dem_DTC_FTB_Table[65]  Dem_DTC_FTB_Table[66]  Dem_DTC_FTB_Table[67]  Dem_DTC_FTB_Table[68]  Dem_DTC_FTB_Table[69]  Dem_DTC_FTB_Table[70]  Dem_DTC_FTB_Table[71]	203 157 1 195 112 195 200 99 157 157 1 195 203		
Dem_DTC_FTB_Table[58]  Dem_DTC_FTB_Table[59]  Dem_DTC_FTB_Table[60]  Dem_DTC_FTB_Table[61]  Dem_DTC_FTB_Table[62]  Dem_DTC_FTB_Table[63]  Dem_DTC_FTB_Table[64]  Dem_DTC_FTB_Table[65]  Dem_DTC_FTB_Table[66]  Dem_DTC_FTB_Table[67]  Dem_DTC_FTB_Table[68]  Dem_DTC_FTB_Table[69]  Dem_DTC_FTB_Table[71]  Dem_DTC_FTB_Table[72]	203 157 1 195 112 195 200 99 157 157 1 195 203		
Dem_DTC_FTB_Table[58]  Dem_DTC_FTB_Table[59]  Dem_DTC_FTB_Table[60]  Dem_DTC_FTB_Table[61]  Dem_DTC_FTB_Table[62]  Dem_DTC_FTB_Table[63]  Dem_DTC_FTB_Table[64]  Dem_DTC_FTB_Table[65]  Dem_DTC_FTB_Table[66]  Dem_DTC_FTB_Table[67]  Dem_DTC_FTB_Table[68]  Dem_DTC_FTB_Table[69]  Dem_DTC_FTB_Table[71]  Dem_DTC_FTB_Table[72]  Dem_DTC_FTB_Table[73]	203 157 1 195 112 195 200 99 157 157 1 195 203		
Dem_DTC_FTB_Table[58]  Dem_DTC_FTB_Table[59]  Dem_DTC_FTB_Table[60]  Dem_DTC_FTB_Table[61]  Dem_DTC_FTB_Table[62]  Dem_DTC_FTB_Table[63]  Dem_DTC_FTB_Table[64]  Dem_DTC_FTB_Table[65]  Dem_DTC_FTB_Table[66]  Dem_DTC_FTB_Table[67]  Dem_DTC_FTB_Table[68]  Dem_DTC_FTB_Table[69]  Dem_DTC_FTB_Table[71]  Dem_DTC_FTB_Table[72]	203 157 1 195 112 195 200 99 157 157 1 195 203		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74]	203 157 1 195 112 195 200 99 157 157 1 195 203 195		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76] Name	203 157 1 195 112 195 200 99 157 157 1 1 195 203 195 112 195 200 99 Actual Value	Expected Value	
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76] Name CTCFailedBuf_Cnt_M_lgc[0]	203 157 1 195 112 195 200 99 157 157 1 195 203 195 112 195 200 99 Actual Value 1	1	~
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76] Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1]	203 157 1 195 112 195 200 99 157 157 1 195 203 195 112 195 200 99  Actual Value 1	1 0	~
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[76] Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2]	203 157 1 195 112 195 200 99 157 157 1 195 203 195 112 195 200 99 Actual Value 1	1 0 1	* *
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[2]	203 157 1 195 112 195 200 99 157 157 1 195 203 195 2112 195 200 99 Actual Value 1 0	1 0	* *
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[6]	203 157 1 195 112 195 200 99 157 157 1 195 203 195 112 195 200 99 Actual Value 1 0 1	1 0 1 1	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6]	203 157 1 195 112 195 200 99 157 157 1 195 203 195 203 195 112 195 200 99  Actual Value 1 0 1 1 1 1	1 0 1 1 1 1 1	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7]	203 157 1 195 112 195 200 99 157 157 1 195 203 195 201 195 200 99 Actual Value 1 0 1 1 1 1 1	1 0 1 1 1 1 1 1	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8]	203 157 1 195 112 195 200 99 157 157 1 195 203 195 203 195 112 195 200 99 Actual Value 1 0 1 1 1 1 1 1 1	1 0 1 1 1 1 1 1 1	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7]	203 157 1 195 112 195 200 99 157 157 1 195 203 195 201 195 200 99 Actual Value 1 0 1 1 1 1 1	1 0 1 1 1 1 1 1	\rightarrow \right

2018-04-10, 18:44:44+0530



Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[11]	1	1	Ž
CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13]	0	0	
CTCFailedBuf_Cnt_M_lgc[14]	1	1	
CTCFailedBuf_Cnt_M_lgc[15]	1	1	~
CTCFailedBuf_Cnt_M_lgc[16]	1	1	~
CTCFailedBuf_Cnt_M_lgc[17]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[18]	1	1	~
CTCFailedBuf_Cnt_M_lgc[19]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[20]	0	0	~
CTCFailedBuf_Cnt_M_lgc[21]	0	0	~
CTCFailedBuf_Cnt_M_lgc[22]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[23]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[24]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[25]	1	1	· ·
CTCFailedBuf_Cnt_M_lgc[26]	1	1	
CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28]	1	1	
CTCFailedBuf_Cnt_M_lgc[29]	1	1	_
CTCFailedBuf_Cnt_M_lgc[30]	0	0	
CTCFailedBuf_Cnt_M_lgc[31]	1	1	·
CTCFailedBuf_Cnt_M_lgc[32]	1	1	
CTCFailedBuf_Cnt_M_lgc[33]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[34]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[35]	0	0	~
CTCFailedBuf_Cnt_M_lgc[36]	0	0	~
CTCFailedBuf_Cnt_M_lgc[37]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[38]	0	0	~
CTCFailedBuf_Cnt_M_lgc[39]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[40]	0	0	~
CTCFailedBuf_Cnt_M_lgc[41]	0	0	~
CTCFailedBuf_Cnt_M_lgc[42]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[43]	0	0	•
CTCFailedBuf_Cnt_M_lgc[44]	0	0	· · · · · · · · · · · · · · · · · · ·
CTCFailedBuf_Cnt_M_lgc[45]	0 0	0	
CTCFailedBuf_Cnt_M_lgc[46] CTCFailedBuf_Cnt_M_lgc[47]	0	0	
CTCFailedBuf_Cnt_M_lgc[48]	0	0	
CTCFailedBuf_Cnt_M_lgc[49]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[50]	0	0	~
CTCFailedBuf Cnt M lgc[51]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[52]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[53]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[54]	1	1	~
CTCFailedBuf_Cnt_M_lgc[55]	0	0	~
CTCFailedBuf_Cnt_M_lgc[56]	1	1	~
CTCFailedBuf_Cnt_M_lgc[57]	1	1	~
CTCFailedBuf_Cnt_M_lgc[58]	1	1	~
CTCFailedBuf_Cnt_M_lgc[59]	1	1	·
CTCFailedBuf_Cnt_M_lgc[60]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[61]	1	1	
CTCFailedBuf_Cnt_M_lgc[62]	1	1	· ·
CTCFailedBuf_Cnt_M_lgc[63]	1 1	1	Ž
CTCFailedBuf_Cnt_M_lgc[64] CTCFailedBuf_Cnt_M_lgc[65]	0	0	-
CTCFailedBuf_Cnt_M_lgc[66]	0	0	
CTCFailedBuf_Cnt_M_lgc[67]	0	0	-
CTCFailedBuf_Cnt_M_lgc[68]	0	0	-
CTCFailedBuf_Cnt_M_lgc[69]	0	0	·
CTCFailedBuf_Cnt_M_lgc[70]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[71]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[72]	0	0	~
CTCFailedBuf_Cnt_M_lgc[73]	0	0	•
CTCFailedBuf_Cnt_M_lgc[74]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[75]	0	0	~
CTCFailedBuf_Cnt_M_lgc[76]	0	0	•
CTCFailed_Cnt_M_lgc	0	0	~
Demlf_DTCStatusChanged()	0	0	✓
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc(c	data) 0	0	✓

Demlf\_DTCS

2018-04-10, 18:44:44+0530



Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte Write An Demlf CTCFailed Cnt loc	1	Rte Write An Demlf CTCFailed Cnt loc	1	_

Test Step 2.22 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf Cnt M Igc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf Cnt M lgc[20]	0
CTCFailedBuf Cnt M Igc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38] CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf Cnt M Igc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	
CTCFailedBuf_Cnt_M_lgc[47] CTCFailedBuf Cnt M lgc[48]	0
CTCFailedBuf_Cnt_M_[gc[48]  CTCFailedBuf_Cnt_M_[gc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57] CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_igc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1

Demlf\_DTCS

2018-04-10, 18:44:44+0530



Input Value CTCFailedBuf\_Cnt\_M\_lgc[64] CTCFailedBuf\_Cnt\_M\_lgc[65] 0 CTCFailedBuf\_Cnt\_M\_lgc[66] 1 CTCFailedBuf\_Cnt\_M\_lgc[67] 0 CTCFailedBuf Cnt M lqc[68] 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 CTCFailedBuf\_Cnt\_M\_lgc[73] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[74] CTCFailedBuf\_Cnt\_M\_lgc[75] 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 CTCFailed\_Cnt\_M\_lgc 1 DTC 598152539 DTCKind 1 DTCStatusNew DTCStatusOld 239 Dem\_DTCNumberTable[0] 69 Dem\_DTCNumberTable[1] 30 Dem\_DTCNumberTable[2] 148 Dem\_DTCNumberTable[3] 120 Dem\_DTCNumberTable[4] 135 Dem\_DTCNumberTable[5] 193 Dem\_DTCNumberTable[6] 53 Dem\_DTCNumberTable[7] 53 Dem DTCNumberTable[8] 69 Dem\_DTCNumberTable[9] 30 Dem DTCNumberTable[10] 53 Dem\_DTCNumberTable[11] 189 Dem DTCNumberTable[12] 30 Dem\_DTCNumberTable[13] 53 Dem DTCNumberTable[14] 69 Dem\_DTCNumberTable[15] 30 Dem\_DTCNumberTable[16] 30 Dem\_DTCNumberTable[17] 53 Dem\_DTCNumberTable[18] 127 Dem\_DTCNumberTable[19] 69 Dem\_DTCNumberTable[20] 30 Dem\_DTCNumberTable[21] 53 Dem\_DTCNumberTable[22] 69 Dem\_DTCNumberTable[23] 148 Dem\_DTCNumberTable[24] 120 Dem\_DTCNumberTable[25] 135 Dem\_DTCNumberTable[26] 193 Dem\_DTCNumberTable[27] 30 Dem\_DTCNumberTable[28] 69 Dem\_DTCNumberTable[29] 30 Dem DTCNumberTable[30] 69 Dem\_DTCNumberTable[31] 69 Dem DTCNumberTable[32] 30 Dem\_DTCNumberTable[33] 30 Dem\_DTCNumberTable[34] 69 Dem\_DTCNumberTable[35] 30 Dem\_DTCNumberTable[36] 69 Dem\_DTCNumberTable[37] 69 Dem\_DTCNumberTable[38] 69 Dem\_DTCNumberTable[39] 30 Dem\_DTCNumberTable[40] 30 Dem\_DTCNumberTable[41] 148 Dem\_DTCNumberTable[42] 120 135 Dem\_DTCNumberTable[43] Dem\_DTCNumberTable[44] 193 Dem\_DTCNumberTable[45] 53 Dem\_DTCNumberTable[46] 69 Dem DTCNumberTable[47] 30 Dem\_DTCNumberTable[48] 120 Dem DTCNumberTable[49] 69 Dem\_DTCNumberTable[50] 30 Dem\_DTCNumberTable[51] 69 Dem DTCNumberTable[52] 69 Dem\_DTCNumberTable[53] 30 Dem\_DTCNumberTable[54] 120

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value Dem DTCNumberTable[55] 53 Dem\_DTCNumberTable[56] Dem\_DTCNumberTable[57] 30 Dem\_DTCNumberTable[58] 69 53 Dem\_DTCNumberTable[59] Dem\_DTCNumberTable[60] 69 Dem\_DTCNumberTable[61] 30 Dem\_DTCNumberTable[62] 120 Dem\_DTCNumberTable[63] 148 Dem DTCNumberTable[64] 120 Dem\_DTCNumberTable[65] 135 Dem\_DTCNumberTable[66] 193 Dem\_DTCNumberTable[67] 69 Dem DTCNumberTable[68] 69 Dem\_DTCNumberTable[69] 30 Dem\_DTCNumberTable[70] 120 Dem\_DTCNumberTable[71] 53 Dem\_DTCNumberTable[72] 120 Dem\_DTCNumberTable[73] 148 Dem\_DTCNumberTable[74] 120 Dem\_DTCNumberTable[75] 135 Dem\_DTCNumberTable[76] 193 Dem\_DTC\_FTB\_Table[0] 0 Dem\_DTC\_FTB\_Table[1] 0 Dem\_DTC\_FTB\_Table[2] 0 Dem\_DTC\_FTB\_Table[3] 0 Dem\_DTC\_FTB\_Table[4] 0 Dem\_DTC\_FTB\_Table[5] 0 Dem\_DTC\_FTB\_Table[6] 0 Dem\_DTC\_FTB\_Table[7] 0 Dem\_DTC\_FTB\_Table[8] 0 Dem\_DTC\_FTB\_Table[9] 0 Dem DTC FTB Table[10] 0 Dem\_DTC\_FTB\_Table[11] 0 Dem\_DTC\_FTB\_Table[12] 0 Dem\_DTC\_FTB\_Table[13] 0 Dem\_DTC\_FTB\_Table[14] 0 Dem\_DTC\_FTB\_Table[15] 0 Dem\_DTC\_FTB\_Table[16] 0 Dem DTC\_FTB\_Table[17] 0 Dem\_DTC\_FTB\_Table[18] 0 Dem DTC FTB Table[19] 0 Dem\_DTC\_FTB\_Table[20] 0 Dem\_DTC\_FTB\_Table[21] 0 0 Dem\_DTC\_FTB\_Table[22] Dem\_DTC\_FTB\_Table[23] 0 Dem\_DTC\_FTB\_Table[24] 0 Dem\_DTC\_FTB\_Table[25] 0 Dem\_DTC\_FTB\_Table[26] 0 Dem\_DTC\_FTB\_Table[27] 0 Dem\_DTC\_FTB\_Table[28] 0 Dem\_DTC\_FTB\_Table[29] 0 Dem\_DTC\_FTB\_Table[30] 0 Dem\_DTC\_FTB\_Table[31] 0 Dem\_DTC\_FTB\_Table[32] 0 Dem\_DTC\_FTB\_Table[33] 0 0 Dem\_DTC\_FTB\_Table[34] Dem\_DTC\_FTB\_Table[35] 0 Dem\_DTC\_FTB\_Table[36] 0 Dem\_DTC\_FTB\_Table[37] 0 Dem\_DTC\_FTB\_Table[38] 0 Dem\_DTC\_FTB\_Table[39] 0 Dem\_DTC\_FTB\_Table[40] 0 Dem\_DTC\_FTB\_Table[41] 0 Dem\_DTC\_FTB\_Table[42] 0 Dem DTC FTB Table[43] 0 Dem\_DTC\_FTB\_Table[44] 0 Dem DTC FTB Table[45] 0 Dem\_DTC\_FTB\_Table[46] 0 Dem\_DTC\_FTB\_Table[47] 0 Dem\_DTC\_FTB\_Table[48] 0 Dem\_DTC\_FTB\_Table[49] 0 Dem\_DTC\_FTB\_Table[50] 0

2018-04-10, 18:44:44+0530



Name	Input Value		
Dem_DTC_FTB_Table[51]	0		
Dem_DTC_FTB_Table[52]	0		
Dem_DTC_FTB_Table[53]	0		
Dem_DTC_FTB_Table[54]	0		
Dem_DTC_FTB_Table[55]	0		
Dem_DTC_FTB_Table[56]	0		
Dem_DTC_FTB_Table[57]	0		
Dem_DTC_FTB_Table[58]	0		
Dem_DTC_FTB_Table[59]	0		
Dem_DTC_FTB_Table[60]	0		
Dem_DTC_FTB_Table[61]	0		
Dem_DTC_FTB_Table[62]	0		
Dem_DTC_FTB_Table[63]	0		
Dem_DTC_FTB_Table[64]	0		
Dem_DTC_FTB_Table[65]	0		
Dem_DTC_FTB_Table[66]	0		
Dem_DTC_FTB_Table[67]	0		
Dem_DTC_FTB_Table[68]	0		
Dem_DTC_FTB_Table[69]	0		
Dem_DTC_FTB_Table[70]	0		
Dem_DTC_FTB_Table[71]	0		
Dem_DTC_FTB_Table[72]	0		
Dem_DTC_FTB_Table[73]	0		
Dem_DTC_FTB_Table[74]	0		
Dem_DTC_FTB_Table[75]	0		
Dem_DTC_FTB_Table[76]	0		
Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[0]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[1]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[2]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[3]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[4]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[5]	1	1	
CTCFailedBuf_Cnt_M_lgc[6]	1	1	~

DemIf\_DTCS

2018-04-10, 18:44:44+0530



**Actual Value Expected Value** CTCFailedBuf\_Cnt\_M\_lgc[46] CTCFailedBuf\_Cnt\_M\_lgc[47] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[48] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[49] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[50] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[51] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[52] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[53] 1 CTCFailedBuf\_Cnt\_M\_lgc[54] CTCFailedBuf\_Cnt\_M\_lgc[55] 1 CTCFailedBuf\_Cnt\_M\_lgc[56] CTCFailedBuf\_Cnt\_M\_lgc[57] 1 CTCFailedBuf\_Cnt\_M\_lgc[58] CTCFailedBuf\_Cnt\_M\_lgc[59] CTCFailedBuf\_Cnt\_M\_lgc[60] CTCFailedBuf\_Cnt\_M\_lgc[61] 1 CTCFailedBuf\_Cnt\_M\_lgc[62] CTCFailedBuf\_Cnt\_M\_lgc[63] 1 1  $CTCFailedBuf\_Cnt\_M\_lgc[64]$ 1 CTCFailedBuf\_Cnt\_M\_lgc[65] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[66] 1 CTCFailedBuf\_Cnt\_M\_lgc[67] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[68] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[73] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[74] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[75] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 0 CTCFailed\_Cnt\_M\_lgc 1 1 Demlf DTCStatusChanged() 0 0 Rte\_Write\_Ap\_DemIf\_CTCFailed\_Cnt\_lgc(data)

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte Write Ap Demlf CTCFailed Cnt lgc	1	Rte Write Ap Demlf CTCFailed Cnt lgc	1	~

Test Step 2.23 (Repeat Count = 1)	🗸
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	0
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_Igc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value CTCFailedBuf\_Cnt\_M\_lgc[29] 1 CTCFailedBuf\_Cnt\_M\_lgc[30] CTCFailedBuf\_Cnt\_M\_lgc[31] 1 CTCFailedBuf\_Cnt\_M\_lgc[32] CTCFailedBuf\_Cnt\_M\_lgc[33] 1 CTCFailedBuf\_Cnt\_M\_lgc[34] 0 CTCFailedBuf\_Cnt\_M\_lgc[35] 0 CTCFailedBuf\_Cnt\_M\_lgc[36] 0 CTCFailedBuf\_Cnt\_M\_lgc[37] 0 CTCFailedBuf\_Cnt\_M\_lgc[38] n CTCFailedBuf\_Cnt\_M\_lgc[39] 0 CTCFailedBuf\_Cnt\_M\_lgc[40] n CTCFailedBuf\_Cnt\_M\_lgc[41] 0 CTCFailedBuf\_Cnt\_M\_lgc[42] n CTCFailedBuf\_Cnt\_M\_lgc[43] 0 CTCFailedBuf\_Cnt\_M\_lgc[44] 0 CTCFailedBuf\_Cnt\_M\_lgc[45] 0 CTCFailedBuf\_Cnt\_M\_lgc[46] 0  $CTCFailedBuf\_Cnt\_M\_lgc[47]$ 0 CTCFailedBuf\_Cnt\_M\_lgc[48] 0 CTCFailedBuf\_Cnt\_M\_lgc[49] 0 CTCFailedBuf\_Cnt\_M\_lgc[50] 0 CTCFailedBuf\_Cnt\_M\_lgc[51] 0 CTCFailedBuf\_Cnt\_M\_lgc[52] 0 CTCFailedBuf\_Cnt\_M\_lgc[53] 1 CTCFailedBuf\_Cnt\_M\_lgc[54] CTCFailedBuf\_Cnt\_M\_lgc[55] 1 CTCFailedBuf\_Cnt\_M\_lgc[56] 0 CTCFailedBuf\_Cnt\_M\_lgc[57] 1 CTCFailedBuf\_Cnt\_M\_lgc[58] 1 CTCFailedBuf Cnt M Igc[59] 1 CTCFailedBuf\_Cnt\_M\_lgc[60] CTCFailedBuf Cnt M Igc[61] 1 CTCFailedBuf\_Cnt\_M\_lgc[62] 1 CTCFailedBuf\_Cnt\_M\_lgc[63] CTCFailedBuf\_Cnt\_M\_lgc[64] 1 CTCFailedBuf\_Cnt\_M\_lgc[65] 0 CTCFailedBuf\_Cnt\_M\_lgc[66] 0 CTCFailedBuf\_Cnt\_M\_lgc[67] 0 CTCFailedBuf\_Cnt\_M\_lgc[68] 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 CTCFailedBuf Cnt M lqc[70] 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[73] CTCFailedBuf\_Cnt\_M\_lgc[74] 0 CTCFailedBuf\_Cnt\_M\_lgc[75] 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 CTCFailed\_Cnt\_M\_lgc 0 DTC 4118147944 DTCKind 2 DTCStatusNew 200 DTCStatusOld 203 Dem\_DTCNumberTable[0] 254 Dem\_DTCNumberTable[1] 153 Dem\_DTCNumberTable[2] 91 Dem\_DTCNumberTable[3] 138 Dem DTCNumberTable[4] 54 108 Dem\_DTCNumberTable[5] Dem\_DTCNumberTable[6] 239 Dem\_DTCNumberTable[7] 239 Dem DTCNumberTable[8] 254 Dem\_DTCNumberTable[9] 153 Dem DTCNumberTable[10] 239 Dem\_DTCNumberTable[11] 200 Dem DTCNumberTable[12] 153 Dem\_DTCNumberTable[13] 239 Dem DTCNumberTable[14] 254 Dem\_DTCNumberTable[15] 153 Dem\_DTCNumberTable[16] 153 Dem\_DTCNumberTable[17] 239 Dem\_DTCNumberTable[18] 33 Dem\_DTCNumberTable[19] 254

Demlf\_DTCS

2018-04-10, 18:44:44+0530



Name Input Value Dem\_DTCNumberTable[20] 153 Dem\_DTCNumberTable[21] 239 Dem DTCNumberTable[22] 254 Dem\_DTCNumberTable[23] 91 Dem DTCNumberTable[24] 138 Dem\_DTCNumberTable[25] 54 Dem\_DTCNumberTable[26] 108 Dem\_DTCNumberTable[27] 153 Dem\_DTCNumberTable[28] 254 Dem\_DTCNumberTable[29] 153 Dem\_DTCNumberTable[30] 254 Dem\_DTCNumberTable[31] 254 Dem\_DTCNumberTable[32] 153 Dem\_DTCNumberTable[33] 153 Dem\_DTCNumberTable[34] 254 Dem\_DTCNumberTable[35] 153 Dem\_DTCNumberTable[36] 254 Dem\_DTCNumberTable[37] 254 Dem\_DTCNumberTable[38] 254 Dem\_DTCNumberTable[39] 153 Dem\_DTCNumberTable[40] 153 Dem\_DTCNumberTable[41] 91 Dem\_DTCNumberTable[42] 138 Dem\_DTCNumberTable[43] 54 Dem\_DTCNumberTable[44] 108 Dem\_DTCNumberTable[45] 239 Dem DTCNumberTable[46] 254 Dem\_DTCNumberTable[47] 153 Dem DTCNumberTable[48] 138 Dem\_DTCNumberTable[49] 254 Dem DTCNumberTable[50] 153 Dem\_DTCNumberTable[51] 254 Dem DTCNumberTable[52] 254 Dem\_DTCNumberTable[53] 153 Dem\_DTCNumberTable[54] 138 Dem\_DTCNumberTable[55] 239 Dem\_DTCNumberTable[56] 254 153 Dem\_DTCNumberTable[57] Dem\_DTCNumberTable[58] 254 Dem\_DTCNumberTable[59] 239 Dem\_DTCNumberTable[60] 254 Dem\_DTCNumberTable[61] 153 Dem\_DTCNumberTable[62] 138 Dem\_DTCNumberTable[63] 91 Dem\_DTCNumberTable[64] 138 Dem\_DTCNumberTable[65] 54 Dem DTCNumberTable[66] 108 Dem\_DTCNumberTable[67] 254 Dem DTCNumberTable[68] 254 Dem\_DTCNumberTable[69] 153 Dem\_DTCNumberTable[70] 138 Dem\_DTCNumberTable[71] 239 Dem\_DTCNumberTable[72] 138 Dem\_DTCNumberTable[73] 91 Dem\_DTCNumberTable[74] 138 Dem\_DTCNumberTable[75] 54 Dem\_DTCNumberTable[76] 108 Dem\_DTC\_FTB\_Table[0] 255 Dem\_DTC\_FTB\_Table[1] 255 Dem\_DTC\_FTB\_Table[2] 255 Dem\_DTC\_FTB\_Table[3] 255 255 Dem\_DTC\_FTB\_Table[4] Dem\_DTC\_FTB\_Table[5] 255 Dem\_DTC\_FTB\_Table[6] 255 Dem\_DTC\_FTB\_Table[7] 255 Dem DTC FTB Table[8] 255 Dem\_DTC\_FTB\_Table[9] 255 Dem DTC FTB Table[10] 255 Dem\_DTC\_FTB\_Table[11] 255 Dem\_DTC\_FTB\_Table[12] 255 Dem\_DTC\_FTB\_Table[13] 255 Dem\_DTC\_FTB\_Table[14] 255 Dem\_DTC\_FTB\_Table[15] 255

2018-04-10, 18:44:44+0530



Name	Lucial Materia		
Name Dem_DTC_FTB_Table[16]	Input Value		
Dem_DTC_FTB_Table[10]	255		
Dem_DTC_FTB_Table[18]	255		
Dem_DTC_FTB_Table[19]	255		
Dem_DTC_FTB_Table[20]	255		
Dem_DTC_FTB_Table[21]	255		
Dem_DTC_FTB_Table[22]	255 255		
Dem_DTC_FTB_Table[23] Dem_DTC_FTB_Table[24]	255		
Dem_DTC_FTB_Table[25]	255		
Dem_DTC_FTB_Table[26]	255		
Dem_DTC_FTB_Table[27]	255		
Dem_DTC_FTB_Table[28]	255		
Dem_DTC_FTB_Table[29] Dem_DTC_FTB_Table[30]	255 255		
Dem_DTC_FTB_Table[31]	255		
Dem_DTC_FTB_Table[32]	255		
Dem_DTC_FTB_Table[33]	255		
Dem_DTC_FTB_Table[34]	255		
Dem_DTC_FTB_Table[35]	255 255		
Dem_DTC_FTB_Table[36] Dem_DTC_FTB_Table[37]	255		
Dem_DTC_FTB_Table[38]	255		
Dem_DTC_FTB_Table[39]	255		
Dem_DTC_FTB_Table[40]	255		
Dem_DTC_FTB_Table[41]	255		
Dem_DTC_FTB_Table[42] Dem_DTC_FTB_Table[43]	255 255		
Dem_DTC_FTB_Table[44]	255		
Dem_DTC_FTB_Table[45]	255		
Dem_DTC_FTB_Table[46]	255		
Dem_DTC_FTB_Table[47]	255		
Dem_DTC_FTB_Table[48] Dem_DTC_FTB_Table[49]	255 255		
Dem_DTC_FTB_Table[49]	255		
Dem_DTC_FTB_Table[51]	255		
Dem_DTC_FTB_Table[52]	255		
Dem_DTC_FTB_Table[53]	255		
Dem_DTC_FTB_Table[54] Dem_DTC_FTB_Table[55]	255 255		
Dem_DTC_FTB_Table[56]	255		
Dem_DTC_FTB_Table[57]	255		
Dem_DTC_FTB_Table[58]	255		
Dem_DTC_FTB_Table[59]	255		
Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61]	255 255		
Dem_DTC_FTB_Table[62]	255		
Dem_DTC_FTB_Table[63]	255		
Dem_DTC_FTB_Table[64]	255		
Dem_DTC_FTB_Table[65]	255		
Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67]	255 255		
Dem_DTC_FTB_Table[68]	255		
Dem_DTC_FTB_Table[69]	255		
Dem DTC FTB Table[70]			
	255		
Dem_DTC_FTB_Table[71]	255		
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72]	255 255		
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73]	255 255 255		
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72]	255 255		
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74]	255 255 255 255		
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76] Name	255 255 255 255 255 255	Expected Value	Result
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]	255 255 255 255 255 255 255 255 <b>Actual Value</b>	1	•
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1]	255 255 255 255 255 255 255 <b>Actual Value</b> 1	1	~
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2]	255 255 255 255 255 255 255 <b>Actual Value</b> 1	1 1 1	<i>y</i>
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1]	255 255 255 255 255 255 255 <b>Actual Value</b> 1	1	\ \ \ \
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3]	255 255 255 255 255 255 255 <b>Actual Value</b> 1 1	1 1 1 1	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6]	255 255 255 255 255 255 Actual Value 1 1 1 1 1 1 1	1 1 1 1 1 1 1	\rightarrow \right
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6]	255 255 255 255 255 255 Actual Value 1 1 1 1 1 1 0	1 1 1 1 1 1 1 1 0	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7]	255 255 255 255 255 255  Actual Value 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 0	~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6]	255 255 255 255 255 255 Actual Value 1 1 1 1 1 1 0	1 1 1 1 1 1 1 1 0	Result

2018-04-10, 18:44:44+0530



COTORNISOL OCK M (\$400)  COTORNISOL OCK M (\$40	Name	Actual Value	Expected Value	Result
CICCHARDED CON Mage19				
CICHardent Core, M. getted CICHARDEN, Core, M. g		1	1	~
CICCHaesebut, Cell Mujor(16)  CICCHaesebut, Cell Mujor(17)  CICCHaesebut, Cell Mujor(17)  CICCHaesebut, Cell Mujor(18)  CICCHa				
COT-Griedord, Cott, Migd 19				-
CCP-anicellar, Col. Mu, Styles				
CICHAROSSI, COM, Muglety 1				
CICHARDAL CAN M. 19620  CICHARDAL CAN M. 19622  CICHARDAL CAN M. 19622  CICHARDAL CAN M. 19622  CICHARDAL CAN M. 19622  CICHARDAL CAN M. 19623  1 1 1				~
COFFRIEND CM M, 9(27)  O	CTCFailedBuf_Cnt_M_lgc[19]	1	1	
COTABBUS CM, M, 19622  1 1 1  1 COTABBUS CM, M, 19624  1 1 1  1 COTABBUS CM, M, 19624  1 1 1  1 COTABBUS CM, M, 19625  1 1 1  2 COTABBUS CM, M, 19625  1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			1	
CICCRAIGNED CON N. 19673  CICCRAIGNED CON N. 19673  1 1 1				
CICFaleoduck Ce, Ma 19624) 1 1 1 1				
CCFGraedbull_Cort_M_logS9				
CICFaeldedU_CRT_M_DCSR	CTCFailedBuf_Cnt_M_lgc[25]	1	1	~
CICFaiedBuf, Citt, M, p028				
CICFalledBuff_CITM_Ng0439				
CCFGaledBuf Cnt M pg630 CTGFaledBuf Cnt M pg633 CTGFaledBuf Cnt M pg636 CTGFaledBuf Cnt M pg636 CTGFaledBuf Cnt M pg636 CTGFaledBuf Cnt M pg636 CTGFaledBuf Cnt M pg637 CTGFaledBuf Cnt M pg637 CTGFaledBuf Cnt M pg637 CTGFaledBuf Cnt M pg637 CTGFaledBuf Cnt M pg647 CTGFaledBuf Cnt M pg648 CTGFaledBuf Cnt M pg688 CTGFal				
CICFaledBull Cnt M. Jogd33 1 1 1 1				
CICPalestidu Cnt. M. Jog433  1 1 1 1 1 1 CTCPalestidu Cnt. M. Jog459  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0				~
CICFaiceBut_Crt, M_19439 CICFAiceBut_Crt, M_19449 CICFAiceBut_Crt, M_19459 CICFAiceBut_Crt, M_19479 CICFAiceBut_Crt, M_19	CTCFailedBuf_Cnt_M_lgc[32]	1	1	
CICFaledBuf, Crit, M. 19d535  CICFaledBuf, Crit, M. 19d537  O O O O O O O O O O O O O O O O O O O				
CTCFaiedBuf, Cnt, M, 1gc358]  O O O O CTCFaiedBuf, Cnt, M, 1gc378]  O O O O O CTCFaiedBuf, Cnt, M, 1gc438]  O O O O O O O O O O O O O O O O O O O				
CTCFaiedBuf_Cn_M_lgct38  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0				
CTCFailedBuf_Cnt_Migd39				
CICFailedful, Cnt, M. lpg43] CICFailedful, Cnt, M. lpg41] CICFailedful, Cnt, M. lpg41] CICFailedful, Cnt, M. lpg42] O O O O CICFailedful, Cnt, M. lpg43] O O O O CICFailedful, Cnt, M. lpg44] O O O O O CICFailedful, Cnt, M. lpg44] O O O O O CICFailedful, Cnt, M. lpg44] O O O O O CICFailedful, Cnt, M. lpg44] O O O O O O CICFailedful, Cnt, M. lpg48] O O O O O O CICFailedful, Cnt, M. lpg48] O O O O O O O O O O O O O O O O O O O				
CTCFailedBuf_Cnt_M_lgcl41] 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		0	0	~
CTCFailedBut_Cnt_M_lgc[42]  CTCFailedBut_Cnt_M_lgc[43]  CTCFailedBut_Cnt_M_lgc[44]  CTCFailedBut_Cnt_M_lgc[45]  CTCFailedBut_Cnt_M_lgc[45]  CTCFailedBut_Cnt_M_lgc[46]  CTCFailedBut_Cnt_M_lgc[46]  CTCFailedBut_Cnt_M_lgc[47]  O  O  CTCFailedBut_Cnt_M_lgc[47]  O  O  CTCFailedBut_Cnt_M_lgc[48]  O  CTCFailedBut_Cnt_M_lgc[48]  O  CTCFailedBut_Cnt_M_lgc[48]  O  CTCFailedBut_Cnt_M_lgc[48]  O  CTCFailedBut_Cnt_M_lgc[48]  O  CTCFailedBut_Cnt_M_lgc[50]  CTCFailedBut_Cnt_M_lgc[50]  CTCFailedBut_Cnt_M_lgc[50]  CTCFailedBut_Cnt_M_lgc[51]  O  CTCFailedBut_Cnt_M_lgc[53]  TI  TI  TCCFailedBut_Cnt_M_lgc[53]  TI  TI  TCCFailedBut_Cnt_M_lgc[53]  TI  TCCFailedBut_Cnt_M_lgc[53]  TCCFailedBut_Cnt_M_lgc[63]  TCCFaile	CTCFailedBuf_Cnt_M_lgc[40]			
CTCFaiedBut_Cnt_M_lgc[43]  CTCFaiedBut_Cnt_M_lgc[44]  CTCFaiedBut_Cnt_M_lgc[45]  CTCFaiedBut_Cnt_M_lgc[46]  CTCFaiedBut_Cnt_M_lgc[46]  CTCFaiedBut_Cnt_M_lgc[47]  CTCFaiedBut_Cnt_M_lgc[48]  CTCFaiedBut_Cnt_M_lgc[48]  CTCFaiedBut_Cnt_M_lgc[48]  CTCFaiedBut_Cnt_M_lgc[48]  CTCFaiedBut_Cnt_M_lgc[48]  CTCFaiedBut_Cnt_M_lgc[48]  CTCFaiedBut_Cnt_M_lgc[48]  CTCFaiedBut_Cnt_M_lgc[51]  CTCFaiedBut_Cnt_M_lgc[51]  CTCFaiedBut_Cnt_M_lgc[53]  CTCFaiedBut_Cnt_M_lgc[53]  CTCFaiedBut_Cnt_M_lgc[53]  CTCFaiedBut_Cnt_M_lgc[53]  CTCFaiedBut_Cnt_M_lgc[58]  CTCFaiedBut_Cnt_M_lgc[68]  CTCFaiedBut_Cnt_M_lgc				
CTCFailedBuf_Cnt_M_lgc[44]  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0				
CTCFaiedBuf_Cnt_M_lgcl45  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0				
CTCFalledBuf_Cnt_M_lgc[46] CTCFalledBuf_Cnt_M_lgc[47] O O O O O CTCFalledBuf_Cnt_M_lgc[48] O O O O O O O O O O O O O O O O O O O				<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[48] 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		0	0	
CTCFailedBuf_Cnt_M_lgc[49]         0         0         V           CTCFailedBuf_Cnt_M_lgc[51]         0         0         V           CTCFailedBuf_Cnt_M_lgc[52]         0         0         V           CTCFailedBuf_Cnt_M_lgc[52]         0         0         V           CTCFailedBuf_Cnt_M_lgc[53]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[54]         1         1         1         V         CTCFailedBuf_Cnt_M_lgc[55]         1         1         1         V         CTCFailedBuf_Cnt_M_lgc[57]         1         1         1         V         CTCFailedBuf_Cnt_M_lgc[58]         1         1         1         V         CTCFailedBuf_Cnt_M_lgc[58]         1         1         1         V         CTCFailedBuf_Cnt_M_lgc[60]         0         0         V         CTCFailedBuf_Cnt_M_lgc[60]         0         0         V         CT				
CTCFailedBuf_Cnt_M_lgc[51]         0         0         0           CTCFailedBuf_Cnt_M_lgc[52]         0         0         0           CTCFailedBuf_Cnt_M_lgc[52]         0         0         0           CTCFailedBuf_Cnt_M_lgc[53]         1         1         1           CTCFailedBuf_Cnt_M_lgc[55]         1         1         1           CTCFailedBuf_Cnt_M_lgc[56]         0         0         0           CTCFailedBuf_Cnt_M_lgc[58]         1         1         1           CTCFailedBuf_Cnt_M_lgc[58]         1         1         1           CTCFailedBuf_Cnt_M_lgc[58]         1         1         1           CTCFailedBuf_Cnt_M_lgc[58]         1         1         1           CTCFailedBuf_Cnt_M_lgc[69]         1         1         1           CTCFailedBuf_Cnt_M_lgc[61]         1         1         1           CTCFailedBuf_Cnt_M_lgc[62]         1         1         1           CTCFailedBuf_Cnt_M_lgc[63]         1         1         1           CTCFailedBuf_Cnt_M_lgc[64]         1         1         1           CTCFailedBuf_Cnt_M_lgc[65]         0         0         0           CTCFailedBuf_Cnt_M_lgc[66]         0         0         0				
CTCFailedBuf_Cn_M_lgc[51]         0         0         0           CTCFailedBuf_Cn_M_lgc[53]         1         1         1           CTCFailedBuf_Cn_M_lgc[54]         1         1         1           CTCFailedBuf_Cn_M_lgc[54]         1         1         1           CTCFailedBuf_Cn_M_lgc[56]         0         0         0           CTCFailedBuf_Cn_M_lgc[57]         1         1         1           CTCFailedBuf_Cn_M_lgc[58]         1         1         1           CTCFailedBuf_Cn_M_lgc[58]         1         1         1           CTCFailedBuf_Cn_M_lgc[58]         1         1         1           CTCFailedBuf_Cn_M_lgc[69]         1         1         1           CTCFailedBuf_Cn_M_lgc[60]         1         1         1           CTCFailedBuf_Cn_M_lgc[63]         1         1         1           CTCFailedBuf_Cn_M_lgc[63]         1         1         1           CTCFailedBuf_Cn_M_lgc[64]         1         1         1           CTCFailedBuf_Cn_M_lgc[65]         0         0         0           CTCFailedBuf_Cn_M_lgc[68]         0         0         0           CTCFailedBuf_Cn_M_lgc[68]         0         0         0				
CTCFailedBuf_Cnt_M_lgc[52]         0         0         V           CTCFailedBuf_Cnt_M_lgc[54]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[54]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[55]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[57]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[58]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[58]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[60]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[60]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[62]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[62]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[63]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[64]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[67]         0         0         V         V           CTCFailedBuf_Cnt_M_lgc[67]         0         0         V				
CTCFailedBuf_Cnt_M_lgc[54]         1         1         1           CTCFailedBuf_Cnt_M_lgc[56]         0         0         -           CTCFailedBuf_Cnt_M_lgc[57]         1         1         -           CTCFailedBuf_Cnt_M_lgc[57]         1         1         -           CTCFailedBuf_Cnt_M_lgc[58]         1         1         1         -           CTCFailedBuf_Cnt_M_lgc[60]         1         1         -         -           CTCFailedBuf_Cnt_M_lgc[61]         1         1         -         -           CTCFailedBuf_Cnt_M_lgc[62]         1         1         1         -           CTCFailedBuf_Cnt_M_lgc[62]         1         1         1         -           CTCFailedBuf_Cnt_M_lgc[63]         1         1         1         -           CTCFailedBuf_Cnt_M_lgc[64]         1         1         -         -           CTCFailedBuf_Cnt_M_lgc[65]         0         0         -         -           CTCFailedBuf_Cnt_M_lgc[68]         0         0         -         -           CTCFailedBuf_Cnt_M_lgc[68]         0         0         -         -           CTCFailedBuf_Cnt_M_lgc[68]         0         0         -         -           CTCFailedBuf_C			0	~
CTCFailedBul_Cnt_M_lgc[55]         1         1         9           CTCFailedBul_Cnt_M_lgc[56]         0         0         0           CTCFailedBul_Cnt_M_lgc[57]         1         1         1           CTCFailedBul_Cnt_M_lgc[58]         1         1         1           CTCFailedBul_Cnt_M_lgc[69]         1         1         1           CTCFailedBul_Cnt_M_lgc[60]         1         1         1           CTCFailedBul_Cnt_M_lgc[61]         1         1         1           CTCFailedBul_Cnt_M_lgc[62]         1         1         1           CTCFailedBul_Cnt_M_lgc[63]         1         1         1           CTCFailedBul_Cnt_M_lgc[64]         1         1         1           CTCFailedBul_Cnt_M_lgc[65]         0         0         0           CTCFailedBul_Cnt_M_lgc[66]         0         0         0           CTCFailedBul_Cnt_M_lgc[67]         0         0         0           CTCFailedBul_Cnt_M_lgc[69]         0         0         0           CTCFailedBul_Cnt_M_lgc[69]         0         0         0           CTCFailedBul_Cnt_M_lgc[69]         0         0         0           CTCFailedBul_Cnt_M_lgc[69]         0         0         0				
CTCFailedBuf_Cnt_M_lgc[56]         0         0         ✓           CTCFailedBuf_Cnt_M_lgc[57]         1         1         1         ✓           CTCFailedBuf_Cnt_M_lgc[58]         1         1         1         ✓           CTCFailedBuf_Cnt_M_lgc[59]         1         1         1         ✓           CTCFailedBuf_Cnt_M_lgc[60]         1         1         1         ✓           CTCFailedBuf_Cnt_M_lgc[61]         1         1         1         ✓           CTCFailedBuf_Cnt_M_lgc[62]         1         1         1         ✓           CTCFailedBuf_Cnt_M_lgc[63]         1         1         1         ✓           CTCFailedBuf_Cnt_M_lgc[64]         1         1         1         ✓           CTCFailedBuf_Cnt_M_lgc[65]         0         0         0         ✓           CTCFailedBuf_Cnt_M_lgc[67]         0         0         ✓         ✓           CTCFailedBuf_Cnt_M_lgc[68]         0         0         0         ✓           CTCFailedBuf_Cnt_M_lgc[68]         0         0         0         ✓           CTCFailedBuf_Cnt_M_lgc[68]         0         0         0         ✓           CTCFailedBuf_Cnt_M_lgc[70]         0         0         ✓ <td></td> <td></td> <td></td> <td>~</td>				~
CTCFailedBuf_Cnt_M_lgc[57]         1         1         1         CTCFailedBuf_Cnt_M_lgc[58]         1         1         1         CTCFailedBuf_Cnt_M_lgc[59]         1         1         1         CTCFailedBuf_Cnt_M_lgc[60]         1         1         CTCFailedBuf_Cnt_M_lgc[60]         1         1         CTCFailedBuf_Cnt_M_lgc[61]         1         1         CTCFailedBuf_Cnt_M_lgc[62]         1         1         CTCFailedBuf_Cnt_M_lgc[62]         1         1         CTCFailedBuf_Cnt_M_lgc[63]         1         1         CTCFailedBuf_Cnt_M_lgc[63]         1         1         CTCFailedBuf_Cnt_M_lgc[63]         0         0         CTCFailedBuf_Cnt_M_lgc[63]         0         0         0         CTCFailedBuf_Cnt_M_lgc[63]         0         0         0         CTCFailedBuf_Cnt_M_lgc[63]         0         0         0         0         0         CTCFailedBuf_Cnt_M_lgc[63]         0				-
CTCFailedBuf_Cnt_M_lgc[58]       1       1          CTCFailedBuf_Cnt_M_lgc[60]       1       1           CTCFailedBuf_Cnt_M_lgc[60]       1       1  .				-
CTCFailedBuf_Cnt_M_lgc[60]       1       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1       4         CTCFailedBuf_Cnt_M_lgc[62]       1       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1       1         CTCFailedBuf_Cnt_M_lgc[65]       0       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0       0         CTCFailedBuf_Cnt_M_lgc[68]       0       0       0         CTCFailedBuf_Cnt_M_lgc[70]       0       0       0         CTCFailedBuf_Cnt_M_lgc[71]       0       0       0         CTCFailedBuf_Cnt_M_lgc[72]       0       0       0         CTCFailedBuf_Cnt_M_lgc[73]       0       0       0         CTCFailedBuf_Cnt_M_lgc[74]       0       0       0         CTCFailedBuf_Cnt_M_lgc[75]       0       0       0         CTCFailedBuf_Cnt_M_lgc[75]       0       0       0         CTCFailedBuf_Cnt_M_lgc[76]       0       0       0         CTCFailedBuf_Cnt_M_lgc[76]       0       0       0 <td< td=""><td></td><td></td><td></td><td>~</td></td<>				~
CTCFailedBuf_Cnt_M_lgc[61]       1       1       4         CTCFailedBuf_Cnt_M_lgc[62]       1       1       1       4         CTCFailedBuf_Cnt_M_lgc[63]       1       1       1       4         CTCFailedBuf_Cnt_M_lgc[64]       1       1       1       4         CTCFailedBuf_Cnt_M_lgc[65]       0       0       0       4         CTCFailedBuf_Cnt_M_lgc[66]       0       0       0       4         CTCFailedBuf_Cnt_M_lgc[67]       0       0       0       4         CTCFailedBuf_Cnt_M_lgc[68]       0       0       0       4         CTCFailedBuf_Cnt_M_lgc[70]       0       0       0       4         CTCFailedBuf_Cnt_M_lgc[71]       0       0       0       4         CTCFailedBuf_Cnt_M_lgc[73]       0       0       0       4         CTCFailedBuf_Cnt_M_lgc[73]       0       0       0       4         CTCFailedBuf_Cnt_M_lgc[75]       0       0       0       4         CTCFailedBuf_Cnt_M_lgc[76]       0       0       0       4         CTCFailedBuf_Cnt_M_lgc[76]       0       0       0       4         CTCFailedBuf_Cnt_M_lgc[76]       0       0       0       4 <td></td> <td></td> <td>1</td> <td>~</td>			1	~
CTCFailedBuf_Cnt_M_lgc[62]       1       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1       1         CTCFailedBuf_Cnt_M_lgc[65]       0       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0       0         CTCFailedBuf_Cnt_M_lgc[69]       0       0       0         CTCFailedBuf_Cnt_M_lgc[70]       0       0       0         CTCFailedBuf_Cnt_M_lgc[71]       0       0       0         CTCFailedBuf_Cnt_M_lgc[72]       0       0       0         CTCFailedBuf_Cnt_M_lgc[73]       0       0       0         CTCFailedBuf_Cnt_M_lgc[74]       0       0       0         CTCFailedBuf_Cnt_M_lgc[75]       0       0       0         CTCFailedBuf_Cnt_M_lgc[76]       0       0       0 <td< td=""><td></td><td></td><td></td><td></td></td<>				
CTCFailedBuf_Cnt_M_lgc[63]       1       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1       1         CTCFailedBuf_Cnt_M_lgc[65]       0       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0       0         CTCFailedBuf_Cnt_M_lgc[68]       0       0       0         CTCFailedBuf_Cnt_M_lgc[70]       0       0       0         CTCFailedBuf_Cnt_M_lgc[70]       0       0       0         CTCFailedBuf_Cnt_M_lgc[71]       0       0       0         CTCFailedBuf_Cnt_M_lgc[72]       0       0       0         CTCFailedBuf_Cnt_M_lgc[73]       0       0       0         CTCFailedBuf_Cnt_M_lgc[74]       0       0       0         CTCFailedBuf_Cnt_M_lgc[75]       0       0       0         CTCFailedBuf_Cnt_M_lgc[76]       0       0       0         CTCFailedBuf_Cnt_M_lgc[76]       0       0       0         CTCFailed_Cnt_M_lgc       0       0       0         CTCFailed_Cnt_M_lgc       0       0       0         CTCFailed_Cnt_M_lgc       0       0       0				
CTCFailedBuf_Cnt_M_lgc[64]       1       1       4         CTCFailedBuf_Cnt_M_lgc[65]       0       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0       0         CTCFailedBuf_Cnt_M_lgc[68]       0       0       0         CTCFailedBuf_Cnt_M_lgc[69]       0       0       0         CTCFailedBuf_Cnt_M_lgc[70]       0       0       0         CTCFailedBuf_Cnt_M_lgc[71]       0       0       0         CTCFailedBuf_Cnt_M_lgc[72]       0       0       0         CTCFailedBuf_Cnt_M_lgc[73]       0       0       0         CTCFailedBuf_Cnt_M_lgc[74]       0       0       0         CTCFailedBuf_Cnt_M_lgc[75]       0       0       0         CTCFailedBuf_Cnt_M_lgc[76]       0       0       0         CTCFailed_Cnt_M_lgc       0       0       0         CTCFailed_Cnt_M_lgc       0       0       0         CTCFailed_Cnt_M_lgc       0       0       0         CTCFailed_Cnt_M_lgc       0       0       0				
CTCFailedBuf_Cnt_M_lgc[65]       0       0       •         CTCFailedBuf_Cnt_M_lgc[66]       0       0       •         CTCFailedBuf_Cnt_M_lgc[67]       0       0       •         CTCFailedBuf_Cnt_M_lgc[68]       0       0       •         CTCFailedBuf_Cnt_M_lgc[69]       0       0       •         CTCFailedBuf_Cnt_M_lgc[70]       0       0       •         CTCFailedBuf_Cnt_M_lgc[71]       0       0       •         CTCFailedBuf_Cnt_M_lgc[72]       0       0       •         CTCFailedBuf_Cnt_M_lgc[73]       0       0       •         CTCFailedBuf_Cnt_M_lgc[74]       0       0       •         CTCFailedBuf_Cnt_M_lgc[75]       0       0       •         CTCFailedBuf_Cnt_M_lgc[76]       0       0       •         CTCFailed_Cnt_M_lgc       0       0       •				
CTCFailedBuf_Cnt_M_lgc[67]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[68]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[69]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[70]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[71]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[72]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[73]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[74]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[75]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[76]       0       0       ✓         CTCFailed_Cnt_M_lgc       0       0       ✓         Demlf_DTCStatusChanged()       0       0       ✓			0	~
CTCFailedBuf_Cnt_M_lgc[68]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[70]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[71]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[72]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[73]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[74]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[75]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[76]       0       0       ✓         CTCFailed_Cnt_M_lgc       0       0       ✓         CTCFailed_Cnt_M_lgc       0       0       ✓         Demlf_DTCStatusChanged()       0       0       ✓				
CTCFailedBuf_Cnt_M_lgc[69]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[70]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[71]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[72]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[73]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[74]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[75]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[76]       0       0       ✓         CTCFailed_Cnt_M_lgc       0       0       ✓         Demlf_DTCStatusChanged()       0       0       ✓				
CTCFailedBuf_Cnt_M_lgc[70]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[71]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[72]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[73]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[74]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[75]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[76]       0       0       ✓         CTCFailed_Cnt_M_lgc       0       0       ✓         Demlf_DTCStatusChanged()       0       0       ✓				
CTCFailedBuf_Cnt_M_lgc[71]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[72]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[73]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[74]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[75]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[76]       0       0       ✓         CTCFailed_Cnt_M_lgc       0       0       ✓         Demlf_DTCStatusChanged()       0       0       ✓				
CTCFailedBuf_Cnt_M_lgc[72]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[73]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[74]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[75]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[76]       0       0       ✓         CTCFailed_Cnt_M_lgc       0       0       ✓         Demlf_DTCStatusChanged()       0       0       ✓				
CTCFailedBuf_Cnt_M_lgc[73]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[74]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[75]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[76]       0       0       ✓         CTCFailed_Cnt_M_lgc       0       0       ✓         Demlf_DTCStatusChanged()       0       0       ✓				
CTCFailedBuf_Cnt_M_lgc[75]         0         0         ✓           CTCFailedBuf_Cnt_M_lgc[76]         0         0         ✓           CTCFailed_Cnt_M_lgc         0         0         ✓           Demlf_DTCStatusChanged()         0         0         ✓				
CTCFailedBuf_Cnt_M_lgc[76]         0         0         ✓           CTCFailed_Cnt_M_lgc         0         0         ✓           Demlf_DTCStatusChanged()         0         0         ✓				
CTCFailed_Cnt_M_lgc         0         0           Demlf_DTCStatusChanged()         0         0				
Demlf_DTCStatusChanged() 0 0 ✓				
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc(data) 0				
	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	0	0	~

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2018-04-10, 18:44:44+0530





Test Step 2.24 (Repeat Count = 1)	
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	0
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	0
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf Cnt M Igc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_Igc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27]	1 0
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_Igc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35] CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf Cnt M Igc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_Igc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44] CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52] CTCFailedBuf_Cnt_M_lgc[53]	0 1
CTCFailedBuf_Cnt_M_lgc[53] CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62] CTCFailedBuf_Cnt_M_lgc[63]	1
0.0. aaaaa aont_m_ga[oo]	

Demlf\_DTCS

2018-04-10, 18:44:44+0530



Name Input Value CTCFailedBuf\_Cnt\_M\_lgc[64] CTCFailedBuf\_Cnt\_M\_lgc[65] 0 CTCFailedBuf\_Cnt\_M\_lgc[66] 0 CTCFailedBuf\_Cnt\_M\_lgc[67] 0 CTCFailedBuf Cnt M lqc[68] 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 CTCFailedBuf\_Cnt\_M\_lgc[73] 0 CTCFailedBuf\_Cnt\_M\_lgc[74] 1 CTCFailedBuf\_Cnt\_M\_lgc[75] 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 CTCFailed\_Cnt\_M\_lgc 0 DTC 2120792415 DTCKind 2 DTCStatusNew 226 DTCStatusOld 69 Dem\_DTCNumberTable[0] 157 Dem\_DTCNumberTable[1] 1 Dem\_DTCNumberTable[2] 112 Dem\_DTCNumberTable[3] 195 Dem\_DTCNumberTable[4] 200 Dem\_DTCNumberTable[5] 99 Dem\_DTCNumberTable[6] 203 Dem\_DTCNumberTable[7] 203 Dem DTCNumberTable[8] 157 Dem\_DTCNumberTable[9] 1 Dem DTCNumberTable[10] 203 Dem\_DTCNumberTable[11] 201 Dem DTCNumberTable[12] Dem\_DTCNumberTable[13] 203 Dem DTCNumberTable[14] 157 Dem\_DTCNumberTable[15] 1 Dem\_DTCNumberTable[16] Dem\_DTCNumberTable[17] 203 Dem\_DTCNumberTable[18] 101 Dem\_DTCNumberTable[19] 157 Dem\_DTCNumberTable[20] Dem\_DTCNumberTable[21] 203 Dem\_DTCNumberTable[22] 157 112 Dem\_DTCNumberTable[23] Dem\_DTCNumberTable[24] 195 Dem\_DTCNumberTable[25] 200 Dem\_DTCNumberTable[26] 99 Dem\_DTCNumberTable[27] 1 Dem\_DTCNumberTable[28] 157 Dem\_DTCNumberTable[29] 1 Dem DTCNumberTable[30] 157 Dem\_DTCNumberTable[31] 157 Dem DTCNumberTable[32] 1 Dem\_DTCNumberTable[33] Dem\_DTCNumberTable[34] 157 Dem\_DTCNumberTable[35] 1 Dem\_DTCNumberTable[36] 157 Dem\_DTCNumberTable[37] 157 Dem\_DTCNumberTable[38] 157 Dem\_DTCNumberTable[39] 1 Dem\_DTCNumberTable[40] Dem\_DTCNumberTable[41] 112 Dem\_DTCNumberTable[42] 195 200 Dem\_DTCNumberTable[43] Dem\_DTCNumberTable[44] 99 Dem\_DTCNumberTable[45] 203 Dem\_DTCNumberTable[46] 157 Dem DTCNumberTable[47] 1 Dem\_DTCNumberTable[48] 195 Dem DTCNumberTable[49] 157 Dem DTCNumberTable[50] Dem\_DTCNumberTable[51] 157 Dem DTCNumberTable[52] 157 Dem\_DTCNumberTable[53] 1 Dem\_DTCNumberTable[54] 195

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Name Input Value Dem DTCNumberTable[55] 203 Dem\_DTCNumberTable[56] 157 Dem\_DTCNumberTable[57] 1 Dem\_DTCNumberTable[58] 157 Dem\_DTCNumberTable[59] 203 Dem\_DTCNumberTable[60] 157 Dem\_DTCNumberTable[61] 1 Dem\_DTCNumberTable[62] 195 Dem\_DTCNumberTable[63] 112 Dem DTCNumberTable[64] 195 Dem\_DTCNumberTable[65] 200 Dem\_DTCNumberTable[66] 99 Dem\_DTCNumberTable[67] 157 Dem DTCNumberTable[68] 157 Dem\_DTCNumberTable[69] Dem\_DTCNumberTable[70] 195 Dem\_DTCNumberTable[71] 203 Dem\_DTCNumberTable[72] 195 Dem\_DTCNumberTable[73] 112 Dem\_DTCNumberTable[74] 195 Dem\_DTCNumberTable[75] 200 Dem\_DTCNumberTable[76] 99 Dem\_DTC\_FTB\_Table[0] 31 Dem\_DTC\_FTB\_Table[1] 227 Dem\_DTC\_FTB\_Table[2] 66 Dem\_DTC\_FTB\_Table[3] 96 Dem\_DTC\_FTB\_Table[4] 130 Dem\_DTC\_FTB\_Table[5] 24 Dem\_DTC\_FTB\_Table[6] 240 Dem\_DTC\_FTB\_Table[7] 240 Dem\_DTC\_FTB\_Table[8] 31 Dem\_DTC\_FTB\_Table[9] 227 Dem DTC FTB Table[10] 240 Dem\_DTC\_FTB\_Table[11] 151 Dem\_DTC\_FTB\_Table[12] 227 Dem DTC FTB Table[13] 240 Dem\_DTC\_FTB\_Table[14] 31 Dem\_DTC\_FTB\_Table[15] 227 Dem\_DTC\_FTB\_Table[16] 227 Dem DTC\_FTB\_Table[17] 240 Dem\_DTC\_FTB\_Table[18] 241 Dem DTC FTB Table[19] 31 Dem\_DTC\_FTB\_Table[20] 227 Dem\_DTC\_FTB\_Table[21] 240 Dem\_DTC\_FTB\_Table[22] 31 Dem\_DTC\_FTB\_Table[23] 66 96 Dem\_DTC\_FTB\_Table[24] Dem\_DTC\_FTB\_Table[25] 130 Dem\_DTC\_FTB\_Table[26] 24 Dem\_DTC\_FTB\_Table[27] 227 Dem\_DTC\_FTB\_Table[28] 31 Dem\_DTC\_FTB\_Table[29] 227 Dem\_DTC\_FTB\_Table[30] 31 Dem\_DTC\_FTB\_Table[31] 31 Dem\_DTC\_FTB\_Table[32] 227 Dem\_DTC\_FTB\_Table[33] 227 Dem\_DTC\_FTB\_Table[34] 31 Dem\_DTC\_FTB\_Table[35] 227 Dem\_DTC\_FTB\_Table[36] 31 Dem\_DTC\_FTB\_Table[37] 31 Dem\_DTC\_FTB\_Table[38] 31 Dem\_DTC\_FTB\_Table[39] 227 Dem\_DTC\_FTB\_Table[40] 227 Dem\_DTC\_FTB\_Table[41] 66 Dem\_DTC\_FTB\_Table[42] 96 Dem DTC FTB Table[43] 130 Dem\_DTC\_FTB\_Table[44] 24 Dem DTC FTB Table[45] 240 Dem\_DTC\_FTB\_Table[46] 31 Dem\_DTC\_FTB\_Table[47] 227 Dem\_DTC\_FTB\_Table[48] 96 Dem\_DTC\_FTB\_Table[49] 31 Dem\_DTC\_FTB\_Table[50] 227

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value Dem\_DTC\_FTB\_Table[51] 31 Dem\_DTC\_FTB\_Table[52] 31 Dem DTC\_FTB\_Table[53] 227 Dem\_DTC\_FTB\_Table[54] 96 Dem\_DTC\_FTB\_Table[55] 240 Dem\_DTC\_FTB\_Table[56] 31 Dem\_DTC\_FTB\_Table[57] 227 Dem\_DTC\_FTB\_Table[58] 31 Dem\_DTC\_FTB\_Table[59] 240 Dem\_DTC\_FTB\_Table[60] 31 Dem\_DTC\_FTB\_Table[61] 227 Dem\_DTC\_FTB\_Table[62] 96 Dem\_DTC\_FTB\_Table[63] 66 Dem\_DTC\_FTB\_Table[64] 96 Dem\_DTC\_FTB\_Table[65] 130 24 Dem DTC FTB Table[66] Dem\_DTC\_FTB\_Table[67] 31 Dem\_DTC\_FTB\_Table[68] 31 Dem\_DTC\_FTB\_Table[69] 227 Dem\_DTC\_FTB\_Table[70] 96 Dem\_DTC\_FTB\_Table[71] 240 Dem\_DTC\_FTB\_Table[72] 96 Dem\_DTC\_FTB\_Table[73] 66 Dem\_DTC\_FTB\_Table[74] 96 Dem\_DTC\_FTB\_Table[75] 130 Dem\_DTC\_FTB\_Table[76] 24 Name **Actual Value Expected Value** Result CTCFailedBuf Cnt M Igc[0] 1 CTCFailedBuf\_Cnt\_M\_lgc[1] CTCFailedBuf\_Cnt\_M\_lgc[2] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[3] 0 0 CTCFailedBuf Cnt M lgc[4] 1 CTCFailedBuf\_Cnt\_M\_lgc[5] 1 1 CTCFailedBuf Cnt M Igc[6] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[7] 1 CTCFailedBuf\_Cnt\_M\_lgc[8] CTCFailedBuf\_Cnt\_M\_lgc[9] CTCFailedBuf\_Cnt\_M\_lgc[10] CTCFailedBuf\_Cnt\_M\_lgc[11] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[12] CTCFailedBuf Cnt M lqc[13] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[14] CTCFailedBuf\_Cnt\_M\_lgc[15] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[16] **~** CTCFailedBuf\_Cnt\_M\_lgc[17] 1 CTCFailedBuf\_Cnt\_M\_lgc[18] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[19] 1 1 ~ CTCFailedBuf\_Cnt\_M\_lgc[20] n 0 CTCFailedBuf\_Cnt\_M\_lgc[21] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[22] n n CTCFailedBuf\_Cnt\_M\_lgc[23] 1 CTCFailedBuf Cnt M lqc[24] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[25] CTCFailedBuf\_Cnt\_M\_lgc[26] CTCFailedBuf\_Cnt\_M\_lgc[27] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[28] 1  $CTCFailedBuf\_Cnt\_M\_lgc[29]$ 1 CTCFailedBuf\_Cnt\_M\_lgc[30] CTCFailedBuf\_Cnt\_M\_lgc[31] 1 CTCFailedBuf\_Cnt\_M\_lgc[32] 1 CTCFailedBuf\_Cnt\_M\_lgc[33] 1 1 0 CTCFailedBuf\_Cnt\_M\_lgc[34] 0 CTCFailedBuf\_Cnt\_M\_lgc[35] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[36] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[37] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[38] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[39] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[40] 0 0 CTCFailedBuf Cnt M Igc[41] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[42] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[43] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[44] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[45] 0 0

2018-04-10, 18:44:44+0530



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Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[46]	0	0	
CTCFailedBuf_Cnt_M_lgc[47]	0	0	~
CTCFailedBuf_Cnt_M_lgc[48]	0	0	~
CTCFailedBuf_Cnt_M_lgc[49]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[50]	0	0	~
CTCFailedBuf_Cnt_M_lgc[51]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[52]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[53]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[54]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[55]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[56]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[57]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[58]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[59]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[60]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[61]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[62]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[63]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[64]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[65]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[66]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[67]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[68]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[69]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[70]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[71]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[72]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[73]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[74]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[75]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[76]	0	0	<b>✓</b>
CTCFailed_Cnt_M_lgc	0	0	<b>✓</b>
Demlf_DTCStatusChanged()	0	0	<b>✓</b>
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	0	0	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte Write Ap Demlf CTCFailed Cnt lgc	1	Rte Write Ap Demlf CTCFailed Cnt lgc	1	~

#### Test Case 3: Path Test

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

CPU Cycles:

TS 3.1 3237.00 Cycles TS 3.2 2512.00 Cycles TS 3.3 2424.00 Cycles TS 3.4 680.00 Cycles TS 3.5 3208.00 Cycles

Description Vector Description:

Test Step 3.1 (Repeat Count = 1)	✓
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	0
CTCFailedBuf_Cnt_M_lgc[1]	0
CTCFailedBuf_Cnt_M_lgc[2]	0
CTCFailedBuf_Cnt_M_lgc[3]	0
CTCFailedBuf_Cnt_M_lgc[4]	0
CTCFailedBuf_Cnt_M_lgc[5]	0

### **TEST DETAILS REPORT** Ch n e

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Name	Input Value
CTCFailedBuf_Cnt_M_lgc[6]	0
CTCFailedBuf_Cnt_M_lgc[7]	0
CTCFailedBuf_Cnt_M_lgc[8]	0
CTCFailedBuf_Cnt_M_lgc[9]	0
CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11]	0
CTCFailedBuf_Cnt_M_lgc[12]	0
CTCFailedBuf_Cnt_M_lgc[13]	0
CTCFailedBuf_Cnt_M_lgc[14]	0
CTCFailedBuf_Cnt_M_lgc[15]	0
CTCFailedBuf_Cnt_M_lgc[16]	0
CTCFailedBuf_Cnt_M_lgc[17]	0
CTCFailedBuf_Cnt_M_lgc[18]	0
CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	0
CTCFailedBuf_Cnt_M_lgc[24]	0
CTCFailedBuf_Cnt_M_lgc[25]	0
CTCFailedBuf_Cnt_M_lgc[26]	0
CTCFailedBuf_Cnt_M_lgc[27]	0
CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29]	0
CTCFailedBuf_Cnt_M_lgc[30]	0
CTCFailedBuf_Cnt_M_lgc[31]	0
CTCFailedBuf_Cnt_M_lgc[32]	0
CTCFailedBuf_Cnt_M_lgc[33]	0
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37] CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45] CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf Cnt M Igc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53] CTCFailedBuf_Cnt_M_lgc[54]	0
CTCFailedBuf_Cnt_M_lgc[54]	0
CTCFailedBuf_Cnt_M_lgc[56]	0
CTCFailedBuf_Cnt_M_Igc[57]	0
CTCFailedBuf_Cnt_M_lgc[58]	0
CTCFailedBuf_Cnt_M_Igc[59]	0
CTCFailedBuf_Cnt_M_lgc[60]	0
CTCFailedBuf_Cnt_M_lgc[61] CTCFailedBuf_Cnt_M_lgc[62]	0
CTCFailedBuf_Cnt_M_lgc[63]	0
CTCFailedBuf_Cnt_M_lgc[64]	0
CTCFailedBuf_Cnt_M_lgc[65]	0
CTCFailedBuf_Cnt_M_lgc[66]	0
CTCFailedBuf_Cnt_M_lgc[67]	0
CTCFailedBuf_Cnt_M_lgc[68]	0
CTCFailedBuf_Cnt_M_lgc[69]	0
CTCFailedBuf_Cnt_M_lgc[70]	0
CTCFailedBuf_Cnt_M_lgc[71] CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[72] CTCFailedBuf_Cnt_M_lgc[73]	0
CTCFailedBuf_Cnt_M_lgc[74]	0
CTCFailedBuf_Cnt_M_lgc[75]	0
CTCFailedBuf_Cnt_M_lgc[76]	0
CTCFailed_Cnt_M_lgc	0
DTC	0

2018-04-10, 18:44:44+0530



Name	Input Value
DTCKind	1
DTCStatusNew	0
DTCStatusOld	0
Dem_DTCNumberTable[0]	0
Dem_DTCNumberTable[1]	0
Dem_DTCNumberTable[2]	0
Dem_DTCNumberTable[3]	0
Dem_DTCNumberTable[4]	0
Dem_DTCNumberTable[5]	0
Dem_DTCNumberTable[6]	0
Dem_DTCNumberTable[7]	0
Dem_DTCNumberTable[8]	0
Dem_DTCNumberTable[9]	0
Dem_DTCNumberTable[10]	0
Dem_DTCNumberTable[11] Dem_DTCNumberTable[12]	0
Dem_DTCNumberTable[12] Dem_DTCNumberTable[13]	0
Dem_DTCNumberTable[14]	0
Dem DTCNumberTable[15]	0
Dem_DTCNumberTable[16]	0
Dem DTCNumberTable[17]	0
Dem_DTCNumberTable[18]	0
Dem_DTCNumberTable[19]	0
Dem_DTCNumberTable[20]	0
Dem_DTCNumberTable[21]	0
Dem_DTCNumberTable[22]	0
Dem_DTCNumberTable[23]	0
Dem_DTCNumberTable[24]	0
Dem_DTCNumberTable[25]	0
Dem_DTCNumberTable[26]	0
Dem_DTCNumberTable[27]	0
Dem_DTCNumberTable[28]	0
Dem_DTCNumberTable[29]	0
Dem_DTCNumberTable[30]	0
Dem_DTCNumberTable[31] Dem_DTCNumberTable[32]	0
Dem_DTCNumberTable[32]	0
Dem_DTCNumberTable[34]	0
Dem_DTCNumberTable[35]	0
Dem_DTCNumberTable[36]	0
Dem_DTCNumberTable[37]	0
Dem_DTCNumberTable[38]	0
Dem_DTCNumberTable[39]	0
Dem_DTCNumberTable[40]	0
Dem_DTCNumberTable[41]	0
Dem_DTCNumberTable[42]	0
Dem_DTCNumberTable[43]	0
Dem_DTCNumberTable[44]	0
Dem_DTCNumberTable[45]	0
Dem_DTCNumberTable[46]	0
Dem_DTCNumberTable[47]	0
Dem_DTCNumberTable[48]	0
Dem_DTCNumberTable[49]	0
Dem_DTCNumberTable[50]	0
Dem_DTCNumberTable[51] Dem_DTCNumberTable[52]	0
Dem_DTCNumberTable[52] Dem_DTCNumberTable[53]	0
Dem_DTCNumberTable[53] Dem_DTCNumberTable[54]	0
Dem_DTCNumberTable[55]	0
Dem_DTCNumberTable[55]	0
Dem_DTCNumberTable[57]	0
Dem_DTCNumberTable[58]	0
Dem_DTCNumberTable[59]	0
Dem_DTCNumberTable[60]	0
Dem_DTCNumberTable[61]	0
Dem_DTCNumberTable[62]	0
Dem_DTCNumberTable[63]	0
Dem_DTCNumberTable[64]	0
Dem_DTCNumberTable[65]	0
Dem_DTCNumberTable[66]	0
zez : e.tase. rasie[ee]	
Dem_DTCNumberTable[67]	0
	0 0 0

### **TEST DETAILS REPORT** Ch n e

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Den   Discharger   abelity   Den   Discharger   D	Denni_DTC3 Ch n e		IMACITAL
Des.   Dickmarks   Des.   Dick	Name	Input Value	
Dee DICAMENTE FAMILY DEED DICAMENTE FAMILY DEE DICAMENTE FAMILY DEE DICAMENTE FAMILY DEED DICAMENTE FAMILY DEE DICAMENTE FAMILY DEE DICAMENTE FAMILY DEED DICAMENTE FAMILY DEE DICAMENTE FAMILY DEE DICAMENTE FAMILY DEED DICAMENTE FAMILY DEE DICAMENTE FAMILY DEE DICAMENTE FAMILY DEED DICAMENTE FAMILY DEE DICAMENTE FAMILY DEE DICAMENTE FAMILY DEED DICAMENTE FAMILY DEE DICAMENTE FAMILY DEE DICAMENTE FAMILY DEE			
Dem DTC Author Forbeits   Dem DTC Author For		0	
Den_DICKounterSate(24) 0 Den_DICKounterSate(24) 0 Den_DICK_DICK_DICK_DICK_DICK_DICK_DICK_DICK		0	
Dest_DCVAlmost faller(1)	Dem_DTCNumberTable[73]	0	
Des_DITAC_HER_Intelled  Des_	Dem_DTCNumberTable[74]	0	
Des.   DOT     The Tester   Des.   DOT   DOT   Part   Dest   DOT   DOT   Part   Dest   DOT   DOT   Part   Dest   DOT   DOT   Part   DOT	Dem_DTCNumberTable[75]	0	
Den Dr.   The Table     255   Den Dr.   Th. Table   255	Dem_DTCNumberTable[76]	0	
Dem. DCT_PTI_Teste(2)   255   Dem. DCT_PTI_Teste(4)   255   Dem. DCT_PTI_Teste(6)   256   Dem. DCT_PTI_Teste(7)   256   Dem. DCT_PTI_Teste(8)   256   Dem. DCT_PTI_Teste(9)   256   Dem. DCT_PTI_Teste(10)   256   Dem. DCT_PTI_Teste(20)   256   Dem. DCT	Dem_DTC_FTB_Table[0]	255	
Dem_DTC_FTB_Take[9]	Dem_DTC_FTB_Table[1]	255	
Den_DTC_FIS_Table[4]   256   Den_DTC_FIS_Table[6]   256   Den_DTC_FIS_Ta	Dem_DTC_FTB_Table[2]		
Dem_DTC_FIR_Take[6] Dem_DTC_FIR_Take[6] Dem_DTC_FIR_Take[7] Dem_DTC_FIR_Take[7] Dem_DTC_FIR_Take[7] Dem_DTC_FIR_Take[8] Dem_DT			
Descript   Test   Table   1955   19			
Den. DCC_FER_Tabel(F)			
Dee, DTC_FFR_Table(9)   255   Dee, DTC_FFR_Table(9)   255   Dee, DTC_FFR_Table(10)   255   Dee, DTC_FFR_Table(12)   256   Dee, DTC_FFR_Table(12)   256   Dee, DTC_FFR_Table(12)   256   Dee, DTC_FFR_Table(12)   256   Dee, DTC_FFR_Table(14)   266   Dee, DTC_FFR_Table(15)   265			
Dem. DTC_FFE_Tabel(9)   255			
Dem DTC_FIS Table(1) Dem DTC_FIS Table(2) Dem DTC_FIS Table(3) Dem DTC_F			
Dem DCF_FIB_Table[1]			
Dem   DTC_FTS   Table15    255			
Dem DTC_FRE_Table(14) Dem_DTC_FRE_Table(15) Dem_DTC_FRE_Table(15) Dem_DTC_FRE_Table(16) Dem_DTC_FRE_Table(17) Dem_DTC_FRE_Table(17) Dem_DTC_FRE_Table(17) Dem_DTC_FRE_Table(17) Dem_DTC_FRE_Table(17) Dem_DTC_FRE_Table(18) Dem_DTC_FRE_Table(19)			
Dem DTC_FTB_Table(19)   255			
Dem DIC_FIB_Table(19)			
Dem DTC_FIB_Table(18)   255			
Dem DTC_FTR_Tabel(19)			
Dem DTC_FFE_Table(19)   255			
Dem DTC_FTR_Table(19)			
Dem DTC_FTB_Table2[2] Dem_DTC_FTB_Table2[2] Dem_DTC_FTB_Table2[2] Dem_DTC_FTB_Table2[2] Dem_DTC_FTB_Table2[2] Dem_DTC_FTB_Table2[3] Dem_DTC_FTB_Table3[3] Dem_DTC_FTB_Table3[4] Dem_DTC_FTB_Table3[4] Dem_DTC_FTB_Table3[4] Dem_DTC_FTB_Table3[4] Dem_DTC_FTB_Table4[4]			
Dem DTC_FTB_Table(2)			
Dem. DTC_FFE_Table(2)   255		255	
Dem_DTC_FTB_Table(24)         255           Dem_DTC_FTB_Table(25)         255           Dem_DTC_FTB_Table(27)         255           Dem_DTC_FTB_Table(27)         255           Dem_DTC_FTB_Table(28)         255           Dem_DTC_FTB_Table(29)         255           Dem_DTC_FTB_Table(21)         255           Dem_DTC_FTB_Table(22)         255           Dem_DTC_FTB_Table(23)         255           Dem_DTC_FTB_Table(24)         255           Dem_DTC_FTB_Table(24)         255           Dem_DTC_FTB_Table(24)         255           Dem_DTC_FTB_Table(26)         255           Dem_DTC_FTB_Table(26)         255           Dem_DTC_FTB_Table(26)         255           Dem_DTC_FTB_Table(26)         255           Dem_DTC_FTB_Table(26)         255           Dem_DTC_FTB_Table(26)         255           Dem_DTC_FTB_Table(27)         255           Dem_DTC_FTB_Table(28)         255		255	
Dem_DTC_FTB_Table(2F) Dem_DTC_FTB_Table(EF)	Dem_DTC_FTB_Table[23]	255	
Dem DTC FTB Table(2R)         255           Dem DTC FTB Table(2R)         255           Dem DTC FTB Table(2R)         255           Dem DTC FTB Table(3R)         255           Dem DTC FTB Table(4R)         255	Dem_DTC_FTB_Table[24]	255	
Dem_DTC_FIB_Table(27)         255           Dem_DTC_FIB_Table(28)         255           Dem_DTC_FIB_Table(20)         255           Dem_DTC_FIB_Table(30)         255           Dem_DTC_FIB_Table(31)         255           Dem_DTC_FIB_Table(32)         255           Dem_DTC_FIB_Table(33)         255           Dem_DTC_FIB_Table(34)         255           Dem_DTC_FIB_Table(35)         255           Dem_DTC_FIB_Table(36)         255           Dem_DTC_FIB_Table(37)         255           Dem_DTC_FIB_Table(37)         255           Dem_DTC_FIB_Table(37)         255           Dem_DTC_FIB_Table(40)         255           Dem_DTC_FIB_Table(40)         255           Dem_DTC_FIB_Table(40)         255           Dem_DTC_FIB_Table(41)         255           Dem_DTC_FIB_Table(42)         255           Dem_DTC_FIB_Table(43)         255           Dem_DTC_FIB_Table(44)         255           Dem_DTC_FIB_Table(44)         255           Dem_DTC_FIB_Table(46)         255           Dem_DTC_FIB_Table(46)         255           Dem_DTC_FIB_Table(46)         255           Dem_DTC_FIB_Table(46)         255           Dem_DTC_FIB_Table(46)         255	Dem_DTC_FTB_Table[25]	255	
Dem_DTC_FTB_Table(28)         255           Dem_DTC_FTB_Table(30)         255           Dem_DTC_FTB_Table(31)         255           Dem_DTC_FTB_Table(31)         255           Dem_DTC_FTB_Table(33)         255           Dem_DTC_FTB_Table(33)         255           Dem_DTC_FTB_Table(34)         255           Dem_DTC_FTB_Table(35)         255           Dem_DTC_FTB_Table(36)         255           Dem_DTC_FTB_Table(37)         255           Dem_DTC_FTB_Table(38)         255           Dem_DTC_FTB_Table(38)         255           Dem_DTC_FTB_Table(38)         255           Dem_DTC_FTB_Table(48)         255           Dem_DTC_FTB_Table(49)         255           Dem_DTC_FTB_Table(41)         255           Dem_DTC_FTB_Table(42)         255           Dem_DTC_FTB_Table(44)         255           Dem_DTC_FTB_Table(44)         255           Dem_DTC_FTB_Table(44)         255           Dem_DTC_FTB_Table(46)         255           Dem_DTC_FTB_Table(47)         255           Dem_DTC_FTB_Table(48)         255           Dem_DTC_FTB_Table(49)         255           Dem_DTC_FTB_Table(49)         255           Dem_DTC_FTB_Table(49)         255	Dem_DTC_FTB_Table[26]	255	
Dem_DTC_FTB_Table(30)         255           Dem_DTC_FTB_Table(31)         255           Dem_DTC_FTB_Table(32)         255           Dem_DTC_FTB_Table(33)         255           Dem_DTC_FTB_Table(33)         255           Dem_DTC_FTB_Table(35)         255           Dem_DTC_FTB_Table(37)         255           Dem_DTC_FTB_Table(37)         255           Dem_DTC_FTB_Table(38)         255           Dem_DTC_FTB_Table(38)         255           Dem_DTC_FTB_Table(38)         255           Dem_DTC_FTB_Table(40)         255           Dem_DTC_FTB_Table(41)         255           Dem_DTC_FTB_Table(42)         255           Dem_DTC_FTB_Table(43)         255           Dem_DTC_FTB_Table(43)         255           Dem_DTC_FTB_Table(44)         255           Dem_DTC_FTB_Table(45)         255           Dem_DTC_FTB_Table(46)         255           Dem_DTC_FTB_Table(47)         255           Dem_DTC_FTB_Table(48)         255           Dem_DTC_FTB_Table(48)         255           Dem_DTC_FTB_Table(48)         255           Dem_DTC_FTB_Table(48)         255           Dem_DTC_FTB_Table(48)         255           Dem_DTC_FTB_Table(51)         255	Dem_DTC_FTB_Table[27]	255	
Dem_DTC_FTB_Table(31)         255           Dem_DTC_FTB_Table(32)         255           Dem_DTC_FTB_Table(33)         255           Dem_DTC_FTB_Table(33)         255           Dem_DTC_FTB_Table(34)         255           Dem_DTC_FTB_Table(35)         255           Dem_DTC_FTB_Table(36)         255           Dem_DTC_FTB_Table(37)         255           Dem_DTC_FTB_Table(38)         255           Dem_DTC_FTB_Table(39)         255           Dem_DTC_FTB_Table(40)         255           Dem_DTC_FTB_Table(41)         255           Dem_DTC_FTB_Table(42)         255           Dem_DTC_FTB_Table(43)         255           Dem_DTC_FTB_Table(44)         255           Dem_DTC_FTB_Table(43)         255           Dem_DTC_FTB_Table(44)         255           Dem_DTC_FTB_Table(44)         255           Dem_DTC_FTB_Table(45)         255           Dem_DTC_FTB_Table(46)         255           Dem_DTC_FTB_Table(47)         255           Dem_DTC_FTB_Table(48)         255           Dem_DTC_FTB_Table(49)         255           Dem_DTC_FTB_Table(49)         255           Dem_DTC_FTB_Table(51)         255           Dem_DTC_FTB_Table(51)         255	Dem_DTC_FTB_Table[28]		
Dem_ DTC_FTB_ Table(32)         255           Dem_ DTC_FTB_ Table(33)         255           Dem_ DTC_FTB_ Table(34)         255           Dem_ DTC_FTB_ Table(35)         255           Dem_ DTC_FTB_ Table(36)         255           Dem_ DTC_FTB_ Table(37)         255           Dem_ DTC_FTB_ Table(37)         255           Dem_ DTC_FTB_ Table(39)         255           Dem_ DTC_FTB_ Table(40)         255           Dem_ DTC_FTB_ Table(41)         255           Dem_ DTC_FTB_ Table(42)         255           Dem_ DTC_FTB_ Table(43)         255           Dem_ DTC_FTB_ Table(44)         255           Dem_ DTC_FTB_ Table(45)         255           Dem_ DTC_FTB_ Table(47)         255           Dem_ DTC_FTB_ Table(51)         255           Dem_ DTC_FTB_ Table(51)         255 <t< td=""><td>Dem_DTC_FTB_Table[29]</td><td></td><td></td></t<>	Dem_DTC_FTB_Table[29]		
Dem_DTC_FTB_Table(32)         255           Dem_DTC_FTB_Table(33)         255           Dem_DTC_FTB_Table(35)         255           Dem_DTC_FTB_Table(36)         255           Dem_DTC_FTB_Table(37)         255           Dem_DTC_FTB_Table(37)         255           Dem_DTC_FTB_Table(39)         255           Dem_DTC_FTB_Table(40)         255           Dem_DTC_FTB_Table(41)         255           Dem_DTC_FTB_Table(42)         255           Dem_DTC_FTB_Table(43)         255           Dem_DTC_FTB_Table(44)         255           Dem_DTC_FTB_Table(44)         255           Dem_DTC_FTB_Table(44)         255           Dem_DTC_FTB_Table(44)         255           Dem_DTC_FTB_Table(46)         255           Dem_DTC_FTB_Table(46)         255           Dem_DTC_FTB_Table(47)         255           Dem_DTC_FTB_Table(48)         255           Dem_DTC_FTB_Table(49)         255           Dem_DTC_FTB_Table(49)         255           Dem_DTC_FTB_Table(50)         255           Dem_DTC_FTB_Table(51)         255           Dem_DTC_FTB_Table(53)         255           Dem_DTC_FTB_Table(53)         255           Dem_DTC_FTB_Table(54)         255			
Dem_DTC_FTB_Table(34)         255           Dem_DTC_FTB_Table(34)         255           Dem_DTC_FTB_Table(35)         255           Dem_DTC_FTB_Table(37)         255           Dem_DTC_FTB_Table(37)         255           Dem_DTC_FTB_Table(38)         255           Dem_DTC_FTB_Table(39)         255           Dem_DTC_FTB_Table(40)         255           Dem_DTC_FTB_Table(41)         255           Dem_DTC_FTB_Table(42)         255           Dem_DTC_FTB_Table(43)         255           Dem_DTC_FTB_Table(44)         255           Dem_DTC_FTB_Table(44)         255           Dem_DTC_FTB_Table(45)         255           Dem_DTC_FTB_Table(46)         255           Dem_DTC_FTB_Table(47)         255           Dem_DTC_FTB_Table(47)         255           Dem_DTC_FTB_Table(48)         255           Dem_DTC_FTB_Table(48)         255           Dem_DTC_FTB_Table(49)         255           Dem_DTC_FTB_Table(51)         255           Dem_DTC_FTB_Table(51)         255           Dem_DTC_FTB_Table(51)         255           Dem_DTC_FTB_Table(51)         255           Dem_DTC_FTB_Table(52)         255           Dem_DTC_FTB_Table(53)         255			
Dem_DTC_FTB_Table(54)         255           Dem_DTC_FTB_Table(55)         255           Dem_DTC_FTB_Table(36)         255           Dem_DTC_FTB_Table(37)         255           Dem_DTC_FTB_Table(38)         255           Dem_DTC_FTB_Table(40)         255           Dem_DTC_FTB_Table(41)         255           Dem_DTC_FTB_Table(42)         255           Dem_DTC_FTB_Table(43)         255           Dem_DTC_FTB_Table(43)         255           Dem_DTC_FTB_Table(44)         255           Dem_DTC_FTB_Table(44)         255           Dem_DTC_FTB_Table(46)         255           Dem_DTC_FTB_Table(46)         255           Dem_DTC_FTB_Table(46)         255           Dem_DTC_FTB_Table(47)         255           Dem_DTC_FTB_Table(47)         255           Dem_DTC_FTB_Table(48)         255           Dem_DTC_FTB_Table(50)         255           Dem_DTC_FTB_Table(50)         255           Dem_DTC_FTB_Table(51)         255           Dem_DTC_FTB_Table(53)         255           Dem_DTC_FTB_Table(53)         255           Dem_DTC_FTB_Table(56)         255           Dem_DTC_FTB_Table(56)         255           Dem_DTC_FTB_Table(56)         255			
Dem_DTC_FTB_Table(35)         255           Dem_DTC_FTB_Table(37)         255           Dem_DTC_FTB_Table(38)         255           Dem_DTC_FTB_Table(38)         255           Dem_DTC_FTB_Table(40)         255           Dem_DTC_FTB_Table(41)         255           Dem_DTC_FTB_Table(42)         255           Dem_DTC_FTB_Table(42)         255           Dem_DTC_FTB_Table(43)         255           Dem_DTC_FTB_Table(44)         255           Dem_DTC_FTB_Table(45)         255           Dem_DTC_FTB_Table(46)         255           Dem_DTC_FTB_Table(46)         255           Dem_DTC_FTB_Table(46)         255           Dem_DTC_FTB_Table(46)         255           Dem_DTC_FTB_Table(48)         255           Dem_DTC_FTB_Table(48)         255           Dem_DTC_FTB_Table(49)         255           Dem_DTC_FTB_Table(50)         255           Dem_DTC_FTB_Table(50)         255           Dem_DTC_FTB_Table(51)         255           Dem_DTC_FTB_Table(52)         255           Dem_DTC_FTB_Table(53)         255           Dem_DTC_FTB_Table(54)         255           Dem_DTC_FTB_Table(55)         255           Dem_DTC_FTB_Table(56)         255			
Dem_DTC_FTB_Table[36]         255           Dem_DTC_FTB_Table[37]         255           Dem_DTC_FTB_Table[38]         255           Dem_DTC_FTB_Table[40]         255           Dem_DTC_FTB_Table[40]         255           Dem_DTC_FTB_Table[41]         255           Dem_DTC_FTB_Table[42]         255           Dem_DTC_FTB_Table[43]         255           Dem_DTC_FTB_Table[44]         255           Dem_DTC_FTB_Table[44]         255           Dem_DTC_FTB_Table[45]         255           Dem_DTC_FTB_Table[46]         255           Dem_DTC_FTB_Table[47]         255           Dem_DTC_FTB_Table[48]         255           Dem_DTC_FTB_Table[47]         255           Dem_DTC_FTB_Table[48]         255           Dem_DTC_FTB_Table[49]         255           Dem_DTC_FTB_Table[49]         255           Dem_DTC_FTB_Table[50]         255           Dem_DTC_FTB_Table[51]         255           Dem_DTC_FTB_Table[52]         255           Dem_DTC_FTB_Table[63]         255           Dem_DTC_FTB_Table[64]         255           Dem_DTC_FTB_Table[65]         255           Dem_DTC_FTB_Table[66]         255           Dem_DTC_FTB_Table[66]         255			
Dem_DTC_FTB_Table[37]         255           Dem_DTC_FTB_Table[38]         255           Dem_DTC_FTB_Table[40]         255           Dem_DTC_FTB_Table[41]         255           Dem_DTC_FTB_Table[42]         255           Dem_DTC_FTB_Table[43]         255           Dem_DTC_FTB_Table[43]         255           Dem_DTC_FTB_Table[44]         255           Dem_DTC_FTB_Table[45]         255           Dem_DTC_FTB_Table[46]         255           Dem_DTC_FTB_Table[47]         255           Dem_DTC_FTB_Table[48]         255           Dem_DTC_FTB_Table[48]         255           Dem_DTC_FTB_Table[49]         255           Dem_DTC_FTB_Table[49]         255           Dem_DTC_FTB_Table[50]         255           Dem_DTC_FTB_Table[51]         255           Dem_DTC_FTB_Table[52]         255           Dem_DTC_FTB_Table[53]         255           Dem_DTC_FTB_Table[54]         255           Dem_DTC_FTB_Table[55]         255           Dem_DTC_FTB_Table[56]         255           Dem_DTC_FTB_Table[68]         255           Dem_DTC_FTB_Table[69]         255           Dem_DTC_FTB_Table[69]         255           Dem_DTC_FTB_Table[61]         255			
Dem_DTC_FTB_Table[38]         255           Dem_DTC_FTB_Table[40]         255           Dem_DTC_FTB_Table[41]         255           Dem_DTC_FTB_Table[42]         255           Dem_DTC_FTB_Table[43]         255           Dem_DTC_FTB_Table[44]         255           Dem_DTC_FTB_Table[44]         255           Dem_DTC_FTB_Table[46]         255           Dem_DTC_FTB_Table[47]         255           Dem_DTC_FTB_Table[48]         255           Dem_DTC_FTB_Table[49]         255           Dem_DTC_FTB_Table[49]         255           Dem_DTC_FTB_Table[49]         255           Dem_DTC_FTB_Table[50]         255           Dem_DTC_FTB_Table[51]         255           Dem_DTC_FTB_Table[52]         255           Dem_DTC_FTB_Table[52]         255           Dem_DTC_FTB_Table[53]         255           Dem_DTC_FTB_Table[54]         255           Dem_DTC_FTB_Table[55]         255           Dem_DTC_FTB_Table[65]         255           Dem_DTC_FTB_Table[66]         255           Dem_DTC_FTB_Table[67]         255           Dem_DTC_FTB_Table[68]         255           Dem_DTC_FTB_Table[68]         255           Dem_DTC_FTB_Table[68]         255			
Dem_DTC_FTB_Table(39)         255           Dem_DTC_FTB_Table(40)         255           Dem_DTC_FTB_Table(41)         255           Dem_DTC_FTB_Table(42)         255           Dem_DTC_FTB_Table(43)         255           Dem_DTC_FTB_Table(44)         255           Dem_DTC_FTB_Table(45)         255           Dem_DTC_FTB_Table(46)         255           Dem_DTC_FTB_Table(47)         255           Dem_DTC_FTB_Table(48)         255           Dem_DTC_FTB_Table(49)         255           Dem_DTC_FTB_Table(50)         255           Dem_DTC_FTB_Table(51)         255           Dem_DTC_FTB_Table(52)         255           Dem_DTC_FTB_Table(51)         255           Dem_DTC_FTB_Table(52)         255           Dem_DTC_FTB_Table(53)         255           Dem_DTC_FTB_Table(53)         255           Dem_DTC_FTB_Table(54)         255           Dem_DTC_FTB_Table(56)         255           Dem_DTC_FTB_Table(56)         255           Dem_DTC_FTB_Table(56)         255           Dem_DTC_FTB_Table(57)         255           Dem_DTC_FTB_Table(59)         255           Dem_DTC_FTB_Table(59)         255           Dem_DTC_FTB_Table(61)         255			
Dem_DTC_FTB_Table[41]         255           Dem_DTC_FTB_Table[42]         255           Dem_DTC_FTB_Table[43]         255           Dem_DTC_FTB_Table[44]         255           Dem_DTC_FTB_Table[44]         255           Dem_DTC_FTB_Table[46]         255           Dem_DTC_FTB_Table[46]         255           Dem_DTC_FTB_Table[47]         255           Dem_DTC_FTB_Table[48]         255           Dem_DTC_FTB_Table[48]         255           Dem_DTC_FTB_Table[48]         255           Dem_DTC_FTB_Table[60]         255           Dem_DTC_FTB_Table[61]         255           Dem_DTC_FTB_Table[62]         255           Dem_DTC_FTB_Table[62]         255           Dem_DTC_FTB_Table[62]         255           Dem_DTC_FTB_Table[63]         255           Dem_DTC_FTB_Table[64]         255           Dem_DTC_FTB_Table[65]         255           Dem_DTC_FTB_Table[66]         255           Dem_DTC_FTB_Table[67]         255           Dem_DTC_FTB_Table[68]         255           Dem_DTC_FTB_Table[69]         255           Dem_DTC_FTB_Table[60]         255           Dem_DTC_FTB_Table[61]         255           Dem_DTC_FTB_Table[61]         255			
Dem_DTC_FTB_Table[41]         255           Dem_DTC_FTB_Table[42]         255           Dem_DTC_FTB_Table[43]         255           Dem_DTC_FTB_Table[44]         255           Dem_DTC_FTB_Table[45]         255           Dem_DTC_FTB_Table[46]         255           Dem_DTC_FTB_Table[47]         255           Dem_DTC_FTB_Table[48]         255           Dem_DTC_FTB_Table[48]         255           Dem_DTC_FTB_Table[49]         255           Dem_DTC_FTB_Table[50]         255           Dem_DTC_FTB_Table[51]         255           Dem_DTC_FTB_Table[52]         255           Dem_DTC_FTB_Table[53]         255           Dem_DTC_FTB_Table[53]         255           Dem_DTC_FTB_Table[54]         255           Dem_DTC_FTB_Table[55]         255           Dem_DTC_FTB_Table[56]         255           Dem_DTC_FTB_Table[56]         255           Dem_DTC_FTB_Table[56]         255           Dem_DTC_FTB_Table[66]         255           Dem_DTC_FTB_Table[67]         255           Dem_DTC_FTB_Table[68]         255           Dem_DTC_FTB_Table[69]         255           Dem_DTC_FTB_Table[60]         255           Dem_DTC_FTB_Table[61]         255			
Dem_DTC_FTB_Table[42]         255           Dem_DTC_FTB_Table[43]         255           Dem_DTC_FTB_Table[44]         255           Dem_DTC_FTB_Table[45]         255           Dem_DTC_FTB_Table[46]         255           Dem_DTC_FTB_Table[47]         255           Dem_DTC_FTB_Table[48]         255           Dem_DTC_FTB_Table[49]         255           Dem_DTC_FTB_Table[50]         255           Dem_DTC_FTB_Table[51]         255           Dem_DTC_FTB_Table[52]         255           Dem_DTC_FTB_Table[53]         255           Dem_DTC_FTB_Table[53]         255           Dem_DTC_FTB_Table[53]         255           Dem_DTC_FTB_Table[54]         255           Dem_DTC_FTB_Table[55]         255           Dem_DTC_FTB_Table[55]         255           Dem_DTC_FTB_Table[56]         255           Dem_DTC_FTB_Table[57]         255           Dem_DTC_FTB_Table[58]         255           Dem_DTC_FTB_Table[58]         255           Dem_DTC_FTB_Table[60]         255           Dem_DTC_FTB_Table[61]         255           Dem_DTC_FTB_Table[62]         255           Dem_DTC_FTB_Table[62]         255           Dem_DTC_FTB_Table[63]         255			
Dem_DTC_FTB_Table[43]         255           Dem_DTC_FTB_Table[44]         255           Dem_DTC_FTB_Table[45]         255           Dem_DTC_FTB_Table[46]         255           Dem_DTC_FTB_Table[47]         255           Dem_DTC_FTB_Table[48]         255           Dem_DTC_FTB_Table[49]         255           Dem_DTC_FTB_Table[50]         255           Dem_DTC_FTB_Table[51]         255           Dem_DTC_FTB_Table[52]         255           Dem_DTC_FTB_Table[53]         255           Dem_DTC_FTB_Table[53]         255           Dem_DTC_FTB_Table[54]         255           Dem_DTC_FTB_Table[55]         255           Dem_DTC_FTB_Table[56]         255           Dem_DTC_FTB_Table[56]         255           Dem_DTC_FTB_Table[56]         255           Dem_DTC_FTB_Table[56]         255           Dem_DTC_FTB_Table[57]         255           Dem_DTC_FTB_Table[68]         255           Dem_DTC_FTB_Table[69]         255           Dem_DTC_FTB_Table[69]         255           Dem_DTC_FTB_Table[60]         255           Dem_DTC_FTB_Table[61]         255           Dem_DTC_FTB_Table[62]         255           Dem_DTC_FTB_Table[63]         255			
Dem_DTC_FTB_Table[44]         255           Dem_DTC_FTB_Table[45]         255           Dem_DTC_FTB_Table[47]         255           Dem_DTC_FTB_Table[48]         255           Dem_DTC_FTB_Table[48]         255           Dem_DTC_FTB_Table[49]         255           Dem_DTC_FTB_Table[50]         255           Dem_DTC_FTB_Table[51]         255           Dem_DTC_FTB_Table[52]         255           Dem_DTC_FTB_Table[53]         255           Dem_DTC_FTB_Table[53]         255           Dem_DTC_FTB_Table[54]         255           Dem_DTC_FTB_Table[55]         255           Dem_DTC_FTB_Table[56]         255           Dem_DTC_FTB_Table[57]         255           Dem_DTC_FTB_Table[57]         255           Dem_DTC_FTB_Table[58]         255           Dem_DTC_FTB_Table[59]         255           Dem_DTC_FTB_Table[69]         255           Dem_DTC_FTB_Table[61]         255           Dem_DTC_FTB_Table[62]         255           Dem_DTC_FTB_Table[63]         255           Dem_DTC_FTB_Table[63]         255           Dem_DTC_FTB_Table[63]         255           Dem_DTC_FTB_Table[64]         255           Dem_DTC_FTB_Table[63]         255			
Dem_DTC_FTB_Table[45]         255           Dem_DTC_FTB_Table[47]         255           Dem_DTC_FTB_Table[48]         255           Dem_DTC_FTB_Table[49]         255           Dem_DTC_FTB_Table[50]         255           Dem_DTC_FTB_Table[51]         255           Dem_DTC_FTB_Table[52]         255           Dem_DTC_FTB_Table[52]         255           Dem_DTC_FTB_Table[53]         255           Dem_DTC_FTB_Table[54]         255           Dem_DTC_FTB_Table[55]         255           Dem_DTC_FTB_Table[56]         255           Dem_DTC_FTB_Table[57]         255           Dem_DTC_FTB_Table[57]         255           Dem_DTC_FTB_Table[58]         255           Dem_DTC_FTB_Table[58]         255           Dem_DTC_FTB_Table[69]         255           Dem_DTC_FTB_Table[61]         255           Dem_DTC_FTB_Table[61]         255           Dem_DTC_FTB_Table[61]         255           Dem_DTC_FTB_Table[62]         255           Dem_DTC_FTB_Table[63]         255           Dem_DTC_FTB_Table[64]         255           Dem_DTC_FTB_Table[63]         255           Dem_DTC_FTB_Table[64]         255			
Dem_DTC_FTB_Table[46]       255         Dem_DTC_FTB_Table[47]       255         Dem_DTC_FTB_Table[48]       255         Dem_DTC_FTB_Table[49]       255         Dem_DTC_FTB_Table[50]       255         Dem_DTC_FTB_Table[51]       255         Dem_DTC_FTB_Table[52]       255         Dem_DTC_FTB_Table[53]       255         Dem_DTC_FTB_Table[53]       255         Dem_DTC_FTB_Table[54]       255         Dem_DTC_FTB_Table[55]       255         Dem_DTC_FTB_Table[56]       255         Dem_DTC_FTB_Table[57]       255         Dem_DTC_FTB_Table[58]       255         Dem_DTC_FTB_Table[59]       255         Dem_DTC_FTB_Table[69]       255         Dem_DTC_FTB_Table[60]       255         Dem_DTC_FTB_Table[61]       255         Dem_DTC_FTB_Table[62]       255         Dem_DTC_FTB_Table[62]       255         Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[64]       255         Dem_DTC_FTB_Table[64]       255			
Dem_DTC_FTB_Table[47]       255         Dem_DTC_FTB_Table[48]       255         Dem_DTC_FTB_Table[49]       255         Dem_DTC_FTB_Table[50]       255         Dem_DTC_FTB_Table[51]       255         Dem_DTC_FTB_Table[52]       255         Dem_DTC_FTB_Table[53]       255         Dem_DTC_FTB_Table[53]       255         Dem_DTC_FTB_Table[54]       255         Dem_DTC_FTB_Table[55]       255         Dem_DTC_FTB_Table[56]       255         Dem_DTC_FTB_Table[57]       255         Dem_DTC_FTB_Table[58]       255         Dem_DTC_FTB_Table[58]       255         Dem_DTC_FTB_Table[69]       255         Dem_DTC_FTB_Table[60]       255         Dem_DTC_FTB_Table[61]       255         Dem_DTC_FTB_Table[62]       255         Dem_DTC_FTB_Table[62]       255         Dem_DTC_FTB_Table[62]       255         Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[64]       255			
Dem_DTC_FTB_Table[48]       255         Dem_DTC_FTB_Table[49]       255         Dem_DTC_FTB_Table[50]       255         Dem_DTC_FTB_Table[51]       255         Dem_DTC_FTB_Table[52]       255         Dem_DTC_FTB_Table[53]       255         Dem_DTC_FTB_Table[54]       255         Dem_DTC_FTB_Table[55]       255         Dem_DTC_FTB_Table[56]       255         Dem_DTC_FTB_Table[57]       255         Dem_DTC_FTB_Table[58]       255         Dem_DTC_FTB_Table[58]       255         Dem_DTC_FTB_Table[69]       255         Dem_DTC_FTB_Table[60]       255         Dem_DTC_FTB_Table[60]       255         Dem_DTC_FTB_Table[61]       255         Dem_DTC_FTB_Table[62]       255         Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[64]       255			
Dem_DTC_FTB_Table[49]       255         Dem_DTC_FTB_Table[51]       255         Dem_DTC_FTB_Table[52]       255         Dem_DTC_FTB_Table[53]       255         Dem_DTC_FTB_Table[54]       255         Dem_DTC_FTB_Table[55]       255         Dem_DTC_FTB_Table[56]       255         Dem_DTC_FTB_Table[56]       255         Dem_DTC_FTB_Table[57]       255         Dem_DTC_FTB_Table[58]       255         Dem_DTC_FTB_Table[58]       255         Dem_DTC_FTB_Table[59]       255         Dem_DTC_FTB_Table[60]       255         Dem_DTC_FTB_Table[61]       255         Dem_DTC_FTB_Table[62]       255         Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[62]       255         Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[64]       255	Dem_DTC_FTB_Table[48]		
Dem_DTC_FTB_Table[50]       255         Dem_DTC_FTB_Table[51]       255         Dem_DTC_FTB_Table[52]       255         Dem_DTC_FTB_Table[53]       255         Dem_DTC_FTB_Table[54]       255         Dem_DTC_FTB_Table[55]       255         Dem_DTC_FTB_Table[56]       255         Dem_DTC_FTB_Table[57]       255         Dem_DTC_FTB_Table[58]       255         Dem_DTC_FTB_Table[59]       255         Dem_DTC_FTB_Table[60]       255         Dem_DTC_FTB_Table[61]       255         Dem_DTC_FTB_Table[62]       255         Dem_DTC_FTB_Table[62]       255         Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[64]       255			
Dem_DTC_FTB_Table[51]       255         Dem_DTC_FTB_Table[52]       255         Dem_DTC_FTB_Table[53]       255         Dem_DTC_FTB_Table[54]       255         Dem_DTC_FTB_Table[55]       255         Dem_DTC_FTB_Table[56]       255         Dem_DTC_FTB_Table[57]       255         Dem_DTC_FTB_Table[58]       255         Dem_DTC_FTB_Table[58]       255         Dem_DTC_FTB_Table[59]       255         Dem_DTC_FTB_Table[60]       255         Dem_DTC_FTB_Table[61]       255         Dem_DTC_FTB_Table[62]       255         Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[64]       255	Dem_DTC_FTB_Table[50]		
Dem_DTC_FTB_Table[53]       255         Dem_DTC_FTB_Table[54]       255         Dem_DTC_FTB_Table[55]       255         Dem_DTC_FTB_Table[56]       255         Dem_DTC_FTB_Table[57]       255         Dem_DTC_FTB_Table[58]       255         Dem_DTC_FTB_Table[59]       255         Dem_DTC_FTB_Table[60]       255         Dem_DTC_FTB_Table[61]       255         Dem_DTC_FTB_Table[62]       255         Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[64]       255	Dem_DTC_FTB_Table[51]	255	
Dem_DTC_FTB_Table[54]       255         Dem_DTC_FTB_Table[55]       255         Dem_DTC_FTB_Table[56]       255         Dem_DTC_FTB_Table[57]       255         Dem_DTC_FTB_Table[58]       255         Dem_DTC_FTB_Table[59]       255         Dem_DTC_FTB_Table[60]       255         Dem_DTC_FTB_Table[61]       255         Dem_DTC_FTB_Table[62]       255         Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[64]       255	Dem_DTC_FTB_Table[52]	255	
Dem_DTC_FTB_Table[55]       255         Dem_DTC_FTB_Table[56]       255         Dem_DTC_FTB_Table[57]       255         Dem_DTC_FTB_Table[58]       255         Dem_DTC_FTB_Table[59]       255         Dem_DTC_FTB_Table[60]       255         Dem_DTC_FTB_Table[61]       255         Dem_DTC_FTB_Table[62]       255         Dem_DTC_FTB_Table[62]       255         Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[64]       255	Dem_DTC_FTB_Table[53]	255	
Dem_DTC_FTB_Table[56]       255         Dem_DTC_FTB_Table[57]       255         Dem_DTC_FTB_Table[58]       255         Dem_DTC_FTB_Table[59]       255         Dem_DTC_FTB_Table[60]       255         Dem_DTC_FTB_Table[61]       255         Dem_DTC_FTB_Table[62]       255         Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[64]       255	Dem_DTC_FTB_Table[54]		
Dem_DTC_FTB_Table[57]       255         Dem_DTC_FTB_Table[58]       255         Dem_DTC_FTB_Table[59]       255         Dem_DTC_FTB_Table[60]       255         Dem_DTC_FTB_Table[61]       255         Dem_DTC_FTB_Table[62]       255         Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[64]       255			
Dem_DTC_FTB_Table[58]       255         Dem_DTC_FTB_Table[59]       255         Dem_DTC_FTB_Table[60]       255         Dem_DTC_FTB_Table[61]       255         Dem_DTC_FTB_Table[62]       255         Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[64]       255	Dem_DTC_FTB_Table[56]		
Dem_DTC_FTB_Table[59]       255         Dem_DTC_FTB_Table[60]       255         Dem_DTC_FTB_Table[61]       255         Dem_DTC_FTB_Table[62]       255         Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[64]       255			
Dem_DTC_FTB_Table[60]       255         Dem_DTC_FTB_Table[61]       255         Dem_DTC_FTB_Table[62]       255         Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[64]       255	Dem_DTC_FTB_Table[58]		
Dem_DTC_FTB_Table[61]       255         Dem_DTC_FTB_Table[62]       255         Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[64]       255			
Dem_DTC_FTB_Table[62]       255         Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[64]       255	Dem_DTC_FTB_Table[60]		
Dem_DTC_FTB_Table[63]       255         Dem_DTC_FTB_Table[64]       255			
Dem_DTC_FTB_Table[64] 255	Dem_DTC_FTB_Table[62]		
Dew_D1C_F1R_1abie[62]   522			
	Dem_DTC_FTB_Table[65]	255	

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value Dem DTC FTB Table[66] 255 Dem\_DTC\_FTB\_Table[67] 255 Dem\_DTC\_FTB\_Table[68] 255 Dem\_DTC\_FTB\_Table[69] 255 Dem\_DTC\_FTB\_Table[70] 255 Dem\_DTC\_FTB\_Table[71] 255 Dem DTC FTB Table[72] 255 Dem\_DTC\_FTB\_Table[73] 255 Dem\_DTC\_FTB\_Table[74] 255 Dem\_DTC\_FTB\_Table[75] 255 Dem\_DTC\_FTB\_Table[76] 255 **Actual Value Expected Value** Name Result CTCFailedBuf\_Cnt\_M\_lgc[0] 0 0 0 0 CTCFailedBuf\_Cnt\_M\_lgc[1] n n CTCFailedBuf Cnt M lgc[2] CTCFailedBuf\_Cnt\_M\_lgc[3] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[4] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[5] 0 0 CTCFailedBuf Cnt M lqc[6] 0 0  ${\sf CTCFailedBuf\_Cnt\_M\_lgc[7]}$ 0 0 CTCFailedBuf\_Cnt\_M\_lgc[8] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[9] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[10] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[11] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[12] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[13] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[14] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[15] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[16] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[17] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[18] 0 0 0 0 CTCFailedBuf\_Cnt\_M\_lgc[19] CTCFailedBuf\_Cnt\_M\_lgc[20] n n CTCFailedBuf Cnt M Igc[21] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[22] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[23] 0 0 ~ CTCFailedBuf\_Cnt\_M\_lgc[24] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[25] 0 CTCFailedBuf\_Cnt\_M\_lgc[26] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[27] 0 0 CTCFailedBuf Cnt M lqc[28] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[29] 0 0 CTCFailedBuf Cnt M lqc[30] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[31] 0 0 CTCFailedBuf Cnt M lqc[32] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[33] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[34] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[35] 0 0 0 CTCFailedBuf\_Cnt\_M\_lgc[36] 0 **~** CTCFailedBuf\_Cnt\_M\_lgc[37] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[38] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[39] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[40] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[41] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[42] 0 0 **~** CTCFailedBuf\_Cnt\_M\_lgc[43] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[44] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[45] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[46] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[47] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[48] 0 0 0 0 CTCFailedBuf\_Cnt\_M\_lgc[49] CTCFailedBuf Cnt M Igc[50] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[51] 0 0 CTCFailedBuf Cnt M lqc[52] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[53] 0 0 0 CTCFailedBuf Cnt M lqc[54] 0 CTCFailedBuf\_Cnt\_M\_lgc[55] 0 0 CTCFailedBuf Cnt M Igc[56] 0 0 CTCFailedBuf\_Cnt\_M\_Igc[57] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[58] 0 0  $CTCFailedBuf\_Cnt\_M\_lgc[59]$ 0 0 CTCFailedBuf\_Cnt\_M\_lgc[60] 0 0

Rte\_Write\_Ap\_DemIf\_CTCFailed\_Cnt\_lgc(data)

Demlf\_DTCS

2018-04-10, 18:44:44+0530



**Actual Value Expected Value** CTCFailedBuf\_Cnt\_M\_lgc[61] CTCFailedBuf\_Cnt\_M\_lgc[62] CTCFailedBuf\_Cnt\_M\_lgc[63] CTCFailedBuf\_Cnt\_M\_lgc[64] CTCFailedBuf\_Cnt\_M\_lgc[65] CTCFailedBuf\_Cnt\_M\_lgc[66] CTCFailedBuf\_Cnt\_M\_lgc[67] CTCFailedBuf\_Cnt\_M\_lgc[68] CTCFailedBuf\_Cnt\_M\_lgc[69] CTCFailedBuf\_Cnt\_M\_lgc[70] CTCFailedBuf\_Cnt\_M\_lgc[71] CTCFailedBuf\_Cnt\_M\_lgc[72] CTCFailedBuf\_Cnt\_M\_lgc[73] CTCFailedBuf\_Cnt\_M\_lgc[74] CTCFailedBuf\_Cnt\_M\_lgc[75] CTCFailedBuf\_Cnt\_M\_lgc[76] CTCFailed\_Cnt\_M\_lgc Demlf\_DTCStatusChanged() 

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	•

Test Step 3.2 (Repeat Count = 1)	Innut Value
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	0
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
TCFailedBuf_Cnt_M_lgc[18]	1
TCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	1
CTCFailedBuf_Cnt_M_lgc[21]	1
CTCFailedBuf_Cnt_M_lgc[22]	1
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf Cnt M lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
TCF alledBut_Crit_M_igc[20]	1
CTCFailedBut_Crit_ivi_igc[27]	1
	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	
TCFailedBuf_Cnt_M_lgc[31]	1
TCFailedBuf_Cnt_M_lgc[32]	1
TCFailedBuf_Cnt_M_lgc[33]	1
TCFailedBuf_Cnt_M_lgc[34]	1
TCFailedBuf_Cnt_M_lgc[35]	1
TCFailedBuf_Cnt_M_lgc[36]	1
TCFailedBuf_Cnt_M_lgc[37]	1
CTCFailedBuf_Cnt_M_lgc[38]	1
CTCFailedBuf_Cnt_M_lgc[39]	1
CTCFailedBuf_Cnt_M_lgc[40]	1
CTCFailedBuf_Cnt_M_lgc[41]	1
CTCFailedBuf_Cnt_M_lgc[42]	1
CTCFailedBuf Cnt M lgc[43]	1

Demlf\_DTCS

2018-04-10, 18:44:44+0530



Input Value CTCFailedBuf\_Cnt\_M\_lgc[44] CTCFailedBuf\_Cnt\_M\_lgc[45] CTCFailedBuf\_Cnt\_M\_lgc[46] CTCFailedBuf\_Cnt\_M\_lgc[47] CTCFailedBuf Cnt M lqc[48] CTCFailedBuf\_Cnt\_M\_lgc[49] CTCFailedBuf\_Cnt\_M\_lgc[50] 1 CTCFailedBuf\_Cnt\_M\_lgc[51] 1 CTCFailedBuf\_Cnt\_M\_lgc[52] CTCFailedBuf\_Cnt\_M\_lgc[53] 1 CTCFailedBuf\_Cnt\_M\_lgc[54] CTCFailedBuf\_Cnt\_M\_lgc[55] 1 CTCFailedBuf\_Cnt\_M\_lgc[56] CTCFailedBuf\_Cnt\_M\_lgc[57] 1 CTCFailedBuf\_Cnt\_M\_lgc[58] CTCFailedBuf\_Cnt\_M\_lgc[59] 1 CTCFailedBuf\_Cnt\_M\_lgc[60] CTCFailedBuf\_Cnt\_M\_lgc[61] 1 CTCFailedBuf\_Cnt\_M\_lgc[62] 1 CTCFailedBuf\_Cnt\_M\_lgc[63] CTCFailedBuf\_Cnt\_M\_lgc[64] 1 CTCFailedBuf\_Cnt\_M\_lgc[65] 1 CTCFailedBuf\_Cnt\_M\_lgc[66] 1 CTCFailedBuf\_Cnt\_M\_lgc[67] 1 CTCFailedBuf\_Cnt\_M\_lgc[68] CTCFailedBuf\_Cnt\_M\_lgc[69] CTCFailedBuf\_Cnt\_M\_lgc[70] 1 CTCFailedBuf\_Cnt\_M\_lgc[71] CTCFailedBuf\_Cnt\_M\_lgc[72] 1 CTCFailedBuf\_Cnt\_M\_lgc[73] 1 CTCFailedBuf Cnt M Igc[74] CTCFailedBuf\_Cnt\_M\_lgc[75] 1 CTCFailedBuf Cnt M Igc[76] 1 CTCFailed\_Cnt\_M\_lgc 0 DTC 0 DTCKind 1 DTCStatusNew 0 DTCStatusOld 0 Dem\_DTCNumberTable[0] 0 Dem\_DTCNumberTable[1] 0 Dem\_DTCNumberTable[2] 0 Dem\_DTCNumberTable[3] 0 Dem\_DTCNumberTable[4] 0 Dem\_DTCNumberTable[5] 0 Dem\_DTCNumberTable[6] n Dem\_DTCNumberTable[7] 0 Dem DTCNumberTable[8] n Dem\_DTCNumberTable[9] 0 Dem DTCNumberTable[10] n Dem\_DTCNumberTable[11] 0 Dem\_DTCNumberTable[12] 0 Dem\_DTCNumberTable[13] 0 Dem\_DTCNumberTable[14] 0 Dem\_DTCNumberTable[15] 0 Dem\_DTCNumberTable[16] 0 Dem\_DTCNumberTable[17] 0 Dem\_DTCNumberTable[18] 0 Dem\_DTCNumberTable[19] 0 Dem\_DTCNumberTable[20] 0 Dem\_DTCNumberTable[21] 0 Dem\_DTCNumberTable[22] 0 0 Dem\_DTCNumberTable[23] Dem\_DTCNumberTable[24] 0 Dem\_DTCNumberTable[25] 0 Dem\_DTCNumberTable[26] 0 Dem DTCNumberTable[27] 0 Dem\_DTCNumberTable[28] 0 0 Dem DTCNumberTable[29] Dem\_DTCNumberTable[30] 0 Dem\_DTCNumberTable[31] 0 Dem DTCNumberTable[32] 0 Dem\_DTCNumberTable[33] 0 Dem\_DTCNumberTable[34] 0

Demlf\_DTCS

2018-04-10, 18:44:44+0530



Input Value Dem DTCNumberTable[35] 0 Dem\_DTCNumberTable[36] 0 Dem\_DTCNumberTable[37] 0 Dem\_DTCNumberTable[38] 0 0 Dem\_DTCNumberTable[39] Dem\_DTCNumberTable[40] 0 Dem\_DTCNumberTable[41] 0 Dem\_DTCNumberTable[42] 0 Dem\_DTCNumberTable[43] 0 Dem DTCNumberTable[44] n Dem\_DTCNumberTable[45] 0 Dem\_DTCNumberTable[46] n Dem\_DTCNumberTable[47] 0 n Dem DTCNumberTable[48] Dem\_DTCNumberTable[49] 0 Dem\_DTCNumberTable[50] 0 Dem\_DTCNumberTable[51] 0 Dem\_DTCNumberTable[52] 0 Dem\_DTCNumberTable[53] 0 Dem\_DTCNumberTable[54] 0 Dem\_DTCNumberTable[55] 0 Dem\_DTCNumberTable[56] 0 Dem\_DTCNumberTable[57] 0 Dem\_DTCNumberTable[58] 0 Dem\_DTCNumberTable[59] 0 Dem\_DTCNumberTable[60] 0 Dem\_DTCNumberTable[61] 0 Dem\_DTCNumberTable[62] 0 Dem\_DTCNumberTable[63] 0 Dem\_DTCNumberTable[64] 0 Dem\_DTCNumberTable[65] 0 Dem\_DTCNumberTable[66] 0 Dem DTCNumberTable[67] 0 Dem\_DTCNumberTable[68] 0 Dem\_DTCNumberTable[69] 0 Dem DTCNumberTable[70] 0 Dem\_DTCNumberTable[71] 0 Dem\_DTCNumberTable[72] 0 Dem\_DTCNumberTable[73] 0 Dem DTCNumberTable[74] 0 Dem\_DTCNumberTable[75] 0 Dem DTCNumberTable[76] 0 Dem\_DTC\_FTB\_Table[0] 0 Dem\_DTC\_FTB\_Table[1] 0 Dem\_DTC\_FTB\_Table[2] 0 Dem\_DTC\_FTB\_Table[3] 0 Dem\_DTC\_FTB\_Table[4] 0 Dem\_DTC\_FTB\_Table[5] 0 Dem\_DTC\_FTB\_Table[6] 0 Dem\_DTC\_FTB\_Table[7] 0 Dem\_DTC\_FTB\_Table[8] 0 Dem\_DTC\_FTB\_Table[9] 0 Dem\_DTC\_FTB\_Table[10] 0 Dem\_DTC\_FTB\_Table[11] 0 Dem\_DTC\_FTB\_Table[12] 0 Dem\_DTC\_FTB\_Table[13] 0 0 Dem\_DTC\_FTB\_Table[14] Dem\_DTC\_FTB\_Table[15] 0 Dem\_DTC\_FTB\_Table[16] 0 Dem\_DTC\_FTB\_Table[17] 0 Dem\_DTC\_FTB\_Table[18] 0 Dem\_DTC\_FTB\_Table[19] 0 Dem\_DTC\_FTB\_Table[20] 0 Dem\_DTC\_FTB\_Table[21] 0 Dem\_DTC\_FTB\_Table[22] 0 Dem DTC FTB Table[23] 0 Dem\_DTC\_FTB\_Table[24] 0 Dem DTC FTB Table[25] 0 Dem\_DTC\_FTB\_Table[26] 0 Dem\_DTC\_FTB\_Table[27] 0 Dem\_DTC\_FTB\_Table[28] 0 Dem\_DTC\_FTB\_Table[29] 0 Dem\_DTC\_FTB\_Table[30] 0

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value Dem\_DTC\_FTB\_Table[31] 0 Dem\_DTC\_FTB\_Table[32] 0 Dem DTC\_FTB\_Table[33] 0 Dem\_DTC\_FTB\_Table[34] 0 Dem\_DTC\_FTB\_Table[35] 0 Dem\_DTC\_FTB\_Table[36] 0 Dem\_DTC\_FTB\_Table[37] 0 Dem\_DTC\_FTB\_Table[38] 0 Dem\_DTC\_FTB\_Table[39] 0 Dem\_DTC\_FTB\_Table[40] 0 Dem\_DTC\_FTB\_Table[41] 0 Dem\_DTC\_FTB\_Table[42] 0 Dem\_DTC\_FTB\_Table[43] 0 Dem\_DTC\_FTB\_Table[44] 0 Dem\_DTC\_FTB\_Table[45] 0 Dem\_DTC\_FTB\_Table[46] 0 Dem\_DTC\_FTB\_Table[47] 0 Dem\_DTC\_FTB\_Table[48] 0 Dem\_DTC\_FTB\_Table[49] 0 Dem\_DTC\_FTB\_Table[50] 0 Dem\_DTC\_FTB\_Table[51] 0 Dem\_DTC\_FTB\_Table[52] 0 Dem\_DTC\_FTB\_Table[53] 0 Dem\_DTC\_FTB\_Table[54] 0 Dem\_DTC\_FTB\_Table[55] 0 Dem\_DTC\_FTB\_Table[56] 0 Dem\_DTC\_FTB\_Table[57] 0 Dem\_DTC\_FTB\_Table[58] 0 Dem DTC FTB Table[59] 0 Dem\_DTC\_FTB\_Table[60] 0 Dem DTC FTB Table[61] 0 Dem\_DTC\_FTB\_Table[62] 0 Dem DTC FTB Table[63] 0 Dem\_DTC\_FTB\_Table[64] 0 Dem\_DTC\_FTB\_Table[65] 0 Dem\_DTC\_FTB\_Table[66] 0 Dem\_DTC\_FTB\_Table[67] 0 0 Dem\_DTC\_FTB\_Table[68] Dem\_DTC\_FTB\_Table[69] 0 Dem\_DTC\_FTB\_Table[70] 0 Dem\_DTC\_FTB\_Table[71] 0 Dem\_DTC\_FTB\_Table[72] 0 Dem\_DTC\_FTB\_Table[73] 0 Dem\_DTC\_FTB\_Table[74] 0 Dem\_DTC\_FTB\_Table[75] n Dem\_DTC\_FTB\_Table[76] 0 **Actual Value Expected Value** Result CTCFailedBuf\_Cnt\_M\_lgc[0] n n CTCFailedBuf\_Cnt\_M\_lgc[1] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[2] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[3] CTCFailedBuf\_Cnt\_M\_lgc[4] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[5] CTCFailedBuf\_Cnt\_M\_lgc[6] CTCFailedBuf\_Cnt\_M\_lgc[7] 1 CTCFailedBuf\_Cnt\_M\_lgc[8] 1 CTCFailedBuf\_Cnt\_M\_lgc[9] 1 CTCFailedBuf\_Cnt\_M\_lgc[10] CTCFailedBuf\_Cnt\_M\_lgc[11] CTCFailedBuf\_Cnt\_M\_lgc[12] 1 CTCFailedBuf\_Cnt\_M\_lgc[13] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[14] CTCFailedBuf\_Cnt\_M\_lgc[15] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[16] CTCFailedBuf\_Cnt\_M\_lgc[17] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[18] CTCFailedBuf\_Cnt\_M\_lgc[19] 1 CTCFailedBuf\_Cnt\_M\_lgc[20] 1 1 CTCFailedBuf Cnt M Igc[21] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[22] 1 CTCFailedBuf\_Cnt\_M\_lgc[23] 1 1 ~ CTCFailedBuf\_Cnt\_M\_lgc[24] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[25]

## **TEST DETAILS REPORT** Ch n e

Demlf\_DTCS

2018-04-10, 18:44:44+0530



Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[26]	1	1	~
CTCFailedBuf_Cnt_M_lgc[27]	1	1	~
CTCFailedBuf_Cnt_M_lgc[28]	1	1	~
CTCFailedBuf_Cnt_M_lgc[29]	1	1	~
CTCFailedBuf_Cnt_M_lgc[30]	1	1	~
CTCFailedBuf_Cnt_M_lgc[31]	1	1	•
CTCFailedBuf_Cnt_M_lgc[32]	1	1	~
CTCFailedBuf_Cnt_M_lgc[33]	1	1	~
CTCFailedBuf_Cnt_M_lgc[34]	1	1	~
CTCFailedBuf_Cnt_M_lgc[35]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[36]	1	1	~
CTCFailedBuf_Cnt_M_lgc[37]	1	1	~
CTCFailedBuf_Cnt_M_lgc[38]	1	1	~
CTCFailedBuf_Cnt_M_lgc[39]	1	1	•
CTCFailedBuf_Cnt_M_lgc[40]	1	1	~
CTCFailedBuf_Cnt_M_lgc[41]	1	1	•
CTCFailedBuf_Cnt_M_lgc[42]	1	1	~
CTCFailedBuf_Cnt_M_lgc[43]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[44]	1	1	~
CTCFailedBuf_Cnt_M_lgc[45]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[46]	1	1	~
CTCFailedBuf_Cnt_M_lgc[47]	1	1	~
CTCFailedBuf_Cnt_M_lgc[48]	1	1	~
CTCFailedBuf_Cnt_M_lgc[49]	1	1	•
CTCFailedBuf_Cnt_M_lgc[50]	1	1	~
CTCFailedBuf_Cnt_M_lgc[51]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[52]	1	1	~
CTCFailedBuf_Cnt_M_lgc[53]	1	1	~
CTCFailedBuf_Cnt_M_lgc[54]	1	1	~
CTCFailedBuf_Cnt_M_lgc[55]	1	1	~
CTCFailedBuf_Cnt_M_lgc[56]	1	1	~
CTCFailedBuf_Cnt_M_lgc[57]	1	1	~
CTCFailedBuf_Cnt_M_lgc[58]	1	1	~
CTCFailedBuf_Cnt_M_lgc[59]	1	1	~
CTCFailedBuf_Cnt_M_lgc[60]	1	1	~
CTCFailedBuf_Cnt_M_lgc[61]	1	1	~
CTCFailedBuf_Cnt_M_lgc[62]	1	1	~
CTCFailedBuf_Cnt_M_lgc[63]	1	1	~
CTCFailedBuf_Cnt_M_lgc[64]	1	1	~
CTCFailedBuf_Cnt_M_lgc[65]	1	1	~
CTCFailedBuf_Cnt_M_lgc[66]	1	1	~
CTCFailedBuf_Cnt_M_lgc[67]	1	1	~
CTCFailedBuf_Cnt_M_lgc[68]	1	1	~
CTCFailedBuf_Cnt_M_lgc[69]	1	1	~
CTCFailedBuf_Cnt_M_lgc[70]	1	1	~
CTCFailedBuf_Cnt_M_lgc[71]	1	1	~
CTCFailedBuf_Cnt_M_lgc[72]	1	1	~
CTCFailedBuf_Cnt_M_lgc[73]	1	1	~
CTCFailedBuf_Cnt_M_lgc[74]	1	1	~
CTCFailedBuf_Cnt_M_lgc[75]	1	1	~
CTCFailedBuf_Cnt_M_lgc[76]	1	1	~
CTCFailed_Cnt_M_lgc	1	1	~
DemIf_DTCStatusChanged()	0	0	~
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	1	1	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	<b>✓</b>

Test Step 3.3 (Repeat Count = 1)		<b>✓</b>
Name	Input Value	
CTCFailedBuf_Cnt_M_lgc[0]	0	
CTCFailedBuf_Cnt_M_lgc[1]	0	
CTCFailedBuf_Cnt_M_lgc[2]	0	
CTCFailedBuf_Cnt_M_lgc[3]	0	
CTCFailedBuf_Cnt_M_lgc[4]	0	
CTCFailedBuf_Cnt_M_lgc[5]	0	
CTCFailedBuf_Cnt_M_lgc[6]	0	
CTCFailedBuf_Cnt_M_lgc[7]	0	
CTCFailedBuf_Cnt_M_lgc[8]	0	

2018-04-10, 18:44:44+0530



DemIf\_DTCS Input Value CTCFailedBuf\_Cnt\_M\_lgc[9] 0 CTCFailedBuf\_Cnt\_M\_lgc[10] 0 CTCFailedBuf\_Cnt\_M\_lgc[11] 0 CTCFailedBuf\_Cnt\_M\_lgc[12] 0 CTCFailedBuf\_Cnt\_M\_lgc[13] 0 CTCFailedBuf\_Cnt\_M\_lgc[14] 0 CTCFailedBuf\_Cnt\_M\_lgc[15] 0 CTCFailedBuf\_Cnt\_M\_lgc[16] n CTCFailedBuf\_Cnt\_M\_lgc[17] 0 CTCFailedBuf\_Cnt\_M\_lgc[18] n CTCFailedBuf\_Cnt\_M\_lgc[19] 0 CTCFailedBuf\_Cnt\_M\_lgc[20] n CTCFailedBuf\_Cnt\_M\_lgc[21] 0 CTCFailedBuf\_Cnt\_M\_lgc[22] n CTCFailedBuf\_Cnt\_M\_lgc[23] 0 CTCFailedBuf\_Cnt\_M\_lgc[24] 0 CTCFailedBuf\_Cnt\_M\_lgc[25] 0 CTCFailedBuf\_Cnt\_M\_lgc[26] 0 CTCFailedBuf\_Cnt\_M\_lgc[27] 0 CTCFailedBuf\_Cnt\_M\_lgc[28] 0 CTCFailedBuf\_Cnt\_M\_lgc[29] 0 CTCFailedBuf\_Cnt\_M\_lgc[30] 0 CTCFailedBuf\_Cnt\_M\_lgc[31] 0 CTCFailedBuf\_Cnt\_M\_lgc[32] 0 CTCFailedBuf\_Cnt\_M\_lgc[33] 0 CTCFailedBuf\_Cnt\_M\_lgc[34] 0 CTCFailedBuf\_Cnt\_M\_lgc[35] 0 CTCFailedBuf\_Cnt\_M\_lgc[36] 0 CTCFailedBuf\_Cnt\_M\_lgc[37] 0 CTCFailedBuf\_Cnt\_M\_lgc[38] 0 CTCFailedBuf Cnt M Igc[39] 0 CTCFailedBuf\_Cnt\_M\_lgc[40] n CTCFailedBuf Cnt M Igc[41] 0 CTCFailedBuf\_Cnt\_M\_lgc[42] 0 CTCFailedBuf\_Cnt\_M\_lgc[43] 0 CTCFailedBuf\_Cnt\_M\_lgc[44] 0 CTCFailedBuf\_Cnt\_M\_lgc[45] 0 CTCFailedBuf\_Cnt\_M\_lgc[46] 0 CTCFailedBuf\_Cnt\_M\_lgc[47] 0 CTCFailedBuf\_Cnt\_M\_lgc[48] 0 CTCFailedBuf\_Cnt\_M\_lgc[49] 0 CTCFailedBuf Cnt M lqc[50] 0 CTCFailedBuf\_Cnt\_M\_lgc[51] 0 CTCFailedBuf\_Cnt\_M\_lgc[52] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[53] CTCFailedBuf\_Cnt\_M\_lgc[54] 0 CTCFailedBuf\_Cnt\_M\_lgc[55] 0 CTCFailedBuf\_Cnt\_M\_lgc[56] 0 CTCFailedBuf\_Cnt\_M\_lgc[57] 0 CTCFailedBuf\_Cnt\_M\_lgc[58] 0 CTCFailedBuf\_Cnt\_M\_lgc[59] 0 CTCFailedBuf\_Cnt\_M\_lgc[60] 0

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CTCFailedBuf\_Cnt\_M\_lgc[61]

CTCFailedBuf\_Cnt\_M\_lgc[62]

CTCFailedBuf\_Cnt\_M\_lgc[63]

CTCFailedBuf\_Cnt\_M\_lgc[64]

CTCFailedBuf\_Cnt\_M\_lgc[65]

CTCFailedBuf\_Cnt\_M\_lgc[66]

CTCFailedBuf\_Cnt\_M\_lgc[67]

CTCFailedBuf\_Cnt\_M\_lgc[68]

CTCFailedBuf\_Cnt\_M\_lgc[69]

CTCFailedBuf\_Cnt\_M\_lgc[70]

CTCFailedBuf\_Cnt\_M\_lgc[71]

CTCFailedBuf\_Cnt\_M\_lgc[72]

CTCFailedBuf\_Cnt\_M\_lgc[73]

CTCFailedBuf Cnt M Igc[74]

CTCFailedBuf\_Cnt\_M\_Igc[75]

CTCFailedBuf Cnt M Igc[76]

CTCFailed\_Cnt\_M\_lgc

DTC

DTCKind

DTCStatusNew

DTCStatusOld

Demlf\_DTCS

2018-04-10, 18:44:44+0530



Name Input Value Dem\_DTCNumberTable[0] 0 Dem\_DTCNumberTable[1] 0 Dem DTCNumberTable[2] 0 Dem\_DTCNumberTable[3] 0 Dem DTCNumberTable[4] 0 Dem\_DTCNumberTable[5] 0 Dem\_DTCNumberTable[6] 0 Dem\_DTCNumberTable[7] 0 Dem\_DTCNumberTable[8] 0 Dem\_DTCNumberTable[9] 0 Dem\_DTCNumberTable[10] 0 Dem\_DTCNumberTable[11] 0 Dem\_DTCNumberTable[12] 0 0 Dem\_DTCNumberTable[13] Dem\_DTCNumberTable[14] 0 0 Dem\_DTCNumberTable[15] Dem\_DTCNumberTable[16] 0 Dem\_DTCNumberTable[17] 0 Dem\_DTCNumberTable[18] 0 Dem\_DTCNumberTable[19] 0 Dem\_DTCNumberTable[20] 0 Dem\_DTCNumberTable[21] 0 Dem\_DTCNumberTable[22] 0 Dem\_DTCNumberTable[23] 0 Dem\_DTCNumberTable[24] 0 Dem\_DTCNumberTable[25] 0 Dem DTCNumberTable[26] 0 Dem\_DTCNumberTable[27] 0 Dem DTCNumberTable[28] 0 Dem\_DTCNumberTable[29] 0 Dem DTCNumberTable[30] 0 Dem\_DTCNumberTable[31] 0 Dem DTCNumberTable[32] 0 Dem\_DTCNumberTable[33] 0 Dem\_DTCNumberTable[34] 0 Dem\_DTCNumberTable[35] 0 Dem\_DTCNumberTable[36] 0 Dem\_DTCNumberTable[37] 0 Dem\_DTCNumberTable[38] 0 Dem\_DTCNumberTable[39] 0 Dem\_DTCNumberTable[40] 0 0 Dem\_DTCNumberTable[41] Dem\_DTCNumberTable[42] 0 Dem\_DTCNumberTable[43] 0 Dem\_DTCNumberTable[44] n Dem\_DTCNumberTable[45] 0 Dem\_DTCNumberTable[46] n Dem\_DTCNumberTable[47] 0 Dem DTCNumberTable[48] n Dem\_DTCNumberTable[49] 0 Dem\_DTCNumberTable[50] 0 Dem\_DTCNumberTable[51] 0 Dem\_DTCNumberTable[52] 0 Dem\_DTCNumberTable[53] 0 Dem\_DTCNumberTable[54] 0 Dem\_DTCNumberTable[55] 0 Dem\_DTCNumberTable[56] 0 0 Dem\_DTCNumberTable[57] Dem\_DTCNumberTable[58] 0 Dem\_DTCNumberTable[59] 0 Dem\_DTCNumberTable[60] 0 0 Dem\_DTCNumberTable[61] Dem\_DTCNumberTable[62] 0 Dem\_DTCNumberTable[63] 0 Dem\_DTCNumberTable[64] 0 Dem\_DTCNumberTable[65] 0 Dem\_DTCNumberTable[66] 0 0 Dem DTCNumberTable[67] Dem DTCNumberTable[68] 0 Dem\_DTCNumberTable[69] 0 Dem\_DTCNumberTable[70] 0 Dem\_DTCNumberTable[71] 0 Dem\_DTCNumberTable[72] 0

2018-04-10, 18:44:44+0530



Demlf\_DTCS Ch n e

Name	Input Value
Dem_DTCNumberTable[73]	0
Dem_DTCNumberTable[74]	0
Dem_DTCNumberTable[75]	0
Dem_DTCNumberTable[76]	0
Dem_DTC_FTB_Table[0]	0
Dem_DTC_FTB_Table[1]	0
Dem_DTC_FTB_Table[2]	0
Dem_DTC_FTB_Table[3]	0
Dem_DTC_FTB_Table[4]	0
Dem_DTC_FTB_Table[5]	0
Dem_DTC_FTB_Table[6]	0
Dem_DTC_FTB_Table[7] Dem DTC FTB Table[8]	0
Dem_DTC_FTB_Table[9]	0
Dem_DTC_FTB_Table[10]	0
Dem_DTC_FTB_Table[11]	0
Dem_DTC_FTB_Table[12]	0
Dem_DTC_FTB_Table[13]	0
Dem_DTC_FTB_Table[14]	0
Dem_DTC_FTB_Table[15]	0
Dem_DTC_FTB_Table[16]	0
Dem_DTC_FTB_Table[17]	0
Dem_DTC_FTB_Table[18]	0
Dem_DTC_FTB_Table[19]	0
Dem_DTC_FTB_Table[20]	0
Dem_DTC_FTB_Table[21]	0
Dem_DTC_FTB_Table[22]	0
Dem_DTC_FTB_Table[23]	0
Dem_DTC_FTB_Table[24]	0
Dem_DTC_FTB_Table[25]	0
Dem_DTC_FTB_Table[26] Dem_DTC_FTB_Table[27]	0
Dem_DTC_FTB_Table[28]	0
Dem_DTC_FTB_Table[29]	0
Dem_DTC_FTB_Table[30]	0
Dem_DTC_FTB_Table[31]	0
Dem_DTC_FTB_Table[32]	0
Dem_DTC_FTB_Table[33]	0
Dem_DTC_FTB_Table[34]	0
Dem_DTC_FTB_Table[35]	0
Dem_DTC_FTB_Table[36]	0
Dem_DTC_FTB_Table[37]	0
Dem_DTC_FTB_Table[38]	0
Dem_DTC_FTB_Table[39]	0
Dem_DTC_FTB_Table[40]	
Dem_DTC_FTB_Table[41]	0
Dem_DTC_FTB_Table[42]	0
Dem_DTC_FTB_Table[43]	0
Dem_DTC_FTB_Table[44]	0
Dem_DTC_FTB_Table[45] Dem_DTC_FTB_Table[46]	0
Dem_DTC_FTB_Table[46] Dem_DTC_FTB_Table[47]	0
Dem_DTC_FTB_Table[48]	0
Dem_DTC_FTB_Table[49]	0
Dem_DTC_FTB_Table[50]	0
Dem_DTC_FTB_Table[51]	0
Dem_DTC_FTB_Table[52]	0
Dem_DTC_FTB_Table[53]	0
Dem_DTC_FTB_Table[54]	0
Dem_DTC_FTB_Table[55]	0
Dem_DTC_FTB_Table[56]	0
Dem_DTC_FTB_Table[57]	0
Dem_DTC_FTB_Table[58]	0
Dem_DTC_FTB_Table[59]	0
Dem_DTC_FTB_Table[60]	0
Dem_DTC_FTB_Table[61]	0
Dem_DTC_FTB_Table[62]	0
Dem_DTC_FTB_Table[63]	0
Dem_DTC_FTB_Table[64]	0
Dem_DTC_FTB_Table[65]	0 0
Dem_DTC_FTB_Table[66]	0
Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68]	0
DSII_D 1 0_1 1D_1 abic[00]	ı V

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value Dem\_DTC\_FTB\_Table[69] 0 Dem\_DTC\_FTB\_Table[70] 0 Dem DTC\_FTB\_Table[71] 0 Dem\_DTC\_FTB\_Table[72] 0 Dem\_DTC\_FTB\_Table[73] 0 Dem\_DTC\_FTB\_Table[74] 0 Dem\_DTC\_FTB\_Table[75] 0 Dem\_DTC\_FTB\_Table[76] 0 **Actual Value Expected Value** Name Result CTCFailedBuf\_Cnt\_M\_lgc[0] 0 CTCFailedBuf\_Cnt\_M\_lgc[1] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[2] 0 0 n CTCFailedBuf\_Cnt\_M\_lgc[3] 0 CTCFailedBuf\_Cnt\_M\_lgc[4] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[5] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[6] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[7] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[8] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[9] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[10] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[11] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[12] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[13] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[14] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[15] 0 0 V CTCFailedBuf\_Cnt\_M\_lgc[16] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[17] 0 0 CTCFailedBuf Cnt M Igc[18] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[19] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[20] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[21] 0 0 CTCFailedBuf Cnt M Igc[22] 0 0 CTCFailedBuf\_Cnt\_M\_Igc[23] 0 0 CTCFailedBuf Cnt M Igc[24] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[25] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[26] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[27] 0 0 0 CTCFailedBuf\_Cnt\_M\_lgc[28] 0 CTCFailedBuf\_Cnt\_M\_lgc[29] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[30] 0 0 CTCFailedBuf Cnt M lqc[31] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[32] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[33] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[34] 0 0 **~** CTCFailedBuf\_Cnt\_M\_lgc[35] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[36] n n CTCFailedBuf\_Cnt\_M\_lgc[37] 0 0 ~ CTCFailedBuf\_Cnt\_M\_lgc[38] n 0 CTCFailedBuf\_Cnt\_M\_lgc[39] 0 0 CTCFailedBuf Cnt M Igc[40] n 0 CTCFailedBuf\_Cnt\_M\_lgc[41] 0 0 CTCFailedBuf Cnt M Igc[42] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[43] 0 0 CTCFailedBuf Cnt M lqc[44] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[45] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[46] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[47] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[48] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[49] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[50] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[51] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[52] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[53] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[54] 0 0 0 CTCFailedBuf\_Cnt\_M\_lgc[55] 0 CTCFailedBuf\_Cnt\_M\_lgc[56] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[57] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[58] 0 0 CTCFailedBuf Cnt M lqc[59] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[60] n 0 CTCFailedBuf\_Cnt\_M\_lgc[61] 0 0 ~ CTCFailedBuf\_Cnt\_M\_lgc[62] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[63] 0 0

Demlf\_DTCS

2018-04-10, 18:44:44+0530



**Actual Value Expected Value** CTCFailedBuf\_Cnt\_M\_lgc[64] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[65] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[66] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[67] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[68] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[73] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[74] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[75] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 0 CTCFailed\_Cnt\_M\_lgc 0 0 DemIf\_DTCStatusChanged() 0 0 Rte\_Write\_Ap\_Demlf\_CTCFailed\_Cnt\_lgc(data) 0 0

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	~

Test Step 3.4 (Repeat Count = 1)	
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf Cnt M lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf Cnt M Igc[20]	1
CTCFailedBuf_Cnt_M_lgc[21]	1
CTCFailedBuf_Cnt_M_lgc[22]	1
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	1
CTCFailedBuf_Cnt_M_lgc[35]	1
CTCFailedBuf_Cnt_M_lgc[36]	1
CTCFailedBuf Cnt M Igc[37]	1
CTCFailedBuf_Cnt_M_lgc[38]	1
CTCFailedBuf_Cnt_M_lgc[39]	1
CTCFailedBuf_Cnt_M_lgc[40]	1
CTCFailedBuf_Cnt_M_lgc[41]	1
CTCFailedBuf_Cnt_M_lgc[41] CTCFailedBuf_Cnt_M_lgc[42]	1
CTCFailedBuf_Cnt_M_lgc[42] CTCFailedBuf_Cnt_M_lgc[43]	1
	1
CTCFailedBuf_Cnt_M_lgc[44]	1
CTCFailedBuf_Cnt_M_lgc[45]	1
CTCFailedBuf_Cnt_M_lgc[46]	<u>                                     </u>

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value CTCFailedBuf\_Cnt\_M\_lgc[47] 1 CTCFailedBuf\_Cnt\_M\_lgc[48] CTCFailedBuf\_Cnt\_M\_lgc[49] 1 CTCFailedBuf\_Cnt\_M\_lgc[50] CTCFailedBuf\_Cnt\_M\_lgc[51] 1 CTCFailedBuf\_Cnt\_M\_lgc[52] CTCFailedBuf\_Cnt\_M\_lgc[53] 1 CTCFailedBuf\_Cnt\_M\_lgc[54] 1 CTCFailedBuf\_Cnt\_M\_lgc[55] 1 CTCFailedBuf\_Cnt\_M\_lgc[56] CTCFailedBuf\_Cnt\_M\_lgc[57] 1 CTCFailedBuf\_Cnt\_M\_lgc[58] 1 CTCFailedBuf\_Cnt\_M\_lgc[59] CTCFailedBuf\_Cnt\_M\_lgc[60] 1 CTCFailedBuf\_Cnt\_M\_lgc[61] 1 CTCFailedBuf\_Cnt\_M\_lgc[62] 1 CTCFailedBuf\_Cnt\_M\_lgc[63] 1 CTCFailedBuf\_Cnt\_M\_lgc[64] 1  $CTCFailedBuf\_Cnt\_M\_lgc[65]$ 1 CTCFailedBuf\_Cnt\_M\_lgc[66] CTCFailedBuf\_Cnt\_M\_lgc[67] 1 CTCFailedBuf\_Cnt\_M\_lgc[68] 1 CTCFailedBuf\_Cnt\_M\_lgc[69] 1 CTCFailedBuf\_Cnt\_M\_lgc[70] CTCFailedBuf\_Cnt\_M\_lgc[71] 1 CTCFailedBuf\_Cnt\_M\_lgc[72] CTCFailedBuf\_Cnt\_M\_lgc[73] 1 CTCFailedBuf\_Cnt\_M\_lgc[74] CTCFailedBuf\_Cnt\_M\_lgc[75] 1 CTCFailedBuf\_Cnt\_M\_lgc[76] 1 CTCFailed\_Cnt\_M\_lgc 1 4294967295 DTC DTCKind 2 DTCStatusNew 255 DTCStatusOld 255 Dem DTCNumberTable[0] 65535 Dem\_DTCNumberTable[1] 65535 Dem\_DTCNumberTable[2] 65535 Dem\_DTCNumberTable[3] 65535 Dem DTCNumberTable[4] 65535 Dem\_DTCNumberTable[5] 65535 Dem DTCNumberTable[6] 65535 Dem\_DTCNumberTable[7] 65535 Dem\_DTCNumberTable[8] 65535 Dem\_DTCNumberTable[9] 65535 Dem\_DTCNumberTable[10] 65535 65535 Dem\_DTCNumberTable[11] Dem\_DTCNumberTable[12] 65535 Dem\_DTCNumberTable[13] 65535 Dem\_DTCNumberTable[14] 65535 Dem\_DTCNumberTable[15] 65535 Dem\_DTCNumberTable[16] 65535 Dem\_DTCNumberTable[17] 65535 Dem\_DTCNumberTable[18] 65535 Dem\_DTCNumberTable[19] 65535 Dem\_DTCNumberTable[20] 65535 Dem\_DTCNumberTable[21] 65535 Dem DTCNumberTable[22] 65535 Dem\_DTCNumberTable[23] 65535 Dem\_DTCNumberTable[24] 65535 Dem\_DTCNumberTable[25] 65535 Dem DTCNumberTable[26] 65535 Dem\_DTCNumberTable[27] 65535 Dem DTCNumberTable[28] 65535 Dem\_DTCNumberTable[29] 65535 Dem DTCNumberTable[30] 65535 Dem\_DTCNumberTable[31] 65535 Dem DTCNumberTable[32] 65535 Dem\_DTCNumberTable[33] 65535 Dem\_DTCNumberTable[34] 65535 Dem\_DTCNumberTable[35] 65535 Dem\_DTCNumberTable[36] 65535 Dem\_DTCNumberTable[37] 65535

Demlf\_DTCS

2018-04-10, 18:44:44+0530



Name Input Value Dem\_DTCNumberTable[38] 65535 Dem\_DTCNumberTable[39] 65535 Dem DTCNumberTable[40] 65535 Dem\_DTCNumberTable[41] 65535 Dem DTCNumberTable[42] 65535 Dem\_DTCNumberTable[43] 65535 Dem\_DTCNumberTable[44] 65535 Dem\_DTCNumberTable[45] 65535 Dem\_DTCNumberTable[46] 65535 Dem\_DTCNumberTable[47] 65535 Dem\_DTCNumberTable[48] 65535 Dem\_DTCNumberTable[49] 65535 Dem\_DTCNumberTable[50] 65535 Dem\_DTCNumberTable[51] 65535 Dem\_DTCNumberTable[52] 65535 Dem\_DTCNumberTable[53] 65535 Dem\_DTCNumberTable[54] 65535 Dem\_DTCNumberTable[55] 65535 Dem\_DTCNumberTable[56] 65535 Dem\_DTCNumberTable[57] 65535 Dem\_DTCNumberTable[58] 65535 Dem\_DTCNumberTable[59] 65535 Dem\_DTCNumberTable[60] 65535 Dem\_DTCNumberTable[61] 65535 Dem\_DTCNumberTable[62] 65535 Dem\_DTCNumberTable[63] 65535 Dem DTCNumberTable[64] 65535 Dem\_DTCNumberTable[65] 65535 Dem DTCNumberTable[66] 65535 Dem\_DTCNumberTable[67] 65535 Dem DTCNumberTable[68] 65535 Dem\_DTCNumberTable[69] 65535 Dem DTCNumberTable[70] 65535 Dem\_DTCNumberTable[71] 65535 Dem\_DTCNumberTable[72] 65535 Dem\_DTCNumberTable[73] 65535 Dem\_DTCNumberTable[74] 65535 Dem\_DTCNumberTable[75] 65535 Dem\_DTCNumberTable[76] 65535 Dem\_DTC\_FTB\_Table[0] 255 Dem\_DTC\_FTB\_Table[1] 255 255 Dem\_DTC\_FTB\_Table[2] Dem\_DTC\_FTB\_Table[3] 255 Dem\_DTC\_FTB\_Table[4] 255 Dem\_DTC\_FTB\_Table[5] 255 Dem\_DTC\_FTB\_Table[6] 255 Dem\_DTC\_FTB\_Table[7] 255 Dem\_DTC\_FTB\_Table[8] 255 Dem\_DTC\_FTB\_Table[9] 255 Dem\_DTC\_FTB\_Table[10] 255 Dem DTC FTB Table[11] 255 Dem\_DTC\_FTB\_Table[12] 255 Dem\_DTC\_FTB\_Table[13] 255 Dem\_DTC\_FTB\_Table[14] 255 Dem\_DTC\_FTB\_Table[15] 255 Dem\_DTC\_FTB\_Table[16] 255 Dem\_DTC\_FTB\_Table[17] 255 Dem\_DTC\_FTB\_Table[18] 255 Dem\_DTC\_FTB\_Table[19] 255 Dem\_DTC\_FTB\_Table[20] 255 Dem\_DTC\_FTB\_Table[21] 255 255 Dem\_DTC\_FTB\_Table[22] Dem\_DTC\_FTB\_Table[23] 255 Dem\_DTC\_FTB\_Table[24] 255 Dem\_DTC\_FTB\_Table[25] 255 Dem DTC FTB Table[26] 255 Dem\_DTC\_FTB\_Table[27] 255 Dem DTC FTB Table[28] 255 Dem\_DTC\_FTB\_Table[29] 255 Dem\_DTC\_FTB\_Table[30] 255 Dem\_DTC\_FTB\_Table[31] 255 Dem\_DTC\_FTB\_Table[32] 255 Dem\_DTC\_FTB\_Table[33] 255

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value Dem\_DTC\_FTB\_Table[34] 255 Dem\_DTC\_FTB\_Table[35] 255 Dem\_DTC\_FTB\_Table[36] 255 Dem\_DTC\_FTB\_Table[37] 255 Dem\_DTC\_FTB\_Table[38] 255 Dem\_DTC\_FTB\_Table[39] 255 Dem\_DTC\_FTB\_Table[40] 255 Dem\_DTC\_FTB\_Table[41] 255 Dem\_DTC\_FTB\_Table[42] 255 Dem\_DTC\_FTB\_Table[43] 255 Dem\_DTC\_FTB\_Table[44] 255 Dem\_DTC\_FTB\_Table[45] 255 Dem\_DTC\_FTB\_Table[46] 255 Dem DTC FTB Table[47] 255 Dem\_DTC\_FTB\_Table[48] 255 Dem\_DTC\_FTB\_Table[49] 255 Dem\_DTC\_FTB\_Table[50] 255 Dem\_DTC\_FTB\_Table[51] 255 Dem\_DTC\_FTB\_Table[52] 255 Dem\_DTC\_FTB\_Table[53] 255 Dem\_DTC\_FTB\_Table[54] 255 Dem\_DTC\_FTB\_Table[55] 255 Dem\_DTC\_FTB\_Table[56] 255 Dem\_DTC\_FTB\_Table[57] 255 Dem\_DTC\_FTB\_Table[58] 255 Dem\_DTC\_FTB\_Table[59] 255 Dem\_DTC\_FTB\_Table[60] 255 Dem\_DTC\_FTB\_Table[61] 255 Dem DTC FTB Table[62] 255 Dem\_DTC\_FTB\_Table[63] 255 Dem\_DTC\_FTB\_Table[64] 255 Dem\_DTC\_FTB\_Table[65] 255 Dem DTC FTB Table[66] 255 Dem\_DTC\_FTB\_Table[67] 255 255 Dem\_DTC\_FTB\_Table[68] Dem DTC FTB Table[69] 255 Dem\_DTC\_FTB\_Table[70] 255 Dem\_DTC\_FTB\_Table[71] 255 Dem\_DTC\_FTB\_Table[72] 255 Dem DTC\_FTB\_Table[73] 255 Dem\_DTC\_FTB\_Table[74] 255 Dem DTC FTB Table[75] 255 Dem\_DTC\_FTB\_Table[76] 255 **Actual Value Expected Value** Result Name CTCFailedBuf\_Cnt\_M\_lgc[0] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[1] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[2] CTCFailedBuf\_Cnt\_M\_lgc[3] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[4] CTCFailedBuf\_Cnt\_M\_lgc[5] 1 CTCFailedBuf\_Cnt\_M\_lgc[6] CTCFailedBuf\_Cnt\_M\_lgc[7] 1 CTCFailedBuf\_Cnt\_M\_lgc[8] CTCFailedBuf\_Cnt\_M\_lgc[9] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[10] CTCFailedBuf\_Cnt\_M\_lgc[11] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[12] 1 CTCFailedBuf\_Cnt\_M\_lgc[13] 1 CTCFailedBuf\_Cnt\_M\_lgc[14] CTCFailedBuf\_Cnt\_M\_lgc[15] 1 CTCFailedBuf\_Cnt\_M\_lgc[16] CTCFailedBuf\_Cnt\_M\_lgc[17] 1 CTCFailedBuf Cnt M Igc[18] CTCFailedBuf\_Cnt\_M\_lgc[19] CTCFailedBuf\_Cnt\_M\_lgc[20] 1 CTCFailedBuf\_Cnt\_M\_lgc[21] 1 CTCFailedBuf Cnt M lqc[22] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[23] 1 1 CTCFailedBuf Cnt M Igc[24] 1 CTCFailedBuf\_Cnt\_M\_lgc[25] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[26] 1 1  $CTCFailedBuf\_Cnt\_M\_lgc[27]$ 1 1 CTCFailedBuf\_Cnt\_M\_lgc[28]

## **TEST DETAILS REPORT** Ch n e

Demlf\_DTCS

2018-04-10, 18:44:44+0530



Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[29]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_Igc[30]	1	1	~
CTCFailedBuf_Cnt_M_lgc[31]	1	1	~
CTCFailedBuf_Cnt_M_lgc[32]	1	1	~
CTCFailedBuf_Cnt_M_lgc[33]	1	1	~
CTCFailedBuf_Cnt_M_Igc[34]	1	1	~
CTCFailedBuf_Cnt_M_Igc[35]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[36]	1	1	~
CTCFailedBuf_Cnt_M_Igc[37]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[38]	1	1	~
CTCFailedBuf_Cnt_M_lgc[39]	1	1	~
CTCFailedBuf_Cnt_M_Igc[40]	1	1	~
CTCFailedBuf_Cnt_M_lgc[41]	1	1	~
CTCFailedBuf_Cnt_M_lgc[42]	1	1	~
CTCFailedBuf_Cnt_M_lgc[43]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[44]	1	1	~
CTCFailedBuf_Cnt_M_lgc[45]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[46]	1	1	~
CTCFailedBuf_Cnt_M_lgc[47]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[48]	1	1	~
CTCFailedBuf_Cnt_M_lgc[49]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[50]	1	1	~
CTCFailedBuf_Cnt_M_lgc[51]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[52]	1	1	
CTCFailedBuf_Cnt_M_lgc[53]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[54]	1	1	_
CTCFailedBuf_Cnt_M_lgc[55]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[56]	1	1	_
CTCFailedBuf_Cnt_M_lgc[57]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[58]	1	1	~
CTCFailedBuf_Cnt_M_lgc[59]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[60]	1	1	
CTCFailedBuf_Cnt_M_lgc[61]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[62]	1	1	_
CTCFailedBuf_Cnt_M_lgc[63]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[64]	1	1	_
CTCFailedBuf_Cnt_M_lgc[65]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[66]	1	1	
CTCFailedBuf_Cnt_M_lgc[67]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[68]	1	1	-
CTCFailedBuf_Cnt_M_lgc[69]	1	1	~
CTCFailedBuf_Cnt_M_lgc[70]	1	1	
CTCFailedBuf_Cnt_M_lgc[71]	1	1	-
CTCFailedBuf_Cnt_M_lgc[72]	1	1	
CTCFailedBuf_Cnt_M_lgc[72] CTCFailedBuf_Cnt_M_lgc[73]	1	1	-
CTCFailedBuf_Cnt_M_lgc[74]	1	1	
	1	1	-
CTCFailedBuf_Cnt_M_lgc[75]		1	
CTCFailed Cot M Iss	1		
CTCFailed_Cnt_M_lgc	1	1	~
Demlf_DTCStatusChanged()	0	0	_
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc(data)	1	1	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte Write Ap Demlf CTCFailed Cnt lgc	1	Rte Write Ap Demlf CTCFailed Cnt Igc	1	_

Test Step 3.5 (Repeat Count = 1)		<b>✓</b>
Name	Input Value	
CTCFailedBuf_Cnt_M_lgc[0]	1	
CTCFailedBuf_Cnt_M_lgc[1]	1	
CTCFailedBuf_Cnt_M_lgc[2]	1	
CTCFailedBuf_Cnt_M_lgc[3]	1	
CTCFailedBuf_Cnt_M_lgc[4]	1	
CTCFailedBuf_Cnt_M_lgc[5]	0	
CTCFailedBuf_Cnt_M_lgc[6]	1	
CTCFailedBuf_Cnt_M_lgc[7]	1	
CTCFailedBuf_Cnt_M_lgc[8]	1	
CTCFailedBuf_Cnt_M_lgc[9]	1	
CTCFailedBuf_Cnt_M_lgc[10]	1	
CTCFailedBuf_Cnt_M_lgc[11]	1	

Demlf\_DTCS

2018-04-10, 18:44:44+0530



Input Value CTCFailedBuf\_Cnt\_M\_lgc[12] CTCFailedBuf\_Cnt\_M\_lgc[13] CTCFailedBuf\_Cnt\_M\_lgc[14] CTCFailedBuf\_Cnt\_M\_lgc[15] CTCFailedBuf Cnt M lqc[16] CTCFailedBuf\_Cnt\_M\_lgc[17] CTCFailedBuf\_Cnt\_M\_lgc[18] 1 CTCFailedBuf\_Cnt\_M\_lgc[19] 1 CTCFailedBuf\_Cnt\_M\_lgc[20] 0 CTCFailedBuf\_Cnt\_M\_lgc[21] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[22] CTCFailedBuf\_Cnt\_M\_lgc[23] 1 CTCFailedBuf\_Cnt\_M\_lgc[24] CTCFailedBuf\_Cnt\_M\_lgc[25] 0 CTCFailedBuf\_Cnt\_M\_lgc[26] 1 CTCFailedBuf\_Cnt\_M\_lgc[27] 1 CTCFailedBuf\_Cnt\_M\_lgc[28] CTCFailedBuf\_Cnt\_M\_lgc[29] 1 CTCFailedBuf\_Cnt\_M\_lgc[30] 1 CTCFailedBuf\_Cnt\_M\_lgc[31] 1 CTCFailedBuf\_Cnt\_M\_lgc[32] 1 CTCFailedBuf\_Cnt\_M\_lgc[33] 1 CTCFailedBuf\_Cnt\_M\_lgc[34] 0 CTCFailedBuf\_Cnt\_M\_lgc[35] 0 CTCFailedBuf\_Cnt\_M\_lgc[36] 0 CTCFailedBuf\_Cnt\_M\_lgc[37] 0 CTCFailedBuf\_Cnt\_M\_lgc[38] 0 CTCFailedBuf\_Cnt\_M\_lgc[39] 0 CTCFailedBuf\_Cnt\_M\_lgc[40] 0 CTCFailedBuf\_Cnt\_M\_lgc[41] 0 CTCFailedBuf Cnt M Igc[42] 0 CTCFailedBuf\_Cnt\_M\_lgc[43] 0 CTCFailedBuf Cnt M Igc[44] 0 CTCFailedBuf\_Cnt\_M\_lgc[45] 0 CTCFailedBuf\_Cnt\_M\_lgc[46] 0 CTCFailedBuf\_Cnt\_M\_lgc[47] 0 CTCFailedBuf\_Cnt\_M\_lgc[48] 0 CTCFailedBuf\_Cnt\_M\_lgc[49] 0 CTCFailedBuf\_Cnt\_M\_lgc[50] 0 CTCFailedBuf\_Cnt\_M\_lgc[51] 0 CTCFailedBuf\_Cnt\_M\_lgc[52] 0 CTCFailedBuf\_Cnt\_M\_lgc[53] 1 CTCFailedBuf\_Cnt\_M\_lgc[54] CTCFailedBuf\_Cnt\_M\_lgc[55] 1 CTCFailedBuf\_Cnt\_M\_lgc[56] 1 CTCFailedBuf\_Cnt\_M\_lgc[57] 1 CTCFailedBuf\_Cnt\_M\_lgc[58] 1 CTCFailedBuf\_Cnt\_M\_lgc[59] 1 CTCFailedBuf\_Cnt\_M\_lgc[60] 1 CTCFailedBuf\_Cnt\_M\_lgc[61] CTCFailedBuf\_Cnt\_M\_lgc[62] 1 CTCFailedBuf\_Cnt\_M\_lgc[63] 0 CTCFailedBuf\_Cnt\_M\_lgc[64] CTCFailedBuf\_Cnt\_M\_lgc[65] 0 CTCFailedBuf\_Cnt\_M\_lgc[66] 0 CTCFailedBuf\_Cnt\_M\_lgc[67] 0 CTCFailedBuf\_Cnt\_M\_lgc[68] 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[70] CTCFailedBuf\_Cnt\_M\_lgc[71] 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 CTCFailedBuf\_Cnt\_M\_lgc[73] 0 CTCFailedBuf\_Cnt\_M\_lgc[74] 0 CTCFailedBuf\_Cnt\_M\_lgc[75] 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 CTCFailed\_Cnt\_M\_lgc 0 DTC 0 DTCKind 1 DTCStatusNew 148 DTCStatusOld 39 Dem DTCNumberTable[0] 181 Dem\_DTCNumberTable[1] 1 Dem\_DTCNumberTable[2] 41

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Name Input Value Dem\_DTCNumberTable[3] 22 Dem\_DTCNumberTable[4] Dem\_DTCNumberTable[5] 254 Dem\_DTCNumberTable[6] 209 Dem\_DTCNumberTable[7] 209 Dem\_DTCNumberTable[8] 181 Dem\_DTCNumberTable[9] 1 Dem\_DTCNumberTable[10] 209 Dem\_DTCNumberTable[11] 128 Dem DTCNumberTable[12] Dem\_DTCNumberTable[13] 209 Dem\_DTCNumberTable[14] 181 Dem\_DTCNumberTable[15] 1 Dem\_DTCNumberTable[16] 1 Dem\_DTCNumberTable[17] 209 Dem\_DTCNumberTable[18] 33 Dem\_DTCNumberTable[19] 181 Dem\_DTCNumberTable[20] Dem\_DTCNumberTable[21] 209 Dem\_DTCNumberTable[22] 181 Dem\_DTCNumberTable[23] 41 Dem\_DTCNumberTable[24] 22 Dem\_DTCNumberTable[25] 24 Dem\_DTCNumberTable[26] 254 Dem\_DTCNumberTable[27] 1 Dem\_DTCNumberTable[28] 181 Dem\_DTCNumberTable[29] 1 Dem\_DTCNumberTable[30] 181 Dem\_DTCNumberTable[31] 181 Dem\_DTCNumberTable[32] 1 Dem\_DTCNumberTable[33] 1 Dem\_DTCNumberTable[34] 181 Dem DTCNumberTable[35] 1 Dem\_DTCNumberTable[36] 181 Dem\_DTCNumberTable[37] 181 Dem DTCNumberTable[38] 181 Dem\_DTCNumberTable[39] 1 Dem\_DTCNumberTable[40] Dem\_DTCNumberTable[41] 41 Dem DTCNumberTable[42] 22 Dem\_DTCNumberTable[43] 24 Dem DTCNumberTable[44] 254 Dem\_DTCNumberTable[45] 209 Dem\_DTCNumberTable[46] 181 Dem\_DTCNumberTable[47] 1 Dem\_DTCNumberTable[48] 22 181 Dem DTCNumberTable[49] Dem\_DTCNumberTable[50] Dem\_DTCNumberTable[51] 181 Dem\_DTCNumberTable[52] 181 Dem\_DTCNumberTable[53] 1 Dem\_DTCNumberTable[54] 22 Dem\_DTCNumberTable[55] 209 Dem\_DTCNumberTable[56] 181 Dem\_DTCNumberTable[57] 1 Dem\_DTCNumberTable[58] 181 Dem\_DTCNumberTable[59] 209 Dem\_DTCNumberTable[60] 181 Dem\_DTCNumberTable[61] 1 Dem\_DTCNumberTable[62] 22 Dem\_DTCNumberTable[63] 41 Dem DTCNumberTable[64] 22 Dem\_DTCNumberTable[65] 24 Dem DTCNumberTable[66] 254 Dem\_DTCNumberTable[67] 181 Dem DTCNumberTable[68] 181 Dem\_DTCNumberTable[69] 1 Dem DTCNumberTable[70] 22 Dem\_DTCNumberTable[71] 209 Dem\_DTCNumberTable[72] 22 Dem\_DTCNumberTable[73] 41 Dem\_DTCNumberTable[74] 22 Dem\_DTCNumberTable[75] 24

## **TEST DETAILS REPORT** Ch n e

Demlf\_DTCS

2018-04-10, 18:44:44+0530



		(14.10.10.10
Name	Input Value	
Dem_DTCNumberTable[76]	254	
Dem_DTC_FTB_Table[0]	245	
Dem_DTC_FTB_Table[1]	151	
Dem_DTC_FTB_Table[2]	199	
Dem_DTC_FTB_Table[3]	160	
Dem_DTC_FTB_Table[4]	30	
Dem_DTC_FTB_Table[5]	136	
Dem_DTC_FTB_Table[6]	178	
	178	
Dem_DTC_FTB_Table[7]		
Dem_DTC_FTB_Table[8]	245	
Dem_DTC_FTB_Table[9]	151	
Dem_DTC_FTB_Table[10]	178	
Dem_DTC_FTB_Table[11]	31	
Dem_DTC_FTB_Table[12]	151	
Dem_DTC_FTB_Table[13]	178	
Dem_DTC_FTB_Table[14]	245	
	151	
Dem_DTC_FTB_Table[15]		
Dem_DTC_FTB_Table[16]	151	
Dem_DTC_FTB_Table[17]	178	
Dem_DTC_FTB_Table[18]	234	
Dem_DTC_FTB_Table[19]	245	
Dem_DTC_FTB_Table[20]	151	
Dem DTC FTB Table[21]	178	
Dem_DTC_FTB_Table[22]	245	
Dem_DTC_FTB_Table[23]	199	
Dem_DTC_FTB_Table[24]	160	
Dem_DTC_FTB_Table[25]	30	
Dem_DTC_FTB_Table[26]	136	
Dem_DTC_FTB_Table[27]	151	
Dem_DTC_FTB_Table[28]	245	
Dem_DTC_FTB_Table[29]	151	
Dem_DTC_FTB_Table[30]	245	
	245	
Dem_DTC_FTB_Table[31]		
Dem_DTC_FTB_Table[32]	151	
Dem_DTC_FTB_Table[33]	151	
Dem_DTC_FTB_Table[34]	245	
Dem_DTC_FTB_Table[35]	151	
Dem_DTC_FTB_Table[36]	245	
Dem_DTC_FTB_Table[37]	245	
Dem_DTC_FTB_Table[38]	245	
Dem_DTC_FTB_Table[39]	151	
Dem_DTC_FTB_Table[40]	151	
Dem_DTC_FTB_Table[41]	199	
Dem_DTC_FTB_Table[42]	160	
Dem_DTC_FTB_Table[43]	30	
Dem_DTC_FTB_Table[44]	136	
Dem_DTC_FTB_Table[45]	178	
Dem_DTC_FTB_Table[46]	245	
Dem_DTC_FTB_Table[47]	151	
Dem_DTC_FTB_Table[48]	160	
Dem_DTC_FTB_Table[49]	245	
Dem_DTC_FTB_Table[50]	151	
Dem_DTC_FTB_Table[51]	245	
Dem_DTC_FTB_Table[52]	245	
Dem_DTC_FTB_Table[53]	151	
Dem_DTC_FTB_Table[54]	160	
	178	
Dem_DTC_FTB_Table[55]		
Dem_DTC_FTB_Table[56]	245	
Dem_DTC_FTB_Table[57]	151	
Dem_DTC_FTB_Table[58]	245	
Dem_DTC_FTB_Table[59]	178	
Dem_DTC_FTB_Table[60]	245	
Dem_DTC_FTB_Table[61]	151	
Dem_DTC_FTB_Table[61]	160	
Dem_DTC_FTB_Table[63]	199	
Dem_DTC_FTB_Table[64]	160	
Dem_DTC_FTB_Table[65]	30	
Dem_DTC_FTB_Table[66]	136	
Dem_DTC_FTB_Table[67]	245	
Dem_DTC_FTB_Table[68]	245	
Dem_DTC_FTB_Table[69]	151	
Dem_DTC_FTB_Table[70]	160	
Dem_DTC_FTB_Table[71]	178	

DemIf\_DTCS

2018-04-10, 18:44:44+0530



Input Value Dem DTC FTB Table[72] 160 Dem\_DTC\_FTB\_Table[73] 199 Dem\_DTC\_FTB\_Table[74] 160 Dem\_DTC\_FTB\_Table[75] 30 136 Dem\_DTC\_FTB\_Table[76] **Actual Value Expected Value** Name Result CTCFailedBuf\_Cnt\_M\_lgc[0] CTCFailedBuf\_Cnt\_M\_lgc[1] 1 CTCFailedBuf\_Cnt\_M\_lgc[2] CTCFailedBuf\_Cnt\_M\_lgc[3] 1 CTCFailedBuf\_Cnt\_M\_lgc[4] CTCFailedBuf\_Cnt\_M\_lgc[5] 0 CTCFailedBuf\_Cnt\_M\_lgc[6] 1 CTCFailedBuf\_Cnt\_M\_lgc[7] CTCFailedBuf\_Cnt\_M\_lgc[8] 1 CTCFailedBuf\_Cnt\_M\_lgc[9] CTCFailedBuf\_Cnt\_M\_lgc[10] CTCFailedBuf\_Cnt\_M\_lgc[11] CTCFailedBuf Cnt M lqc[12]  $CTCFailedBuf\_Cnt\_M\_lgc[13]$ CTCFailedBuf\_Cnt\_M\_lgc[14] CTCFailedBuf\_Cnt\_M\_lgc[15] CTCFailedBuf\_Cnt\_M\_lgc[16] 1 CTCFailedBuf\_Cnt\_M\_lgc[17] 1 CTCFailedBuf\_Cnt\_M\_lgc[18] 1 CTCFailedBuf\_Cnt\_M\_lgc[19] 1 0 CTCFailedBuf\_Cnt\_M\_lgc[20] 0 CTCFailedBuf\_Cnt\_M\_lgc[21] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[22] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[23] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[24] CTCFailedBuf\_Cnt\_M\_lgc[25] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[26] CTCFailedBuf Cnt M Igc[27] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[28] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[29] 1 ~ CTCFailedBuf\_Cnt\_M\_lgc[30] CTCFailedBuf\_Cnt\_M\_lgc[31] CTCFailedBuf\_Cnt\_M\_lgc[32] CTCFailedBuf\_Cnt\_M\_lgc[33] CTCFailedBuf Cnt M lqc[34] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[35] 0 0 CTCFailedBuf Cnt M lqc[36] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[37] 0 0 CTCFailedBuf Cnt M lqc[38] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[39] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[40] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[41] 0 0 0 CTCFailedBuf\_Cnt\_M\_lgc[42] 0 CTCFailedBuf\_Cnt\_M\_lgc[43] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[44] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[45] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[46] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[47] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[48] 0 0 **~** CTCFailedBuf\_Cnt\_M\_lgc[49] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[50] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[51] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[52] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[53] 1 CTCFailedBuf\_Cnt\_M\_lgc[54] CTCFailedBuf\_Cnt\_M\_lgc[55] 1 CTCFailedBuf Cnt M Igc[56] CTCFailedBuf\_Cnt\_M\_lgc[57] CTCFailedBuf Cnt M lqc[58] CTCFailedBuf\_Cnt\_M\_lgc[59] CTCFailedBuf Cnt M lqc[60] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[61] 1 CTCFailedBuf Cnt M Igc[62] 1 CTCFailedBuf\_Cnt\_M\_lgc[63] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[64] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[65] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[66] 0 0

Demlf\_DTCS

2018-04-10, 18:44:44+0530



**Actual Value Expected Value** CTCFailedBuf\_Cnt\_M\_lgc[67] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[68] 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[73] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[74] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[75] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 0 CTCFailed\_Cnt\_M\_lgc 0 0 Demlf\_DTCStatusChanged() 0 0 Rte\_Write\_Ap\_DemIf\_CTCFailed\_Cnt\_lgc(data) 0 0

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	~

2018-04-10, 18:50:29+0530



DemIf\_VehSpdControl

Project Demlf

Module Demlf

DemIf\_VehSpdControl

## Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

#### **Statistics**

**Test Object** 

Total Testcases	1	
Successful	1	~
Failed	0	
Not Executed	0	

### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config \TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\Demif\src\Ap_Demif.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I\$(PROJECTROOT)\Demlf\utp\contract -I\$(PROJECTROOT)\Demlf\utp\contract\Ap_Demlf -I\$ (PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include

Name	Text
Module 'Demif'	Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_Demlf.c Code File(s) Version:3 Module Design Document:Demlf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):104 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note 1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference.

Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4
Time Unit	cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



## Test Case 1: Range Test

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

TS 1.1 12.00 Cycles TS 1.2 12.00 Cycles

Description Vector Description:

TS 1.1 Enable\_Cnt\_T\_lgc=>Min TS 1.2 Enable\_Cnt\_T\_lgc=>Max

Test Step 1.1 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
Enable_Cnt_T_lgc	0		
Name	Actual Value	Expected Value	Result
VehSpdControl_Cnt_M_lgc	0	0	✓

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 1.2 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
Enable_Cnt_T_lgc	1		
Name	Actual Value	Expected Value	Result
VehSpdControl_Cnt_M_lgc	1	1	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

2018-04-10, 18:49:59+0530



Demlf_SetOperationCycleState	Razorcat
Project	
Module	
Test Object	

## Instrumentation: Test Object Only

Statement (C0) Coverage	
Branch (C1) Coverage	

#### **Statistics**

Total Testcases	
Successful	<b>~</b>
Failed	
Not Executed	

## **Module Properties**

Project Root Directory
Configuration File
Target Environment
Kind of Test
Linker Options
Source File(s)
File
Compiler Options

ame	Text			

Attributes				
Name	Value			
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5			
Float Precision	9			
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj			
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src			
Linker File	\$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd			
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl			
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4			
Time Unit	cycles			
Timer Enabled	false			
Timer Prescale	0			
Timer Resolution				
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg			
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP			

DemIf\_SetOperationCycleState

2018-04-10, 18:49:59+0530



## Test Case 1: Range Test

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

CPU Cycles:

TS 1.1 502.00 Cycles

Description

Test Step 1.1 (Repeat Count = 1)				<b>~</b>
Name		Input Value		
Test Step Call Trace				<b>~</b>
Actual Function	Count	Expected Function	Count	Result

2018-04-10, 18:48:23+0530



. –	<b>.</b>			·	<b>.</b>	<b>`</b>	_	•	•	•
Dem	If R	estari	Dem	,						

Project	
Module	
Test Object	

## Instrumentation: Test Object Only

Statement (C0) Coverage	
Branch (C1) Coverage	

#### **Statistics**

Total Testcases	
Successful	<b>~</b>
Failed	
Not Executed	

## **Module Properties**

пе	Text			

Attributes				
Name	Value			
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5			
Float Precision	9			
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj			
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src			
Linker File	\$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd			
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl			
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4			
Time Unit	cycles			
Timer Enabled	false			
Timer Prescale	0			
Timer Resolution	1			
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg			
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP			

Demlf\_RestartDem

2018-04-10, 18:48:23+0530



# Test Case 1: Range Test

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

CPU Cycles:

TS 1.1 500.00 Cycles

Description

## Test Step 1.1 (Repeat Count = 1)

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
				•

2018-04-10, 18:40:20+0530



Demlf\_CheckVoltageRange

Project	Demlf
Module	Demlf
Test Object	Demlf_CheckVoltageRange

## Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MC/DC Coverage	100 %

### **Statistics**

Total Testcases	2	
Successful	2	✓
Failed	0	
Not Executed	0	

## **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf	
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config \TMS570_GCC_UDE_CCS4_Config.xml	
Target Environment	TI TMS 570 PLS UDE (Default)	
Kind of Test	Unit Test	
Linker Options		
Source File(s)		
File	\$(PROJECTROOT)\Demif\src\Ap_Demif.c	
Compiler Options	-D_DATA_ACCESS= -Dconst= -I\$(PROJECTROOT)\Demlflutp\contract -I\$(PROJECTROOT)\Demlflutp\contract\Ap_Demlf -I\$ (PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include	

Name	Text
Module 'Demi <b>f</b> '	Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_Demlf.c Code File(s) Version:3 Module Design Document:Demlf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):104 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference.

Attributes					
Name	Value				
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5				
Float Precision	9				
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj				
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src				
Linker File	\$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd				
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl				
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4				
Time Unit	cycles				
Timer Enabled	false				
Timer Prescale	0				
Timer Resolution	1				
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg				

2018-04-10, 18:40:20+0530



Demlf\_CheckVoltageRange

Attributes	
Name	Value
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



Demlf\_CheckVoltageRange

#### Test Case 1: Metrics Test

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

TS 1.1 76.00 Cycles TS 1.2 97.00 Cycles

Description Vector Description:

 $TS 1.1 \ Shortest \ Execution \ Path=>if ((voltage_Volt_T_f32 < min_Volt_T_f32)=>False \mid (max_Volt_T_f32 < voltage_Volt_T_f32)>>False) \\ TS 1.2 \ Longest \ Execution \ Path=>if ((voltage_Volt_T_f32 < min_Volt_T_f32)=>True \mid (max_Volt_T_f32 < voltage_Volt_T_f32))$ 

Test Step 1.1 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
max_Volt_T_f32	0		
min_Volt_T_f32	0		
time_cnt_T_u32	0		
timer_cnt_T_u32	target_timer_cnt_T_u32		
voltage_Volt_T_f32	0		
Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	0	0	<b>✓</b>

Test Step Call Trace					<b>✓</b>
A	ctual Function	Count	Expected Function	Count	Result
*r	none*	0	*** No Call Expected ***	0	~

Test Step 1.2 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
max_Volt_T_f32	0.426099986		
min_Volt_T_f32	12.3562002		
time_cnt_T_u32	1452352		
timer_cnt_T_u32	target_timer_cnt_T_u32		
voltage_Volt_T_f32	0		
Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	1452352	1452352	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count E	expected Function	Count	Result
*none*	0 *	** No Call Expected ***	0	~



#### Test Case 2: Range Test

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

CPU Cycles:

TS 2.1 76.00 Cycles
TS 2.2 76.00 Cycles
TS 2.2 76.00 Cycles
TS 2.3 97.00 Cycles
TS 2.4 101.00 Cycles
TS 2.5 78.00 Cycles
TS 2.6 78.00 Cycles
TS 2.7 99.00 Cycles
TS 2.8 99.00 Cycles
TS 2.9 78.00 Cycles
TS 2.10 96.00 Cycles
TS 2.11 76.00 Cycles
TS 2.12 97.00 Cycles
TS 2.12 97.00 Cycles
TS 2.13 101.00 Cycles
TS 2.14 99.00 Cycles

#### Description

#### Vector Description:

TS 1.1All Min TS 1.2All Max

TS 1.2All Max
TS 1.3voltage\_Volt\_T\_f32=>Min
TS 1.4voltage\_Volt\_T\_f32=>Min
TS 1.5voltage\_Volt\_T\_f32=>Mon
TS 1.5voltage\_Volt\_T\_f32=>Pos
TS 1.6min\_Volt\_T\_f32=>Min
TS 1.7min\_Volt\_T\_f32=>Pos
TS 1.9max\_Volt\_T\_f32=>Min
TS 1.10max\_Volt\_T\_f32=>Max
TS 1.11max\_Volt\_T\_f32=>Pos
TS 1.12time\_cnt\_T\_u32=>Min
TS 1.13time\_cnt\_T\_u32=>Mon
TS 1.14time\_cnt\_T\_u32=>Pos

#### Test Step 2.1 (Repeat Count = 1) Input Value Name max\_Volt\_T\_f32 0 $min\_Volt\_T\_f32$ 0 time\_cnt\_T\_u32 timer\_cnt\_T\_u32 target\_timer\_cnt\_T\_u32 voltage\_Volt\_T\_f32 **Expected Value Actual Value** Result target\_timer\_cnt\_T\_u32 0 0

Test Step Call Trace				<b>✓</b>	
Ac	tual Function	Count	Expected Function	Count	Result
*no	ne*	0	*** No Call Expected ***	0	~

Test Step 2.2 (Repeat Count = 1)			
Name	Input Value		
max_Volt_T_f32	31		
min_Volt_T_f32	31		
time_cnt_T_u32	4294967295		
timer_cnt_T_u32	target_timer_cnt_T_u32		
voltage_Volt_T_f32	31		
Name	Actual Value	Expected Value	Result
target timer cnt T u32	0	0	<b>✓</b>

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
*none*	0	*** No Call Expected ***	0	~	

Test Step 2.3 (Repeat Count = 1)			
Name	Input Value		
max_Volt_T_f32	0.426099986		
min_Volt_T_f32	12.3562002		
time_cnt_T_u32	1452352		
timer_cnt_T_u32	target_timer_cnt_T_u32		
voltage_Volt_T_f32	0		
Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	1452352	1452352	<b>✓</b>

2018-04-10, 18:40:20+0530



Demlf\_CheckVoltageRange

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.4 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
max_Volt_T_f32	0.125400007		
min_Volt_T_f32	8.41409969		
time_cnt_T_u32	2151351		
timer_cnt_T_u32	target_timer_cnt_T_u32		
voltage_Volt_T_f32	31		
Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	2151351	2151351	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.5 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
max_Volt_T_f32	9.11979961		
min_Volt_T_f32	5.12400007		
time_cnt_T_u32	1241		
timer_cnt_T_u32	target_timer_cnt_T_u32		
voltage_Volt_T_f32	12.1353998		
Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	1241	1241	~

Test Step Call Trace					<b>✓</b>
	Actual Function	Count	Expected Function	Count	Result
,	none*	0	*** No Call Expected ***	0	~

Test Step 2.6 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
max_Volt_T_f32	5.07380009		
min_Volt_T_f32	0		
time_cnt_T_u32	1151336		
timer_cnt_T_u32	target_timer_cnt_T_u32		
voltage_Volt_T_f32	19.5648003		
Name	Actual Value	Expected Value	Result
target timer cnt T u32	1151336	1151336	<b>✓</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.7 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
max_Volt_T_f32	1.73090005		
min_Volt_T_f32	31		
time_cnt_T_u32	52		
timer_cnt_T_u32	target_timer_cnt_T_u32		
voltage_Volt_T_f32	12.3786001		
Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	52	52	<b>✓</b>

2018-04-10, 18:40:20+0530



Demii_CheckvollageRange

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.8 (Repeat Count = 1)			✓
Name	Input Value		
max_Volt_T_f32	2.5236001		
min_Volt_T_f32	8.14509964		
time_cnt_T_u32	78073		
timer_cnt_T_u32	target_timer_cnt_T_u32		
voltage_Volt_T_f32	0.0706999972		
Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	78073	78073	•

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.9 (Repeat Count = 1)			<b>✓</b>	
Name	Input Value			
max_Volt_T_f32	0			
min_Volt_T_f32	0.262400001			
time_cnt_T_u32	3424	3424		
timer_cnt_T_u32	target_timer_cnt_T_u32			
voltage_Volt_T_f32	1.22490001			
Name	Actual Value	Expected Value	Result	
target_timer_cnt_T_u32	3424	3424	✓	

Test Step Call Trace				<b>✓</b>	
	Actual Function	Count	Expected Function	Count	Result
,	none*	0	*** No Call Expected ***	0	~

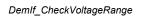
Test Step 2.10 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
max_Volt_T_f32	31		
min_Volt_T_f32	9.23530006		
time_cnt_T_u32	857634		
timer_cnt_T_u32	target_timer_cnt_T_u32		
voltage_Volt_T_f32	12.9097004		
Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	3424	3424	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.11 (Repeat Count = 1)			✓
Name	Input Value		
max_Volt_T_f32	14.2140999		
min_Volt_T_f32	1.46340001		
time_cnt_T_u32	352624		
timer_cnt_T_u32	target_timer_cnt_T_u32		
voltage_Volt_T_f32	10.7594995		
Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	3424	3424	<b>✓</b>

2018-04-10, 18:40:20+0530





Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.12 (Repeat Count = 1)			<b>✓</b>	
Name	Input Value			
max_Volt_T_f32	16.8927994			
min_Volt_T_f32	26.1240997			
time_cnt_T_u32	0	0		
timer_cnt_T_u32	target_timer_cnt_T_u32	!		
voltage_Volt_T_f32	0			
Name	Actual Value	Expected Value	Result	
target_timer_cnt_T_u32	0	0	<b>✓</b>	

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.13 (Repeat Count = 1)		✓
Name	Input Value	
max_Volt_T_f32	12.0332003	
min_Volt_T_f32	12.1252003	
time_cnt_T_u32	4294967295	
timer_cnt_T_u32	target_timer_cnt_T_u32	
voltage_Volt_T_f32	21.4778004	
Name	Actual Value	

