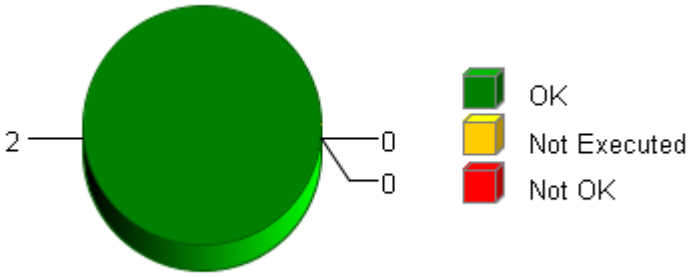
Summary

Total Test Objects:	2
Successful:	2
Failed:	0
Not Executed:	0
Date:	2015-11-06
Time:	13:15:48+0530

Overall Test Object Results (including Coverage)



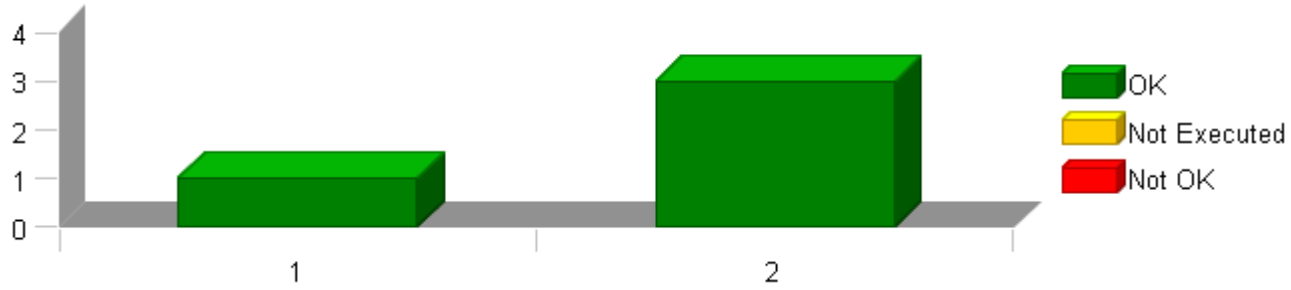
Selected Project Items

Test Collection "CBD_UnitTest"

Used Test Environments

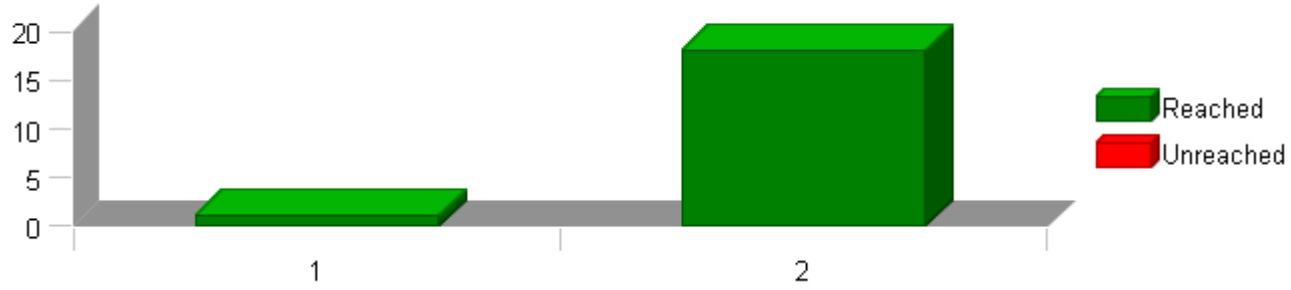
TI TMS 570 PLS UDE (Default)

Test Case Results for Each Test Object (without Coverage)



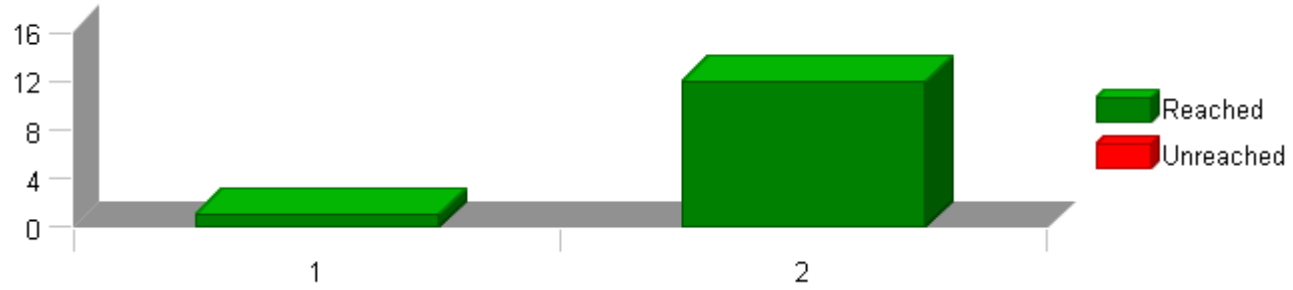
The table above shows each test object on the x axis and the number of test cases of the respective test object on the y axis. Each bar is divided into passed, not executed and failed test cases. The test case results do not take into account any coverage result (i.e. if all test cases of a test object are passed in this table but the coverage is failed, the overall test object result will be failed).

Statement (C0) Coverage: Total Statements for Each Test Object



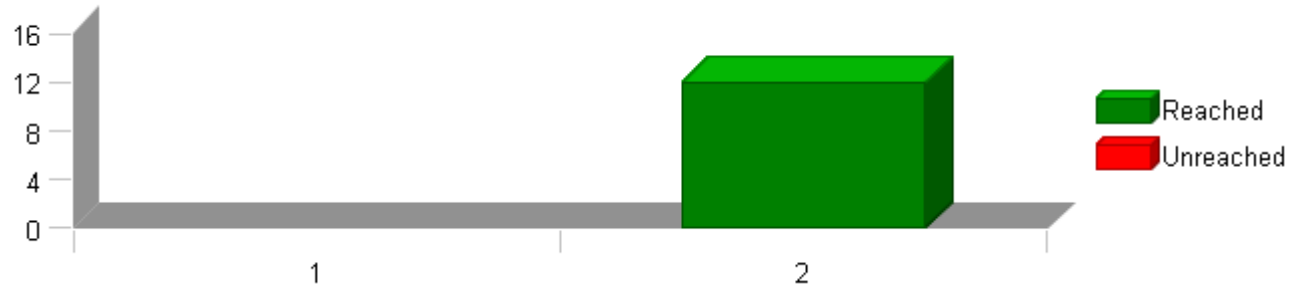
The table above shows each test object on the x axis and the number of statements of the respective test object on the y axis. Each bar is divided into reached statements (i.e. statements that have been executed during the test) and unreached statements.

Branch (C1) Coverage: Total Branches for Each Test Object



The table above shows each test object on the x axis and the number of branches of the respective test object on the y axis. Each bar is divided into reached branches (i.e. branches that have been executed during the test) and unreached branches.

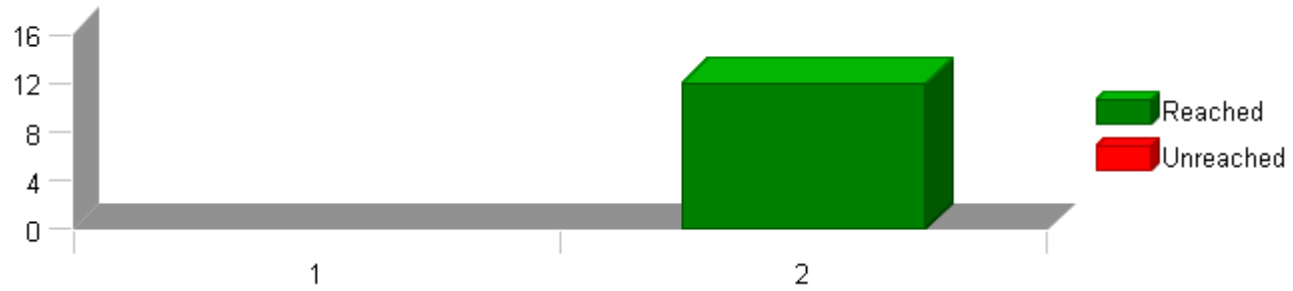
Decision Coverage: Total Decision Outcomes for Each Test Object



The table above shows test objects on the x axis and the number of possible outcomes of all decisions of the respective test object on the y axis. To achieve full DC coverage, each decision must evaluate to both true and false.

Each bar is divided into reached and unreached decision outcomes.

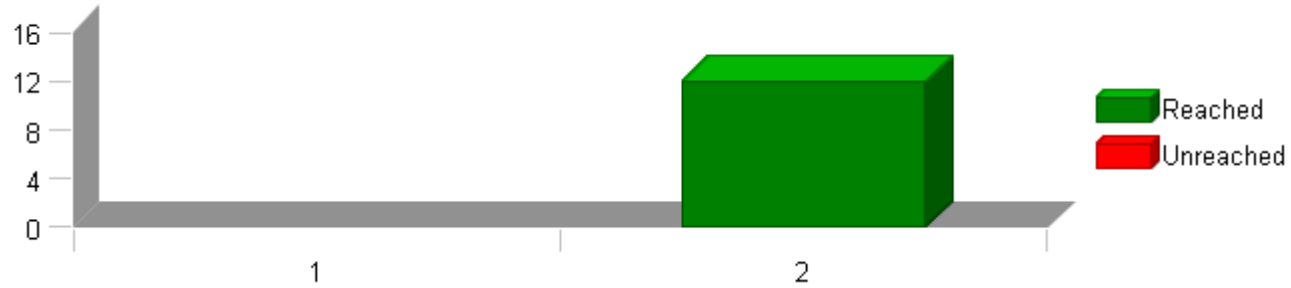
MC/DC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MC/DC coverage, each decision requires all contained atomic conditions to evaluate to both true and false independently of all other conditions. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

MCC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MCC coverage, each decision requires all contained atomic conditions to evaluate to all possible combinations of true and false values. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

Test Object List

The following table lists all test objects with their test case and coverage results. The cumulated results for modules, folders and test collections are also displayed, the indentation within the name column indicates the parent relationship of the elements.

Please note that only test objects are numbered within the first column. This number is referenced on the x axis within the overview charts for test case and coverage results available on previous pages (if included into the report).

No.	Name	C0	C1	DC	MC/DC	MCC	Test Cases	Result
	Ap_ePWM_1	100 %	100 %	100 %	100 %	100 %	4 of 4 passed	✔
	CBD_UnitTest	100 %	100 %	100 %	100 %	100 %	4 of 4 passed	✔
	ePWM_1	100 %	100 %	100 %	100 %	100 %	4 of 4 passed	✔
1	ePWM_Init1	100 %	100 %	-	-	-	1 of 1 passed	✔
2	ePWM_Per1	100 %	100 %	100 %	100 %	100 %	3 of 3 passed	✔

TEST DETAILS REPORT

ePWM_Init1

2015-11-06, 13:12:52+0530

Project	Ap_ePWM_1
Module	ePWM_1
Test Object	ePWM_Init1

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

Statistics

Total Testcases	1
Successful	1
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\9BXX_ePWM_Up
Configuration File	D:\Synergy_Work_Area\9BXX_ePWM_Up\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\ePWM_Up\src\ePWM.c
Compiler Options	-DSTATIC= -D_DATA_ACCESS= -D__inline= -Dconst= -I$(PROJECTROOT)\ePWM_Up\utp\contract\Ap_ePWM2 -I$(PROJECTROOT)\ePWM_Up\utp\contract -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef\include -I$(PROJECTROOT)\ePWM_Up\include -I$(Compiler Install Path)\include

Comments/Description/Specification

Name	Text
Module 'ePWM_1'	********** UNIT TEST DESCRIPTION********** Name of Tester:Jayesh Jahagirdar Code File(s) Under Test:ePWM.c Code File(s) Version:2 Module Design Document:ePWM MDD.docx Module Design Document Version:2 Data Dictionary Version:2 Unit Test Plan Version:1 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.32 Total FLASH Used (Bytes):564 Total RAM Used (Bytes):28 Total CALS Used (Bytes):6 Special Test Requirements: Test Date:11-06-2015 Comments:""NOTE1: Inline function defined in ""GlobalMacro.h"" are not unit tested. NOTE2: ""CBD_Sandbox_dbg.map"" map file is embedded for reference." **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(ProgramFiles)\pls\UDE 4.0
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
Timer Unit	Cycles
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg

Workspace File	D:\Synergy_Work_Area\9BXX_ePWM_Up\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Boundary Test

Specification

```
Performance metrics
(With "None" Instrumentation and
"WithPS" environment)

TS 1.1   309.00 Cycles
TS 1.2   309.00 Cycles
TS 1.3   309.00 Cycles
TS 1.4   309.00 Cycles
TS 1.5   309.00 Cycles
TS 1.6   309.00 Cycles
TS 1.7    309.00 Cycles
TS 1.8   309.00 Cycles
```

Description

Vector Description:

TS1.1All min
TS1.2All max
TS1.3k_PwmDeadBand_Cnt_u16=min
TS1.4k_PwmDeadBand_Cnt_u16=max
TS1.5k_PwmDeadBand_Cnt_u16=pos/Default
TS1.6k_PwmRelay_Cnt_u16=min
TS1.7k_PwmRelay_Cnt_u16=max
TS1.8k_PwmRelay_Cnt_u16=pos/default

Test Step 1.1 (Repeat Count = 1)

Name	Input Value
ePWM1_temp	target_ePWM1_temp
ePWM2_temp	target_ePWM2_temp
ePWM3_temp	target_ePWM3_temp
ePWM4_temp	target_ePWM4_temp
ePWM7_temp	target_ePWM7_temp
k_PwmDeadBand_Cnt_u16	0
k_PwmRelay_Cnt_u16	0
target_ePWM1_temp.DBCTL	11
target_ePWM2_temp.DBCTL	11
target_ePWM3_temp.DBCTL	11

Name	Actual Value	Expected Value	Result
target_ePWM1_temp.TBCTL	8196	8196	✔
target_ePWM1_temp.TBPHS	0	0	✔
target_ePWM1_temp.TBPRD	65535	65535	✔
target_ePWM1_temp.CMPCTL	0	0	✔
target_ePWM1_temp.CMPA	2499	2499	✔
target_ePWM1_temp.AQCTLA	289	289	✔
target_ePWM1_temp.CMPB	2499	2499	✔
target_ePWM1_temp.DBCTL	8	8	✔
target_ePWM1_temp.AQCSFRC	5	5	✔
target_ePWM1_temp.DBFED	0	0	✔
target_ePWM1_temp.DBRED	0	0	✔
target_ePWM1_temp.TZCTL	4095	4095	✔
target_ePWM1_temp.ETSEL	0	0	✔
target_ePWM1_temp.PCCTL	0	0	✔
target_ePWM2_temp.TBCTL	8196	8196	✔
target_ePWM2_temp.TBPHS	0	0	✔
target_ePWM2_temp.TBPRD	65535	65535	✔
target_ePWM2_temp.CMPCTL	0	0	✔
target_ePWM2_temp.CMPA	2499	2499	✔
target_ePWM2_temp.AQCTLA	288	288	✔
target_ePWM2_temp.CMPB	2499	2499	✔
target_ePWM2_temp.DBCTL	8	8	✔
target_ePWM2_temp.AQCSFRC	5	5	✔
target_ePWM2_temp.DBFED	0	0	✔
target_ePWM2_temp.DBRED	0	0	✔
target_ePWM2_temp.TZCTL	4095	4095	✔
target_ePWM2_temp.ETSEL	0	0	✔
target_ePWM2_temp.PCCTL	0	0	✔
target_ePWM3_temp.TBCTL	8196	8196	✔
target_ePWM3_temp.TBPHS	0	0	✔
target_ePWM3_temp.TBPRD	65535	65535	✔
target_ePWM3_temp.CMPCTL	0	0	✔
target_ePWM3_temp.CMPA	2499	2499	✔
target_ePWM3_temp.AQCTLA	288	288	✔
target_ePWM3_temp.CMPB	2499	2499	✔
target_ePWM3_temp.DBCTL	8	8	✔
target_ePWM3_temp.AQCSFRC	5	5	✔
target_ePWM3_temp.DBFED	0	0	✔
target_ePWM3_temp.DBRED	0	0	✔
target_ePWM3_temp.TZCTL	4095	4095	✔

Name	Actual Value	Expected Value	Result
target_ePWM3_temp.ETSEL	0	0	✔
target_ePWM3_temp.PCCTL	0	0	✔
target_ePWM4_temp.TBCTL	4	4	✔
target_ePWM4_temp.TBPHS	0	0	✔
target_ePWM4_temp.TBPRD	65535	65535	✔
target_ePWM4_temp.CMPCTL	0	0	✔
target_ePWM4_temp.CMPA	2499	2499	✔
target_ePWM4_temp.AQCTLA	0	0	✔
target_ePWM4_temp.CMPB	65535	65535	✔
target_ePWM4_temp.DBCTL	0	0	✔
target_ePWM4_temp.TZCTL	4095	4095	✔
target_ePWM4_temp.ETSEL	60416	60416	✔
target_ePWM4_temp.ETPS	4352	4352	✔
target_ePWM4_temp.PCCTL	0	0	✔
target_ePWM7_temp.TBCTL	4	4	✔
target_ePWM7_temp.TBPHS	0	0	✔
target_ePWM7_temp.TBPRD	65535	65535	✔
target_ePWM7_temp.CMPCTL	0	0	✔
target_ePWM7_temp.CMPA	0	0	✔
target_ePWM7_temp.AQCTLB	33	33	✔
target_ePWM7_temp.DBCTL	0	0	✔
target_ePWM7_temp.TZCTL	4095	4095	✔
target_ePWM7_temp.ETSEL	0	0	✔
target_ePWM7_temp.PCCTL	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 1.2 (Repeat Count = 1) ✔

Name	Input Value
ePWM1_temp	target_ePWM1_temp
ePWM2_temp	target_ePWM2_temp
ePWM3_temp	target_ePWM3_temp
ePWM4_temp	target_ePWM4_temp
ePWM7_temp	target_ePWM7_temp
k_PwmDeadBand_Cnt_u16	1024
k_PwmRelay_Cnt_u16	65535
target_ePWM1_temp.DBCTL	11
target_ePWM2_temp.DBCTL	11
target_ePWM3_temp.DBCTL	11

Name	Actual Value	Expected Value	Result
target_ePWM1_temp.TBCTL	8196	8196	✔
target_ePWM1_temp.TBPHS	0	0	✔
target_ePWM1_temp.TBPRD	65535	65535	✔
target_ePWM1_temp.CMPCTL	0	0	✔
target_ePWM1_temp.CMPA	2499	2499	✔
target_ePWM1_temp.AQCTLA	289	289	✔
target_ePWM1_temp.CMPB	2499	2499	✔
target_ePWM1_temp.DBCTL	8	8	✔
target_ePWM1_temp.AQCSFRC	5	5	✔
target_ePWM1_temp.DBFED	1024	1024	✔
target_ePWM1_temp.DBRED	1024	1024	✔
target_ePWM1_temp.TZCTL	4095	4095	✔
target_ePWM1_temp.ETSEL	0	0	✔
target_ePWM1_temp.PCCTL	0	0	✔
target_ePWM2_temp.TBCTL	8196	8196	✔
target_ePWM2_temp.TBPHS	0	0	✔
target_ePWM2_temp.TBPRD	65535	65535	✔
target_ePWM2_temp.CMPCTL	0	0	✔
target_ePWM2_temp.CMPA	2499	2499	✔
target_ePWM2_temp.AQCTLA	288	288	✔
target_ePWM2_temp.CMPB	2499	2499	✔
target_ePWM2_temp.DBCTL	8	8	✔
target_ePWM2_temp.AQCSFRC	5	5	✔
target_ePWM2_temp.DBFED	1024	1024	✔
target_ePWM2_temp.DBRED	1024	1024	✔
target_ePWM2_temp.TZCTL	4095	4095	✔
target_ePWM2_temp.ETSEL	0	0	✔
target_ePWM2_temp.PCCTL	0	0	✔

Name	Actual Value	Expected Value	Result
target_ePWM3_temp.TBCTL	8196	8196	✔
target_ePWM3_temp.TBPHS	0	0	✔
target_ePWM3_temp.TBPRD	65535	65535	✔
target_ePWM3_temp.CMPCTL	0	0	✔
target_ePWM3_temp.CMPA	2499	2499	✔
target_ePWM3_temp.AQCTLA	288	288	✔
target_ePWM3_temp.CMPB	2499	2499	✔
target_ePWM3_temp.DBCTL	8	8	✔
target_ePWM3_temp.AQCSFRC	5	5	✔
target_ePWM3_temp.DBFED	1024	1024	✔
target_ePWM3_temp.DBRED	1024	1024	✔
target_ePWM3_temp.TZCTL	4095	4095	✔
target_ePWM3_temp.ETSEL	0	0	✔
target_ePWM3_temp.PCCTL	0	0	✔
target_ePWM4_temp.TBCTL	4	4	✔
target_ePWM4_temp.TBPHS	0	0	✔
target_ePWM4_temp.TBPRD	65535	65535	✔
target_ePWM4_temp.CMPCTL	0	0	✔
target_ePWM4_temp.CMPA	2499	2499	✔
target_ePWM4_temp.AQCTLA	0	0	✔
target_ePWM4_temp.CMPB	65535	65535	✔
target_ePWM4_temp.DBCTL	0	0	✔
target_ePWM4_temp.TZCTL	4095	4095	✔
target_ePWM4_temp.ETSEL	60416	60416	✔
target_ePWM4_temp.ETPS	4352	4352	✔
target_ePWM4_temp.PCCTL	0	0	✔
target_ePWM7_temp.TBCTL	4	4	✔
target_ePWM7_temp.TBPHS	0	0	✔
target_ePWM7_temp.TBPRD	65535	65535	✔
target_ePWM7_temp.CMPCTL	0	0	✔
target_ePWM7_temp.CMPA	65535	65535	✔
target_ePWM7_temp.AQCTLB	33	33	✔
target_ePWM7_temp.DBCTL	0	0	✔
target_ePWM7_temp.TZCTL	4095	4095	✔
target_ePWM7_temp.ETSEL	0	0	✔
target_ePWM7_temp.PCCTL	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 1.3 (Repeat Count = 1) ✔

Name	Input Value
ePWM1_temp	target_ePWM1_temp
ePWM2_temp	target_ePWM2_temp
ePWM3_temp	target_ePWM3_temp
ePWM4_temp	target_ePWM4_temp
ePWM7_temp	target_ePWM7_temp
k_PwmDeadBand_Cnt_u16	0
k_PwmRelay_Cnt_u16	1025
target_ePWM1_temp.DBCTL	11
target_ePWM2_temp.DBCTL	11
target_ePWM3_temp.DBCTL	11

Name	Actual Value	Expected Value	Result
target_ePWM1_temp.TBCTL	8196	8196	✔
target_ePWM1_temp.TBPHS	0	0	✔
target_ePWM1_temp.TBPRD	65535	65535	✔
target_ePWM1_temp.CMPCTL	0	0	✔
target_ePWM1_temp.CMPA	2499	2499	✔
target_ePWM1_temp.AQCTLA	289	289	✔
target_ePWM1_temp.CMPB	2499	2499	✔
target_ePWM1_temp.DBCTL	8	8	✔
target_ePWM1_temp.AQCSFRC	5	5	✔
target_ePWM1_temp.DBFED	0	0	✔
target_ePWM1_temp.DBRED	0	0	✔
target_ePWM1_temp.TZCTL	4095	4095	✔
target_ePWM1_temp.ETSEL	0	0	✔
target_ePWM1_temp.PCCTL	0	0	✔
target_ePWM2_temp.TBCTL	8196	8196	✔
target_ePWM2_temp.TBPHS	0	0	✔

Name	Actual Value	Expected Value	Result
target_ePWM2_temp.TBPRD	65535	65535	✔
target_ePWM2_temp.CMPCTL	0	0	✔
target_ePWM2_temp.CMPA	2499	2499	✔
target_ePWM2_temp.AQCTLA	288	288	✔
target_ePWM2_temp.CMPB	2499	2499	✔
target_ePWM2_temp.DBCTL	8	8	✔
target_ePWM2_temp.AQCSFRC	5	5	✔
target_ePWM2_temp.DBFED	0	0	✔
target_ePWM2_temp.DBRED	0	0	✔
target_ePWM2_temp.TZCTL	4095	4095	✔
target_ePWM2_temp.ETSEL	0	0	✔
target_ePWM2_temp.PCCTL	0	0	✔
target_ePWM3_temp.TBCTL	8196	8196	✔
target_ePWM3_temp.TBPHS	0	0	✔
target_ePWM3_temp.TBPRD	65535	65535	✔
target_ePWM3_temp.CMPCTL	0	0	✔
target_ePWM3_temp.CMPA	2499	2499	✔
target_ePWM3_temp.AQCTLA	288	288	✔
target_ePWM3_temp.CMPB	2499	2499	✔
target_ePWM3_temp.DBCTL	8	8	✔
target_ePWM3_temp.AQCSFRC	5	5	✔
target_ePWM3_temp.DBFED	0	0	✔
target_ePWM3_temp.DBRED	0	0	✔
target_ePWM3_temp.TZCTL	4095	4095	✔
target_ePWM3_temp.ETSEL	0	0	✔
target_ePWM3_temp.PCCTL	0	0	✔
target_ePWM4_temp.TBCTL	4	4	✔
target_ePWM4_temp.TBPHS	0	0	✔
target_ePWM4_temp.TBPRD	65535	65535	✔
target_ePWM4_temp.CMPCTL	0	0	✔
target_ePWM4_temp.CMPA	2499	2499	✔
target_ePWM4_temp.AQCTLA	0	0	✔
target_ePWM4_temp.CMPB	65535	65535	✔
target_ePWM4_temp.DBCTL	0	0	✔
target_ePWM4_temp.TZCTL	4095	4095	✔
target_ePWM4_temp.ETSEL	60416	60416	✔
target_ePWM4_temp.ETPS	4352	4352	✔
target_ePWM4_temp.PCCTL	0	0	✔
target_ePWM7_temp.TBCTL	4	4	✔
target_ePWM7_temp.TBPHS	0	0	✔
target_ePWM7_temp.TBPRD	65535	65535	✔
target_ePWM7_temp.CMPCTL	0	0	✔
target_ePWM7_temp.CMPA	1025	1025	✔
target_ePWM7_temp.AQCTLB	33	33	✔
target_ePWM7_temp.DBCTL	0	0	✔
target_ePWM7_temp.TZCTL	4095	4095	✔
target_ePWM7_temp.ETSEL	0	0	✔
target_ePWM7_temp.PCCTL	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 1.4 (Repeat Count = 1) ✔

Name	Input Value
ePWM1_temp	target_ePWM1_temp
ePWM2_temp	target_ePWM2_temp
ePWM3_temp	target_ePWM3_temp
ePWM4_temp	target_ePWM4_temp
ePWM7_temp	target_ePWM7_temp
k_PwmDeadBand_Cnt_u16	1024
k_PwmRelay_Cnt_u16	625
target_ePWM1_temp.DBCTL	11
target_ePWM2_temp.DBCTL	11
target_ePWM3_temp.DBCTL	11

Name	Actual Value	Expected Value	Result
target_ePWM1_temp.TBCTL	8196	8196	✔
target_ePWM1_temp.TBPHS	0	0	✔
target_ePWM1_temp.TBPRD	65535	65535	✔
target_ePWM1_temp.CMPCTL	0	0	✔

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Name	Actual Value	Expected Value	Result
target_ePWM1_temp.CMPA	2499	2499	✔
target_ePWM1_temp.AQCTLA	289	289	✔
target_ePWM1_temp.CMPB	2499	2499	✔
target_ePWM1_temp.DBCTL	8	8	✔
target_ePWM1_temp.AQCSFRC	5	5	✔
target_ePWM1_temp.DBFED	1024	1024	✔
target_ePWM1_temp.DBRED	1024	1024	✔
target_ePWM1_temp.TZCTL	4095	4095	✔
target_ePWM1_temp.ETSEL	0	0	✔
target_ePWM1_temp.PCCTL	0	0	✔
target_ePWM2_temp.TBCTL	8196	8196	✔
target_ePWM2_temp.TBPHS	0	0	✔
target_ePWM2_temp.TBPRD	65535	65535	✔
target_ePWM2_temp.CMPCTL	0	0	✔
target_ePWM2_temp.CMPA	2499	2499	✔
target_ePWM2_temp.AQCTLA	288	288	✔
target_ePWM2_temp.CMPB	2499	2499	✔
target_ePWM2_temp.DBCTL	8	8	✔
target_ePWM2_temp.AQCSFRC	5	5	✔
target_ePWM2_temp.DBFED	1024	1024	✔
target_ePWM2_temp.DBRED	1024	1024	✔
target_ePWM2_temp.TZCTL	4095	4095	✔
target_ePWM2_temp.ETSEL	0	0	✔
target_ePWM2_temp.PCCTL	0	0	✔
target_ePWM3_temp.TBCTL	8196	8196	✔
target_ePWM3_temp.TBPHS	0	0	✔
target_ePWM3_temp.TBPRD	65535	65535	✔
target_ePWM3_temp.CMPCTL	0	0	✔
target_ePWM3_temp.CMPA	2499	2499	✔
target_ePWM3_temp.AQCTLA	288	288	✔
target_ePWM3_temp.CMPB	2499	2499	✔
target_ePWM3_temp.DBCTL	8	8	✔
target_ePWM3_temp.AQCSFRC	5	5	✔
target_ePWM3_temp.DBFED	1024	1024	✔
target_ePWM3_temp.DBRED	1024	1024	✔
target_ePWM3_temp.TZCTL	4095	4095	✔
target_ePWM3_temp.ETSEL	0	0	✔
target_ePWM3_temp.PCCTL	0	0	✔
target_ePWM4_temp.TBCTL	4	4	✔
target_ePWM4_temp.TBPHS	0	0	✔
target_ePWM4_temp.TBPRD	65535	65535	✔
target_ePWM4_temp.CMPCTL	0	0	✔
target_ePWM4_temp.CMPA	2499	2499	✔
target_ePWM4_temp.AQCTLA	0	0	✔
target_ePWM4_temp.CMPB	65535	65535	✔
target_ePWM4_temp.DBCTL	0	0	✔
target_ePWM4_temp.TZCTL	4095	4095	✔
target_ePWM4_temp.ETSEL	60416	60416	✔
target_ePWM4_temp.ETPS	4352	4352	✔
target_ePWM4_temp.PCCTL	0	0	✔
target_ePWM7_temp.TBCTL	4	4	✔
target_ePWM7_temp.TBPHS	0	0	✔
target_ePWM7_temp.TBPRD	65535	65535	✔
target_ePWM7_temp.CMPCTL	0	0	✔
target_ePWM7_temp.CMPA	625	625	✔
target_ePWM7_temp.AQCTLB	33	33	✔
target_ePWM7_temp.DBCTL	0	0	✔
target_ePWM7_temp.TZCTL	4095	4095	✔
target_ePWM7_temp.ETSEL	0	0	✔
target_ePWM7_temp.PCCTL	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 1.5 (Repeat Count = 1) ✔

Name	Input Value
ePWM1_temp	target_ePWM1_temp
ePWM2_temp	target_ePWM2_temp
ePWM3_temp	target_ePWM3_temp

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Name	Input Value
ePWM4_temp	target_ePWM4_temp
ePWM7_temp	target_ePWM7_temp
k_PwmDeadBand_Cnt_u16	15
k_PwmRelay_Cnt_u16	3214
target_ePWM1_temp.DBCTL	11
target_ePWM2_temp.DBCTL	11
target_ePWM3_temp.DBCTL	11

Name	Actual Value	Expected Value	Result
target_ePWM1_temp.TBCTL	8196	8196	✔
target_ePWM1_temp.TBPHS	0	0	✔
target_ePWM1_temp.TBPRD	65535	65535	✔
target_ePWM1_temp.CMPCTL	0	0	✔
target_ePWM1_temp.CMPA	2499	2499	✔
target_ePWM1_temp.AQCTLA	289	289	✔
target_ePWM1_temp.CMPB	2499	2499	✔
target_ePWM1_temp.DBCTL	8	8	✔
target_ePWM1_temp.AQCSFRC	5	5	✔
target_ePWM1_temp.DBFED	15	15	✔
target_ePWM1_temp.DBRED	15	15	✔
target_ePWM1_temp.TZCTL	4095	4095	✔
target_ePWM1_temp.ETSEL	0	0	✔
target_ePWM1_temp.PCCTL	0	0	✔
target_ePWM2_temp.TBCTL	8196	8196	✔
target_ePWM2_temp.TBPHS	0	0	✔
target_ePWM2_temp.TBPRD	65535	65535	✔
target_ePWM2_temp.CMPCTL	0	0	✔
target_ePWM2_temp.CMPA	2499	2499	✔
target_ePWM2_temp.AQCTLA	288	288	✔
target_ePWM2_temp.CMPB	2499	2499	✔
target_ePWM2_temp.DBCTL	8	8	✔
target_ePWM2_temp.AQCSFRC	5	5	✔
target_ePWM2_temp.DBFED	15	15	✔
target_ePWM2_temp.DBRED	15	15	✔
target_ePWM2_temp.TZCTL	4095	4095	✔
target_ePWM2_temp.ETSEL	0	0	✔
target_ePWM2_temp.PCCTL	0	0	✔
target_ePWM3_temp.TBCTL	8196	8196	✔
target_ePWM3_temp.TBPHS	0	0	✔
target_ePWM3_temp.TBPRD	65535	65535	✔
target_ePWM3_temp.CMPCTL	0	0	✔
target_ePWM3_temp.CMPA	2499	2499	✔
target_ePWM3_temp.AQCTLA	288	288	✔
target_ePWM3_temp.CMPB	2499	2499	✔
target_ePWM3_temp.DBCTL	8	8	✔
target_ePWM3_temp.AQCSFRC	5	5	✔
target_ePWM3_temp.DBFED	15	15	✔
target_ePWM3_temp.DBRED	15	15	✔
target_ePWM3_temp.TZCTL	4095	4095	✔
target_ePWM3_temp.ETSEL	0	0	✔
target_ePWM3_temp.PCCTL	0	0	✔
target_ePWM4_temp.TBCTL	4	4	✔
target_ePWM4_temp.TBPHS	0	0	✔
target_ePWM4_temp.TBPRD	65535	65535	✔
target_ePWM4_temp.CMPCTL	0	0	✔
target_ePWM4_temp.CMPA	2499	2499	✔
target_ePWM4_temp.AQCTLA	0	0	✔
target_ePWM4_temp.CMPB	65535	65535	✔
target_ePWM4_temp.DBCTL	0	0	✔
target_ePWM4_temp.TZCTL	4095	4095	✔
target_ePWM4_temp.ETSEL	60416	60416	✔
target_ePWM4_temp.ETPS	4352	4352	✔
target_ePWM4_temp.PCCTL	0	0	✔
target_ePWM7_temp.TBCTL	4	4	✔
target_ePWM7_temp.TBPHS	0	0	✔
target_ePWM7_temp.TBPRD	65535	65535	✔
target_ePWM7_temp.CMPCTL	0	0	✔
target_ePWM7_temp.CMPA	3214	3214	✔
target_ePWM7_temp.AQCTLB	33	33	✔
target_ePWM7_temp.DBCTL	0	0	✔
target_ePWM7_temp.TZCTL	4095	4095	✔
target_ePWM7_temp.ETSEL	0	0	✔
target_ePWM7_temp.PCCTL	0	0	✔

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Actual Function	**Count**	**Expected Function**	**Count**	**Result**
none	0	*** No Call Expected ***	0	✔

Test Step 1.6 (Repeat Count = 1) ✔

Name	Input Value
ePWM1_temp	target_ePWM1_temp
ePWM2_temp	target_ePWM2_temp
ePWM3_temp	target_ePWM3_temp
ePWM4_temp	target_ePWM4_temp
ePWM7_temp	target_ePWM7_temp
k_PwmDeadBand_Cnt_u16	120
k_PwmRelay_Cnt_u16	0
target_ePWM1_temp.DBCTL	11
target_ePWM2_temp.DBCTL	11
target_ePWM3_temp.DBCTL	11

Name	Actual Value	Expected Value	Result
target_ePWM1_temp.TBCTL	8196	8196	✔
target_ePWM1_temp.TBPHS	0	0	✔
target_ePWM1_temp.TBPRD	65535	65535	✔
target_ePWM1_temp.CMPCTL	0	0	✔
target_ePWM1_temp.CMPA	2499	2499	✔
target_ePWM1_temp.AQCTLA	289	289	✔
target_ePWM1_temp.CMPB	2499	2499	✔
target_ePWM1_temp.DBCTL	8	8	✔
target_ePWM1_temp.AQCSFRC	5	5	✔
target_ePWM1_temp.DBFED	120	120	✔
target_ePWM1_temp.DBRED	120	120	✔
target_ePWM1_temp.TZCTL	4095	4095	✔
target_ePWM1_temp.ETSEL	0	0	✔
target_ePWM1_temp.PCCTL	0	0	✔
target_ePWM2_temp.TBCTL	8196	8196	✔
target_ePWM2_temp.TBPHS	0	0	✔
target_ePWM2_temp.TBPRD	65535	65535	✔
target_ePWM2_temp.CMPCTL	0	0	✔
target_ePWM2_temp.CMPA	2499	2499	✔
target_ePWM2_temp.AQCTLA	288	288	✔
target_ePWM2_temp.CMPB	2499	2499	✔
target_ePWM2_temp.DBCTL	8	8	✔
target_ePWM2_temp.AQCSFRC	5	5	✔
target_ePWM2_temp.DBFED	120	120	✔
target_ePWM2_temp.DBRED	120	120	✔
target_ePWM2_temp.TZCTL	4095	4095	✔
target_ePWM2_temp.ETSEL	0	0	✔
target_ePWM2_temp.PCCTL	0	0	✔
target_ePWM3_temp.TBCTL	8196	8196	✔
target_ePWM3_temp.TBPHS	0	0	✔
target_ePWM3_temp.TBPRD	65535	65535	✔
target_ePWM3_temp.CMPCTL	0	0	✔
target_ePWM3_temp.CMPA	2499	2499	✔
target_ePWM3_temp.AQCTLA	288	288	✔
target_ePWM3_temp.CMPB	2499	2499	✔
target_ePWM3_temp.DBCTL	8	8	✔
target_ePWM3_temp.AQCSFRC	5	5	✔
target_ePWM3_temp.DBFED	120	120	✔
target_ePWM3_temp.DBRED	120	120	✔
target_ePWM3_temp.TZCTL	4095	4095	✔
target_ePWM3_temp.ETSEL	0	0	✔
target_ePWM3_temp.PCCTL	0	0	✔
target_ePWM4_temp.TBCTL	4	4	✔
target_ePWM4_temp.TBPHS	0	0	✔
target_ePWM4_temp.TBPRD	65535	65535	✔
target_ePWM4_temp.CMPCTL	0	0	✔
target_ePWM4_temp.CMPA	2499	2499	✔
target_ePWM4_temp.AQCTLA	0	0	✔
target_ePWM4_temp.CMPB	65535	65535	✔
target_ePWM4_temp.DBCTL	0	0	✔
target_ePWM4_temp.TZCTL	4095	4095	✔
target_ePWM4_temp.ETSEL	60416	60416	✔
target_ePWM4_temp.ETPS	4352	4352	✔

Name	Actual Value	Expected Value	Result
target_ePWM4_temp.PCCTL	0	0	✔
target_ePWM7_temp.TBCTL	4	4	✔
target_ePWM7_temp.TBPHS	0	0	✔
target_ePWM7_temp.TBPRD	65535	65535	✔
target_ePWM7_temp.CMPCTL	0	0	✔
target_ePWM7_temp.CMPA	0	0	✔
target_ePWM7_temp.AQCTLB	33	33	✔
target_ePWM7_temp.DBCTL	0	0	✔
target_ePWM7_temp.TZCTL	4095	4095	✔
target_ePWM7_temp.ETSEL	0	0	✔
target_ePWM7_temp.PCCTL	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 1.7 (Repeat Count = 1) ✔

Name	Input Value
ePWM1_temp	target_ePWM1_temp
ePWM2_temp	target_ePWM2_temp
ePWM3_temp	target_ePWM3_temp
ePWM4_temp	target_ePWM4_temp
ePWM7_temp	target_ePWM7_temp
k_PwmDeadBand_Cnt_u16	66
k_PwmRelay_Cnt_u16	65535
target_ePWM1_temp.DBCTL	11
target_ePWM2_temp.DBCTL	11
target_ePWM3_temp.DBCTL	11

Name	Actual Value	Expected Value	Result
target_ePWM1_temp.TBCTL	8196	8196	✔
target_ePWM1_temp.TBPHS	0	0	✔
target_ePWM1_temp.TBPRD	65535	65535	✔
target_ePWM1_temp.CMPCTL	0	0	✔
target_ePWM1_temp.CMPA	2499	2499	✔
target_ePWM1_temp.AQCTLA	289	289	✔
target_ePWM1_temp.CMPB	2499	2499	✔
target_ePWM1_temp.DBCTL	8	8	✔
target_ePWM1_temp.AQCSFRC	5	5	✔
target_ePWM1_temp.DBFED	66	66	✔
target_ePWM1_temp.DBRED	66	66	✔
target_ePWM1_temp.TZCTL	4095	4095	✔
target_ePWM1_temp.ETSEL	0	0	✔
target_ePWM1_temp.PCCTL	0	0	✔
target_ePWM2_temp.TBCTL	8196	8196	✔
target_ePWM2_temp.TBPHS	0	0	✔
target_ePWM2_temp.TBPRD	65535	65535	✔
target_ePWM2_temp.CMPCTL	0	0	✔
target_ePWM2_temp.CMPA	2499	2499	✔
target_ePWM2_temp.AQCTLA	288	288	✔
target_ePWM2_temp.CMPB	2499	2499	✔
target_ePWM2_temp.DBCTL	8	8	✔
target_ePWM2_temp.AQCSFRC	5	5	✔
target_ePWM2_temp.DBFED	66	66	✔
target_ePWM2_temp.DBRED	66	66	✔
target_ePWM2_temp.TZCTL	4095	4095	✔
target_ePWM2_temp.ETSEL	0	0	✔
target_ePWM2_temp.PCCTL	0	0	✔
target_ePWM3_temp.TBCTL	8196	8196	✔
target_ePWM3_temp.TBPHS	0	0	✔
target_ePWM3_temp.TBPRD	65535	65535	✔
target_ePWM3_temp.CMPCTL	0	0	✔
target_ePWM3_temp.CMPA	2499	2499	✔
target_ePWM3_temp.AQCTLA	288	288	✔
target_ePWM3_temp.CMPB	2499	2499	✔
target_ePWM3_temp.DBCTL	8	8	✔
target_ePWM3_temp.AQCSFRC	5	5	✔
target_ePWM3_temp.DBFED	66	66	✔
target_ePWM3_temp.DBRED	66	66	✔
target_ePWM3_temp.TZCTL	4095	4095	✔
target_ePWM3_temp.ETSEL	0	0	✔

Name	Actual Value	Expected Value	Result
target_ePWM3_temp.PCCTL	0	0	✔
target_ePWM4_temp.TBCTL	4	4	✔
target_ePWM4_temp.TBPHS	0	0	✔
target_ePWM4_temp.TBPRD	65535	65535	✔
target_ePWM4_temp.CMPCTL	0	0	✔
target_ePWM4_temp.CMPA	2499	2499	✔
target_ePWM4_temp.AQCTLA	0	0	✔
target_ePWM4_temp.CMPB	65535	65535	✔
target_ePWM4_temp.DBCTL	0	0	✔
target_ePWM4_temp.TZCTL	4095	4095	✔
target_ePWM4_temp.ETSEL	60416	60416	✔
target_ePWM4_temp.ETPS	4352	4352	✔
target_ePWM4_temp.PCCTL	0	0	✔
target_ePWM7_temp.TBCTL	4	4	✔
target_ePWM7_temp.TBPHS	0	0	✔
target_ePWM7_temp.TBPRD	65535	65535	✔
target_ePWM7_temp.CMPCTL	0	0	✔
target_ePWM7_temp.CMPA	65535	65535	✔
target_ePWM7_temp.AQCTLB	33	33	✔
target_ePWM7_temp.DBCTL	0	0	✔
target_ePWM7_temp.TZCTL	4095	4095	✔
target_ePWM7_temp.ETSEL	0	0	✔
target_ePWM7_temp.PCCTL	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 1.8 (Repeat Count = 1) ✔

Name	Input Value
ePWM1_temp	target_ePWM1_temp
ePWM2_temp	target_ePWM2_temp
ePWM3_temp	target_ePWM3_temp
ePWM4_temp	target_ePWM4_temp
ePWM7_temp	target_ePWM7_temp
k_PwmDeadBand_Cnt_u16	485
k_PwmRelay_Cnt_u16	2500
target_ePWM1_temp.DBCTL	11
target_ePWM2_temp.DBCTL	11
target_ePWM3_temp.DBCTL	11

Name	Actual Value	Expected Value	Result
target_ePWM1_temp.TBCTL	8196	8196	✔
target_ePWM1_temp.TBPHS	0	0	✔
target_ePWM1_temp.TBPRD	65535	65535	✔
target_ePWM1_temp.CMPCTL	0	0	✔
target_ePWM1_temp.CMPA	2499	2499	✔
target_ePWM1_temp.AQCTLA	289	289	✔
target_ePWM1_temp.CMPB	2499	2499	✔
target_ePWM1_temp.DBCTL	8	8	✔
target_ePWM1_temp.AQCSFRC	5	5	✔
target_ePWM1_temp.DBFED	485	485	✔
target_ePWM1_temp.DBRED	485	485	✔
target_ePWM1_temp.TZCTL	4095	4095	✔
target_ePWM1_temp.ETSEL	0	0	✔
target_ePWM1_temp.PCCTL	0	0	✔
target_ePWM2_temp.TBCTL	8196	8196	✔
target_ePWM2_temp.TBPHS	0	0	✔
target_ePWM2_temp.TBPRD	65535	65535	✔
target_ePWM2_temp.CMPCTL	0	0	✔
target_ePWM2_temp.CMPA	2499	2499	✔
target_ePWM2_temp.AQCTLA	288	288	✔
target_ePWM2_temp.CMPB	2499	2499	✔
target_ePWM2_temp.DBCTL	8	8	✔
target_ePWM2_temp.AQCSFRC	5	5	✔
target_ePWM2_temp.DBFED	485	485	✔
target_ePWM2_temp.DBRED	485	485	✔
target_ePWM2_temp.TZCTL	4095	4095	✔
target_ePWM2_temp.ETSEL	0	0	✔
target_ePWM2_temp.PCCTL	0	0	✔
target_ePWM3_temp.TBCTL	8196	8196	✔

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Name	Actual Value	Expected Value	Result
target_ePWM3_temp.TBPHS	0	0	✔
target_ePWM3_temp.TBPRD	65535	65535	✔
target_ePWM3_temp.CMPCTL	0	0	✔
target_ePWM3_temp.CMPA	2499	2499	✔
target_ePWM3_temp.AQCTLA	288	288	✔
target_ePWM3_temp.CMPB	2499	2499	✔
target_ePWM3_temp.DBCTL	8	8	✔
target_ePWM3_temp.AQCSFRC	5	5	✔
target_ePWM3_temp.DBFED	485	485	✔
target_ePWM3_temp.DBRED	485	485	✔
target_ePWM3_temp.TZCTL	4095	4095	✔
target_ePWM3_temp.ETSEL	0	0	✔
target_ePWM3_temp.PCCTL	0	0	✔
target_ePWM4_temp.TBCTL	4	4	✔
target_ePWM4_temp.TBPHS	0	0	✔
target_ePWM4_temp.TBPRD	65535	65535	✔
target_ePWM4_temp.CMPCTL	0	0	✔
target_ePWM4_temp.CMPA	2499	2499	✔
target_ePWM4_temp.AQCTLA	0	0	✔
target_ePWM4_temp.CMPB	65535	65535	✔
target_ePWM4_temp.DBCTL	0	0	✔
target_ePWM4_temp.TZCTL	4095	4095	✔
target_ePWM4_temp.ETSEL	60416	60416	✔
target_ePWM4_temp.ETPS	4352	4352	✔
target_ePWM4_temp.PCCTL	0	0	✔
target_ePWM7_temp.TBCTL	4	4	✔
target_ePWM7_temp.TBPHS	0	0	✔
target_ePWM7_temp.TBPRD	65535	65535	✔
target_ePWM7_temp.CMPCTL	0	0	✔
target_ePWM7_temp.CMPA	2500	2500	✔
target_ePWM7_temp.AQCTLB	33	33	✔
target_ePWM7_temp.DBCTL	0	0	✔
target_ePWM7_temp.TZCTL	4095	4095	✔
target_ePWM7_temp.ETSEL	0	0	✔
target_ePWM7_temp.PCCTL	0	0	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
none	0	*** No Call Expected ***	0	✔

TEST DETAILS REPORT

ePWM_Per1

2015-11-06, 13:14:20+0530

Project	Ap_ePWM_1
Module	ePWM_1
Test Object	ePWM_Per1

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MCC Coverage	100 %
MC/DC Coverage	100 %

Statistics

Total Testcases	3
Successful	3
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\9BXX_ePWM_Up
Configuration File	D:\Synergy_Work_Area\9BXX_ePWM_Up\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\ePWM_Up\src\ePWM.c
Compiler Options	-DSTATIC= -D_DATA_ACCESS= -D__inline= -Dconst= -I$(PROJECTROOT)\ePWM_Up\utp\contract\Ap_ePWM2 -I$(PROJECTROOT)\ePWM_Up\utp\contract -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef\include -I$(PROJECTROOT)\ePWM_Up\include -I$(Compiler Install Path)\include

Comments/Description/Specification

Name	Text
Module 'ePWM_1'	********** UNIT TEST DESCRIPTION********** Name of Tester:Jayesh Jahagirdar Code File(s) Under Test:ePWM.c Code File(s) Version:2 Module Design Document:ePWM MDD.docx Module Design Document Version:2 Data Dictionary Version:2 Unit Test Plan Version:1 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.32 Total FLASH Used (Bytes):564 Total RAM Used (Bytes):28 Total CALS Used (Bytes):6 Special Test Requirements: Test Date:11-06-2015 Comments:""NOTE1: Inline function defined in ""GlobalMacro.h"" are not unit tested. NOTE2: ""CBD_Sandbox_dbg.map"" map file is embedded for reference." **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(ProgramFiles)\pls\UDE 4.0
Timer Enabled	false
Timer Prescale	0

Attributes

Name	Value
Timer Resolution	1
Timer Unit	Cycles
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\9BXX_ePWM_Up\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Metrices Test

Specification

```
Performance metrics
(With "None" Instrumentation and
"WithPS" environment)

TS 1.1 107.00 Cycles
TS 1.2 107.00 Cycles
```

Description

Vector Description:

TS1.1"Shortest Execution Path:
(CmpAPhaseA_Cnt_T_u16 > 535U)=True
(CmpBPhaseA_Cnt_T_u16 > (PWMPeriod_Cnt_T_u16 - 1U))=False
(CmpAPhaseB_Cnt_T_u16 > 535U)=True
(CmpBPhaseB_Cnt_T_u16 > (PWMPeriod_Cnt_T_u16 - 1U))=False
(CmpAPhaseC_Cnt_T_u16 > 535U)=True
(CmpBPhaseC_Cnt_T_u16 > (PWMPeriod_Cnt_T_u16 - 1U))=False"
TS1.2"Longest Execution Path:
(CmpAPhaseA_Cnt_T_u16 > 535U)=False
(CmpBPhaseA_Cnt_T_u16 > (PWMPeriod_Cnt_T_u16 - 1U))=True
(CmpAPhaseB_Cnt_T_u16 > 535U)=False
(CmpBPhaseB_Cnt_T_u16 > (PWMPeriod_Cnt_T_u16 - 1U))=True
(CmpAPhaseC_Cnt_T_u16 > 535U)=True
(CmpBPhaseC_Cnt_T_u16 > (PWMPeriod_Cnt_T_u16 - 1U))=True"

Test Step 1.1 (Repeat Count = 1)

Name	Input Value
DummyVar4BIn	0
DummyVarDCA	0
DummyVarDCB	0
DummyVarDCC	0
DummyVarPeriodIn	3632
k_ADCTrig1Offset_Cnt_s16	0

Name	Actual Value	Expected Value	Result
DummyVar1A	1281	1281	✔
DummyVar1B	1281	1281	✔
DummyVar2A	1281	1281	✔
DummyVar2B	1281	1281	✔
DummyVar3A	1281	1281	✔
DummyVar3B	1281	1281	✔
DummyVar4A	1281	1281	✔
DummyVar4B	0	0	✔

T

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 1.2 (Repeat Count = 1)

Name	Input Value
DummyVar4BIn	6000
DummyVarDCA	6000
DummyVarDCB	6000
DummyVarDCC	6000
DummyVarPeriodIn	6000
k_ADCTrig1Offset_Cnt_s16	1000

Name	Actual Value	Expected Value	Result
DummyVar1A	1	1	✔
DummyVar1B	5999	5999	✔
DummyVar2A	1	1	✔
DummyVar2B	5999	5999	✔
DummyVar3A	1	1	✔
DummyVar3B	5999	5999	✔
DummyVar4A	1465	1465	✔
DummyVar4B	6000	6000	✔

T

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Case 2: Boundary Test

Specification

```
Performance metrics
(With "None" Instrumentation and
"WithPS" environment)

TS 2.1  107.00 Cycles
TS 2.2  107.00 Cycles
TS 2.3  107.00 Cycles
TS 2.4  107.00 Cycles
TS 2.5  107.00 Cycles
TS 2.6  107.00 Cycles
TS 2.7  107.00 Cycles
TS 2.8  107.00 Cycles
TS 2.9        107.00 Cycles
TS 2.1        107.00 Cycles
TS 2.11 107.00 Cycles
TS 2.12 107.00 Cycles
TS 2.13 107.00 Cycles
TS 2.14 107.00 Cycles
TS 2.15 107.00 Cycles
TS 2.16 107.00 Cycles
TS 2.17 107.00 Cycles
TS 2.18 107.00 Cycles
TS 2.19 107.00 Cycles
TS 2.20       107.00 Cycles
TS 2.21 107.00 Cycles
```

Description

Vector Description:

TS2.1All min
TS2.2All max
TS2.3PWMPeriod_u16==>Min
TS2.4PWMPeriod_u16==>Max
TS2.5PWMPeriod_u16==>Pos
TS2.6DCPhsAComp_u16==>Min
TS2.7DCPhsAComp_u16==>Max
TS2.8DCPhsAComp_u16==>Pos
TS2.9DCPhsBComp_u16==>Min
TS2.10DCPhsBComp_u16==>Max
TS2.11DCPhsBComp_u16==>Pos
TS2.12DCPhsCComp_u16==>Min
TS2.13DCPhsCComp_u16==>Max
TS2.14DCPhsCComp_u16==>Pos
TS2.15ePWM4CMPB_Cnt_u16==>Min
TS2.16ePWM4CMPB_Cnt_u16==>Max
TS2.17ePWM4CMPB_Cnt_u16==>Pos
TS2.18k_ADCTrig1Offset_Cnt_s16==>Min
TS2.19k_ADCTrig1Offset_Cnt_s16==>Max
TS2.20k_ADCTrig1Offset_Cnt_s16==>Pos
TS2.21k_ADCTrig1Offset_Cnt_s16==>Def

Test Step 2.1 (Repeat Count = 1)

Name	Input Value
DummyVar4BIn	0
DummyVarDCA	0
DummyVarDCB	0
DummyVarDCC	0
DummyVarPeriodIn	3632
k_ADCTrig1Offset_Cnt_s16	0

Name	Actual Value	Expected Value	Result
DummyVar1A	1281	1281	✔
DummyVar1B	1281	1281	✔
DummyVar2A	1281	1281	✔
DummyVar2B	1281	1281	✔
DummyVar3A	1281	1281	✔
DummyVar3B	1281	1281	✔
DummyVar4A	1281	1281	✔
DummyVar4B	0	0	✔

T

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.2 (Repeat Count = 1)

Name	Input Value
DummyVar4BIn	6000
DummyVarDCA	6000
DummyVarDCB	6000
DummyVarDCC	6000
DummyVarPeriodIn	6000
k_ADCTrig1Offset_Cnt_s16	1000

Name	Actual Value	Expected Value	Result
DummyVar1A	1	1	✔

Name	Actual Value	Expected Value	Result
DummyVar1B	5999	5999	✔
DummyVar2A	1	1	✔
DummyVar2B	5999	5999	✔
DummyVar3A	1	1	✔
DummyVar3B	5999	5999	✔
DummyVar4A	1465	1465	✔
DummyVar4B	6000	6000	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
none	0	*** No Call Expected ***	0	✔

Test Step 2.3 (Repeat Count = 1) ✔

Name	Input Value
DummyVar4BIn	4948
DummyVarDCA	2663
DummyVarDCB	4707
DummyVarDCC	5777
DummyVarPeriodIn	3632
k_ADCTrig1Offset_Cnt_s16	645

Name	Actual Value	Expected Value	Result
DummyVar1A	1	1	✔
DummyVar1B	2664	2664	✔
DummyVar2A	64463	64463	✔
DummyVar2B	3631	3631	✔
DummyVar3A	63928	63928	✔
DummyVar3B	3631	3631	✔
DummyVar4A	636	636	✔
DummyVar4B	4948	4948	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
none	0	*** No Call Expected ***	0	✔

Test Step 2.4 (Repeat Count = 1) ✔

Name	Input Value
DummyVar4BIn	4313
DummyVarDCA	1637
DummyVarDCB	301
DummyVarDCC	5599
DummyVarPeriodIn	6000
k_ADCTrig1Offset_Cnt_s16	982

Name	Actual Value	Expected Value	Result
DummyVar1A	1646	1646	✔
DummyVar1B	3283	3283	✔
DummyVar2A	2314	2314	✔
DummyVar2B	2615	2615	✔
DummyVar3A	1	1	✔
DummyVar3B	5600	5600	✔
DummyVar4A	1483	1483	✔
DummyVar4B	4313	4313	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
none	0	*** No Call Expected ***	0	✔

Test Step 2.5 (Repeat Count = 1) ✔

Name	Input Value
DummyVar4BIn	5376
DummyVarDCA	5236
DummyVarDCB	3108
DummyVarDCC	5956
DummyVarPeriodIn	3632

Name	Input Value
k_ADCTrig1Offset_Cnt_s16	312

Name	Actual Value	Expected Value	Result
DummyVar1A	64199	64199	✔
DummyVar1B	3631	3631	✔
DummyVar2A	1	1	✔
DummyVar2B	3109	3109	✔
DummyVar3A	63839	63839	✔
DummyVar3B	3631	3631	✔
DummyVar4A	969	969	✔
DummyVar4B	5376	5376	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.6 (Repeat Count = 1) ✔

Name	Input Value
DummyVar4BIn	1335
DummyVarDCA	0
DummyVarDCB	4542
DummyVarDCC	5038
DummyVarPeriodIn	4317
k_ADCTrig1Offset_Cnt_s16	240

Name	Actual Value	Expected Value	Result
DummyVar1A	1623	1623	✔
DummyVar1B	1623	1623	✔
DummyVar2A	64888	64888	✔
DummyVar2B	3894	3894	✔
DummyVar3A	64640	64640	✔
DummyVar3B	4142	4142	✔
DummyVar4A	1383	1383	✔
DummyVar4B	1335	1335	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.7 (Repeat Count = 1) ✔

Name	Input Value
DummyVar4BIn	2136
DummyVarDCA	6000
DummyVarDCB	4804
DummyVarDCC	2456
DummyVarPeriodIn	4347
k_ADCTrig1Offset_Cnt_s16	879

Name	Actual Value	Expected Value	Result
DummyVar1A	64174	64174	✔
DummyVar1B	4346	4346	✔
DummyVar2A	64772	64772	✔
DummyVar2B	4040	4040	✔
DummyVar3A	410	410	✔
DummyVar3B	2866	2866	✔
DummyVar4A	759	759	✔
DummyVar4B	2136	2136	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.8 (Repeat Count = 1) ✔

Name	Input Value
DummyVar4BIn	3320
DummyVarDCA	5878

Name	Input Value
DummyVarDCB	1951
DummyVarDCC	4832
DummyVarPeriodIn	5467
k_ADCTrig1Offset_Cnt_s16	129

Name	Actual Value	Expected Value	Result
DummyVar1A	64795	64795	✔
DummyVar1B	5137	5137	✔
DummyVar2A	1223	1223	✔
DummyVar2B	3174	3174	✔
DummyVar3A	1	1	✔
DummyVar3B	4833	4833	✔
DummyVar4A	2069	2069	✔
DummyVar4B	3320	3320	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.9 (Repeat Count = 1) ✔

Name	Input Value
DummyVar4BIn	2133
DummyVarDCA	1540
DummyVarDCB	0
DummyVarDCC	5937
DummyVarPeriodIn	3665
k_ADCTrig1Offset_Cnt_s16	570

Name	Actual Value	Expected Value	Result
DummyVar1A	527	527	✔
DummyVar1B	2067	2067	✔
DummyVar2A	1297	1297	✔
DummyVar2B	1297	1297	✔
DummyVar3A	63865	63865	✔
DummyVar3B	3664	3664	✔
DummyVar4A	727	727	✔
DummyVar4B	2133	2133	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.10 (Repeat Count = 1) ✔

Name	Input Value
DummyVar4BIn	1226
DummyVarDCA	539
DummyVarDCB	6000
DummyVarDCC	1550
DummyVarPeriodIn	5434
k_ADCTrig1Offset_Cnt_s16	607

Name	Actual Value	Expected Value	Result
DummyVar1A	1912	1912	✔
DummyVar1B	2451	2451	✔
DummyVar2A	64718	64718	✔
DummyVar2B	5182	5182	✔
DummyVar3A	1407	1407	✔
DummyVar3B	2957	2957	✔
DummyVar4A	1575	1575	✔
DummyVar4B	1226	1226	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.11 (Repeat Count = 1)

Name	Input Value
DummyVar4BIn	3474
DummyVarDCA	185
DummyVarDCB	3474
DummyVarDCC	1047
DummyVarPeriodIn	5561
k_ADCTrig1Offset_Cnt_s16	610

Name	Actual Value	Expected Value	Result
DummyVar1A	2153	2153	✔
DummyVar1B	2338	2338	✔
DummyVar2A	508	508	✔
DummyVar2B	3982	3982	✔
DummyVar3A	1722	1722	✔
DummyVar3B	2769	2769	✔
DummyVar4A	1635	1635	✔
DummyVar4B	3474	3474	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.12 (Repeat Count = 1)

Name	Input Value
DummyVar4BIn	3780
DummyVarDCA	1936
DummyVarDCB	5431
DummyVarDCC	0
DummyVarPeriodIn	5311
k_ADCTrig1Offset_Cnt_s16	694

Name	Actual Value	Expected Value	Result
DummyVar1A	1152	1152	✔
DummyVar1B	3088	3088	✔
DummyVar2A	64941	64941	✔
DummyVar2B	4836	4836	✔
DummyVar3A	2120	2120	✔
DummyVar3B	2120	2120	✔
DummyVar4A	1426	1426	✔
DummyVar4B	3780	3780	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.13 (Repeat Count = 1)

Name	Input Value
DummyVar4BIn	836
DummyVarDCA	4741
DummyVarDCB	5255
DummyVarDCC	6000
DummyVarPeriodIn	3739
k_ADCTrig1Offset_Cnt_s16	850

Name	Actual Value	Expected Value	Result
DummyVar1A	64500	64500	✔
DummyVar1B	3705	3705	✔
DummyVar2A	64243	64243	✔
DummyVar2B	3738	3738	✔
DummyVar3A	63870	63870	✔
DummyVar3B	3738	3738	✔
DummyVar4A	484	484	✔
DummyVar4B	836	836	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.14 (Repeat Count = 1) ✔

Name	Input Value
DummyVar4BIn	365
DummyVarDCA	1783
DummyVarDCB	2500
DummyVarDCC	3160
DummyVarPeriodIn	4612
k_ADCTrig1Offset_Cnt_s16	97

Name	Actual Value	Expected Value	Result
DummyVar1A	879	879	✔
DummyVar1B	2662	2662	✔
DummyVar2A	521	521	✔
DummyVar2B	3021	3021	✔
DummyVar3A	191	191	✔
DummyVar3B	3351	3351	✔
DummyVar4A	1674	1674	✔
DummyVar4B	365	365	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.15 (Repeat Count = 1) ✔

Name	Input Value
DummyVar4BIn	0
DummyVarDCA	1411
DummyVarDCB	738
DummyVarDCC	4155
DummyVarPeriodIn	5675
k_ADCTrig1Offset_Cnt_s16	394

Name	Actual Value	Expected Value	Result
DummyVar1A	1597	1597	✔
DummyVar1B	3008	3008	✔
DummyVar2A	1933	1933	✔
DummyVar2B	2671	2671	✔
DummyVar3A	225	225	✔
DummyVar3B	4380	4380	✔
DummyVar4A	1908	1908	✔
DummyVar4B	0	0	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.16 (Repeat Count = 1) ✔

Name	Input Value
DummyVar4BIn	6000
DummyVarDCA	2883
DummyVarDCB	5725
DummyVarDCC	662
DummyVarPeriodIn	5504
k_ADCTrig1Offset_Cnt_s16	823

Name	Actual Value	Expected Value	Result
DummyVar1A	775	775	✔
DummyVar1B	3658	3658	✔
DummyVar2A	64890	64890	✔
DummyVar2B	5079	5079	✔
DummyVar3A	1886	1886	✔
DummyVar3B	2548	2548	✔
DummyVar4A	1394	1394	✔
DummyVar4B	6000	6000	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
none	0	*** No Call Expected ***	0	✔

Test Step 2.17 (Repeat Count = 1) ✔

Name	Input Value
DummyVar4BIn	804
DummyVarDCA	1527
DummyVarDCB	4784
DummyVarDCC	658
DummyVarPeriodIn	4516
k_ADCTrig1Offset_Cnt_s16	268

Name	Actual Value	Expected Value	Result
DummyVar1A	959	959	✔
DummyVar1B	2486	2486	✔
DummyVar2A	64867	64867	✔
DummyVar2B	4115	4115	✔
DummyVar3A	1394	1394	✔
DummyVar3B	2052	2052	✔
DummyVar4A	1455	1455	✔
DummyVar4B	804	804	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
none	0	*** No Call Expected ***	0	✔

Test Step 2.18 (Repeat Count = 1) ✔

Name	Input Value
DummyVar4BIn	2549
DummyVarDCA	2043
DummyVarDCB	4178
DummyVarDCC	1743
DummyVarPeriodIn	5910
k_ADCTrig1Offset_Cnt_s16	0

Name	Actual Value	Expected Value	Result
DummyVar1A	1398	1398	✔
DummyVar1B	3441	3441	✔
DummyVar2A	331	331	✔
DummyVar2B	4509	4509	✔
DummyVar3A	1548	1548	✔
DummyVar3B	3291	3291	✔
DummyVar4A	2420	2420	✔
DummyVar4B	2549	2549	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
none	0	*** No Call Expected ***	0	✔

Test Step 2.19 (Repeat Count = 1) ✔

Name	Input Value
DummyVar4BIn	1122
DummyVarDCA	269
DummyVarDCB	2410
DummyVarDCC	2393
DummyVarPeriodIn	5696
k_ADCTrig1Offset_Cnt_s16	1000

Name	Actual Value	Expected Value	Result
DummyVar1A	2178	2178	✔
DummyVar1B	2447	2447	✔
DummyVar2A	1108	1108	✔
DummyVar2B	3518	3518	✔
DummyVar3A	1116	1116	✔
DummyVar3B	3509	3509	✔

Name	Actual Value	Expected Value	Result
DummyVar4A	1313	1313	✔
DummyVar4B	1122	1122	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.20 (Repeat Count = 1) ✔

Name	Input Value
DummyVar4BIn	2973
DummyVarDCA	2895
DummyVarDCB	97
DummyVarDCC	3354
DummyVarPeriodIn	3765
k_ADCTrig1Offset_Cnt_s16	899

Name	Actual Value	Expected Value	Result
DummyVar1A	1	1	✔
DummyVar1B	2896	2896	✔
DummyVar2A	1299	1299	✔
DummyVar2B	1396	1396	✔
DummyVar3A	1	1	✔
DummyVar3B	3355	3355	✔
DummyVar4A	448	448	✔
DummyVar4B	2973	2973	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.21 (Repeat Count = 1) ✔

Name	Input Value
DummyVar4BIn	2973
DummyVarDCA	2895
DummyVarDCB	97
DummyVarDCC	3354
DummyVarPeriodIn	3765
k_ADCTrig1Offset_Cnt_s16	15

Name	Actual Value	Expected Value	Result
DummyVar1A	1	1	✔
DummyVar1B	2896	2896	✔
DummyVar2A	1299	1299	✔
DummyVar2B	1396	1396	✔
DummyVar3A	1	1	✔
DummyVar3B	3355	3355	✔
DummyVar4A	1332	1332	✔
DummyVar4B	2973	2973	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Case 3: Path Test

Specification

```
Performance metrics
(With "None" Instrumentation and
"WithPS" environment)

TS 3.1 107.00 Cycles
TS 3.2 107.00 Cycles
```

Description

Vector Description:

TS3.1"
(CmpAPhaseA_Cnt_T_u16 > 535U)=True,
(CmpBPhaseA_Cnt_T_u16 > (PWMPeriod_Cnt_T_u16 - 1U))=False,
(CmpAPhaseB_Cnt_T_u16 > 535U)=True,
(CmpBPhaseB_Cnt_T_u16 > (PWMPeriod_Cnt_T_u16 - 1U))=False,
(CmpAPhaseC_Cnt_T_u16 > 535U)=True,
(CmpBPhaseC_Cnt_T_u16 > (PWMPeriod_Cnt_T_u16 - 1U))=False,"
TS3.2"
(CmpAPhaseA_Cnt_T_u16 > 535U)=False,
(CmpBPhaseA_Cnt_T_u16 > (PWMPeriod_Cnt_T_u16 - 1U))=True,
(CmpAPhaseB_Cnt_T_u16 > 535U)=False,
(CmpBPhaseB_Cnt_T_u16 > (PWMPeriod_Cnt_T_u16 - 1U))=True,
(CmpAPhaseC_Cnt_T_u16 > 535U)=False,
(CmpBPhaseC_Cnt_T_u16 > (PWMPeriod_Cnt_T_u16 - 1U))=True,"

Test Step 3.1 (Repeat Count = 1)

Name	Input Value
DummyVar4BIn	0
DummyVarDCA	0
DummyVarDCB	0
DummyVarDCC	0
DummyVarPeriodIn	3632
k_ADCTrig1Offset_Cnt_s16	0

Name	Actual Value	Expected Value	Result
DummyVar1A	1281	1281	✔
DummyVar1B	1281	1281	✔
DummyVar2A	1281	1281	✔
DummyVar2B	1281	1281	✔
DummyVar3A	1281	1281	✔
DummyVar3B	1281	1281	✔
DummyVar4A	1281	1281	✔
DummyVar4B	0	0	✔

T

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 3.2 (Repeat Count = 1)

Name	Input Value
DummyVar4BIn	6000
DummyVarDCA	6000
DummyVarDCB	6000
DummyVarDCC	6000
DummyVarPeriodIn	6000
k_ADCTrig1Offset_Cnt_s16	1000

Name	Actual Value	Expected Value	Result
DummyVar1A	1	1	✔
DummyVar1B	5999	5999	✔
DummyVar2A	1	1	✔
DummyVar2B	5999	5999	✔
DummyVar3A	1	1	✔
DummyVar3B	5999	5999	✔
DummyVar4A	1465	1465	✔
DummyVar4B	6000	6000	✔

T

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔