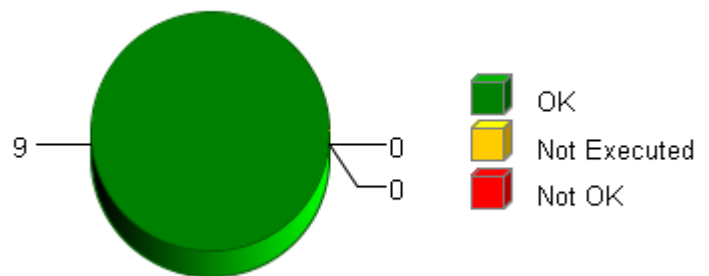


Summary

Total Test Objects: 9
Successful: 9
Failed: 0
Not Executed: 0
Date: 2016-10-26
Time: 20:05:15+0530

Overall Test Object Results (including Coverage)



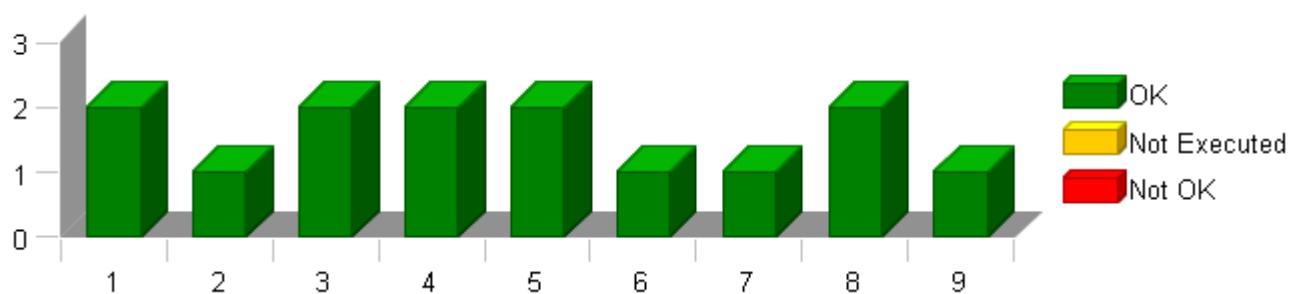
Selected Project Items

Test Object "CBD_UnitTest/HwTqArbn/ArbnSigAvlChk"
Test Object "CBD_UnitTest/HwTqArbn/HwTqArbn_Init1"
Test Object "CBD_UnitTest/HwTqArbn/HwTqArbn_Per1"
Test Object "CBD_UnitTest/HwTqArbn/HwTqArbn_Per2"
Test Object "CBD_UnitTest/HwTqArbn/HwTqArbn_Per3"
Test Object "CBD_UnitTest/HwTqArbn/HwTrqArbn_SCom_ClrHwTrqArbOffsetTrim"
Test Object "CBD_UnitTest/HwTqArbn/HwTrqArbn_SCom_ReadHwTrqArbOffsetTrim"
Test Object "CBD_UnitTest/HwTqArbn/HwTrqArbn_SCom_SetHwTrqArbOffsetTrim"
Test Object "CBD_UnitTest/HwTqArbn/HwTrqArbn_SCom_WriteHwTrqArbOffsetTrim"

Used Test Environments

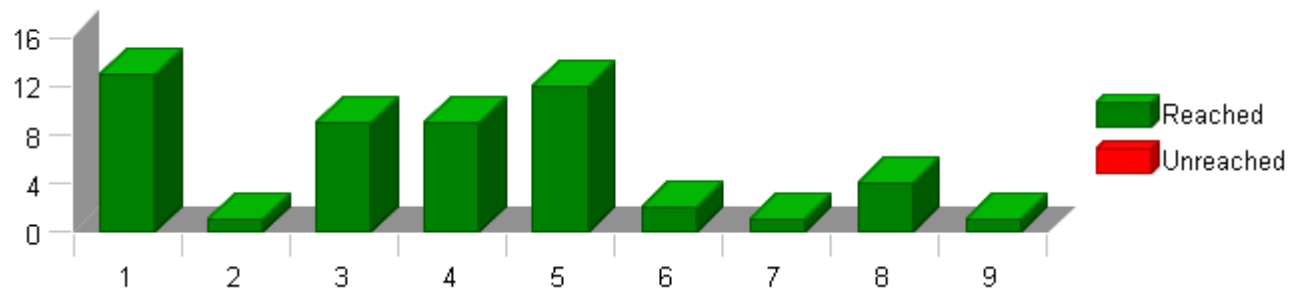
TI TMS 570 PLS UDE (Default)

Test Case Results for Each Test Object (without Coverage)



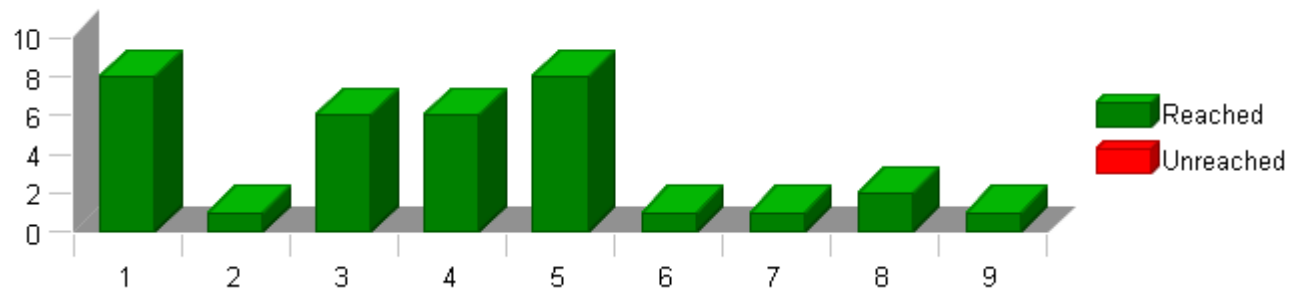
The table above shows each test object on the x axis and the number of test cases of the respective test object on the y axis. Each bar is divided into passed, not executed and failed test cases. The test case results do not take into account any coverage result (i.e. if all test cases of a test object are passed in this table but the coverage is failed, the overall test object result will be failed).

Statement (C0) Coverage: Total Statements for Each Test Object



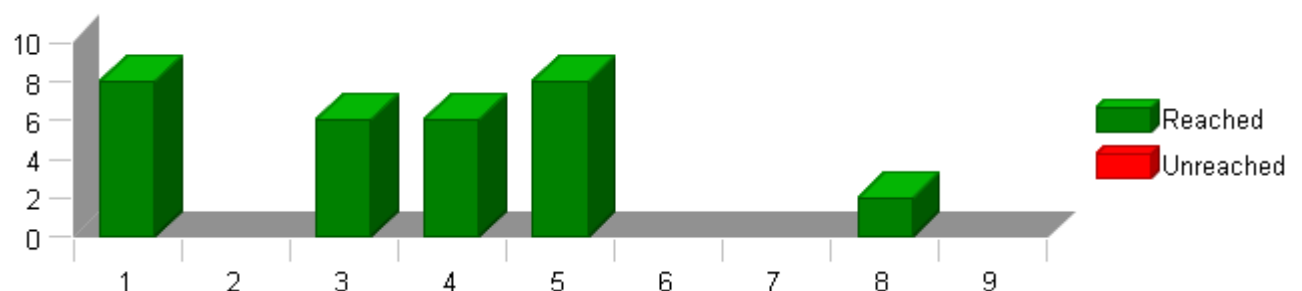
The table above shows each test object on the x axis and the number of statements of the respective test object on the y axis. Each bar is divided into reached statements (i.e. statements that have been executed during the test) and unreached statements.

Branch (C1) Coverage: Total Branches for Each Test Object



The table above shows each test object on the x axis and the number of branches of the respective test object on the y axis. Each bar is divided into reached branches (i.e. branches that have been executed during the test) and unreached branches.

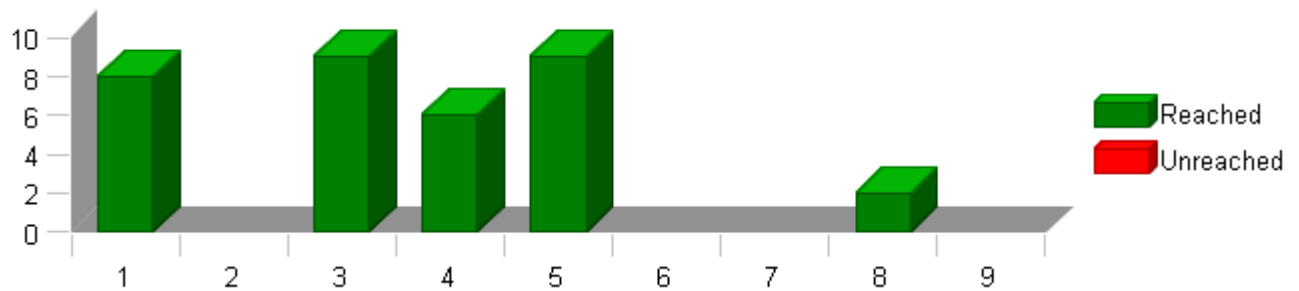
Decision Coverage: Total Decision Outcomes for Each Test Object



The table above shows test objects on the x axis and the number of possible outcomes of all decisions of the respective test object on the y axis. To achieve full DC coverage, each decision must evaluate to both true and false.

Each bar is divided into reached and unreached decision outcomes.

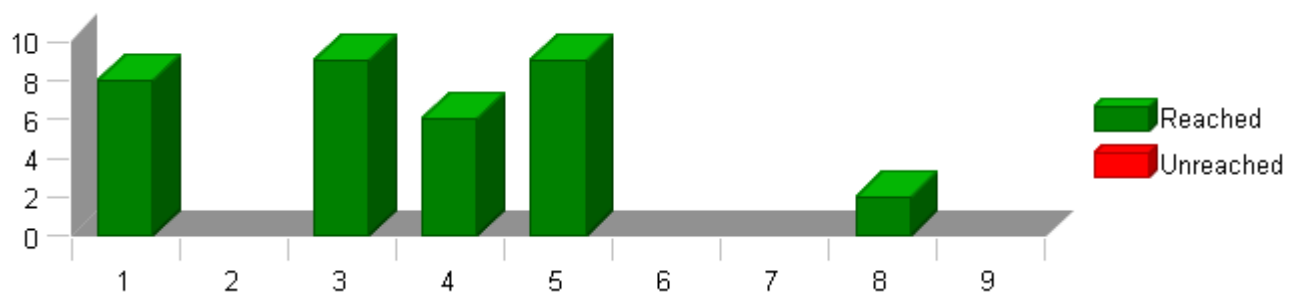
MC/DC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MC/DC coverage, each decision requires all contained atomic conditions to evaluate to both true and false independently of all other conditions. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

MCC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MCC coverage, each decision requires all contained atomic conditions to evaluate to all possible combinations of true and false values. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

Test Object List

The following table lists all test objects with their test case and coverage results. The cumulated results for modules, folders and test collections are also displayed, the indentation within the name column indicates the parent relationship of the elements.

Please note that only test objects are numbered within the first column. This number is referenced on the x axis within the overview charts for test case and coverage results available on previous pages (if included into the report).

No.	Name	C0	C1	DC	MC/DC	MCC	Test Cases	Result
	HwTqArbn	100 %	100 %	100 %	100 %	100 %	14 of 14 passed	✓
	CBD_UnitTest	100 %	100 %	100 %	100 %	100 %	14 of 14 passed	✓
	HwTqArbn	100 %	100 %	100 %	100 %	100 %	14 of 14 passed	✓
1	ArbnSigAvlChk	100 %	100 %	100 %	100 %	100 %	2 of 2 passed	✓
2	HwTqArbn_Init1	100 %	100 %	-	-	-	1 of 1 passed	✓
3	HwTqArbn_Per1	100 %	100 %	100 %	100 %	100 %	2 of 2 passed	✓
4	HwTqArbn_Per2	100 %	100 %	100 %	100 %	100 %	2 of 2 passed	✓
5	HwTqArbn_Per3	100 %	100 %	100 %	100 %	100 %	2 of 2 passed	✓
6	HwTrqArbn_SCom_ClrHwTrqArbOffsetTrim	100 %	100 %	-	-	-	1 of 1 passed	✓
7	HwTrqArbn_SCom_ReadHwTrqArbOffsetTrim	100 %	100 %	-	-	-	1 of 1 passed	✓
8	HwTrqArbn_SCom_SetHwTrqArbOffsetTrim	100 %	100 %	100 %	100 %	100 %	2 of 2 passed	✓
9	HwTrqArbn_SCom_WriteHwTrqArbOffsetTrim	100 %	100 %	-	-	-	1 of 1 passed	✓

TEST DETAILS REPORT

2016-10-26, 20:00:06+0530

HwTrqArbn_SCom_WriteHwTrqArbOffsetTrim



Project	HwTqArbn
Module	HwTqArbn
Test Object	HwTrqArbn_SCom_WriteHwTrqArbOffsetTrim

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

Statistics

Total Testcases	1
Successful	1 ✓
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\HwTqArbn_2TqADAS_
Configuration File	D:\Synergy_Work_Area\HwTqArbn_2TqADAS\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(SOURCEROOT)\Sa_HwTqArbn.c
Compiler Options	-D_DATA_ACCESS=-D_STATIC=-D_inline=-Dconst=-I\$(PROJECTROOT)\Inputs\utp\contract\Sa_HwTqArbn -I\$(PROJECTROOT)\Inputs\utp\contract -I\$(PROJECTROOT)\NxtLib\include -I\$(PROJECTROOT)\StdDef\include -I\$(Compiler Install Path)\include

Comments/Description/Specification

Name	Text
Module 'HwTqArbn'	*****Unit Test Information***** Name of Tester:Ghazala Parvin Ansari Code File(s) Under Test:Sa_HwTqArbn.c Code File(s) Version:3 Module Design Document:HwTqArbn_MDD.doc Module Design Document Version:2 Data Dictionary Version:1 Unit Test Plan Version: 3 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/ EPS Library 1.32 Total FLASH Used (Bytes): 604 Total RAM Used (Bytes): 12 Total CALS Used (Bytes): 4 Special Test Requirements:NA Test Date:10/26/2016 Comments: "NOTE1: Inline functions defined in GlobalMacro.h are not unit tested. NOTE2: "CBD_Sandbox_dbg.map"map file is embedded for reference." *****

Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_PS.tpl
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
Timer Unit	Cycles
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg

TEST DETAILS REPORT

2016-10-26, 20:00:06+0530



HwTrqArbn_SCom_WriteHwTrqArbOffsetTrim

Workspace File

D:\Synergy_Work_Area\HwTqArbn_2TqADAS_\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

TEST DETAILS REPORT

2016-10-26, 20:00:06+0530

HwTrqArbn_SCom_WriteHwTrqArbOffsetTrim



Test Case 1: Range Test

Specification Performance Metrics
(With None Instrumentation and WithPS Environment)

CPU Cycles:

TS1.1 529.00 Cycles
TS1.2 499.00 Cycles
TS1.3 499.00 Cycles
TS1.4 499.00 Cycles
TS1.5 499.00 Cycles

Description Vector Description:

TS1.1HwTqCh1OfstTrmWr_HwNm_f32==>Min
TS1.2HwTqCh1OfstTrmWr_HwNm_f32==>Max
TS1.3HwTqCh1OfstTrmWr_HwNm_f32==>Pos
TS1.4HwTqCh1OfstTrmWr_HwNm_f32==>Zero
TS1.5HwTqCh1OfstTrmWr_HwNm_f32==>Neg

Test Step 1.1 (Repeat Count = 1)

Name	Input Value		
EOLChOffsetTrim_HwNm_f32	-10		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	-10	-10	✓
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	1	1	✓

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Sa_HwTqArbn_HwTqArbnEOLCh1OffsetTrim_WriteBlock	1	Rte_Call_Sa_HwTqArbn_HwTqArbnEOLCh1OffsetTrim_WriteBlock	1	✓

Test Step 1.2 (Repeat Count = 1)

Name	Input Value		
EOLChOffsetTrim_HwNm_f32	10		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	10	10	✓
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	1	1	✓

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Sa_HwTqArbn_HwTqArbnEOLCh1OffsetTrim_WriteBlock	1	Rte_Call_Sa_HwTqArbn_HwTqArbnEOLCh1OffsetTrim_WriteBlock	1	✓

Test Step 1.3 (Repeat Count = 1)

Name	Input Value		
EOLChOffsetTrim_HwNm_f32	6.7658		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	6.7658	6.7658	✓
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	1	1	✓

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Sa_HwTqArbn_HwTqArbnEOLCh1OffsetTrim_WriteBlock	1	Rte_Call_Sa_HwTqArbn_HwTqArbnEOLCh1OffsetTrim_WriteBlock	1	✓

Test Step 1.4 (Repeat Count = 1)

Name	Input Value		
EOLChOffsetTrim_HwNm_f32	0		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	0	0	✓

TEST DETAILS REPORT

2016-10-26, 20:00:06+0530



HwTrqArbn_SCom_WriteHwTrqArbOffsetTrim

Name	Actual Value	Expected Value	Result
target_Pim_HwTrqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	1	1	✓

T					✓
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_Sa_HwTqArbn_HwTqArbnEOLCh1OffsetTrim_WriteBlock	1	Rte_Call_Sa_HwTqArbn_HwTqArbnEOLCh1OffsetTrim_WriteBlock	1		✓

Test Step 1.5 (Repeat Count = 1)					✓
Name	Input Value				
EOLChOffsetTrim_HwNm_f32	-4.751				
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn				
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData				
Name	Actual Value	Expected Value	Result		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	-4.75099993	-4.75099993	✓		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	1	1	✓		

T					✓
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_Sa_HwTqArbn_HwTqArbnEOLCh1OffsetTrim_WriteBlock	1	Rte_Call_Sa_HwTqArbn_HwTqArbnEOLCh1OffsetTrim_WriteBlock	1		✓

TEST DETAILS REPORT



Project	HwTqArbn
Module	HwTqArbn
Test Object	HwTqArbn_Per2

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MCC Coverage	100 %
MC/DC Coverage	100 %

Statistics

Total Testcases	2
Successful	2 ✓
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\HwTqArbn_2TqADAS_
Configuration File	D:\Synergy_Work_Area\HwTqArbn_2TqADAS_\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(SOURCEROOT)\Sa_HwTqArbn.c
Compiler Options	-D_DATA_ACCESS=-D_STATIC=-D_inline=-Dconst=-I\$(PROJECTROOT)\Inputs\utp\contract\Sa_HwTqArbn -I\$(PROJECTROOT)\Inputs\utp\contract -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include -I\$(Compiler Install Path)\include

Comments/Description/Specification

Name	Text
Module 'HwTqArbn'	*****Unit Test Information***** Name of Tester:Ghazala Parvin Ansari Code File(s) Under Test:Sa_HwTqArbn.c Code File(s) Version:3 Module Design Document:HwTqArbn_MDD.doc Module Design Document Version:2 Data Dictionary Version:1 Unit Test Plan Version: 3 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/ EPS Library 1.32 Total FLASH Used (Bytes): 604 Total RAM Used (Bytes): 12 Total CALS Used (Bytes): 4 Special Test Requirements:NA Test Date:10/26/2016 Comments: "NOTE1: Inline functions defined in GlobalMacro.h are not unit tested. NOTE2: ""CBD_Sandbox_dbg.map""map file is embedded for reference." *****

Attributes

Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_PS.tpl
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1

Attributes	
Name	Value
Timer Unit	Cycles
UDE Config File	\${PROJECTROOT}\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\HwTqArbn_2TqADAS_\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Metrics Test

Specification	Performance Metrics (With None Instrumentation and WithPS Environment)
	CPU Cycles:
	TS1.1 70.00 Cycles
	TS1.2 116.00 Cycles
Description	Vector Description:
	TS1.1"Shortest Path: if(HwTqArb_HwTqCh1Avl_Cnt_M_lgc == TRUE)==true HwTqVal_HwNm_T_f32 = Limit_m(HwTqVal_HwNm_T_f32, D_HWTRQMINLMT_HWNM_F32, D_HWTRQMAXLMT_HWNM_F32);==true"
	TS1.2"Longest Path: if(HwTqArb_HwTqCh1Avl_Cnt_M_lgc == TRUE)==false HwTqVal_HwNm_T_f32 = Limit_m(HwTqVal_HwNm_T_f32, D_HWTRQMINLMT_HWNM_F32, D_HWTRQMAXLMT_HWNM_F32);==false HwTqVal_HwNm_T_f32 = Limit_m(HwTqVal_HwNm_T_f32, D_HWTRQMINLMT_HWNM_F32, D_HWTRQMAXLMT_HWNM_F32);==true"

Test Step 1.1 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	1		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	10		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per2_HwTq1Val_HwNm_f32.value	10		
target_HwTqArbn_Per2_HwTq2Val_HwNm_f32.value	10		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	10		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq1Val_HwNm_f32	target_HwTqArbn_Per2_HwTq1Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq2Val_HwNm_f32	target_HwTqArbn_Per2_HwTq2Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTqVal_HwNm_f32	target_HwTqArbn_Per2_HwTqVal_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	10	10 ± 0.005	✓
target_HwTqArbn_Per2_HwTqVal_HwNm_f32.value	0	0 ± 0.005	✓

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 1.2 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	-10		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per2_HwTq1Val_HwNm_f32.value	-10		
target_HwTqArbn_Per2_HwTq2Val_HwNm_f32.value	-10		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	-10		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq1Val_HwNm_f32	target_HwTqArbn_Per2_HwTq1Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq2Val_HwNm_f32	target_HwTqArbn_Per2_HwTq2Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTqVal_HwNm_f32	target_HwTqArbn_Per2_HwTqVal_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	-10	-10 ± 0.005	✓
target_HwTqArbn_Per2_HwTqVal_HwNm_f32.value	0	0 ± 0.005	✓

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓



Test Case 2: Range Test

Specification Performance Metrics
(With None Instrumentation and WithPS Environment)

CPU Cycles:

TS2.1 95.00 Cycles
TS2.2 70.00 Cycles
TS2.3 98.00 Cycles
TS2.4 107.00 Cycles
TS2.5 88.00 Cycles
TS2.6 98.00 Cycles
TS2.7 76.00 Cycles
TS2.8 107.00 Cycles
TS2.9 76.00 Cycles
TS2.10 88.00 Cycles
TS2.11 70.00 Cycles
TS2.12 98.00 Cycles
TS2.13 116.00 Cycles
TS2.14 76.00 Cycles
TS2.15 76.00 Cycles
TS2.16 76.00 Cycles
TS2.17 88.00 Cycles
TS2.18 116.00 Cycles
TS2.19 107.00 Cycles
TS2.20 95.00 Cycles
TS2.21 95.00 Cycles
TS2.22 98.00 Cycles

Description Vector Description:

TS2.1All Min
TS2.2All Max
TS2.3HwTq1Val_HwNm_f32==>Min
TS2.4HwTq1Val_HwNm_f32==>Max
TS2.5HwTq1Val_HwNm_f32==>Pos
TS2.6HwTq1Val_HwNm_f32==>Zero
TS2.7HwTq1Val_HwNm_f32==>Neg
TS2.8HwTq2Val_HwNm_f32==>Min
TS2.9HwTq2Val_HwNm_f32==>Max
TS2.10HwTq2Val_HwNm_f32==>Pos
TS2.11HwTq2Val_HwNm_f32==>Zero
TS2.12HwTq2Val_HwNm_f32==>Neg
TS2.13HwTqArb_HwTqCh1Avl_Cnt_M_lgc==>Min
TS2.14HwTqArb_HwTqCh1Avl_Cnt_M_lgc==>Max
TS2.15HwTqArb_HwTqCh1PrevVal_HwNm_M_f32==>Min
TS2.16HwTqArb_HwTqCh1PrevVal_HwNm_M_f32==>Max
TS2.17HwTqArb_HwTqCh1PrevVal_HwNm_M_f32==>Pos
TS2.18Rte_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm_f32==>Min
TS2.19Rte_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm_f32==>Max
TS2.20Rte_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm_f32==>Pos
TS2.21Rte_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm_f32==>Zero
TS2.22Rte_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm_f32==>Neg

Test Step 2.1 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	-10		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per2_HwTq1Val_HwNm_f32.value	-10		
target_HwTqArbn_Per2_HwTq2Val_HwNm_f32.value	-10		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	-10		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq1Val_HwNm_f32	target_HwTqArbn_Per2_HwTq1Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq2Val_HwNm_f32	target_HwTqArbn_Per2_HwTq2Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTqVal_HwNm_f32	target_HwTqArbn_Per2_HwTqVal_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	-10	-10 ± 0.005	✓
target_HwTqArbn_Per2_HwTqVal_HwNm_f32.value	0	0 ± 0.005	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.2 (Repeat Count = 1)

Name	Input Value
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	1
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	10
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn
target_HwTqArbn_Per2_HwTq1Val_HwNm_f32.value	10
target_HwTqArbn_Per2_HwTq2Val_HwNm_f32.value	10
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	10
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq1Val_HwNm_f32	target_HwTqArbn_Per2_HwTq1Val_HwNm_f32
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq2Val_HwNm_f32	target_HwTqArbn_Per2_HwTq2Val_HwNm_f32

TEST DETAILS REPORT



Name	Input Value		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTqVal_HwNm_f32	target_HwTqArbn_Per2_HwTqVal_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	10	10 ± 0.005	✓
target_HwTqArbn_Per2_HwTqVal_HwNm_f32.value	0	0 ± 0.005	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.3 (Repeat Count = 1) ✓

Name	Input Value		
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	1		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	5.97520018		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per2_HwTq1Val_HwNm_f32.value	-10		
target_HwTqArbn_Per2_HwTq2Val_HwNm_f32.value	-0.678900003		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	5.97520018		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq1Val_HwNm_f32	target_HwTqArbn_Per2_HwTq1Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq2Val_HwNm_f32	target_HwTqArbn_Per2_HwTq2Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTqVal_HwNm_f32	target_HwTqArbn_Per2_HwTqVal_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	-5.33944988	-5.33944988 ± 0.005	✔
target_HwTqArbn_Per2_HwTqVal_HwNm_f32.value	-10	-10 ± 0.005	✔

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.4 (Repeat Count = 1) ✓

Name	Input Value		
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	7.10430002		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per2_HwTq1Val_HwNm_f32.value	10		
target_HwTqArbn_Per2_HwTq2Val_HwNm_f32.value	-4.26809978		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	7.10430002		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq1Val_HwNm_f32	target_HwTqArbn_Per2_HwTq1Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq2Val_HwNm_f32	target_HwTqArbn_Per2_HwTq2Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTqVal_HwNm_f32	target_HwTqArbn_Per2_HwTqVal_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	7.10430002	7.10430002 ± 0.005	✓
target_HwTqArbn_Per2_HwTqVal_HwNm_f32.value	0	0 ± 0.005	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

TEST DETAILS REPORT



Test Step 2.5 (Repeat Count = 1)				
Name		Input Value		
HwTqArb_HwTqCh1Avl_Cnt_M_lgc		1		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32		4.88980007		
Rte_Inst_Sa_HwTqArbn		target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per2_HwTq1Val_HwNm_f32.value		3.45000005		
target_HwTqArbn_Per2_HwTq2Val_HwNm_f32.value		8.32349968		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm		4.88980007		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq1Val_HwNm_f32		target_HwTqArbn_Per2_HwTq1Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq2Val_HwNm_f32		target_HwTqArbn_Per2_HwTq2Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTqVal_HwNm_f32		target_HwTqArbn_Per2_HwTqVal_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData		target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name		Actual Value	Expected Value	Result
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32		5.88674974	5.88675022 ± 0.005	✓
target_HwTqArbn_Per2_HwTqVal_HwNm_f32.value		0.996949673	0.99695 ± 0.005	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.6 (Repeat Count = 1)				
Name		Input Value		
HwTqArb_HwTqCh1Avl_Cnt_M_lgc		1		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32		-9.04759979		
Rte_Inst_Sa_HwTqArbn		target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per2_HwTq1Val_HwNm_f32.value		0		
target_HwTqArbn_Per2_HwTq2Val_HwNm_f32.value		5.76440001		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm		-9.04759979		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq1Val_HwNm_f32		target_HwTqArbn_Per2_HwTq1Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq2Val_HwNm_f32		target_HwTqArbn_Per2_HwTq2Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTqVal_HwNm_f32		target_HwTqArbn_Per2_HwTqVal_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData		target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name		Actual Value	Expected Value	Result
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32		2.8822	2.8822 ± 0.005	✓
target_HwTqArbn_Per2_HwTqVal_HwNm_f32.value		10	10 ± 0.005	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.7 (Repeat Count = 1)				
Name		Input Value		
HwTqArb_HwTqCh1Avl_Cnt_M_lgc		1		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32		-4.55999994		
Rte_Inst_Sa_HwTqArbn		target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per2_HwTq1Val_HwNm_f32.value		-5.75600004		
target_HwTqArbn_Per2_HwTq2Val_HwNm_f32.value		-4.26819992		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm		-4.55999994		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq1Val_HwNm_f32		target_HwTqArbn_Per2_HwTq1Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq2Val_HwNm_f32		target_HwTqArbn_Per2_HwTq2Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTqVal_HwNm_f32		target_HwTqArbn_Per2_HwTqVal_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData		target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name		Actual Value	Expected Value	Result
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32		-5.01210022	-5.01210022 ± 0.005	✓
target_HwTqArbn_Per2_HwTqVal_HwNm_f32.value		-0.452100277	-0.4521 ± 0.005	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.8 (Repeat Count = 1)				
Name		Input Value		
HwTqArb_HwTqCh1Avl_Cnt_M_lgc		0		

TEST DETAILS REPORT



Name	Input Value		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	6.26949978		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per2_HwTq1Val_HwNm_f32.value	6.26949978		
target_HwTqArbn_Per2_HwTq2Val_HwNm_f32.value	-10		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	6.26949978		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq1Val_HwNm_f32	target_HwTqArbn_Per2_HwTq1Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq2Val_HwNm_f32	target_HwTqArbn_Per2_HwTq2Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTqVal_HwNm_f32	target_HwTqArbn_Per2_HwTqVal_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	6.26949978	6.26949978 ± 0.005	✔
target_HwTqArbn_Per2_HwTqVal_HwNm_f32.value	0	0 ± 0.005	✔

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.9 (Repeat Count = 1)				
Name		Input Value		
HwTqArb_HwTqCh1Avl_Cnt_M_lgc		1		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32		-9.70559978		
Rte_Inst_Sa_HwTqArbn		target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per2_HwTq1Val_HwNm_f32.value		-9.70559978		
target_HwTqArbn_Per2_HwTq2Val_HwNm_f32.value		10		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm		-9.70559978		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq1Val_HwNm_f32		target_HwTqArbn_Per2_HwTq1Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq2Val_HwNm_f32		target_HwTqArbn_Per2_HwTq2Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTqVal_HwNm_f32		target_HwTqArbn_Per2_HwTqVal_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData		target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result	
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	0.147200108	0.147200003 ± 0.005	✔	
target_HwTqArbn_Per2_HwTqVal_HwNm_f32.value	9.85280037	9.8528 ± 0.005	✔	

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.10 (Repeat Count = 1)				
Name		Input Value		
HwTqArb_HwTqCh1Avl_Cnt_M_lgc		1		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32		5.97520018		
Rte_Inst_Sa_HwTqArbn		target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per2_HwTq1Val_HwNm_f32.value		5.97520018		
target_HwTqArbn_Per2_HwTq2Val_HwNm_f32.value		4.78000021		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm		5.97520018		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq1Val_HwNm_f32		target_HwTqArbn_Per2_HwTq1Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq2Val_HwNm_f32		target_HwTqArbn_Per2_HwTq2Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTqVal_HwNm_f32		target_HwTqArbn_Per2_HwTqVal_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData		target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name		Actual Value	Expected Value	Result
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32		5.37760019	5.37760019 ± 0.005	✓
target_HwTqArbn_Per2_HwTqVal_HwNm_f32.value		-0.597599983	-0.5976 ± 0.005	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.11 (Repeat Count = 1)		
Name	Input Value	
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	1	
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	7.10430002	
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn	
target_HwTqArbn_Per2_HwTq1Val_HwNm_f32.value	7.10430002	

TEST DETAILS REPORT



Name	Input Value		
target_HwTqArbn_Per2_HwTq2Val_HwNm_f32.value	0		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	7.10430002		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq1Val_HwNm_f32	target_HwTqArbn_Per2_HwTq1Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq2Val_HwNm_f32	target_HwTqArbn_Per2_HwTq2Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTqVal_HwNm_f32	target_HwTqArbn_Per2_HwTqVal_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	3.55215001	3.55215001 ± 0.005	✔
target_HwTqArbn_Per2_HwTqVal_HwNm_f32.value	-3.55215001	-3.55215 ± 0.005	✔

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.12 (Repeat Count = 1) ✓

Name	Input Value		
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	1		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	4.88980007		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per2_HwTq1Val_HwNm_f32.value	4.88980007		
target_HwTqArbn_Per2_HwTq2Val_HwNm_f32.value	-5.86600018		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	4.88980007		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq1Val_HwNm_f32	target_HwTqArbn_Per2_HwTq1Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq2Val_HwNm_f32	target_HwTqArbn_Per2_HwTq2Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTqVal_HwNm_f32	target_HwTqArbn_Per2_HwTqVal_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	-0.488100052	-0.488099992 ± 0.005	✔
target_HwTqArbn_Per2_HwTqVal_HwNm_f32.value	-5.37790012	-5.3779 ± 0.005	✔

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.13 (Repeat Count = 1) ✓

Name	Input Value		
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	-9.04759979		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per2_HwTq1Val_HwNm_f32.value	-9.04759979		
target_HwTqArbn_Per2_HwTq2Val_HwNm_f32.value	6.5927		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	-9.04759979		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq1Val_HwNm_f32	target_HwTqArbn_Per2_HwTq1Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq2Val_HwNm_f32	target_HwTqArbn_Per2_HwTq2Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTqVal_HwNm_f32	target_HwTqArbn_Per2_HwTqVal_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	-9.04759979	-9.04759979 ± 0.005	✔
target_HwTqArbn_Per2_HwTqVal_HwNm_f32.value	0	0 ± 0.005	✔

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.14 (Repeat Count = 1) ✓

Name	Input Value
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	1
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	-1.3053
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn
target_HwTqArbn_Per2_HwTq1Val_HwNm_f32.value	-1.3053
target_HwTqArbn_Per2_HwTq2Val_HwNm_f32.value	-3.75760007
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	-1.3053
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq1Val_HwNm_f32	target_HwTqArbn_Per2_HwTq1Val_HwNm_f32

TEST DETAILS REPORT



Name	Input Value		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq2Val_HwNm_f32	target_HwTqArbn_Per2_HwTq2Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTqVal_HwNm_f32	target_HwTqArbn_Per2_HwTqVal_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	-2.53145003	-2.53145003 ± 0.005	✓
target_HwTqArbn_Per2_HwTqVal_HwNm_f32.value	-1.22615004	-1.22615 ± 0.005	✓

T					✓
Actual Function	Count	Expected Function	Count	Result	
none	0	*** No Call Expected ***	0	✓	

Test Step 2.15 (Repeat Count = 1) ✓

Name	Input Value		
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	-10		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per2_HwTq1Val_HwNm_f32.value	6.60010004		
target_HwTqArbn_Per2_HwTq2Val_HwNm_f32.value	0.0900000036		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	6.60010004		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq1Val_HwNm_f32	target_HwTqArbn_Per2_HwTq1Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq2Val_HwNm_f32	target_HwTqArbn_Per2_HwTq2Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTqVal_HwNm_f32	target_HwTqArbn_Per2_HwTqVal_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	-10	-10 ± 0.005	✔
target_HwTqArbn_Per2_HwTqVal_HwNm_f32.value	-10	-10 ± 0.005	✔

T					✓
Actual Function	Count	Expected Function	Count	Result	
none	0	*** No Call Expected ***	0	✓	

Test Step 2.16 (Repeat Count = 1) ✓

Name	Input Value		
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	10		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per2_HwTq1Val_HwNm_f32.value	-2.15569997		
target_HwTqArbn_Per2_HwTq2Val_HwNm_f32.value	-4.65339994		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	-2.15569997		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq1Val_HwNm_f32	target_HwTqArbn_Per2_HwTq1Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq2Val_HwNm_f32	target_HwTqArbn_Per2_HwTq2Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTqVal_HwNm_f32	target_HwTqArbn_Per2_HwTqVal_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	10	10 ± 0.005	✔
target_HwTqArbn_Per2_HwTqVal_HwNm_f32.value	10	10 ± 0.005	✔

T					✓
Actual Function	Count	Expected Function	Count	Result	
none	0	*** No Call Expected ***	0	✓	

TEST DETAILS REPORT



Test Step 2.17 (Repeat Count = 1)				
Name		Input Value		
HwTqArb_HwTqCh1Avl_Cnt_M_lgc		0		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32		5.45200014		
Rte_Inst_Sa_HwTqArbn		target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per2_HwTq1Val_HwNm_f32.value		9.44999981		
target_HwTqArbn_Per2_HwTq2Val_HwNm_f32.value		-2.84730005		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm		10		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq1Val_HwNm_f32		target_HwTqArbn_Per2_HwTq1Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq2Val_HwNm_f32		target_HwTqArbn_Per2_HwTq2Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTqVal_HwNm_f32		target_HwTqArbn_Per2_HwTqVal_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData		target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name		Actual Value	Expected Value	Result
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32		5.45200014	5.45200014 ± 0.005	✓
target_HwTqArbn_Per2_HwTqVal_HwNm_f32.value		-4.54799986	-4.548 ± 0.005	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.18 (Repeat Count = 1)				
Name		Input Value		
HwTqArb_HwTqCh1Avl_Cnt_M_lgc		0		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32		7.10430002		
Rte_Inst_Sa_HwTqArbn		target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per2_HwTq1Val_HwNm_f32.value		8.30039978		
target_HwTqArbn_Per2_HwTq2Val_HwNm_f32.value		-9.0564003		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm		-10		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq1Val_HwNm_f32		target_HwTqArbn_Per2_HwTq1Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq2Val_HwNm_f32		target_HwTqArbn_Per2_HwTq2Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTqVal_HwNm_f32		target_HwTqArbn_Per2_HwTqVal_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData		target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name		Actual Value	Expected Value	Result
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32		7.10430002	7.10430002 ± 0.005	✓
target_HwTqArbn_Per2_HwTqVal_HwNm_f32.value		10	10 ± 0.005	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.19 (Repeat Count = 1)				
Name		Input Value		
HwTqArb_HwTqCh1Avl_Cnt_M_lgc		0		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32		4.88980007		
Rte_Inst_Sa_HwTqArbn		target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per2_HwTq1Val_HwNm_f32.value		-8.81900024		
target_HwTqArbn_Per2_HwTq2Val_HwNm_f32.value		0.130999997		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm		10		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq1Val_HwNm_f32		target_HwTqArbn_Per2_HwTq1Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq2Val_HwNm_f32		target_HwTqArbn_Per2_HwTq2Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTqVal_HwNm_f32		target_HwTqArbn_Per2_HwTqVal_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData		target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name		Actual Value	Expected Value	Result
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32		4.88980007	4.88980007 ± 0.005	✓
target_HwTqArbn_Per2_HwTqVal_HwNm_f32.value		-5.11019993	-5.1102 ± 0.005	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.20 (Repeat Count = 1)				
Name		Input Value		
HwTqArb_HwTqCh1Avl_Cnt_M_lgc		0		

TEST DETAILS REPORT



Name	Input Value		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	-9.04759979		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per2_HwTq1Val_HwNm_f32.value	9.94069958		
target_HwTqArbn_Per2_HwTq2Val_HwNm_f32.value	-5.6736002		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	3.78900003		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq1Val_HwNm_f32	target_HwTqArbn_Per2_HwTq1Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq2Val_HwNm_f32	target_HwTqArbn_Per2_HwTq2Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTqVal_HwNm_f32	target_HwTqArbn_Per2_HwTqVal_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	-9.04759979	-9.04759979 ± 0.005	✔
target_HwTqArbn_Per2_HwTqVal_HwNm_f32.value	-10	-10 ± 0.005	✔

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.21 (Repeat Count = 1)				
Name		Input Value		
HwTqArb_HwTqCh1Avl_Cnt_M_lgc		0		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32		-1.3053		
Rte_Inst_Sa_HwTqArbn		target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per2_HwTq1Val_HwNm_f32.value		6.60010004		
target_HwTqArbn_Per2_HwTq2Val_HwNm_f32.value		-3.75760007		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm		0		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq1Val_HwNm_f32		target_HwTqArbn_Per2_HwTq1Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq2Val_HwNm_f32		target_HwTqArbn_Per2_HwTq2Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTqVal_HwNm_f32		target_HwTqArbn_Per2_HwTqVal_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData		target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name		Actual Value	Expected Value	Result
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32		-1.3053	-1.3053 ± 0.005	✓
target_HwTqArbn_Per2_HwTqVal_HwNm_f32.value		-1.3053	-1.3053 ± 0.005	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.22 (Repeat Count = 1)				
Name		Input Value		
HwTqArb_HwTqCh1Avl_Cnt_M_lgc		1		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32		6.60010004		
Rte_Inst_Sa_HwTqArbn		target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per2_HwTq1Val_HwNm_f32.value		-2.15569997		
target_HwTqArbn_Per2_HwTq2Val_HwNm_f32.value		0.0900000036		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm		-4.8920002		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq1Val_HwNm_f32		target_HwTqArbn_Per2_HwTq1Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTq2Val_HwNm_f32		target_HwTqArbn_Per2_HwTq2Val_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per2_HwTqVal_HwNm_f32		target_HwTqArbn_Per2_HwTqVal_HwNm_f32		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData		target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name		Actual Value	Expected Value	Result
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32		-1.03285003	-1.03285003 ± 0.005	✓
target_HwTqArbn_Per2_HwTqVal_HwNm_f32.value		3.85915017	3.85915 ± 0.005	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

TEST DETAILS REPORT

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HwTqArbn_Per3



Project	HwTqArbn
Module	HwTqArbn
Test Object	HwTqArbn_Per3

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MCC Coverage	100 %
MC/DC Coverage	100 %

Statistics

Total Testcases	2
Successful	2 ✓
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\HwTqArbn_2TqADAS_
Configuration File	D:\Synergy_Work_Area\HwTqArbn_2TqADAS_\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(SOURCEROOT)\Sa_HwTqArbn.c
Compiler Options	-D_DATA_ACCESS=-D_STATIC=-D_inline=-Dconst=-I\$(PROJECTROOT)\Inputs\utp\contract\Sa_HwTqArbn -I\$(PROJECTROOT)\Inputs\utp\contract -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include -I\$(Compiler Install Path)\include

Comments/Description/Specification

Name	Text
Module 'HwTqArbn'	*****Unit Test Information***** Name of Tester:Ghazala Parvin Ansari Code File(s) Under Test:Sa_HwTqArbn.c Code File(s) Version:3 Module Design Document:HwTqArbn_MDD.doc Module Design Document Version:2 Data Dictionary Version:1 Unit Test Plan Version: 3 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/ EPS Library 1.32 Total FLASH Used (Bytes): 604 Total RAM Used (Bytes): 12 Total CALS Used (Bytes): 4 Special Test Requirements:NA Test Date:10/26/2016 Comments: "NOTE1: Inline functions defined in GlobalMacro.h are not unit tested. NOTE2: ""CBD_Sandbox_dbg.map""map file is embedded for reference." *****

Attributes

Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_PS.tpl
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1

TEST DETAILS REPORT

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HwTqArbn_Per3



Attributes	
Name	Value
Timer Unit	Cycles
UDE Config File	\${PROJECTROOT}\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\HwTqArbn_2TqADAS_\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

TEST DETAILS REPORT

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HwTqArbn_Per3



Test Case 1: Metrics Test

Specification	Performance Metrics (With None Instrumentation and WithPS Environment) CPU Cycles: 1.1 524.00 Cycles 1.2 580.00 Cycles
Description	Vector Description: TS1.1"Shortest Path: if(SVC_ClearCodes_Cnt_T_Igc == TRUE)==true if(NtcActive_Cnt_T_Igc == TRUE)==false" TS1.2"Longest Path: if(SVC_ClearCodes_Cnt_T_Igc == TRUE)==false if((MECCounter_Cnt_T_u08 == 0U) (MECCounter_Cnt_T_u08 == D_MECCNTRMAX_CNT_U08))==true if(EOLChOffsetTrimPerf_Cnt_T_Igc == FALSE)==true if(NtcActive_Cnt_T_Igc == TRUE)==true"

Test Step 1.1 (Repeat Count = 1)

Name	Input Value		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per3_MEC_Counter_Cnt_u08.value	255		
target_HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc.value	1		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	1		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per3_MEC_Counter_Cnt_u08	target_HwTqArbn_Per3_MEC_Counter_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc	target_HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	508	508	✓
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✓
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✓

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus	1	✓

Test Step 1.2 (Repeat Count = 1)

Name	Input Value		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per3_MEC_Counter_Cnt_u08.value	0		
target_HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc.value	0		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cnt	0		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per3_MEC_Counter_Cnt_u08	target_HwTqArbn_Per3_MEC_Counter_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc	target_HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	508	508	✓
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	1	1	✓
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	1	✓

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus	1	✓

TEST DETAILS REPORT

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HwTqArbn_Per3



Test Case 2: Range Test

Specification

Performance Metrics
(With None Instrumentation and WithPS Environment)

CPU Cycles:

TS2.1 554.00 Cycles
TS2.2 565.00 Cycles
TS2.3 558.00 Cycles
TS2.4 524.00 Cycles
TS2.5 524.00 Cycles
TS2.6 577.00 Cycles
TS2.7 558.00 Cycles
TS2.8 524.00 Cycles
TS2.9 542.00 Cycles

Description

Vector Description:

TS2.1All Min
TS2.2All Max
TS2.3SVC_ClearCodes_Cnt_lgc==>Min
TS2.4SVC_ClearCodes_Cnt_lgc==>Max
TS2.5MEC_Counter_Cnt_u08==>Min
TS2.6MEC_Counter_Cnt_u08==>Max
TS2.7MEC_Counter_Cnt_u08==>Pos
TS2.8Rte_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cnt_lgc==>Min
TS2.9Rte_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cnt_lgc==>Max

Test Step 2.1 (Repeat Count = 1)

Name	Input Value		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per3_MEC_Counter_Cnt_u08.value	0		
target_HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc.value	0		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	0		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per3_MEC_Counter_Cnt_u08	target_HwTqArbn_Per3_MEC_Counter_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc	target_HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	508	508	✔
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	1	1	✔
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	1	✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus	1	✓

Test Step 2.2 (Repeat Count = 1)

Name	Input Value		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per3_MEC_Counter_Cnt_u08.value	255		
target_HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc.value	1		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	1		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per3_MEC_Counter_Cnt_u08	target_HwTqArbn_Per3_MEC_Counter_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc	target_HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	508	508	✔
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✔
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus	1	✓

TEST DETAILS REPORT

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HwTqArbn_Per3



Test Step 2.3 (Repeat Count = 1)				✓
Name	Input Value			
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn			
target_HwTqArbn_Per3_MEC_Counter_Cnt_u08.value	124			
target_HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc.value	0			
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	1			
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per3_MEC_Counter_Cnt_u08	target_HwTqArbn_Per3_MEC_Counter_Cnt_u08			
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc	target_HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc			
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData			
Name	Actual Value	Expected Value	Result	
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	508	508	✓	
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✓	
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✓	

T					✓
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus	1	✓	

Test Step 2.4 (Repeat Count = 1)				✓
Name	Input Value			
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn			
target_HwTqArbn_Per3_MEC_Counter_Cnt_u08.value	42			
target_HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc.value	1			
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	0			
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per3_MEC_Counter_Cnt_u08	target_HwTqArbn_Per3_MEC_Counter_Cnt_u08			
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc	target_HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc			
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData			
Name	Actual Value	Expected Value	Result	
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	508	508	✓	
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✓	
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✓	

T					✓
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus	1	✓	

Test Step 2.5 (Repeat Count = 1)				✓
Name	Input Value			
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn			
target_HwTqArbn_Per3_MEC_Counter_Cnt_u08.value	0			
target_HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc.value	1			
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	0			
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per3_MEC_Counter_Cnt_u08	target_HwTqArbn_Per3_MEC_Counter_Cnt_u08			
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc	target_HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc			
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData			
Name	Actual Value	Expected Value	Result	
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	508	508	✓	
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✓	
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✓	

T					✓
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus	1	✓	

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HwTqArbn_Per3



Test Step 2.6 (Repeat Count = 1)				✓
Name	Input Value			
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn			
target_HwTqArbn_Per3_MEC_Counter_Cnt_u08.value	255			
target_HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc.value	0			
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	1			
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per3_MEC_Counter_Cnt_u08	target_HwTqArbn_Per3_MEC_Counter_Cnt_u08			
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc	target_HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc			
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData			
Name	Actual Value	Expected Value	Result	
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	508	508	✓	
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✓	
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✓	

T					✓
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus	1	✓	

Test Step 2.7 (Repeat Count = 1)				✓
Name	Input Value			
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn			
target_HwTqArbn_Per3_MEC_Counter_Cnt_u08.value	120			
target_HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc.value	0			
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	0			
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per3_MEC_Counter_Cnt_u08	target_HwTqArbn_Per3_MEC_Counter_Cnt_u08			
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc	target_HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc			
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData			
Name	Actual Value	Expected Value	Result	
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	508	508	✓	
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✓	
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✓	

T					✓
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus	1	✓	

Test Step 2.8 (Repeat Count = 1)				✓
Name	Input Value			
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn			
target_HwTqArbn_Per3_MEC_Counter_Cnt_u08.value	64			
target_HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc.value	1			
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	0			
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per3_MEC_Counter_Cnt_u08	target_HwTqArbn_Per3_MEC_Counter_Cnt_u08			
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc	target_HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc			
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData			
Name	Actual Value	Expected Value	Result	
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	508	508	✓	
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✓	
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✓	

T					✓
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus	1	✓	

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HwTqArbn_Per3



Test Step 2.9 (Repeat Count = 1)

Name	Input Value		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per3_MEC_Counter_Cnt_u08.value	186		
target_HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc.value	0		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	1		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per3_MEC_Counter_Cnt_u08	target_HwTqArbn_Per3_MEC_Counter_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc	target_HwTqArbn_Per3_SVC_ClearCodes_Cnt_lgc		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	508	508	✔
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✔
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✔

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_HwTqArbn_NxtrDiagMgr_SetNTCStatus	1	✓

TEST DETAILS REPORT

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HwTqArbn_Init1



Project	HwTqArbn
Module	HwTqArbn
Test Object	HwTqArbn_Init1

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

Statistics

Total Testcases	1
Successful	1 ✓
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\HwTqArbn_2TqADAS_
Configuration File	D:\Synergy_Work_Area\HwTqArbn_2TqADAS_UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(SOURCEROOT)\Sa_HwTqArbn.c
Compiler Options	-D_DATA_ACCESS=-D_STATIC=-D_inline=-D_const=-I\$(PROJECTROOT)\Inputs\utp\contract\Sa_HwTqArbn -I\$(PROJECTROOT)\Inputs\utp\contract -I\$(PROJECTROOT)\NxtLib\include -I\$(PROJECTROOT)\StdDef\include -I\$(Compiler Install Path)\include

Comments/Description/Specification

Name	Text
Module 'HwTqArbn'	*****Unit Test Information***** Name of Tester:Ghazala Parvin Ansari Code File(s) Under Test:Sa_HwTqArbn.c Code File(s) Version:3 Module Design Document:HwTqArbn_MDD.doc Module Design Document Version:2 Data Dictionary Version:1 Unit Test Plan Version: 3 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/ EPS Library 1.32 Total FLASH Used (Bytes): 604 Total RAM Used (Bytes): 12 Total CALS Used (Bytes): 4 Special Test Requirements:NA Test Date:10/26/2016 Comments: "NOTE1: Inline functions defined in GlobalMacro.h are not unit tested. NOTE2: ""CBD_Sandbox_dbg.map""map file is embedded for reference." *****

Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_PS.tpl
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
Timer Unit	Cycles
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg

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HwTqArbn_Init1



Workspace File

D:\Synergy_Work_Area\HwTqArbn_2TqADAS_\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

TEST DETAILS REPORT

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HwTqArbn_Init1



Test Case 1: Range Test

Specification Performance Metrics
(With None Instrumentation and WithPS Environment)

CPU Cycles:

TS1.1 7.00 Cycles

Description Vector Description:

TS1.1No functionality in source code

Test Step 1.1 (Repeat Count = 1)

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

TEST DETAILS REPORT

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ArbnSigAvlChk



Project	HwTqArbn
Module	HwTqArbn
Test Object	ArbnSigAvlChk

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MCC Coverage	100 %
MC/DC Coverage	100 %

Statistics

Total Testcases	2
Successful	2 ✓
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\HwTqArbn_2TqADAS_
Configuration File	D:\Synergy_Work_Area\HwTqArbn_2TqADAS_\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\${SOURCEROOT}\Sa_HwTqArbn.c
Compiler Options	-D_DATA_ACCESS=-D_STATIC=-D_inline=-Dconst=-I\$(PROJECTROOT)\Inputs\utp\contract\Sa_HwTqArbn -I\$(PROJECTROOT)\Inputs\utp\contract -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include -I\$(Compiler Install Path)\include

Comments/Description/Specification

Name	Text
Module 'HwTqArbn'	*****Unit Test Information***** Name of Tester:Ghazala Parvin Ansari Code File(s) Under Test:Sa_HwTqArbn.c Code File(s) Version:3 Module Design Document:HwTqArbn_MDD.doc Module Design Document Version:2 Data Dictionary Version:1 Unit Test Plan Version: 3 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/ EPS Library 1.32 Total FLASH Used (Bytes): 604 Total RAM Used (Bytes): 12 Total CALS Used (Bytes): 4 Special Test Requirements:NA Test Date:10/26/2016 Comments: "NOTE1: Inline functions defined in GlobalMacro.h are not unit tested. NOTE2: ""CBD_Sandbox_dbg.map""map file is embedded for reference." *****

Attributes

Name	Value
Compiler Install Path	\${ProgramFiles}\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\${PROJECTROOT}\UnitTestEnv\static_build_files\obj
InitSrcDir	\${PROJECTROOT}\UnitTestEnv\static_build_files\src
Linker File	\${PROJECTROOT}\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	\${PROJECTROOT}\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_PS.tpl
Target Install Path	\${ProgramFiles}\pls\UDE 4.4
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1

TEST DETAILS REPORT

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ArbnSigAvlChk



Attributes	
Name	Value
Timer Unit	Cycles
UDE Config File	\${PROJECTROOT}\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\HwTgArbn_2TqADAS_\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Metrics Test

Specification	Performance Metrics (With None Instrumentation and WithPS Environment)
	CPU Cycles:
	TS1.1 85.00 Cycles
	TS1.2 117.00 Cycles
Description	Vector Description:
	TS1.1"Shortest Path: if (SigRollg_Cnt_T_u08 == LstRollg_Cnt_T_u08)==False if (*StallCntOutp_Cnt_T_u08 >= MaxStall_Cnt_T_u08)==True"
	TS1.2"Longest Path: if (SigRollg_Cnt_T_u08 == LstRollg_Cnt_T_u08)==True if(LstStall_Cnt_T_u08 == D_HWTQNSTALLCNTRMAX_CNT_U08)==False if (*StallCntOutp_Cnt_T_u08 >= MaxStall_Cnt_T_u08)==False if(SigQlfr_Cnt_T_enum < SIGQLFR_FAIL)==True"

Test Step 1.1 (Repeat Count = 1)

Name	Input Value		
LstRollg_Cnt_T_u08	89		
LstStall_Cnt_T_u08	21		
MaxStall_Cnt_T_u08	0		
SigQlfr_Cnt_T_enum	0		
SigRollg_Cnt_T_u08	11		
StallCntOutp_Cnt_T_u08	target_StallCntOutp_Cnt_T_u08		
target_StallCntOutp_Cnt_T_u08	89		
Name	Actual Value	Expected Value	Result
ArbnSigAvlChk()	0	0	✓
target_StallCntOutp_Cnt_T_u08	0	0	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 1.2 (Repeat Count = 1)

Name	Input Value		
LstRollg_Cnt_T_u08	142		
LstStall_Cnt_T_u08	46		
MaxStall_Cnt_T_u08	210		
SigQlfr_Cnt_T_enum	1		
SigRollg_Cnt_T_u08	142		
StallCntOutp_Cnt_T_u08	target_StallCntOutp_Cnt_T_u08		
target_StallCntOutp_Cnt_T_u08	130		
Name	Actual Value	Expected Value	Result
ArbnSigAvlChk()	1	1	✓
target_StallCntOutp_Cnt_T_u08	47	47	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

TEST DETAILS REPORT

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ArbnSigAvlChk



Test Case 2: Range Test

Specification Performance Metrics
(With None Instrumentation and WithPS Environment)

CPU Cycles:

TS2.1 126.00 Cycles
TS2.2 85.00 Cycles
TS2.3 100.00 Cycles
TS2.4 100.00 Cycles
TS2.5 100.00 Cycles
TS2.6 100.00 Cycles
TS2.7 100.00 Cycles
TS2.8 109.00 Cycles
TS2.9 100.00 Cycles
TS2.10 100.00 Cycles
TS2.11 100.00 Cycles
TS2.12 100.00 Cycles
TS2.13 100.00 Cycles
TS2.14 100.00 Cycles
TS2.15 117.00 Cycles
TS2.16 100.00 Cycles
TS2.17 100.00 Cycles
TS2.18 100.00 Cycles
TS2.19 100.00 Cycles
TS2.20 100.00 Cycles

Description Vector Description:

TS2.1All Min
TS2.2All Max
TS2.3SigRollg_Cnt_T_u08==>Min
TS2.4SigRollg_Cnt_T_u08==>Max
TS2.5SigRollg_Cnt_T_u08==>Pos
TS2.6SigQlfr_Cnt_T_enum= SIGQLFR_NORES
TS2.7 SigQlfr_Cnt_T_enum=SIGQLFR_PASS
TS2.8 SigQlfr_Cnt_T_enum=SIGQLFR_FAIL
TS2.9LstRollg_Cnt_T_u08==>Min
TS2.10LstRollg_Cnt_T_u08==>Max
TS2.11LstRollg_Cnt_T_u08==>Pos
TS2.12LstStall_Cnt_T_u08==>Min
TS2.13LstStall_Cnt_T_u08==>Max
TS2.14LstStall_Cnt_T_u08==>Pos
TS2.15MaxStall_Cnt_T_u08==>Min
TS2.16MaxStall_Cnt_T_u08==>Max
TS2.17MaxStall_Cnt_T_u08==>Pos
TS2.18StallCntOutp_Cnt_T_u08==>Min
TS2.19StallCntOutp_Cnt_T_u08==>Max
TS2.20StallCntOutp_Cnt_T_u08==>Pos

Test Step 2.1 (Repeat Count = 1)

Name	Input Value		
LstRollg_Cnt_T_u08	0		
LstStall_Cnt_T_u08	0		
MaxStall_Cnt_T_u08	0		
SigQlfr_Cnt_T_enum	0		
SigRollg_Cnt_T_u08	0		
StallCntOutp_Cnt_T_u08	target_StallCntOutp_Cnt_T_u08		
target_StallCntOutp_Cnt_T_u08	0		
Name	Actual Value	Expected Value	Result
ArbnSigAvlChk()	0	0	✔
target_StallCntOutp_Cnt_T_u08	1	1	✔

T	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.2 (Repeat Count = 1)

Name	Input Value		
LstRollg_Cnt_T_u08	255		
LstStall_Cnt_T_u08	255		
MaxStall_Cnt_T_u08	255		
SigQlfr_Cnt_T_enum	2		
SigRollg_Cnt_T_u08	255		
StallCntOutp_Cnt_T_u08	target_StallCntOutp_Cnt_T_u08		
target_StallCntOutp_Cnt_T_u08	255		
Name	Actual Value	Expected Value	Result
ArbnSigAvlChk()	0	0	✓
target_StallCntOutp_Cnt_T_u08	255	255	✓

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ArbnSigAvlChk



T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.3 (Repeat Count = 1)

Name	Input Value			
LstRollg_Cnt_T_u08	123			
LstStall_Cnt_T_u08	11			
MaxStall_Cnt_T_u08	42			
SigQlfr_Cnt_T_enum	1			
SigRollg_Cnt_T_u08	0			
StallCntOutp_Cnt_T_u08	target_StallCntOutp_Cnt_T_u08			
target_StallCntOutp_Cnt_T_u08	23			
Name	Actual Value	Expected Value	Result	
ArbnSigAvlChk()	1	1	✓	
target_StallCntOutp_Cnt_T_u08	0	0	✓	

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.4 (Repeat Count = 1)

Name	Input Value			
LstRollg_Cnt_T_u08	21			
LstStall_Cnt_T_u08	175			
MaxStall_Cnt_T_u08	142			
SigQlfr_Cnt_T_enum	0			
SigRollg_Cnt_T_u08	255			
StallCntOutp_Cnt_T_u08	target_StallCntOutp_Cnt_T_u08			
target_StallCntOutp_Cnt_T_u08	42			
Name	Actual Value	Expected Value	Result	
ArbnSigAvlChk()	1	1	✓	
target_StallCntOutp_Cnt_T_u08	0	0	✓	

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.5 (Repeat Count = 1)

Name	Input Value			
LstRollg_Cnt_T_u08	130			
LstStall_Cnt_T_u08	186			
MaxStall_Cnt_T_u08	123			
SigQlfr_Cnt_T_enum	1			
SigRollg_Cnt_T_u08	125			
StallCntOutp_Cnt_T_u08	target_StallCntOutp_Cnt_T_u08			
target_StallCntOutp_Cnt_T_u08	142			
Name	Actual Value	Expected Value	Result	
ArbnSigAvlChk()	1	1	✓	
target_StallCntOutp_Cnt_T_u08	0	0	✓	

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.6 (Repeat Count = 1)

Name	Input Value			
LstRollg_Cnt_T_u08	210			
LstStall_Cnt_T_u08	89			
MaxStall_Cnt_T_u08	21			

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ArbnSigAvlChk

Name	Input Value		
SigQlfr_Cnt_T_enum	0		
SigRollg_Cnt_T_u08	23		
StallCntOutp_Cnt_T_u08	target_StallCntOutp_Cnt_T_u08		
target_StallCntOutp_Cnt_T_u08	123		
Name	Actual Value	Expected Value	Result
ArbnSigAvlChk()	1	1	✓
target_StallCntOutp_Cnt_T_u08	0	0	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.7 (Repeat Count = 1)

Name	Input Value		
LstRollg_Cnt_T_u08	10		
LstStall_Cnt_T_u08	127		
MaxStall_Cnt_T_u08	130		
SigQlfr_Cnt_T_enum	2		
SigRollg_Cnt_T_u08	42		
StallCntOutp_Cnt_T_u08	target_StallCntOutp_Cnt_T_u08		
target_StallCntOutp_Cnt_T_u08	21		
Name	Actual Value	Expected Value	Result
ArbnSigAvlChk()	0	0	✔
target_StallCntOutp_Cnt_T_u08	0	0	✔

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.8 (Repeat Count = 1)

Name	Input Value		
LstRollg_Cnt_T_u08	142		
LstStall_Cnt_T_u08	46		
MaxStall_Cnt_T_u08	210		
SigQlfr_Cnt_T_enum	1		
SigRollg_Cnt_T_u08	142		
StallCntOutp_Cnt_T_u08	target_StallCntOutp_Cnt_T_u08		
target_StallCntOutp_Cnt_T_u08	130		
Name	Actual Value	Expected Value	Result
ArbnSigAvlChk()	1	1	✓
target_StallCntOutp_Cnt_T_u08	47	47	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.9 (Repeat Count = 1)

Name	Input Value		
LstRollg_Cnt_T_u08	0		
LstStall_Cnt_T_u08	78		
MaxStall_Cnt_T_u08	10		
SigQlfr_Cnt_T_enum	1		
SigRollg_Cnt_T_u08	123		
StallCntOutp_Cnt_T_u08	target_StallCntOutp_Cnt_T_u08		
target_StallCntOutp_Cnt_T_u08	210		
Name	Actual Value	Expected Value	Result
ArbnSigAvlChk()	1	1	
*none*0	*** No Call Expected ***	0	

Actual Function	Count	Expected Function	Count	Result

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ArbnSigAvlChk



Test Step 2.10 (Repeat Count = 1)				
Name		Input Value		
LstRollg_Cnt_T_u08		255		
LstStall_Cnt_T_u08		125		
MaxStall_Cnt_T_u08		3		
SigQlfr_Cnt_T_enum		0		
SigRollg_Cnt_T_u08		21		
StallCntOutp_Cnt_T_u08		target_StallCntOutp_Cnt_T_u08		
target_StallCntOutp_Cnt_T_u08		10		
Name		Actual Value	Expected Value	Result
ArbnSigAvlChk()		1	1	✓
target_StallCntOutp_Cnt_T_u08		0	0	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.11 (Repeat Count = 1)				
Name		Input Value		
LstRollg_Cnt_T_u08		125		
LstStall_Cnt_T_u08		197		
MaxStall_Cnt_T_u08		130		
SigQlfr_Cnt_T_enum		0		
SigRollg_Cnt_T_u08		130		
StallCntOutp_Cnt_T_u08		target_StallCntOutp_Cnt_T_u08		
target_StallCntOutp_Cnt_T_u08		3		
Name		Actual Value	Expected Value	Result
ArbnSigAvlChk()		1	1	✓
target_StallCntOutp_Cnt_T_u08		0	0	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.12 (Repeat Count = 1)				
Name		Input Value		
LstRollg_Cnt_T_u08		11		
LstStall_Cnt_T_u08		0		
MaxStall_Cnt_T_u08		210		
SigQlfr_Cnt_T_enum		1		
SigRollg_Cnt_T_u08		210		
StallCntOutp_Cnt_T_u08		target_StallCntOutp_Cnt_T_u08		
target_StallCntOutp_Cnt_T_u08		11		
Name		Actual Value	Expected Value	Result
ArbnSigAvlChk()		1	1	✓
target_StallCntOutp_Cnt_T_u08		0	0	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

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ArbnSigAvlChk



Test Step 2.13 (Repeat Count = 1)

Name	Input Value		
LstRollg_Cnt_T_u08	175		
LstStall_Cnt_T_u08	255		
MaxStall_Cnt_T_u08	10		
SigQlfr_Cnt_T_enum	2		
SigRollg_Cnt_T_u08	10		
StallCntOutp_Cnt_T_u08	target_StallCntOutp_Cnt_T_u08		
target_StallCntOutp_Cnt_T_u08	175		
Name	Actual Value	Expected Value	Result
ArbnSigAvlChk()	0	0	✔
target_StallCntOutp_Cnt_T_u08	0	0	✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.14 (Repeat Count = 1)

Name	Input Value		
LstRollg_Cnt_T_u08	186		
LstStall_Cnt_T_u08	125		
MaxStall_Cnt_T_u08	23		
SigQlfr_Cnt_T_enum	1		
SigRollg_Cnt_T_u08	3		
StallCntOutp_Cnt_T_u08	target_StallCntOutp_Cnt_T_u08		
target_StallCntOutp_Cnt_T_u08	186		
Name	Actual Value	Expected Value	Result
ArbnSigAvlChk()	1	1	✓
target_StallCntOutp_Cnt_T_u08	0	0	✓

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.15 (Repeat Count = 1)

Name	Input Value		
LstRollg_Cnt_T_u08	89		
LstStall_Cnt_T_u08	21		
MaxStall_Cnt_T_u08	0		
SigQlfr_Cnt_T_enum	0		
SigRollg_Cnt_T_u08	11		
StallCntOutp_Cnt_T_u08	target_StallCntOutp_Cnt_T_u08		
target_StallCntOutp_Cnt_T_u08	89		
Name	Actual Value	Expected Value	Result
ArbnSigAvlChk()	0	0	✓
target_StallCntOutp_Cnt_T_u08	0	0	✓

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.16 (Repeat Count = 1)

Name	Input Value		
LstRollg_Cnt_T_u08	127		
LstStall_Cnt_T_u08	130		
MaxStall_Cnt_T_u08	255		
SigQlfr_Cnt_T_enum	1		
SigRollg_Cnt_T_u08	175		
StallCntOutp_Cnt_T_u08	target_StallCntOutp_Cnt_T_u08		
target_StallCntOutp_Cnt_T_u08	127		
Name	Actual Value	Expected Value	Result
ArbnSigAvlChk()	1	1	✔

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Name	Actual Value	Expected Value	Result
target_StallCntOutp_Cnt_T_u08	0	0	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.17 (Repeat Count = 1)

Name	Input Value		
LstRollg_Cnt_T_u08	46		
LstStall_Cnt_T_u08	210		
MaxStall_Cnt_T_u08	125		
SigQlfr_Cnt_T_enum	2		
SigRollg_Cnt_T_u08	186		
StallCntOutp_Cnt_T_u08	target_StallCntOutp_Cnt_T_u08		
target_StallCntOutp_Cnt_T_u08	96		
Name	Actual Value	Expected Value	Result
ArbnSigAvlChk()	0	0	✓
target_StallCntOutp_Cnt_T_u08	0	0	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.18 (Repeat Count = 1)

Name	Input Value		
LstRollg_Cnt_T_u08	78		
LstStall_Cnt_T_u08	10		
MaxStall_Cnt_T_u08	14		
SigQlfr_Cnt_T_enum	1		
SigRollg_Cnt_T_u08	89		
StallCntOutp_Cnt_T_u08	target_StallCntOutp_Cnt_T_u08		
target_StallCntOutp_Cnt_T_u08	0		
Name	Actual Value	Expected Value	Result
ArbnSigAvlChk()	1	1	✔
target_StallCntOutp_Cnt_T_u08	0	0	✔

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.19 (Repeat Count = 1)

Name	Input Value		
LstRollg_Cnt_T_u08	125		
LstStall_Cnt_T_u08	23		
MaxStall_Cnt_T_u08	78		
SigQlfr_Cnt_T_enum	0		
SigRollg_Cnt_T_u08	127		
StallCntOutp_Cnt_T_u08	target_StallCntOutp_Cnt_T_u08		
target_StallCntOutp_Cnt_T_u08	255		
Name	Actual Value	Expected Value	Result
ArbnSigAvlChk()	1	1	✓
target_StallCntOutp_Cnt_T_u08	0	0	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

TEST DETAILS REPORT

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ArbnSigAvlChk



Test Step 2.20 (Repeat Count = 1)

Test Step 2.20 (Repeat Count = 1)				✓
Name		Input Value		
LstRollg_Cnt_T_u08		197		
LstStall_Cnt_T_u08		105		
MaxStall_Cnt_T_u08		155		
SigQlfr_Cnt_T_enum		1		
SigRollg_Cnt_T_u08		96		
StallCntOutp_Cnt_T_u08		target_StallCntOutp_Cnt_T_u08		
target_StallCntOutp_Cnt_T_u08		125		
Name		Actual Value	Expected Value	Result
ArbnSigAvlChk()		1	1	✓
target_StallCntOutp_Cnt_T_u08		0	0	✓

T					✓
Actual Function	Count	Expected Function	Count	Result	
none	0	*** No Call Expected ***	0		✓

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HwTrqArbn_SCom_ReadHwTrqArbOffsetTrim



Project	HwTqArbn
Module	HwTqArbn
Test Object	HwTrqArbn_SCom_ReadHwTrqArbOffsetTrim

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

Statistics

Total Testcases	1
Successful	1 ✓
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\HwTqArbn_2TqADAS_
Configuration File	D:\Synergy_Work_Area\HwTqArbn_2TqADAS\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(SOURCEROOT)\Sa_HwTqArbn.c
Compiler Options	-D_DATA_ACCESS=-D_STATIC=-D_inline=-Dconst=-I\$(PROJECTROOT)\Inputs\utp\contract\Sa_HwTqArbn -I\$(PROJECTROOT)\Inputs\utp\contract -I\$(PROJECTROOT)\NxtLib\include -I\$(PROJECTROOT)\StdDef\include -I\$(Compiler Install Path)\include

Comments/Description/Specification

Name	Text
Module 'HwTqArbn'	*****Unit Test Information***** Name of Tester:Ghazala Parvin Ansari Code File(s) Under Test:Sa_HwTqArbn.c Code File(s) Version:3 Module Design Document:HwTqArbn_MDD.doc Module Design Document Version:2 Data Dictionary Version:1 Unit Test Plan Version: 3 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/ EPS Library 1.32 Total FLASH Used (Bytes): 604 Total RAM Used (Bytes): 12 Total CALS Used (Bytes): 4 Special Test Requirements:NA Test Date:10/26/2016 Comments: "NOTE1: Inline functions defined in GlobalMacro.h are not unit tested. NOTE2: "CBD_Sandbox_dbg.map"map file is embedded for reference." *****

Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_PS.tpl
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
Timer Unit	Cycles
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg

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HwTrqArbn_SCom_ReadHwTrqArbOffsetTrim



Workspace File

D:\Synergy_Work_Area\HwTqArbn_2TqADAS_\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

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HwTrqArbn_SCom_ReadHwTrqArbOffsetTrim



Test Case 1: Range Test

Specification	Performance Metrics (With None Instrumentation and WithPS Environment)
	CPU Cycles: TS1.1 23.00 Cycles TS1.2 23.00 Cycles TS1.3 23.00 Cycles TS1.4 23.00 Cycles TS1.5 23.00 Cycles TS1.6 23.00 Cycles TS1.7 23.00 Cycles TS1.8 23.00 Cycles TS1.9 23.00 Cycles
Description	Vector Description: TS1.1All Min TS1.2All Max TS1.3Rte_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cnt_lgc==>Min TS1.4Rte_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cnt_lgc==>Max TS1.5Rte_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm_f32==>Min TS1.6Rte_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm_f32==>Max TS1.7Rte_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm_f32==>Pos TS1.8Rte_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm_f32==>Zero TS1.9Rte_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm_f32==>Neg

Test Step 1.1 (Repeat Count = 1)

Name	Input Value		
EOLChOffsetTrimPerf_Cnt_lgc	target_EOLChOffsetTrimPerf_Cnt_lgc		
EOLChOffsetTrim_HwNm_f32	target_EOLChOffsetTrim_HwNm_f32		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	-10		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	0		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
target_EOLChOffsetTrimPerf_Cnt_lgc	0	0	✓
target_EOLChOffsetTrim_HwNm_f32	-10	-10	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 1.2 (Repeat Count = 1)

Name	Input Value		
EOLChOffsetTrimPerf_Cnt_lgc	target_EOLChOffsetTrimPerf_Cnt_lgc		
EOLChOffsetTrim_HwNm_f32	target_EOLChOffsetTrim_HwNm_f32		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	10		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	1		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
target_EOLChOffsetTrimPerf_Cnt_lgc	1	1	✓
target_EOLChOffsetTrim_HwNm_f32	10	10	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 1.3 (Repeat Count = 1)

Name	Input Value		
EOLChOffsetTrimPerf_Cnt_lgc	target_EOLChOffsetTrimPerf_Cnt_lgc		
EOLChOffsetTrim_HwNm_f32	target_EOLChOffsetTrim_HwNm_f32		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	-4.1225		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	0		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
target_EOLChOffsetTrimPerf_Cnt_lgc	0	0	✓
target_EOLChOffsetTrim_HwNm_f32	-4.12249994	-4.1225	✓

TEST DETAILS REPORT

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HwTrqArbn_SCom_ReadHwTrqArbOffsetTrim

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 1.4 (Repeat Count = 1)

Name	Input Value			
EOLChOffsetTrimPerf_Cnt_lgc	target_EOLChOffsetTrimPerf_Cnt_lgc			
EOLChOffsetTrim_HwNm_f32	target_EOLChOffsetTrim_HwNm_f32			
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn			
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	2.145			
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	1			
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData			
Name	Actual Value	Expected Value	Result	
target_EOLChOffsetTrimPerf_Cnt_lgc	1	1	✓	
target_EOLChOffsetTrim_HwNm_f32	2.14499998	2.145	✓	

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 1.5 (Repeat Count = 1)

Name	Input Value			
EOLChOffsetTrimPerf_Cnt_lgc	target_EOLChOffsetTrimPerf_Cnt_lgc			
EOLChOffsetTrim_HwNm_f32	target_EOLChOffsetTrim_HwNm_f32			
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn			
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	-10			
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	0			
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData			
Name	Actual Value	Expected Value	Result	
target_EOLChOffsetTrimPerf_Cnt_lgc	0	0	✓	
target_EOLChOffsetTrim_HwNm_f32	-10	-10	✓	

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 1.6 (Repeat Count = 1)

Name	Input Value			
EOLChOffsetTrimPerf_Cnt_lgc	target_EOLChOffsetTrimPerf_Cnt_lgc			
EOLChOffsetTrim_HwNm_f32	target_EOLChOffsetTrim_HwNm_f32			
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn			
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	10			
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	1			
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData			
Name	Actual Value	Expected Value	Result	
target_EOLChOffsetTrimPerf_Cnt_lgc	1	1	✓	
target_EOLChOffsetTrim_HwNm_f32	10	10	✓	

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 1.7 (Repeat Count = 1)

Name	Input Value			
EOLChOffsetTrimPerf_Cnt_lgc	target_EOLChOffsetTrimPerf_Cnt_lgc			
EOLChOffsetTrim_HwNm_f32	target_EOLChOffsetTrim_HwNm_f32			
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn			
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	5.756			
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	0			

TEST DETAILS REPORT

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HwTrqArbn_SCom_ReadHwTrqArbOffsetTrim

Name	Input Value		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
target_EOLChOffsetTrimPerf_Cnt_lgc	0	0	✓
target_EOLChOffsetTrim_HwNm_f32	5.75600004	5.756	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 1.8 (Repeat Count = 1)

Name	Input Value		
EOLChOffsetTrimPerf_Cnt_lgc	target_EOLChOffsetTrimPerf_Cnt_lgc		
EOLChOffsetTrim_HwNm_f32	target_EOLChOffsetTrim_HwNm_f32		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	0		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	0		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
target_EOLChOffsetTrimPerf_Cnt_lgc	0	0	✓
target_EOLChOffsetTrim_HwNm_f32	0	0	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 1.9 (Repeat Count = 1)

Name	Input Value		
EOLChOffsetTrimPerf_Cnt_lgc	target_EOLChOffsetTrimPerf_Cnt_lgc		
EOLChOffsetTrim_HwNm_f32	target_EOLChOffsetTrim_HwNm_f32		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	-4.879		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	1		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
target_EOLChOffsetTrimPerf_Cnt_lgc	1	1	✓
target_EOLChOffsetTrim_HwNm_f32	-4.87900019	-4.879	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

TEST DETAILS REPORT



Project	HwTqArbn
Module	HwTqArbn
Test Object	HwTqArbn_Per1

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MCC Coverage	100 %
MC/DC Coverage	100 %

Statistics

Total Testcases	2
Successful	2 ✓
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\HwTqArbn_2TqADAS_
Configuration File	D:\Synergy_Work_Area\HwTqArbn_2TqADAS_\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(SOURCEROOT)\Sa_HwTqArbn.c
Compiler Options	-D_DATA_ACCESS=-D_STATIC=-D_inline=-Dconst=-I\$(PROJECTROOT)\Inputs\utp\contract\Sa_HwTqArbn -I\$(PROJECTROOT)\Inputs\utp\contract -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include -I\$(Compiler Install Path)\include

Comments/Description/Specification

Name	Text
Module 'HwTqArbn'	*****Unit Test Information***** Name of Tester:Ghazala Parvin Ansari Code File(s) Under Test:Sa_HwTqArbn.c Code File(s) Version:3 Module Design Document:HwTqArbn_MDD.doc Module Design Document Version:2 Data Dictionary Version:1 Unit Test Plan Version: 3 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/ EPS Library 1.32 Total FLASH Used (Bytes): 604 Total RAM Used (Bytes): 12 Total CALS Used (Bytes): 4 Special Test Requirements:NA Test Date:10/26/2016 Comments: "NOTE1: Inline functions defined in GlobalMacro.h are not unit tested. NOTE2: ""CBD_Sandbox_dbg.map""map file is embedded for reference." *****

Attributes

Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_PS.tpl
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1

Attributes	
Name	Value
Timer Unit	Cycles
UDE Config File	\${PROJECTROOT}\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\HwTgArbn_2TqADAS_\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

TEST DETAILS REPORT



Test Case 1: Metrics Test

Specification Performance Metrics
(With None Instrumentation and WithPS Environment)

CPU Cycles:

1.1 1088.00 Cycles
1.2 1176.00 Cycles

Description Vector Description:

TS1.1"Shortest Path:
CorrInStsSig0_Cnt_T_lgc = (((HwTqCorrInSts_Cnt_T_u16 & 0x01u) != 0x00u) ? TRUE : FALSE); ==false
CorrInStsSig1_Cnt_T_lgc = (((HwTqCorrInSts_Cnt_T_u16 & 0x02u) != 0x00u) ? TRUE : FALSE); ==false
if((CorrInStsSig0_Cnt_T_lgc == TRUE) &&
(CorrInStsSig1_Cnt_T_lgc == TRUE) &&
(Sig0Avl_Cnt_T_lgc == TRUE) &&
(Sig1Avl_Cnt_T_lgc == TRUE)) == false"

TS1.2"Longest Path:
CorrInStsSig0_Cnt_T_lgc = (((HwTqCorrInSts_Cnt_T_u16 & 0x01u) != 0x00u) ? TRUE : FALSE); ==true
CorrInStsSig1_Cnt_T_lgc = (((HwTqCorrInSts_Cnt_T_u16 & 0x02u) != 0x00u) ? TRUE : FALSE); ==true
if((CorrInStsSig0_Cnt_T_lgc == TRUE) &&
(CorrInStsSig1_Cnt_T_lgc == TRUE) &&
(Sig0Avl_Cnt_T_lgc == TRUE) &&
(Sig1Avl_Cnt_T_lgc == TRUE)) == true"

Test Step 1.1 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	0		
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0		
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	0		
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	0		
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	0		
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	0		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	0		
target_HwTqArbn_Per1_HwTqCorrnInSts_Cnt_u16.value	0		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrnInSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrnInSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTq1StallCnt_Cnt_M_u08	1	1	✔
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTq2StallCnt_Cnt_M_u08	1	1	✔
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✔

T				
Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

Test Step 1.2 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	129		
HwTqArb_HwTq1StallCnt_Cnt_M_u08	167		
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	110		
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	0		
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	243		
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	0		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	52		
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	3		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	243	243	✓

TEST DETAILS REPORT



Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✓
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	52	52	✓
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✓
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	1	1	✓

T					✓
Actual Function	Count	Expected Function	Count	Result	
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓	

Test Case 2: Range Test

Specification Performance Metrics
(With None Instrumentation and WithPS Environment)

CPU Cycles:

TS2.1 1176.00 Cycles
TS2.2 1156.00 Cycles
TS2.3 1133.00 Cycles
TS2.4 1088.00 Cycles
TS2.5 1137.00 Cycles
TS2.6 1088.00 Cycles
TS2.7 1112.00 Cycles
TS2.8 1088.00 Cycles
TS2.9 1112.00 Cycles
TS2.10 1088.00 Cycles
TS2.11 1088.00 Cycles
TS2.12 1088.00 Cycles
TS2.13 1088.00 Cycles
TS2.14 1088.00 Cycles
TS2.15 1088.00 Cycles
TS2.16 1133.00 Cycles
TS2.17 1112.00 Cycles
TS2.18 1112.00 Cycles
TS2.19 1088.00 Cycles
TS2.20 1112.00 Cycles
TS2.21 1141.00 Cycles
TS2.22 1127.00 Cycles
TS2.23 1112.00 Cycles
TS2.24 1112.00 Cycles
TS2.25 1088.00 Cycles
TS2.26 1088.00 Cycles
TS2.27 1088.00 Cycles
TS2.28 1088.00 Cycles
TS2.29 1137.00 Cycles

Description Vector Description:

TS2.1All Min
TS2.2All Max
TS2.3HwTq1RollgCntr_Cnt_u08==>Min
TS2.4HwTq1RollgCntr_Cnt_u08==>Max
TS2.5HwTq1RollgCntr_Cnt_u08==>Pos
TS2.6HwTq2RollgCntr_Cnt_u08==>Min
TS2.7HwTq2RollgCntr_Cnt_u08==>Max
TS2.8HwTq2RollgCntr_Cnt_u08==>Pos
TS2.9HwTq1Qlfr_State_enum=SIGQLFR_NORES
TS2.10 HwTq1Qlfr_State_enum=SIGQLFR_PASS
TS2.11 HwTq1Qlfr_State_enum=SIGQLFR_FAIL
TS2.12 HwTq2Qlfr_State_enum=SIGQLFR_NORES
TS2.13 HwTq2Qlfr_State_enum=SIGQLFR_PASS
TS2.14 HwTq2Qlfr_State_enum=SIGQLFR_FAIL
TS2.15HwTqCorrinSts_Cnt_u16==>Min
TS2.16HwTqCorrinSts_Cnt_u16==>Max
TS2.17HwTqCorrinSts_Cnt_u16==>Pos
TS2.18HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08==>Min
TS2.19HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08==>Max
TS2.20HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08==>Pos
TS2.21HwTqArb_HwTq2StallCnt_Cnt_M_u08==>Min
TS2.22HwTqArb_HwTq2StallCnt_Cnt_M_u08==>Max
TS2.23HwTqArb_HwTq2StallCnt_Cnt_M_u08==>Pos
TS2.24HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08==>Min
TS2.25HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08==>Max
TS2.26HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08==>Pos
TS2.27HwTqArb_HwTq1StallCnt_Cnt_M_u08==>Min
TS2.28HwTqArb_HwTq1StallCnt_Cnt_M_u08==>Max
TS2.29HwTqArb_HwTq1StallCnt_Cnt_M_u08==>Pos

Test Step 2.1 (Repeat Count = 1)

Name	Input Value
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	0
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	0
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	0
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	0
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	0

TEST DETAILS REPORT



Name	Input Value		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	0		
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	0		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTq1StallCnt_Cnt_M_u08	1	1	✔
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTq2StallCnt_Cnt_M_u08	1	1	✔
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✔

T				
Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

Test Step 2.2 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	255		
HwTqArb_HwTq1StallCnt_Cnt_M_u08	255		
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	255		
HwTqArb_HwTq2StallCnt_Cnt_M_u08	255		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	2		
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	255		
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	2		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	255		
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	3		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	255	255	✔
HwTqArb_HwTq1StallCnt_Cnt_M_u08	255	255	✔
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	255	255	✔
HwTqArb_HwTq2StallCnt_Cnt_M_u08	255	255	✔
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✔

T				
Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

Test Step 2.3 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	15		
HwTqArb_HwTq1StallCnt_Cnt_M_u08	210		
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	165		
HwTqArb_HwTq2StallCnt_Cnt_M_u08	83		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	2		
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	0		
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	2		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	113		
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	3		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	0	0	✓
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✓

TEST DETAILS REPORT



Name	Actual Value	Expected Value	Result
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	113	113	✓
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✓
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✓

T				
Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

Test Step 2.4 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	38		
HwTqArb_HwTq1StallCnt_Cnt_M_u08	39		
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	251		
HwTqArb_HwTq2StallCnt_Cnt_M_u08	250		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	0		
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	255		
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	2		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	69		
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	2		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	255	255	✔
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	69	69	✔
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✔

T				
Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

Test Step 2.5 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	80		
HwTqArb_HwTq1StallCnt_Cnt_M_u08	203		
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	79		
HwTqArb_HwTq2StallCnt_Cnt_M_u08	148		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	1		
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	69		
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	2		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	223		
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	3		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	69	69	✔
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	223	223	✔
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✔

T				
Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

TEST DETAILS REPORT



Test Step 2.6 (Repeat Count = 1) ✓

Name	Input Value
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	111
HwTqArb_HwTq1StallCnt_Cnt_M_u08	109
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	61
HwTqArb_HwTq2StallCnt_Cnt_M_u08	134
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	2
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	74
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	2
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	0
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	0
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16

Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	74	74	✓
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✓
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	0	0	✓
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✓
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✓

T ✓

Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

Test Step 2.7 (Repeat Count = 1) ✓

Name	Input Value
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	108
HwTqArb_HwTq1StallCnt_Cnt_M_u08	139
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	224
HwTqArb_HwTq2StallCnt_Cnt_M_u08	34
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	2
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	77
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	1
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	255
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	1
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16

Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	77	77	✓
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✓
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	255	255	✓
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✓
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✓

T ✓

Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

Test Step 2.8 (Repeat Count = 1) ✓

Name	Input Value
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	219
HwTqArb_HwTq1StallCnt_Cnt_M_u08	18
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	33
HwTqArb_HwTq2StallCnt_Cnt_M_u08	230
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	0
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	198
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	2

TEST DETAILS REPORT



Name	Input Value		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	172		
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	2		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	198	198	✔
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	172	172	✔
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✔

T					✓
Actual Function	Count	Expected Function	Count	Result	
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓	

Test Step 2.9 (Repeat Count = 1) ✓

Name	Input Value		
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	14		
HwTqArb_HwTq1StallCnt_Cnt_M_u08	14		
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	145		
HwTqArb_HwTq2StallCnt_Cnt_M_u08	7		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	0		
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	3		
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	2		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	65		
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	1		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	3	3	✔
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	65	65	✔
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✔

T					✓
Actual Function	Count	Expected Function	Count	Result	
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓	

Test Step 2.10 (Repeat Count = 1) ✓

Name	Input Value		
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	229		
HwTqArb_HwTq1StallCnt_Cnt_M_u08	213		
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	155		
HwTqArb_HwTq2StallCnt_Cnt_M_u08	202		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	1		
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	194		
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	0		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	23		
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	0		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	194	194	✓
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✓

TEST DETAILS REPORT



Name	Actual Value	Expected Value	Result
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	23	23	✓
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✓
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✓

T				
Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

Test Step 2.11 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	61		
HwTqArb_HwTq1StallCnt_Cnt_M_u08	251		
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	156		
HwTqArb_HwTq2StallCnt_Cnt_M_u08	184		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	2		
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	208		
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	0		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	7		
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	2		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	208	208	✔
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	7	7	✔
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✔

T				
Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

Test Step 2.12 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	13		
HwTqArb_HwTq1StallCnt_Cnt_M_u08	4		
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	177		
HwTqArb_HwTq2StallCnt_Cnt_M_u08	62		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	2		
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	181		
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	0		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	82		
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	2		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	181	181	✔
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	82	82	✔
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✔

T				
Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

TEST DETAILS REPORT



Test Step 2.13 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	199		
HwTqArb_HwTq1StallCnt_Cnt_M_u08	168		
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	217		
HwTqArb_HwTq2StallCnt_Cnt_M_u08	241		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	2		
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	11		
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	1		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	202		
target_HwTqArbn_Per1_HwTqCorrnSts_Cnt_u16.value	0		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrnSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrnSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	11	11	✔
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	202	202	✔
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✔

Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

Test Step 2.14 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	9		
HwTqArb_HwTq1StallCnt_Cnt_M_u08	244		
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	24		
HwTqArb_HwTq2StallCnt_Cnt_M_u08	119		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	1		
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	105		
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	2		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	76		
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	0		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	105	105	✔
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	76	76	✔
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✔

Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

Test Step 2.15 (Repeat Count = 1)

Name	Input Value
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	34
HwTqArb_HwTq1StallCnt_Cnt_M_u08	30
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	100
HwTqArb_HwTq2StallCnt_Cnt_M_u08	185
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	0
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	220
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	2

TEST DETAILS REPORT



Name	Input Value		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	60		
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	0		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	220	220	✔
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	60	60	✔
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✔

T				
Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

Test Step 2.16 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	171		
HwTqArb_HwTq1StallCnt_Cnt_M_u08	98		
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	210		
HwTqArb_HwTq2StallCnt_Cnt_M_u08	101		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	2		
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	202		
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	0		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	123		
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	3		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	202	202	✔
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	123	123	✔
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✔

T				
Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

Test Step 2.17 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	67		
HwTqArb_HwTq1StallCnt_Cnt_M_u08	126		
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	68		
HwTqArb_HwTq2StallCnt_Cnt_M_u08	59		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	2		
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	95		
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	0		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	65		
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	1		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	95	95	✓
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✓

TEST DETAILS REPORT



Name	Actual Value	Expected Value	Result
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	65	65	✓
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✓
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✓

T				
Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

Test Step 2.18 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	215		
HwTqArb_HwTq1StallCnt_Cnt_M_u08	230		
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	0		
HwTqArb_HwTq2StallCnt_Cnt_M_u08	154		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	2		
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	246		
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	0		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	87		
target_HwTqArbn_Per1_HwTqCorrnSts_Cnt_u16.value	1		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrnSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrnSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	246	246	✔
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	87	87	✔
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✔

T				
Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

Test Step 2.19 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	53		
HwTqArb_HwTq1StallCnt_Cnt_M_u08	43		
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	255		
HwTqArb_HwTq2StallCnt_Cnt_M_u08	141		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	1		
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	223		
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	1		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	11		
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	0		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	223	223	✔
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	11	11	✔
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✔

T				
Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

TEST DETAILS REPORT



Test Step 2.20 (Repeat Count = 1) ✓

Name	Input Value
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	57
HwTqArb_HwTq1StallCnt_Cnt_M_u08	211
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	117
HwTqArb_HwTq2StallCnt_Cnt_M_u08	118
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	0
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	14
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	1
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	123
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	1
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16

Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	14	14	✓
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✓
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	123	123	✓
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✓
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✓

T ✓

Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

Test Step 2.21 (Repeat Count = 1) ✓

Name	Input Value
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	129
HwTqArb_HwTq1StallCnt_Cnt_M_u08	167
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	110
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	0
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	243
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	0
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	52
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	3
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16

Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	243	243	✓
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✓
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	52	52	✓
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✓
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	1	1	✓

T ✓

Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

Test Step 2.22 (Repeat Count = 1) ✓

Name	Input Value
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	158
HwTqArb_HwTq1StallCnt_Cnt_M_u08	56
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	214
HwTqArb_HwTq2StallCnt_Cnt_M_u08	255
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	0
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	93
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	0

TEST DETAILS REPORT



Name	Input Value		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	221		
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	3		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	93	93	✔
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	221	221	✔
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	1	1	✔

T				
Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

Test Step 2.23 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	155		
HwTqArb_HwTq1StallCnt_Cnt_M_u08	11		
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	56		
HwTqArb_HwTq2StallCnt_Cnt_M_u08	184		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	1		
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	134		
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	2		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	150		
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	1		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	134	134	✔
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	150	150	✔
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✔

T				
Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

Test Step 2.24 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	0		
HwTqArb_HwTq1StallCnt_Cnt_M_u08	233		
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	187		
HwTqArb_HwTq2StallCnt_Cnt_M_u08	40		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	1		
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	196		
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	0		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	193		
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	1		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	196	196	✓
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✓

TEST DETAILS REPORT



Name	Actual Value	Expected Value	Result
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	193	193	✓
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✓
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✓

T				
Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

Test Step 2.25 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	255		
HwTqArb_HwTq1StallCnt_Cnt_M_u08	125		
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	230		
HwTqArb_HwTq2StallCnt_Cnt_M_u08	25		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	0		
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	13		
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	1		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	237		
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	2		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	13	13	✔
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	237	237	✔
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✔

T				
Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

Test Step 2.26 (Repeat Count = 1)

Test Step 2: Repeat Count			
Name	Input Value		
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	65		
HwTqArb_HwTq1StallCnt_Cnt_M_u08	171		
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	55		
HwTqArb_HwTq2StallCnt_Cnt_M_u08	13		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	0		
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	151		
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	1		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	84		
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	2		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	151	151	✓
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✓
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	84	84	✓
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✓
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✓

T				
Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

TEST DETAILS REPORT



Test Step 2.27 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	88		
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0		
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	251		
HwTqArb_HwTq2StallCnt_Cnt_M_u08	139		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	1		
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	119		
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	2		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	138		
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	0		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	119	119	✔
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	138	138	✔
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✔

Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

Test Step 2.28 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	10		
HwTqArb_HwTq1StallCnt_Cnt_M_u08	255		
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	247		
HwTqArb_HwTq2StallCnt_Cnt_M_u08	245		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	2		
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	76		
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	1		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	20		
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	2		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	76	76	✔
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	20	20	✔
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✔

Actual Function	Count	Expected Function	Count	Result
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓

Test Step 2.29 (Repeat Count = 1)

Name	Input Value
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	227
HwTqArb_HwTq1StallCnt_Cnt_M_u08	223
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	223
HwTqArb_HwTq2StallCnt_Cnt_M_u08	57
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn
target_HwTqArbn_Per1_HwTq1Qlfr_State_enum.value	1
target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08.value	159
target_HwTqArbn_Per1_HwTq2Qlfr_State_enum.value	2

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Name	Input Value		
target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08.value	162		
target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16.value	3		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1Qlfr_State_enum	target_HwTqArbn_Per1_HwTq1Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq1RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2Qlfr_State_enum	target_HwTqArbn_Per1_HwTq2Qlfr_State_enum		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08	target_HwTqArbn_Per1_HwTq2RollgCntr_Cnt_u08		
target_Rte_Inst_Sa_HwTqArbn.HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16	target_HwTqArbn_Per1_HwTqCorrinSts_Cnt_u16		
Name	Actual Value	Expected Value	Result
HwTqArb_HwTq1LstRollgCnt_Cnt_M_u08	159	159	✔
HwTqArb_HwTq1StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTq2LstRollgCnt_Cnt_M_u08	162	162	✔
HwTqArb_HwTq2StallCnt_Cnt_M_u08	0	0	✔
HwTqArb_HwTqCh1Avl_Cnt_M_lgc	0	0	✔

T					✓
Actual Function	Count	Expected Function	Count	Result	
ArbnSigAvlChk	2	ArbnSigAvlChk	2	✓	

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HwTrqArbn_SCom_SetHwTrqArbOffsetTrim



Project	HwTqArbn
Module	HwTqArbn
Test Object	HwTrqArbn_SCom_SetHwTrqArbOffsetTrim

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MCC Coverage	100 %
MC/DC Coverage	100 %

Statistics

Total Testcases	2
Successful	2 ✓
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\HwTqArbn_2TqADAS_
Configuration File	D:\Synergy_Work_Area\HwTqArbn_2TqADAS_UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\${SOURCEROOT}\Sa_HwTqArbn.c
Compiler Options	-D_DATA_ACCESS=-D_STATIC=-D_inline=-Dconst=-I\$(PROJECTROOT)\Inputs\utp\contract\Sa_HwTqArbn -I\$(PROJECTROOT)\Inputs\utp\contract -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include -I\$(Compiler Install Path)\include

Comments/Description/Specification

Name	Text
Module 'HwTqArbn'	*****Unit Test Information***** Name of Tester:Ghazala Parvin Ansari Code File(s) Under Test:Sa_HwTqArbn.c Code File(s) Version:3 Module Design Document:HwTqArbn_MDD.doc Module Design Document Version:2 Data Dictionary Version:1 Unit Test Plan Version: 3 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/ EPS Library 1.32 Total FLASH Used (Bytes): 604 Total RAM Used (Bytes): 12 Total CALS Used (Bytes): 4 Special Test Requirements:NA Test Date:10/26/2016 Comments: "NOTE1: Inline functions defined in GlobalMacro.h are not unit tested. NOTE2: ""CBD_Sandbox_dbg.map""map file is embedded for reference." *****

Attributes

Name	Value
Compiler Install Path	\${ProgramFiles}\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\${PROJECTROOT}\UnitTestEnv\static_build_files\obj
InitSrcDir	\${PROJECTROOT}\UnitTestEnv\static_build_files\src
Linker File	\${PROJECTROOT}\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	\${PROJECTROOT}\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_PS.tpl
Target Install Path	\${ProgramFiles}\pls\UDE 4.4
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1

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HwTrqArbn_SCom_SetHwTrqArbOffsetTrim



Attributes	
Name	Value
Timer Unit	Cycles
UDE Config File	\${PROJECTROOT}\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\HwTrqArbn_2TqADAS\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

TEST DETAILS REPORT

HwTrqArbn_SCom_SetHwTrqArbOffsetTrim

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Test Case 1: Metrics Test

Specification	Performance Metrics (With None Instrumentation and WithPS Environment) CPU Cycles: TS1.1 34.00 Cycles TS1.2 592.00 Cycles
Description	Vector Description: TS1.1"Shortest Path: if(Abs_f32_m(HwTqArb_HwTqCh1PrevVal_HwNm_M_f32) <= k_HwTqArb_HwTqCh1MaxOfstTrm_HwNm_f32)==true" TS1.2"Longest Path: if(Abs_f32_m(HwTqArb_HwTqCh1PrevVal_HwNm_M_f32) <= k_HwTqArb_HwTqCh1MaxOfstTrm_HwNm_f32)==false"

Test Step 1.1 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	-10		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
k_HwTqArb_HwTqCh1MaxOfstTrm_HwNm_f32	0		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	-10		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	0		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	-10	-10	✔
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	0	0	✔

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 1.2 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	10		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
k_HwTqArb_HwTqCh1MaxOfstTrm_HwNm_f32	13.114		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	10		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	0		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	10	10	✓
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	1	1	✓

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Sa_HwTqArbn_HwTqArbnEOLCh1OffsetTrim_WriteBlock	1	Rte_Call_Sa_HwTqArbn_HwTqArbnEOLCh1OffsetTrim_WriteBlock	1	✓

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HwTrqArbn_SCom_SetHwTrqArbOffsetTrim



Test Case 2: Range Test

Specification Performance Metrics
(With None Instrumentation and WithPS Environment)

CPU Cycles:

TS2.1 34.00 Cycles
TS2.2 525.00 Cycles
TS2.3 34.00 Cycles
TS2.4 508.00 Cycles
TS2.5 508.00 Cycles
TS2.6 34.00 Cycles
TS2.7 508.00 Cycles
TS2.8 34.00 Cycles

Description Vector Description:

TS2.1All Min
TS2.2All Max
TS2.3HwTrqArb_HwTqCh1PrevVal_HwNm_M_f32==>Min
TS2.4HwTrqArb_HwTqCh1PrevVal_HwNm_M_f32==>Max
TS2.5HwTrqArb_HwTqCh1PrevVal_HwNm_M_f32==>Pos
TS2.6k_HwTrqArb_HwTqCh1MaxOfstTrm_HwNm_f32==>Min
TS2.7k_HwTrqArb_HwTqCh1MaxOfstTrm_HwNm_f32==>Max
TS2.8k_HwTrqArb_HwTqCh1MaxOfstTrm_HwNm_f32==>Pos/Default

Test Step 2.1 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	-10		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
k_HwTqArb_HwTqCh1MaxOfstTrm_HwNm_f32	0		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	-10		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	0		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	-10	-10	✓
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	0	0	✓

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.2 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	10		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
k_HwTqArb_HwTqCh1MaxOfstTrm_HwNm_f32	20		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	10		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	0		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	10	10	✔
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	1	1	✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Sa_HwTqArbn_HwTqArbnEOLCh1OffsetTrim_WriteBlock	1	Rte_Call_Sa_HwTqArbn_HwTqArbnEOLCh1OffsetTrim_WriteBlock	1	✓

Test Step 2.3 (Repeat Count = 1)

Name	Input Value		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	-10		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
k_HwTqArb_HwTqCh1MaxOfstTrm_HwNm_f32	4.786		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	-10		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	0		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	-10	-10	✓
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	0	0	✓

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HwTrqArbn_SCom_SetHwTrqArbOffsetTrim

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.4 (Repeat Count = 1)			
Name	Input Value		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	10		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
k_HwTqArb_HwTqCh1MaxOfstTrm_HwNm_f32	13.114		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	10		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	0		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	10	10	✓
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	1	1	✓

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Sa_HwTqArbn_HwTqArbnEOLCh1OffsetTrim_WriteBlock	1	Rte_Call_Sa_HwTqArbn_HwTqArbnEOLCh1OffsetTrim_WriteBlock	1	✓

Test Step 2.5 (Repeat Count = 1)			
Name	Input Value		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	5.124		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
k_HwTqArb_HwTqCh1MaxOfstTrm_HwNm_f32	19.21		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	5.124		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	0		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	5.12400007	5.124	✓
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	1	1	✓

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Sa_HwTqArbn_HwTqArbnEOLCh1OffsetTrim_WriteBlock	1	Rte_Call_Sa_HwTqArbn_HwTqArbnEOLCh1OffsetTrim_WriteBlock	1	✓

Test Step 2.6 (Repeat Count = 1)			
Name	Input Value		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	1.452		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
k_HwTqArb_HwTqCh1MaxOfstTrm_HwNm_f32	0		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	1.452		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	0		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData	target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	1.45200002	1.452	✓
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	0	0	✓

T				
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✓

Test Step 2.7 (Repeat Count = 1)			
Name	Input Value		
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32	4.568		
Rte_Inst_Sa_HwTqArbn	target_Rte_Inst_Sa_HwTqArbn		
k_HwTqArb_HwTqCh1MaxOfstTrm_HwNm_f32	20		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	4.568		
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	0		

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HwTrqArbn_SCom_SetHwTrqArbOffsetTrim

Name		Input Value		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData		target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name		Actual Value	Expected Value	Result
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm		4.56799984	4.568	✓
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn		1	1	✓

T					✓
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_Sa_HwTqArbn_HwTqArbnEOLCh1OffsetTrim_WriteBlock	1	Rte_Call_Sa_HwTqArbn_HwTqArbnEOLCh1OffsetTrim_WriteBlock	1		✓

Test Step 2.8 (Repeat Count = 1)					✓
Name		Input Value			
HwTqArb_HwTqCh1PrevVal_HwNm_M_f32		7.104			
Rte_Inst_Sa_HwTqArbn		target_Rte_Inst_Sa_HwTqArbn			
k_HwTqArb_HwTqCh1MaxOfstTrm_HwNm_f32		0.54348			
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm		7.104			
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn		0			
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData		target_Pim_HwTqArbnEOLCh1OffsetTrimData			
Name		Actual Value	Expected Value	Result	
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm		7.10400009	7.104		✓
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn		0	0		✓

T					✓
Actual Function	Count	Expected Function	Count	Result	
none	0	*** No Call Expected ***	0		✓

TEST DETAILS REPORT

2016-10-26, 19:57:13+0530



HwTrqArbn_SCom_ClrHwTrqArbOffsetTrim

Project	HwTqArbn
Module	HwTqArbn
Test Object	HwTrqArbn_SCom_ClrHwTrqArbOffsetTrim

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

Statistics

Total Testcases	1
Successful	1 ✓
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\HwTqArbn_2TqADAS_
Configuration File	D:\Synergy_Work_Area\HwTqArbn_2TqADAS_UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(SOURCEROOT)\Sa_HwTqArbn.c
Compiler Options	-D_DATA_ACCESS=-D_STATIC=-D_inline=-Dconst=-I\$(PROJECTROOT)\Inputs\utp\contract\Sa_HwTqArbn -I\$(PROJECTROOT)\Inputs\utp\contract -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include -I\$(Compiler Install Path)\include

Comments/Description/Specification

Name	Text
Module 'HwTqArbn'	*****Unit Test Information***** Name of Tester:Ghazala Parvin Ansari Code File(s) Under Test:Sa_HwTqArbn.c Code File(s) Version:3 Module Design Document:HwTqArbn_MDD.doc Module Design Document Version:2 Data Dictionary Version:1 Unit Test Plan Version: 3 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/ EPS Library 1.32 Total FLASH Used (Bytes): 604 Total RAM Used (Bytes): 12 Total CALS Used (Bytes): 4 Special Test Requirements:NA Test Date:10/26/2016 Comments: "NOTE1: Inline functions defined in GlobalMacro.h are not unit tested. NOTE2: ""CBD_Sandbox_dbg.map""map file is embedded for reference." *****

Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_PS.tpl
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
Timer Unit	Cycles
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg

TEST DETAILS REPORT

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HwTrqArbn_SCom_ClrHwTrqArbOffsetTrim



Workspace File

D:\Synergy_Work_Area\HwTqArbn_2TqADAS_\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

TEST DETAILS REPORT

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HwTrqArbn_SCom_ClrHwTrqArbOffsetTrim

Test Case 1: Range Test

Specification Performance Metrics
(With None Instrumentation and WithPS Environment)

CPU Cycles:
TS1.1 539.00 Cycles

Description Vector Description:

TS1.1Check for output

Test Step 1.1 (Repeat Count = 1)

Name		Input Value		
Rte_Inst_Sa_HwTqArbn		target_Rte_Inst_Sa_HwTqArbn		
target_Rte_Inst_Sa_HwTqArbn.Pim_HwTqArbnEOLCh1OffsetTrimData		target_Pim_HwTqArbnEOLCh1OffsetTrimData		
Name	Actual Value	Expected Value	Result	
HwTrqArbn_SCom_ClrHwTrqArbOffsetTrim()	0	0	✓	
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrim_HwNm	0	0	✓	
target_Pim_HwTqArbnEOLCh1OffsetTrimData.HwTqArb_EOLChOffsetTrimPerf_Cn	0	0	✓	

T

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Sa_HwTqArbn_HwTqArbnEOLCh1OffsetTrim_WriteBlock	1	Rte_Call_Sa_HwTqArbn_HwTqArbnEOLCh1OffsetTrim_WriteBlock	1	✓