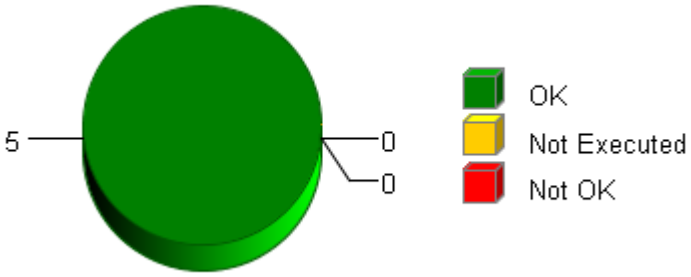
Summary

Total Test Objects:	5
Successful:	5
Failed:	0
Not Executed:	0
Date:	2015-03-10
Time:	17:32:20+0530

Overall Test Object Results (including Coverage)



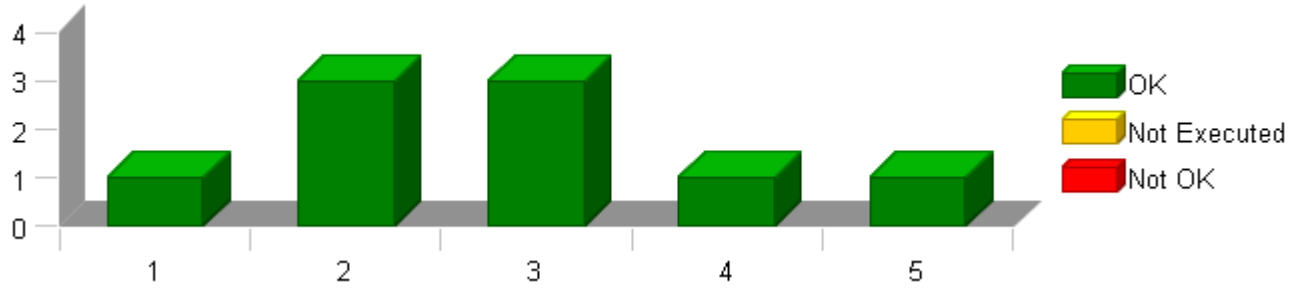
Selected Project Items

Test Object "CBD_UnitTest/TmprlMon/TmprlMon_Per1"
Test Object "CBD_UnitTest/TmprlMon/TmprlMon_Per2"
Test Object "CBD_UnitTest/TmprlMon/TmprlMon_Per3"
Test Object "CBD_UnitTest/TmprlMon/TmprlMon_Trns1"
Test Object "CBD_UnitTest/TmprlMon/TmprlMon_Trns2"

Used Test Environments

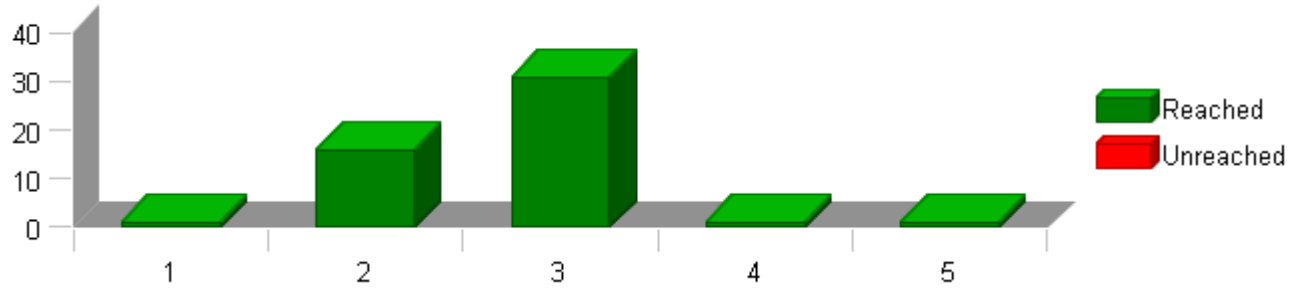
TI TMS 570 PLS UDE (Default)

Test Case Results for Each Test Object (without Coverage)



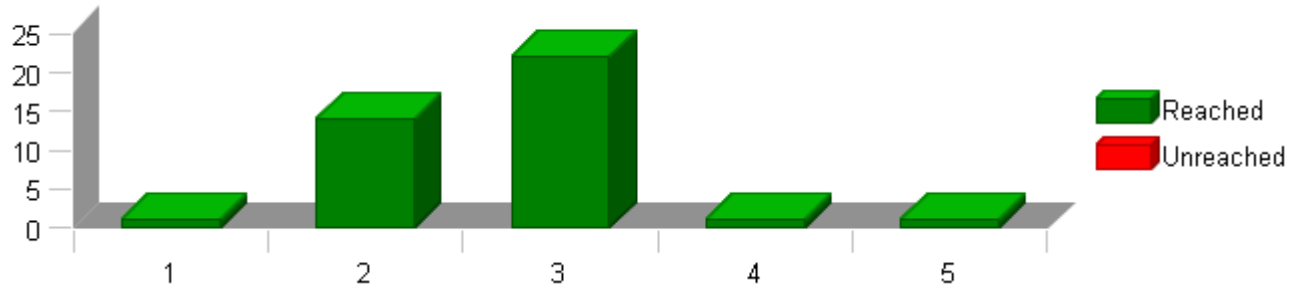
The table above shows each test object on the x axis and the number of test cases of the respective test object on the y axis. Each bar is divided into passed, not executed and failed test cases. The test case results do not take into account any coverage result (i.e. if all test cases of a test object are passed in this table but the coverage is failed, the overall test object result will be failed).

Statement (C0) Coverage: Total Statements for Each Test Object



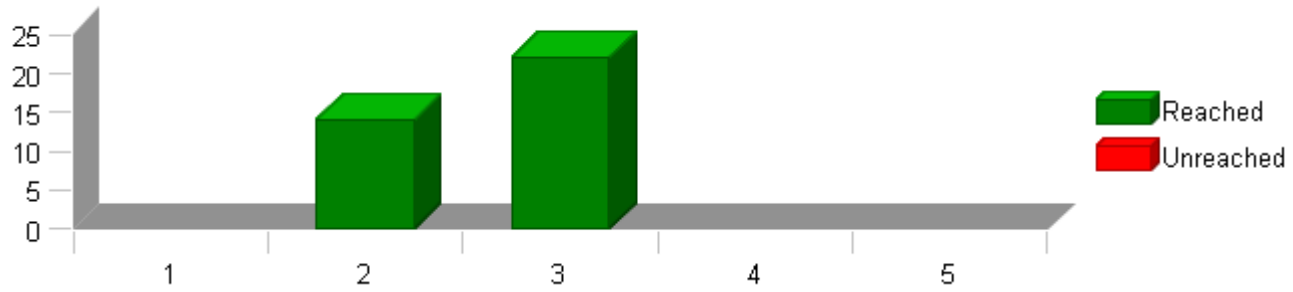
The table above shows each test object on the x axis and the number of statements of the respective test object on the y axis. Each bar is divided into reached statements (i.e. statements that have been executed during the test) and unreached statements.

Branch (C1) Coverage: Total Branches for Each Test Object



The table above shows each test object on the x axis and the number of branches of the respective test object on the y axis. Each bar is divided into reached branches (i.e. branches that have been executed during the test) and unreached branches.

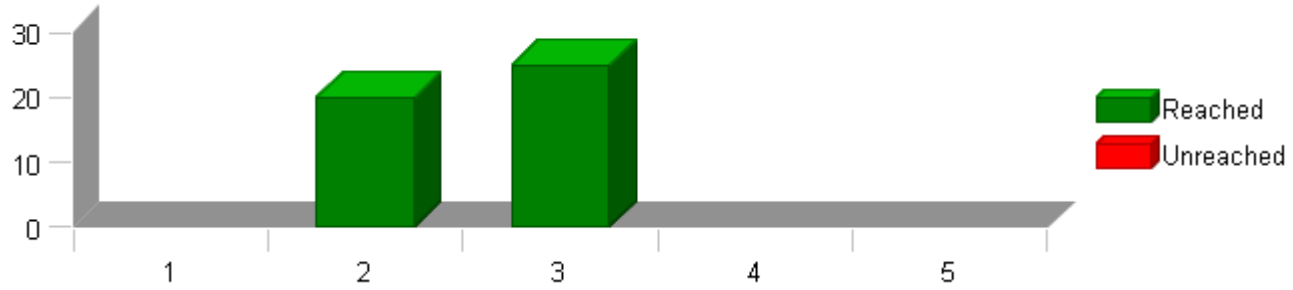
Decision Coverage: Total Decision Outcomes for Each Test Object



The table above shows test objects on the x axis and the number of possible outcomes of all decisions of the respective test object on the y axis. To achieve full DC coverage, each decision must evaluate to both true and false.

Each bar is divided into reached and unreached decision outcomes.

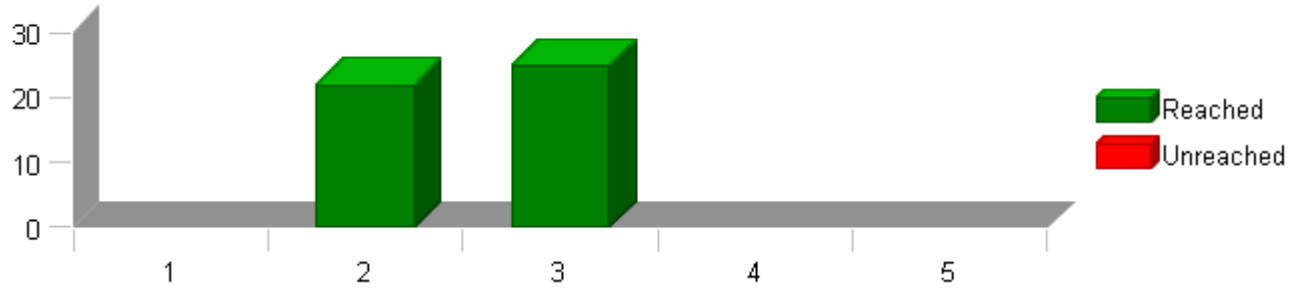
MC/DC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MC/DC coverage, each decision requires all contained atomic conditions to evaluate to both true and false independently of all other conditions. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

MCC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MCC coverage, each decision requires all contained atomic conditions to evaluate to all possible combinations of true and false values. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

Test Object List

The following table lists all test objects with their test case and coverage results. The cumulated results for modules, folders and test collections are also displayed, the indentation within the name column indicates the parent relationship of the elements.

Please note that only test objects are numbered within the first column. This number is referenced on the x axis within the overview charts for test case and coverage results available on previous pages (if included into the report).

No.	Name	C0	C1	DC	MC/DC	MCC	Test Cases	Result
	TmprlMon	100 %	100 %	100 %	100 %	100 %	9 of 9 passed	✔
	CBD_UnitTest	100 %	100 %	100 %	100 %	100 %	9 of 9 passed	✔
	TmprlMon	100 %	100 %	100 %	100 %	100 %	9 of 9 passed	✔
1	TmprlMon_Per1	100 %	100 %	-	-	-	1 of 1 passed	✔
2	TmprlMon_Per2	100 %	100 %	100 %	100 %	100 %	3 of 3 passed	✔
3	TmprlMon_Per3	100 %	100 %	100 %	100 %	100 %	3 of 3 passed	✔
4	TmprlMon_Trns1	100 %	100 %	-	-	-	1 of 1 passed	✔
5	TmprlMon_Trns2	100 %	100 %	-	-	-	1 of 1 passed	✔

TEST DETAILS REPORT

TmprlMon_Per1

2015-03-10, 17:25:01+0530

Project	TmprlMon
Module	TmprlMon
Test Object	TmprlMon_Per1

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

Statistics

Total Testcases	1
Successful	1
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\FORD_TmprlMon
Configuration File	D:\Synergy_Work_Area\FORD_TmprlMon\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\TmprlMon\src\Sa_TmprlMon.c
Compiler Options	-Dconst= -D_DATA_ACCESS= -DSKIP_MAGIC_NUMBER= -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\TmprlMon\utp \contract -I$(PROJECTROOT)\TmprlMon\utp\contract\Sa_TmprlMon -I$(PROJECTROOT)\StdDef\include -I$(Compiler Install Path)\include

Comments/Description/Specification

Name	Text
Module 'TmprlMon'	**********UNIT TEST DESCRIPTION********** Name of Tester:Raghav tripathi Code File(s) Under Test:Sa_TmprlMon.c Code File(s) Version:15 Module Design Document:Temporal_Monitor_MDD.docx Module Design Document Version:15 Data Dictionary Version:8 Unit Test Plan Version:8 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.31 Total FLASH Used (Bytes):980 Total RAM Used (Bytes):14 Total CALS Used (Bytes):6 Special Test Requirements: Test Date:3/10/2015 Comments:NOTE1:Inline functions defined in globalmacro.h are not Unit Tested. NOTE2:"CBD_Sandbox_dbg.map" map file is embedded for reference. **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(ProgramFiles)\pls\UDE 3.2
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg

Workspace File	D:\Synergy_Work_Area\FORD_TmprlMon\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Path Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:

TS1.1 1936 Cycles
```

Description

Vector Description

TS1.1 Check for call trace

Test Step 1.1 (Repeat Count = 1)

T

Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per1_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per1_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_WdMonitor_OP_SET	1	Rte_Call_Sa_TmprlMon_WdMonitor_OP_SET	1	✔
Rte_Call_TmprlMon_Per1_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per1_CP1_CheckpointReached	1	✔

TEST DETAILS REPORT

TmprlMon_Trns1

2015-03-10, 17:29:46+0530

Project	TmprlMon
Module	TmprlMon
Test Object	TmprlMon_Trns1

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

Statistics

Total Testcases	1
Successful	1
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\FORD_TmprlMon
Configuration File	D:\Synergy_Work_Area\FORD_TmprlMon\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\TmprlMon\src\Sa_TmprlMon.c
Compiler Options	-Dconst= -D_DATA_ACCESS= -DSKIP_MAGIC_NUMBER= -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\TmprlMon\utp \contract -I$(PROJECTROOT)\TmprlMon\utp\contract\Sa_TmprlMon -I$(PROJECTROOT)\StdDef\include -I$(Compiler Install Path)\include

Comments/Description/Specification

Name	Text
Module 'TmprlMon'	**********UNIT TEST DESCRIPTION********** Name of Tester:Raghav tripathi Code File(s) Under Test:Sa_TmprlMon.c Code File(s) Version:15 Module Design Document:Temporal_Monitor_MDD.docx Module Design Document Version:15 Data Dictionary Version:8 Unit Test Plan Version:8 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.31 Total FLASH Used (Bytes):980 Total RAM Used (Bytes):14 Total CALS Used (Bytes):6 Special Test Requirements: Test Date:3/10/2015 Comments:NOTE1:Inline functions defined in globalmacro.h are not Unit Tested. NOTE2:"CBD_Sandbox_dbg.map" map file is embedded for reference. **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(ProgramFiles)\pls\UDE 3.2
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg

Workspace File	D:\Synergy_Work_Area\FORD_TmprlMon\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Boundary Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:

TS1.1 1005 Cycles
TS1.2 982 Cycles
TS1.3 981 Cycles
TS1.4 981 Cycles
TS1.5 981 Cycles
```

Description

Vector Description

TS1.1 GetSystemTime_mS_u32 = min
TS1.2 GetSystemTime_mS_u32 = max
TS1.3 GetSystemTime_mS_u32 = mid
TS1.4 all min
TS1.5 all max

Test Step 1.1 (Repeat Count = 1)

Name	Input Value
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	0
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Trns1_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Trns1_TMFTestComplete_Cnt_lgc

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	0	0 ± 1	✔
InitialTime_mS_M_u32	0	0 ± 1	✔
NTCStatusByte_Cnt_M_u08	0	0 ± 1	✔
TMFTestComplete_Cnt_M_lgc	0	0	✔
TmprlMonSt_Cnt_M_enum	TMPMON_RESET1	TMPMON_RESET1 ± 1	✔
tgt_TmprlMon_Trns1_TMFTestComplete_Cnt_lgc.value	0	0	✔

T

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔

Test Step 1.2 (Repeat Count = 1)

Name	Input Value
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	4294967295
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Trns1_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Trns1_TMFTestComplete_Cnt_lgc

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	0	0 ± 1	✔
InitialTime_mS_M_u32	4294967295	4294967295	✔
NTCStatusByte_Cnt_M_u08	0	0 ± 1	✔
TMFTestComplete_Cnt_M_lgc	0	0	✔
TmprlMonSt_Cnt_M_enum	TMPMON_RESET1	TMPMON_RESET1 ± 1	✔
tgt_TmprlMon_Trns1_TMFTestComplete_Cnt_lgc.value	0	0	✔

T

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔

Test Step 1.3 (Repeat Count = 1)

Name	Input Value
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	424242
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Trns1_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Trns1_TMFTestComplete_Cnt_lgc

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	0	0 ± 1	✔
InitialTime_mS_M_u32	424242	424242	✔
NTCStatusByte_Cnt_M_u08	0	0 ± 1	✔
TMFTestComplete_Cnt_M_lgc	0	0	✔
TmprlMonSt_Cnt_M_enum	TMPMON_RESET1	TMPMON_RESET1 ± 1	✔
tgt_TmprlMon_Trns1_TMFTestComplete_Cnt_lgc.value	0	0	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔

Test Step 1.4 (Repeat Count = 1)			✔
Name	**Input Value**		
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren		
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon		
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	0		
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Trns1_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Trns1_TMFTestComplete_Cnt_lgc		
Name	**Actual Value**	**Expected Value**	**Result**
InitTestStatus_Cnt_M_enum	0	0 ± 1	✔
InitialTime_mS_M_u32	0	0	✔
NTCStatusByte_Cnt_M_u08	0	0 ± 1	✔
TMFTestComplete_Cnt_M_lgc	0	0	✔
TmprlMonSt_Cnt_M_enum	TMPMON_RESET1	TMPMON_RESET1 ± 1	✔
tgt_TmprlMon_Trns1_TMFTestComplete_Cnt_lgc.value	0	0	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔

Test Step 1.5 (Repeat Count = 1)			✔
Name	**Input Value**		
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren		
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon		
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	4294967295		
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Trns1_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Trns1_TMFTestComplete_Cnt_lgc		
Name	**Actual Value**	**Expected Value**	**Result**
InitTestStatus_Cnt_M_enum	0	0 ± 1	✔
InitialTime_mS_M_u32	4294967295	4294967295	✔
NTCStatusByte_Cnt_M_u08	0	0 ± 1	✔
TMFTestComplete_Cnt_M_lgc	0	0	✔
TmprlMonSt_Cnt_M_enum	TMPMON_RESET1	TMPMON_RESET1 ± 1	✔
tgt_TmprlMon_Trns1_TMFTestComplete_Cnt_lgc.value	0	0	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔

TEST DETAILS REPORT

TmprlMon_Per3

2015-03-10, 17:28:58+0530

Project	TmprlMon
Module	TmprlMon
Test Object	TmprlMon_Per3

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MCC Coverage	100 %
MC/DC Coverage	100 %

Statistics

Total Testcases	3
Successful	3
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\FORD_TmprlMon
Configuration File	D:\Synergy_Work_Area\FORD_TmprlMon\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\TmprlMon\src\Sa_TmprlMon.c
Compiler Options	-Dconst= -D_DATA_ACCESS= -DSKIP_MAGIC_NUMBER= -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\TmprlMon\utp \contract -I$(PROJECTROOT)\TmprlMon\utp\contract\Sa_TmprlMon -I$(PROJECTROOT)\StdDef\include -I$(Compiler Install Path)\include

Comments/Description/Specification

Name	Text
Module 'TmprlMon'	**********UNIT TEST DESCRIPTION********** Name of Tester:Raghav tripathi Code File(s) Under Test:Sa_TmprlMon.c Code File(s) Version:15 Module Design Document:Temporal_Monitor_MDD.docx Module Design Document Version:15 Data Dictionary Version:8 Unit Test Plan Version:8 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.31 Total FLASH Used (Bytes):980 Total RAM Used (Bytes):14 Total CALS Used (Bytes):6 Special Test Requirements: Test Date:3/10/2015 Comments:NOTE1:Inline functions defined in globalmacro.h are not Unit Tested. NOTE2:"CBD_Sandbox_dbg.map" map file is embedded for reference. **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(ProgramFiles)\pls\UDE 3.2
Time Unit	Cycles
Timer Enabled	false

Attributes

Name	Value
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\FORD_TmprlMon\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Metrics Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:

TS1.1 8287 Cycles
TS1.2 10061 Cycles
```

Description

Vector Description

TS1.1"Shortest Execution Path -:((PwrSwitchEn_Cnt_T_lgc == TRUE) && (FetDrvCntl_Cnt_T_lgc == TRUE))==>True
&&
(TmprlMonPNAccum_Cnt_M_u16 > k_TmprlMonPstepNstep_Cnt_str>Nstep)==>False"
TS1.2"Longest Execution Path-:(SysFault2_Cnt_T_lgc == TRUE)==>FALSE && (SysFault3_Cnt_T_lgc == TRUE)
&&
((PwrSwitchEn_Cnt_T_lgc == TRUE) ==true|| (FetDrvCntl_Cnt_T_lgc == TRUE))"

Test Step 1.1 (Repeat Count = 1)

Name	Input Value
NTCStatusByte_Cnt_M_u08	0
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
TmprlMonPNAccum_Cnt_M_u16	0
k_TmprlMonPstepNstep_Cnt_str.Threshold	1
k_TmprlMonPstepNstep_Cnt_str.PStep	1
k_TmprlMonPstepNstep_Cnt_str.NStep	1
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1

Name	Actual Value	Expected Value	Result
NTCStatusByte_Cnt_M_u08	0	0 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✔
TmprlMonPNAccum_Cnt_M_u16	0	0 ± 1	✔

T

Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 1.2 (Repeat Count = 1)

Name	Input Value
NTCStatusByte_Cnt_M_u08	0
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
TmprlMonPNAccum_Cnt_M_u16	15
k_TmprlMonPstepNstep_Cnt_str.Threshold	1
k_TmprlMonPstepNstep_Cnt_str.PStep	1
k_TmprlMonPstepNstep_Cnt_str.NStep	1
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0

Name	Actual Value	Expected Value	Result
NTCStatusByte_Cnt_M_u08	12	12 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	12	12	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	1	✔
TmprlMonPNAccum_Cnt_M_u16	1	1 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Case 2: Boundary Test ✔

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:

TS2.1 8281 Cycles
TS2.2 8265 Cycles
TS2.3 8315 Cycles
TS2.4 8234 Cycles
TS2.5 8273 Cycles
TS2.6 8298 Cycles
TS2.7 8234 Cycles
TS2.8 8273 Cycles
TS2.9 8298 Cycles
TS2.10 8234 Cycles
TS2.11 8273 Cycles
TS2.12 8298 Cycles
TS2.13 8234 Cycles
TS2.14 8273 Cycles
TS2.15 10532 Cycles
TS2.16 10481 Cycles
TS2.17 9874 Cycles
TS2.18 7880 Cycles
TS2.19 10435 Cycles
TS2.20 7918 Cycles
TS2.21 10435 Cycles
TS2.22 10475 Cycles
TS2.23 10875 Cycles
TS2.24 10477 Cycles
TS2.25 8271 Cycles
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Description

Vector Description

TS2.1 All Min
TS2.2 All Max
TS2.3 TmprlMonPNAccum_Cnt_M_u16 = min
TS2.4 TmprlMonPNAccum_Cnt_M_u16 = max
TS2.5 TmprlMonPNAccum_Cnt_M_u16 = pos
TS2.6 k_TmprlMonPstepNstep_Cnt_str.Threshold = min
TS2.7 k_TmprlMonPstepNstep_Cnt_str.Threshold = max
TS2.8 k_TmprlMonPstepNstep_Cnt_str.Threshold = pos
TS2.9 k_TmprlMonPstepNstep_Cnt_str.Pstep = min
TS2.10 k_TmprlMonPstepNstep_Cnt_str.Pstep = max
TS2.11 k_TmprlMonPstepNstep_Cnt_str.Pstep = pos
TS2.12 k_TmprlMonPstepNstep_Cnt_str.Nstep = min
TS2.13 k_TmprlMonPstepNstep_Cnt_str.Nstep = max
TS2.14 k_TmprlMonPstepNstep_Cnt_str.Nstep = pos
TS2.15 NTCStatusByte_Cnt_M_u08 = min
TS2.16 NTCStatusByte_Cnt_M_u08 = max
TS2.17 NTCStatusByte_Cnt_M_u08 = pos
TS2.18 Rte_Call_SysFault2_OP_GET = min
TS2.19 Rte_Call_SysFault2_OP_GET = max
TS2.20 Rte_Call_SysFault3_OP_GET = min
TS2.21 Rte_Call_SysFault3_OP_GET = max
TS2.22 Rte_Call_PwrSwitchEn_OP_GET = min
TS2.23 Rte_Call_PwrSwitchEn_OP_GET = max
TS2.24 Rte_Call_FetDrvCntl_OP_GET = min
TS2.25 Rte_Call_FetDrvCntl_OP_GET = max

Test Step 2.1 (Repeat Count = 1) ✔

Name	Input Value
NTCStatusByte_Cnt_M_u08	0
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
TmprlMonPNAccum_Cnt_M_u16	0
k_TmprlMonPstepNstep_Cnt_str.Threshold	1
k_TmprlMonPstepNstep_Cnt_str.PStep	1
k_TmprlMonPstepNstep_Cnt_str.NStep	1
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0

Name	Actual Value	Expected Value	Result
NTCStatusByte_Cnt_M_u08	0	0 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✔
TmprlMonPNAccum_Cnt_M_u16	0	0 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 2.2 (Repeat Count = 1)			✔
Name	**Input Value**		
NTCStatusByte_Cnt_M_u08	255		
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal		
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal		
TmprlMonPNAccum_Cnt_M_u16	1000		
k_TmprlMonPstepNstep_Cnt_str.Threshold	1000		
k_TmprlMonPstepNstep_Cnt_str.PStep	50		
k_TmprlMonPstepNstep_Cnt_str.NStep	50		
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1		
Name	**Actual Value**	**Expected Value**	**Result**
NTCStatusByte_Cnt_M_u08	255	255 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✔
TmprlMonPNAccum_Cnt_M_u16	950	950 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 2.3 (Repeat Count = 1)			✔
Name	**Input Value**		
NTCStatusByte_Cnt_M_u08	0		
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal		
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal		
TmprlMonPNAccum_Cnt_M_u16	0		
k_TmprlMonPstepNstep_Cnt_str.Threshold	1		
k_TmprlMonPstepNstep_Cnt_str.PStep	1		
k_TmprlMonPstepNstep_Cnt_str.NStep	1		
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1		
Name	**Actual Value**	**Expected Value**	**Result**
NTCStatusByte_Cnt_M_u08	0	0 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✔
TmprlMonPNAccum_Cnt_M_u16	0	0 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 2.4 (Repeat Count = 1) ✔

Name	**Input Value**
NTCStatusByte_Cnt_M_u08	13
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
TmprlMonPNAccum_Cnt_M_u16	1000
k_TmprlMonPstepNstep_Cnt_str.Threshold	1000
k_TmprlMonPstepNstep_Cnt_str.PStep	50
k_TmprlMonPstepNstep_Cnt_str.NStep	50
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1

Name	**Actual Value**	**Expected Value**	**Result**
NTCStatusByte_Cnt_M_u08	13	13 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✔
TmprlMonPNAccum_Cnt_M_u16	950	950 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 2.5 (Repeat Count = 1) ✔

Name	**Input Value**
NTCStatusByte_Cnt_M_u08	4
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
TmprlMonPNAccum_Cnt_M_u16	20
k_TmprlMonPstepNstep_Cnt_str.Threshold	57
k_TmprlMonPstepNstep_Cnt_str.PStep	4
k_TmprlMonPstepNstep_Cnt_str.NStep	5
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 2.6 (Repeat Count = 1)			✔
Name	**Input Value**		
NTCStatusByte_Cnt_M_u08	0		
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal		
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal		
TmprlMonPNAccum_Cnt_M_u16	0		
k_TmprlMonPstepNstep_Cnt_str.Threshold	1		
k_TmprlMonPstepNstep_Cnt_str.PStep	1		
k_TmprlMonPstepNstep_Cnt_str.NStep	1		
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1		
Name	**Actual Value**	**Expected Value**	**Result**
NTCStatusByte_Cnt_M_u08	0	0 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✔
TmprlMonPNAccum_Cnt_M_u16	0	0 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 2.7 (Repeat Count = 1)			✔
Name	**Input Value**		
NTCStatusByte_Cnt_M_u08	120		
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal		
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal		
TmprlMonPNAccum_Cnt_M_u16	1000		
k_TmprlMonPstepNstep_Cnt_str.Threshold	1000		
k_TmprlMonPstepNstep_Cnt_str.PStep	50		
k_TmprlMonPstepNstep_Cnt_str.NStep	50		
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1		
Name	**Actual Value**	**Expected Value**	**Result**
NTCStatusByte_Cnt_M_u08	120	120 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✔
TmprlMonPNAccum_Cnt_M_u16	950	950 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 2.8 (Repeat Count = 1) ✔

Name	**Input Value**
NTCStatusByte_Cnt_M_u08	4
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
TmprlMonPNAccum_Cnt_M_u16	20
k_TmprlMonPstepNstep_Cnt_str.Threshold	57
k_TmprlMonPstepNstep_Cnt_str.PStep	4
k_TmprlMonPstepNstep_Cnt_str.NStep	5
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1

Name	**Actual Value**	**Expected Value**	**Result**
NTCStatusByte_Cnt_M_u08	4	4 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✔
TmprlMonPNAccum_Cnt_M_u16	15	15 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 2.9 (Repeat Count = 1) ✔

Name	**Input Value**
NTCStatusByte_Cnt_M_u08	0
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
TmprlMonPNAccum_Cnt_M_u16	0
k_TmprlMonPstepNstep_Cnt_str.Threshold	1
k_TmprlMonPstepNstep_Cnt_str.PStep	1
k_TmprlMonPstepNstep_Cnt_str.NStep	1
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1

Name	**Actual Value**	**Expected Value**	**Result**
NTCStatusByte_Cnt_M_u08	0	0 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✔
TmprlMonPNAccum_Cnt_M_u16	0	0 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 2.10 (Repeat Count = 1) ✔

Name	**Input Value**
NTCStatusByte_Cnt_M_u08	13
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
TmprlMonPNAccum_Cnt_M_u16	1000
k_TmprlMonPstepNstep_Cnt_str.Threshold	1000
k_TmprlMonPstepNstep_Cnt_str.PStep	50
k_TmprlMonPstepNstep_Cnt_str.NStep	50
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1

Name	**Actual Value**	**Expected Value**	**Result**
NTCStatusByte_Cnt_M_u08	13	13 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✔
TmprlMonPNAccum_Cnt_M_u16	950	950 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 2.11 (Repeat Count = 1) ✔

Name	**Input Value**
NTCStatusByte_Cnt_M_u08	4
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
TmprlMonPNAccum_Cnt_M_u16	20
k_TmprlMonPstepNstep_Cnt_str.Threshold	57
k_TmprlMonPstepNstep_Cnt_str.PStep	4
k_TmprlMonPstepNstep_Cnt_str.NStep	5
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1

Name	**Actual Value**	**Expected Value**	**Result**
NTCStatusByte_Cnt_M_u08	4	4 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✔
TmprlMonPNAccum_Cnt_M_u16	15	15 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 2.12 (Repeat Count = 1)			✔
Name	**Input Value**		
NTCStatusByte_Cnt_M_u08	0		
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal		
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal		
TmprlMonPNAccum_Cnt_M_u16	0		
k_TmprlMonPstepNstep_Cnt_str.Threshold	1		
k_TmprlMonPstepNstep_Cnt_str.PStep	1		
k_TmprlMonPstepNstep_Cnt_str.NStep	1		
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1		
Name	**Actual Value**	**Expected Value**	**Result**
NTCStatusByte_Cnt_M_u08	0	0 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✔
TmprlMonPNAccum_Cnt_M_u16	0	0 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 2.13 (Repeat Count = 1)			✔
Name	**Input Value**		
NTCStatusByte_Cnt_M_u08	13		
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal		
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal		
TmprlMonPNAccum_Cnt_M_u16	1000		
k_TmprlMonPstepNstep_Cnt_str.Threshold	1000		
k_TmprlMonPstepNstep_Cnt_str.PStep	50		
k_TmprlMonPstepNstep_Cnt_str.NStep	50		
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1		
Name	**Actual Value**	**Expected Value**	**Result**
NTCStatusByte_Cnt_M_u08	13	13 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✔
TmprlMonPNAccum_Cnt_M_u16	950	950 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 2.14 (Repeat Count = 1) ✔

Name	**Input Value**
NTCStatusByte_Cnt_M_u08	4
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
TmprlMonPNAccum_Cnt_M_u16	20
k_TmprlMonPstepNstep_Cnt_str.Threshold	57
k_TmprlMonPstepNstep_Cnt_str.PStep	4
k_TmprlMonPstepNstep_Cnt_str.NStep	5
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1

Name	**Actual Value**	**Expected Value**	**Result**
NTCStatusByte_Cnt_M_u08	4	4 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✔
TmprlMonPNAccum_Cnt_M_u16	15	15 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 2.15 (Repeat Count = 1) ✔

Name	**Input Value**
NTCStatusByte_Cnt_M_u08	0
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
TmprlMonPNAccum_Cnt_M_u16	0
k_TmprlMonPstepNstep_Cnt_str.Threshold	1
k_TmprlMonPstepNstep_Cnt_str.PStep	1
k_TmprlMonPstepNstep_Cnt_str.NStep	1
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1

Name	**Actual Value**	**Expected Value**	**Result**
NTCStatusByte_Cnt_M_u08	3	3 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	3	3	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	1	✔
TmprlMonPNAccum_Cnt_M_u16	1	1 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 2.16 (Repeat Count = 1)			✔
Name	**Input Value**		
NTCStatusByte_Cnt_M_u08	255		
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal		
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal		
TmprlMonPNAccum_Cnt_M_u16	1000		
k_TmprlMonPstepNstep_Cnt_str.Threshold	1000		
k_TmprlMonPstepNstep_Cnt_str.PStep	50		
k_TmprlMonPstepNstep_Cnt_str.NStep	50		
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0		
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0		
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1		
Name	**Actual Value**	**Expected Value**	**Result**
NTCStatusByte_Cnt_M_u08	255	255 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	255	255	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	1	✔
TmprlMonPNAccum_Cnt_M_u16	1000	1000 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 2.17 (Repeat Count = 1)			✔
Name	**Input Value**		
NTCStatusByte_Cnt_M_u08	4		
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal		
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal		
TmprlMonPNAccum_Cnt_M_u16	20		
k_TmprlMonPstepNstep_Cnt_str.Threshold	57		
k_TmprlMonPstepNstep_Cnt_str.PStep	4		
k_TmprlMonPstepNstep_Cnt_str.NStep	5		
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0		
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0		
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1		
Name	**Actual Value**	**Expected Value**	**Result**
NTCStatusByte_Cnt_M_u08	7	7 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	255	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	*none*	✔
TmprlMonPNAccum_Cnt_M_u16	24	24 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 2.18 (Repeat Count = 1)			✔
Name	**Input Value**		
NTCStatusByte_Cnt_M_u08	0		
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal		
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal		
TmprlMonPNAccum_Cnt_M_u16	0		
k_TmprlMonPstepNstep_Cnt_str.Threshold	1		
k_TmprlMonPstepNstep_Cnt_str.PStep	1		
k_TmprlMonPstepNstep_Cnt_str.NStep	1		
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0		
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0		
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	0		
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1		
Name	**Actual Value**	**Expected Value**	**Result**
NTCStatusByte_Cnt_M_u08	0	0 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✔
TmprlMonPNAccum_Cnt_M_u16	0	0 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 2.19 (Repeat Count = 1)			✔
Name	**Input Value**		
NTCStatusByte_Cnt_M_u08	140		
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal		
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal		
TmprlMonPNAccum_Cnt_M_u16	1000		
k_TmprlMonPstepNstep_Cnt_str.Threshold	1000		
k_TmprlMonPstepNstep_Cnt_str.PStep	50		
k_TmprlMonPstepNstep_Cnt_str.NStep	50		
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0		
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0		
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1		
Name	**Actual Value**	**Expected Value**	**Result**
NTCStatusByte_Cnt_M_u08	143	143 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	143	143	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	1	✔
TmprlMonPNAccum_Cnt_M_u16	1000	1000 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 2.20 (Repeat Count = 1)			✔
Name	**Input Value**		
NTCStatusByte_Cnt_M_u08	0		
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal		
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal		
TmprlMonPNAccum_Cnt_M_u16	0		
k_TmprlMonPstepNstep_Cnt_str.Threshold	1		
k_TmprlMonPstepNstep_Cnt_str.PStep	1		
k_TmprlMonPstepNstep_Cnt_str.NStep	1		
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0		
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0		
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	0		
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0		
Name	**Actual Value**	**Expected Value**	**Result**
NTCStatusByte_Cnt_M_u08	0	0 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✔
TmprlMonPNAccum_Cnt_M_u16	0	0 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 2.21 (Repeat Count = 1)			✔
Name	**Input Value**		
NTCStatusByte_Cnt_M_u08	13		
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal		
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal		
TmprlMonPNAccum_Cnt_M_u16	1000		
k_TmprlMonPstepNstep_Cnt_str.Threshold	1000		
k_TmprlMonPstepNstep_Cnt_str.PStep	50		
k_TmprlMonPstepNstep_Cnt_str.NStep	50		
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0		
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0		
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1		
Name	**Actual Value**	**Expected Value**	**Result**
NTCStatusByte_Cnt_M_u08	15	15 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	15	15	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	1	✔
TmprlMonPNAccum_Cnt_M_u16	1000	1000 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 2.22 (Repeat Count = 1) ✔

Name	**Input Value**
NTCStatusByte_Cnt_M_u08	0
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
TmprlMonPNAccum_Cnt_M_u16	12
k_TmprlMonPstepNstep_Cnt_str.Threshold	1
k_TmprlMonPstepNstep_Cnt_str.PStep	1
k_TmprlMonPstepNstep_Cnt_str.NStep	1
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1

Name	**Actual Value**	**Expected Value**	**Result**
NTCStatusByte_Cnt_M_u08	3	3 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	3	3	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	1	✔
TmprlMonPNAccum_Cnt_M_u16	1	1 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 2.23 (Repeat Count = 1) ✔

Name	**Input Value**
NTCStatusByte_Cnt_M_u08	130
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
TmprlMonPNAccum_Cnt_M_u16	102
k_TmprlMonPstepNstep_Cnt_str.Threshold	100
k_TmprlMonPstepNstep_Cnt_str.PStep	50
k_TmprlMonPstepNstep_Cnt_str.NStep	5
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1

Name	**Actual Value**	**Expected Value**	**Result**
NTCStatusByte_Cnt_M_u08	131	131 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	131	131	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	1	✔
TmprlMonPNAccum_Cnt_M_u16	100	100 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 2.24 (Repeat Count = 1) ✔

Name	**Input Value**
NTCStatusByte_Cnt_M_u08	0
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
TmprlMonPNAccum_Cnt_M_u16	1
k_TmprlMonPstepNstep_Cnt_str.Threshold	1
k_TmprlMonPstepNstep_Cnt_str.PStep	1
k_TmprlMonPstepNstep_Cnt_str.NStep	1
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1

Name	**Actual Value**	**Expected Value**	**Result**
NTCStatusByte_Cnt_M_u08	3	3 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	3	3	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	1	✔
TmprlMonPNAccum_Cnt_M_u16	1	1 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 2.25 (Repeat Count = 1) ✔

Name	**Input Value**
NTCStatusByte_Cnt_M_u08	120
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
TmprlMonPNAccum_Cnt_M_u16	10
k_TmprlMonPstepNstep_Cnt_str.Threshold	10
k_TmprlMonPstepNstep_Cnt_str.PStep	4
k_TmprlMonPstepNstep_Cnt_str.NStep	5
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1

Name	**Actual Value**	**Expected Value**	**Result**
NTCStatusByte_Cnt_M_u08	120	120 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✔
TmprlMonPNAccum_Cnt_M_u16	5	5 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Case 3: Path Test ✔

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:

TS3.1 10886 Cycles
TS3.2 9903 Cycles
TS3.3 8287 Cycles
TS3.4 10061 Cycles
TS3.5 9517 Cycles
TS3.6 7960 Cycles
TS3.7 8404 Cycles
TS3.8 9957 Cycles
TS3.9 10847 Cycles
```

Description

Vector Description

TS3.1 "(SysFault2_Cnt_T_lgc == TRUE) && (SysFault3_Cnt_T_lgc == TRUE)==>TRUE
&&
((PwrSwitchEn_Cnt_T_lgc == TRUE)==>False && (FetDrvCntl_Cnt_T_lgc == TRUE))"
TS3.2 (TmprlMonPNAccum_Cnt_M_u16, <(k_TmprlMonPstepNstep_Cnt_str.Threshold-k_TmprlMonPstepNstep_Cnt_str.pstep)
TS3.3 "((PwrSwitchEn_Cnt_T_lgc == TRUE) && (FetDrvCntl_Cnt_T_lgc == TRUE))==>True
&&
(TmprlMonPNAccum_Cnt_M_u16 > k_TmprlMonPstepNstep_Cnt_str>Nstep)==>False"
TS3.4 "(SysFault2_Cnt_T_lgc == TRUE)==>FALSE && (SysFault3_Cnt_T_lgc == TRUE)
&&
((PwrSwitchEn_Cnt_T_lgc == TRUE) ==true|| (FetDrvCntl_Cnt_T_lgc == TRUE))"
TS3.5 (DiagFailed_m(TmprlMonPNAccum_Cnt_M_u16, k_TmprlMonPstepNstep_Cnt_str) == TRUE)==>False
TS3.6 ((PwrSwitchEn_Cnt_T_lgc == TRUE) || (FetDrvCntl_Cnt_T_lgc == TRUE))=>False
TS3.7 (SysFault2_Cnt_T_lgc == TRUE) && (SysFault3_Cnt_T_lgc == TRUE)==>False
TS3.8 ((PwrSwitchEn_Cnt_T_lgc == TRUE) || (FetDrvCntl_Cnt_T_lgc == TRUE)==>True)
TS3.9 ((PwrSwitchEn_Cnt_T_lgc == TRUE) ==>True&& (FetDrvCntl_Cnt_T_lgc == TRUE))

Test Step 3.1 (Repeat Count = 1) ✔

Name	**Input Value**
NTCStatusByte_Cnt_M_u08	0
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
TmprlMonPNAccum_Cnt_M_u16	15
k_TmprlMonPstepNstep_Cnt_str.Threshold	1
k_TmprlMonPstepNstep_Cnt_str.PStep	1
k_TmprlMonPstepNstep_Cnt_str.NStep	1
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1

Name	**Actual Value**	**Expected Value**	**Result**
NTCStatusByte_Cnt_M_u08	3	3 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	3	3	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	1	✔
TmprlMonPNAccum_Cnt_M_u16	1	1 ± 1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 3.2 (Repeat Count = 1)

Name	Input Value
NTCStatusByte_Cnt_M_u08	13
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
TmprlMonPNAccum_Cnt_M_u16	10
k_TmprlMonPstepNstep_Cnt_str.Threshold	1000
k_TmprlMonPstepNstep_Cnt_str.PStep	50
k_TmprlMonPstepNstep_Cnt_str.NStep	50
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1

Name	Actual Value	Expected Value	Result
NTCStatusByte_Cnt_M_u08	15	15 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	3	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	*none*	✔
TmprlMonPNAccum_Cnt_M_u16	60	60 ± 1	✔

T

Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 3.3 (Repeat Count = 1)

Name	Input Value
NTCStatusByte_Cnt_M_u08	0
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
TmprlMonPNAccum_Cnt_M_u16	0
k_TmprlMonPstepNstep_Cnt_str.Threshold	1
k_TmprlMonPstepNstep_Cnt_str.PStep	1
k_TmprlMonPstepNstep_Cnt_str.NStep	1
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1

Name	Actual Value	Expected Value	Result
NTCStatusByte_Cnt_M_u08	0	0 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✔
TmprlMonPNAccum_Cnt_M_u16	0	0 ± 1	✔

T

Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 3.4 (Repeat Count = 1)

Name	Input Value
NTCStatusByte_Cnt_M_u08	0
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
TmprlMonPNAccum_Cnt_M_u16	15
k_TmprlMonPstepNstep_Cnt_str.Threshold	1
k_TmprlMonPstepNstep_Cnt_str.PStep	1
k_TmprlMonPstepNstep_Cnt_str.NStep	1
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0

Name	Actual Value	Expected Value	Result
NTCStatusByte_Cnt_M_u08	12	12 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	12	12	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	1	✔
TmprlMonPNAccum_Cnt_M_u16	1	1 ± 1	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 3.5 (Repeat Count = 1)

Name	Input Value
NTCStatusByte_Cnt_M_u08	0
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
TmprlMonPNAccum_Cnt_M_u16	11
k_TmprlMonPstepNstep_Cnt_str.Threshold	15
k_TmprlMonPstepNstep_Cnt_str.PStep	1
k_TmprlMonPstepNstep_Cnt_str.NStep	1
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0

Name	Actual Value	Expected Value	Result
NTCStatusByte_Cnt_M_u08	12	12 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	12	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	*none*	✔
TmprlMonPNAccum_Cnt_M_u16	12	12 ± 1	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 3.6 (Repeat Count = 1)

Name	Input Value
NTCStatusByte_Cnt_M_u08	0

Name	Input Value
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
TmprlMonPNAccum_Cnt_M_u16	11
k_TmprlMonPstepNstep_Cnt_str.Threshold	15
k_TmprlMonPstepNstep_Cnt_str.PStep	1
k_TmprlMonPstepNstep_Cnt_str.NStep	1
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0

Name	Actual Value	Expected Value	Result
NTCStatusByte_Cnt_M_u08	4	4 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	0	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	0	✔
TmprlMonPNAccum_Cnt_M_u16	12	12 ± 1	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

Test Step 3.9 (Repeat Count = 1) ✔

Name	Input Value
NTCStatusByte_Cnt_M_u08	13
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
TmprlMonPNAccum_Cnt_M_u16	102
k_TmprlMonPstepNstep_Cnt_str.Threshold	100
k_TmprlMonPstepNstep_Cnt_str.PStep	50
k_TmprlMonPstepNstep_Cnt_str.NStep	5
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault2_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1

Name	Actual Value	Expected Value	Result
NTCStatusByte_Cnt_M_u08	13	13 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	65	65	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	13	13	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	1	✔
TmprlMonPNAccum_Cnt_M_u16	100	100 ± 1	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per3_CP1_CheckpointReached	1	✔

TEST DETAILS REPORT

TmprlMon_Trns2

2015-03-10, 17:30:28+0530

Project	TmprlMon
Module	TmprlMon
Test Object	TmprlMon_Trns2

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

Statistics

Total Testcases	1
Successful	1
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\FORD_TmprlMon
Configuration File	D:\Synergy_Work_Area\FORD_TmprlMon\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\TmprlMon\src\Sa_TmprlMon.c
Compiler Options	-Dconst= -D_DATA_ACCESS= -DSKIP_MAGIC_NUMBER= -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\TmprlMon\utp \contract -I$(PROJECTROOT)\TmprlMon\utp\contract\Sa_TmprlMon -I$(PROJECTROOT)\StdDef\include -I$(Compiler Install Path)\include

Comments/Description/Specification

Name	Text
Module 'TmprlMon'	**********UNIT TEST DESCRIPTION********** Name of Tester:Raghav tripathi Code File(s) Under Test:Sa_TmprlMon.c Code File(s) Version:15 Module Design Document:Temporal_Monitor_MDD.docx Module Design Document Version:15 Data Dictionary Version:8 Unit Test Plan Version:8 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.31 Total FLASH Used (Bytes):980 Total RAM Used (Bytes):14 Total CALS Used (Bytes):6 Special Test Requirements: Test Date:3/10/2015 Comments:NOTE1:Inline functions defined in globalmacro.h are not Unit Tested. NOTE2:"CBD_Sandbox_dbg.map" map file is embedded for reference. **********
Test Object 'TmprlMon_Trns2'	

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(ProgramFiles)\pls\UDE 3.2
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg

Attributes

Name	Value
Workspace File	D:\Synergy_Work_Area\FORD_TmprlMon\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Path Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:

TS1.1 1048 Cycles
```

Description Vector Description

TS1.1 Check for call trace

Test Step 1.1 (Repeat Count = 1)

T

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔

TEST DETAILS REPORT

TmprlMon_Per2

2015-03-10, 17:27:09+0530

Project	TmprlMon
Module	TmprlMon
Test Object	TmprlMon_Per2

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MCC Coverage	100 %
MC/DC Coverage	100 %

Statistics

Total Testcases	3
Successful	3
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\FORD_TmprlMon
Configuration File	D:\Synergy_Work_Area\FORD_TmprlMon\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\TmprlMon\src\Sa_TmprlMon.c
Compiler Options	-Dconst= -D_DATA_ACCESS= -DSKIP_MAGIC_NUMBER= -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\TmprlMon\utp \contract -I$(PROJECTROOT)\TmprlMon\utp\contract\Sa_TmprlMon -I$(PROJECTROOT)\StdDef\include -I$(Compiler Install Path)\include

Comments/Description/Specification

Name	Text
Module 'TmprlMon'	**********UNIT TEST DESCRIPTION********** Name of Tester:Raghav tripathi Code File(s) Under Test:Sa_TmprlMon.c Code File(s) Version:15 Module Design Document:Temporal_Monitor_MDD.docx Module Design Document Version:15 Data Dictionary Version:8 Unit Test Plan Version:8 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.31 Total FLASH Used (Bytes):980 Total RAM Used (Bytes):14 Total CALS Used (Bytes):6 Special Test Requirements: Test Date:3/10/2015 Comments:NOTE1:Inline functions defined in globalmacro.h are not Unit Tested. NOTE2:"CBD_Sandbox_dbg.map" map file is embedded for reference. **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(ProgramFiles)\pls\UDE 3.2
Time Unit	Cycles
Timer Enabled	false

Attributes

Name	Value
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\FORD_TmprlMon\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

TEST DETAILS REPORT

TmprlMon_Per2

2015-03-10, 17:27:09+0530

Test Case 1: Metrics Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:

TS1.1 7090 Cycles
TS1.2 13463 Cycles
```

Description

Vector Description

TS1.1Shortest Execution Path -: (TMFPrepCheckFlag_Cnt_M_lgc == FALSE) = True
TS1.2"Longest Execution Path -: (TMFPrepCheckFlag_Cnt_M_lgc == FALSE) = False, ((TmprlMonSt_Cnt_T_enum < TMPMON_OPERATE) &&
(TMFTestStart_Cnt_T_lgc == TRUE)) = True, ((ElapsedTime_T_mS_u16 >=
TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].StepTime_mS_u16) ||
(((TmprlMonSt_Cnt_T_enum == TMPMON_INIT_PICINIT1) ||
(TmprlMonSt_Cnt_T_enum == TMPMON_INIT_PICINIT2)) &&
(TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].FetDrvCntlFdbk_lgc == FetDrvCntlFdbk_Cnt_T_lgc) &&
(TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].PwrSwitchEnFdbk_lgc == PwrSwitchEnFdbk_Cnt_T_lgc))) = True"

Test Step 1.1 (Repeat Count = 1)

Name	Input Value
InitTestStatus_Cnt_M_enum	3
InitialTime_mS_M_u32	500
NTCStatusByte_Cnt_M_u08	120
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	0
TMFTestComplete_Cnt_M_lgc	1
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_SF3OFF
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	0
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	8000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	3	3 ± 1	✔
InitialTime_mS_M_u32	8000	8000 ± 1	✔
NTCStatusByte_Cnt_M_u08	120	120 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_SF3OFF	TMPMON_INIT_SF3OFF ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

T

Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 1.2 (Repeat Count = 1)

Name	Input Value
InitTestStatus_Cnt_M_enum	0
InitialTime_mS_M_u32	600
NTCStatusByte_Cnt_M_u08	9
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal

TEST DETAILS REPORT

TmprlMon_Per2

2015-03-10, 17:27:09+0530

Name	Input Value
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	1
TMFTestComplete_Cnt_M_lgc	0
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	65535
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	9000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	9000	9000 ± 1	✔
NTCStatusByte_Cnt_M_u08	203	203 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	64	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	203	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_OPERATE	TMPMON_OPERATE ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Case 2: Boundary Test ✔

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:

TS2.1 13611 Cycles
TS2.2 7097 Cycles
TS2.3 7085 Cycles
TS2.4 7063 Cycles
TS2.5 7063 Cycles
TS2.6 7063 Cycles
TS2.7 7107 Cycles
TS2.8 7063 Cycles
TS2.9 7063 Cycles
TS2.10 7063 Cycles
TS2.11 7107 Cycles
TS2.12 7107 Cycles
TS2.13 10545 Cycles
TS2.14 13447 Cycles
TS2.15 13090 Cycles
TS2.16 7105 Cycles
TS2.17 7105 Cycles
TS2.18 7090 Cycles
TS2.19 7090 Cycles
TS2.20 7090 Cycles
TS2.21 7090 Cycles
TS2.22 13463 Cycles
TS2.23 7104 Cycles
TS2.24 7104 Cycles
TS2.25 7104 Cycles
TS2.26 7085 Cycles
TS2.27 7063 Cycles
TS2.28 7107 Cycles
TS2.29 7063 Cycles
TS2.30 6814 Cycles
```

Description

Vector Description

TS2.1 TmprlMonSt_Cnt_M_enum = min
TS2.2 TmprlMonSt_Cnt_M_enum = max
TS2.3 InitTestStatus_Cnt_M_enum = min
TS2.4 InitTestStatus_Cnt_M_enum = max
TS2.5 InitialTime_mS_M_u32 = min
TS2.6 InitialTime_mS_M_u32 = max
TS2.7 InitialTime_mS_M_u32 = mid
TS2.8 NTCStatusByte_Cnt_M_u08 = min
TS2.9 NTCStatusByte_Cnt_M_u08 = max
TS2.10 NTCStatusByte_Cnt_M_u08 = mid
TS2.11 TMFTestStart_Cnt_lgc = min
TS2.12 TMFTestStart_Cnt_lgc = max
TS2.13 DtrmnElapsedTime_mS_u16 = min
TS2.14 DtrmnElapsedTime_mS_u16 = max
TS2.15 DtrmnElapsedTime_mS_u16 = mid
TS2.16 GetSystemTime_mS_u32 = min
TS2.17 GetSystemTime_mS_u32 = max
TS2.18 GetSystemTime_mS_u32 = mid
TS2.19 TMFTestComplete_Cnt_M_lgc = min
TS2.20 TMFTestComplete_Cnt_M_lgc max
TS2.21 TMFPrepCheckFlag_Cnt_M_lgc min
TS2.22 TMFPrepCheckFlag_Cnt_M_lgc max
TS2.23 Rte_Call_FetDrvCntl_OP_GET min
TS2.24 Rte_Call_FetDrvCntl_OP_GET max
TS2.25 Rte_Call_PwrSwitchEn_OP_GET min
TS2.26 Rte_Call_PwrSwitchEn_OP_GET max
TS2.27 Rte_Call_SysFault3_OP_GET min
TS2.28 Rte_Call_SysFault3_OP_GET max
TS2.29 all min
TS2.30 all max

Test Step 2.1 (Repeat Count = 1)

Name	Input Value
InitTestStatus_Cnt_M_enum	1
InitialTime_mS_M_u32	100
NTCStatusByte_Cnt_M_u08	1
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	1
TMFTestComplete_Cnt_M_lgc	1
TmprlMonSt_Cnt_M_enum	TMPMON_RESET1
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	123
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	1000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	1000	1000 ± 1	✔
NTCStatusByte_Cnt_M_u08	9	9 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_ALLOFF1	TMPMON_INIT_ALLOFF1 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 2.2 (Repeat Count = 1)

Name	Input Value
InitTestStatus_Cnt_M_enum	2
InitialTime_mS_M_u32	200
NTCStatusByte_Cnt_M_u08	24
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	0
TMFTestComplete_Cnt_M_lgc	0
TmprlMonSt_Cnt_M_enum	TMPMON_OPERATE
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	234
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	2000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	2	2 ± 1	✔

Name	Actual Value	Expected Value	Result
InitialTime_mS_M_u32	2000	2000 ± 1	✔
NTCStatusByte_Cnt_M_u08	24	24 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	0	0 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_OPERATE	TMPMON_OPERATE ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 2.3 (Repeat Count = 1) ✔

Name	Input Value
InitTestStatus_Cnt_M_enum	0
InitialTime_mS_M_u32	100
NTCStatusByte_Cnt_M_u08	0
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	0
TMFTestComplete_Cnt_M_lgc	0
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	111
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	1000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	1000	1000 ± 1	✔
NTCStatusByte_Cnt_M_u08	240	240 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	0	0 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2	TMPMON_INIT_PICINIT2 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 2.4 (Repeat Count = 1) ✔

Name	Actual Value	Expected Value	Result
InitialTime_mS_M_u32	5000	5000 ± 1	✔
NTCStatusByte_Cnt_M_u08	240	240 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT1	TMPMON_INIT_PICINIT1 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 2.6 (Repeat Count = 1) ✔

Name	Input Value
InitTestStatus_Cnt_M_enum	1
InitialTime_mS_M_u32	4294967295
NTCStatusByte_Cnt_M_u08	6
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	0
TMFTestComplete_Cnt_M_lgc	0
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	234
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	6000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	6000	6000 ± 1	✔
NTCStatusByte_Cnt_M_u08	240	240 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	0	0 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2	TMPMON_INIT_PICINIT2 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 2.7 (Repeat Count = 1)

Name	Input Value
InitTestStatus_Cnt_M_enum	2
InitialTime_mS_M_u32	424242
NTCStatusByte_Cnt_M_u08	7
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	0
TMFTestComplete_Cnt_M_lgc	1
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_ALLON2
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	345
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	7000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	0

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	2	2 ± 1	✔
InitialTime_mS_M_u32	7000	7000 ± 1	✔
NTCStatusByte_Cnt_M_u08	7	7 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_ALLON2	TMPMON_INIT_ALLON2 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 2.8 (Repeat Count = 1)

Name	Input Value
InitTestStatus_Cnt_M_enum	0
InitialTime_mS_M_u32	100
NTCStatusByte_Cnt_M_u08	0
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	0
TMFTestComplete_Cnt_M_lgc	0
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	111
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	1000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔

Name	Actual Value	Expected Value	Result
InitialTime_mS_M_u32	1000	1000 ± 1	✔
NTCStatusByte_Cnt_M_u08	240	240 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	0	0 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2	TMPMON_INIT_PICINIT2 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 2.9 (Repeat Count = 1) ✔

Name	Input Value
InitTestStatus_Cnt_M_enum	1
InitialTime_mS_M_u32	200
NTCStatusByte_Cnt_M_u08	255
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	0
TMFTestComplete_Cnt_M_lgc	1
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_ALLON3
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	222
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	2000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	0

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	2000	2000 ± 1	✔
NTCStatusByte_Cnt_M_u08	240	240 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_ALLON3	TMPMON_INIT_ALLON3 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 2.10 (Repeat Count = 1)

Name	Input Value
InitTestStatus_Cnt_M_enum	2
InitialTime_mS_M_u32	300
NTCStatusByte_Cnt_M_u08	7
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	0
TMFTestComplete_Cnt_M_lgc	0
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	433
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	3000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	3000	3000 ± 1	✔
NTCStatusByte_Cnt_M_u08	240	240 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	0	0 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2	TMPMON_INIT_PICINIT2 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 2.11 (Repeat Count = 1)

Name	Input Value
InitTestStatus_Cnt_M_enum	3
InitialTime_mS_M_u32	800
NTCStatusByte_Cnt_M_u08	4
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	0
TMFTestComplete_Cnt_M_lgc	1
TmprlMonSt_Cnt_M_enum	TMPMON_RESET2
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	234
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	1000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	0

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	3	3 ± 1	✔

Name	Actual Value	Expected Value	Result
InitialTime_mS_M_u32	1000	1000 ± 1	✔
NTCStatusByte_Cnt_M_u08	4	4 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_RESET2	TMPMON_RESET2 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 2.12 (Repeat Count = 1) ✔

Name	Input Value
InitTestStatus_Cnt_M_enum	1
InitialTime_mS_M_u32	900
NTCStatusByte_Cnt_M_u08	6
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	0
TMFTestComplete_Cnt_M_lgc	0
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	345
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	2000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	2000	2000 ± 1	✔
NTCStatusByte_Cnt_M_u08	6	6 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	0	0 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2	TMPMON_INIT_PICINIT2 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 2.13 (Repeat Count = 1) ✔

Name	Input Value
InitTestStatus_Cnt_M_enum	3
InitialTime_mS_M_u32	500
NTCStatusByte_Cnt_M_u08	8
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	1
TMFTestComplete_Cnt_M_lgc	1
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_SF3OFF
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	0
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	8000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	3	3 ± 1	✔
InitialTime_mS_M_u32	500	500 ± 1	✔
NTCStatusByte_Cnt_M_u08	8	8 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_SF3OFF	TMPMON_INIT_SF3OFF ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 2.14 (Repeat Count = 1) ✔

Name	Input Value
InitTestStatus_Cnt_M_enum	0
InitialTime_mS_M_u32	600
NTCStatusByte_Cnt_M_u08	9
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	1
TMFTestComplete_Cnt_M_lgc	0
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	65535
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	9000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	9000	9000 ± 1	✔

TEST DETAILS REPORT

TmprlMon_Per2

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Name	Actual Value	Expected Value	Result
NTCStatusByte_Cnt_M_u08	203	203 ± 1	✔

Test Step 2.16 (Repeat Count = 1)

Name	Input Value
InitTestStatus_Cnt_M_enum	2
InitialTime_mS_M_u32	800
NTCStatusByte_Cnt_M_u08	11
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	0
TMFTestComplete_Cnt_M_lgc	0
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	234
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	0
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	0

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	2	2 ± 1	✔
InitialTime_mS_M_u32	0	0 ± 1	✔
NTCStatusByte_Cnt_M_u08	11	11 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	64	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	203	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	0	0 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2	TMPMON_INIT_PICINIT2 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 2.17 (Repeat Count = 1)

Name	Input Value
InitTestStatus_Cnt_M_enum	3
InitialTime_mS_M_u32	900
NTCStatusByte_Cnt_M_u08	40
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	0
TMFTestComplete_Cnt_M_lgc	1
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_ALLOFF2
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	678
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	4294967295
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	0

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	3	3 ± 1	✔

TEST DETAILS REPORT

TmprlMon_Per2

2015-03-10, 17:27:09+0530

Name	Actual Value	Expected Value	Result
InitialTime_mS_M_u32	4294967295	4294967295 ± 1	✔
NTCStatusByte_Cnt_M_u08	40	40 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	64	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	203	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_ALLOFF2	TMPMON_INIT_ALLOFF2 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
	1	Rte_Call_Sa_TmprlMon_SysFault _OP_SET	1	
		Rte_Call_TmprlMon_Per2_CP _CheckpointReached	1	

Test Step 2.19 (Repeat Count = 1)

Name	Input Value
InitTestStatus_Cnt_M_enum	1
InitialTime_mS_M_u32	555
NTCStatusByte_Cnt_M_u08	2
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	0
TMFTestComplete_Cnt_M_lgc	0
TmprlMonSt_Cnt_M_enum	TMPMON_RESET2
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	4234
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	525
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	525	525 ± 1	✔
NTCStatusByte_Cnt_M_u08	2	2 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	64	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	203	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	0	0 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_RESET2	TMPMON_RESET2 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 2.20 (Repeat Count = 1)

Name	Input Value
InitTestStatus_Cnt_M_enum	2
InitialTime_mS_M_u32	67456
NTCStatusByte_Cnt_M_u08	38
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	0
TMFTestComplete_Cnt_M_lgc	1
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_TMOFF1
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	5345
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	52352
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	2	2 ± 1	✔

Name	Actual Value	Expected Value	Result
InitialTime_mS_M_u32	52352	52352 ± 1	✔
NTCStatusByte_Cnt_M_u08	38	38 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	64	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	203	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_TMOFF1	TMPMON_INIT_TMOFF1 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 2.21 (Repeat Count = 1) ✔

Name	Input Value
InitTestStatus_Cnt_M_enum	3
InitialTime_mS_M_u32	500
NTCStatusByte_Cnt_M_u08	120
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	0
TMFTestComplete_Cnt_M_lgc	1
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_SF3OFF
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	0
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	8000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	3	3 ± 1	✔
InitialTime_mS_M_u32	8000	8000 ± 1	✔
NTCStatusByte_Cnt_M_u08	120	120 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	64	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	203	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_SF3OFF	TMPMON_INIT_SF3OFF ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 2.22 (Repeat Count = 1)

Name	Input Value
InitTestStatus_Cnt_M_enum	0
InitialTime_mS_M_u32	600
NTCStatusByte_Cnt_M_u08	9
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	1
TMFTestComplete_Cnt_M_lgc	0
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	65535
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	9000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	9000	9000 ± 1	✔
NTCStatusByte_Cnt_M_u08	203	203 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	64	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	203	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_OPERATE	TMPMON_OPERATE ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 2.23 (Repeat Count = 1)

Name	Input Value
InitTestStatus_Cnt_M_enum	2
InitialTime_mS_M_u32	800
NTCStatusByte_Cnt_M_u08	11
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	0
TMFTestComplete_Cnt_M_lgc	0
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	234
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	0
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	0

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	2	2 ± 1	✔
InitialTime_mS_M_u32	0	0 ± 1	✔
NTCStatusByte_Cnt_M_u08	11	11 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	64	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	203	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	0	0 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2	TMPMON_INIT_PICINIT2 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 2.24 (Repeat Count = 1)

Name	Input Value
InitTestStatus_Cnt_M_enum	3
InitialTime_mS_M_u32	900
NTCStatusByte_Cnt_M_u08	12
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	0
TMFTestComplete_Cnt_M_lgc	1
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_ALLOFF2
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	678
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	4294967295
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	0

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	3	3 ± 1	✔

Name	Actual Value	Expected Value	Result
InitialTime_mS_M_u32	4294967295	4294967295 ± 1	✔
NTCStatusByte_Cnt_M_u08	12	12 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	64	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	203	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_ALLOFF2	TMPMON_INIT_ALLOFF2 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 2.25 (Repeat Count = 1) ✔

Name	Input Value
InitTestStatus_Cnt_M_enum	2
InitialTime_mS_M_u32	800
NTCStatusByte_Cnt_M_u08	130
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	0
TMFTestComplete_Cnt_M_lgc	0
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	234
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	0
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	0

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	2	2 ± 1	✔
InitialTime_mS_M_u32	0	0 ± 1	✔
NTCStatusByte_Cnt_M_u08	130	130 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	64	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	203	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	0	0 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2	TMPMON_INIT_PICINIT2 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 2.26 (Repeat Count = 1)

Name	Input Value
InitTestStatus_Cnt_M_enum	3
InitialTime_mS_M_u32	400
NTCStatusByte_Cnt_M_u08	4
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	0
TMFTestComplete_Cnt_M_lgc	0
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	456
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	4000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	4000	4000 ± 1	✔
NTCStatusByte_Cnt_M_u08	240	240 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	64	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	203	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	0	0 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2	TMPMON_INIT_PICINIT2 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 2.27 (Repeat Count = 1)

Name	Input Value
InitTestStatus_Cnt_M_enum	3
InitialTime_mS_M_u32	800
NTCStatusByte_Cnt_M_u08	4
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	0
TMFTestComplete_Cnt_M_lgc	1
TmprlMonSt_Cnt_M_enum	TMPMON_RESET2
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	234
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	1000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	0

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔

Name	Actual Value	Expected Value	Result
InitialTime_mS_M_u32	1000	1000 ± 1	✔
NTCStatusByte_Cnt_M_u08	240	240 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	64	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	203	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_RESET2	TMPMON_RESET2 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 2.28 (Repeat Count = 1) ✔

Name	Input Value
InitTestStatus_Cnt_M_enum	1
InitialTime_mS_M_u32	900
NTCStatusByte_Cnt_M_u08	6
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	0
TMFTestComplete_Cnt_M_lgc	0
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	345
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	2000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	2000	2000 ± 1	✔
NTCStatusByte_Cnt_M_u08	6	6 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	64	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	203	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	0	0 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2	TMPMON_INIT_PICINIT2 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 2.29 (Repeat Count = 1)

Name	Input Value
InitTestStatus_Cnt_M_enum	0
InitialTime_mS_M_u32	0
NTCStatusByte_Cnt_M_u08	0
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	0
TMFTestComplete_Cnt_M_lgc	0
TmprlMonSt_Cnt_M_enum	TMPMON_RESET1
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	0
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	0
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	0

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	0	0	✔
NTCStatusByte_Cnt_M_u08	240	240 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	64	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	203	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	0	0 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_RESET1	TMPMON_RESET1 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 2.30 (Repeat Count = 1)

Name	Input Value
InitTestStatus_Cnt_M_enum	3
InitialTime_mS_M_u32	4294967295
NTCStatusByte_Cnt_M_u08	255
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	1
TMFTestComplete_Cnt_M_lgc	1
TmprlMonSt_Cnt_M_enum	TMPMON_OPERATE
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	65535
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	4294967295
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	3	3 ± 1	✔

TEST DETAILS REPORT

TmprlMon_Per2

2015-03-10, 17:27:09+0530

Name	Actual Value	Expected Value	Result
InitialTime_mS_M_u32	4294967295	4294967295	✔
NTCStatusByte_Cnt_M_u08	255	255 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	64	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	203	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_OPERATE	TMPMON_OPERATE ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Case 3: Path Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:

TS3.1 7265 Cycles
TS3.2 13347 Cycles
TS3.3 13104 Cycles
TS3.4 11773 Cycles
TS3.5 10481 Cycles
TS3.6 7176 Cycles
TS3.7 13131 Cycles
TS3.8 6761 Cycles
TS3.9 10951 Cycles
TS3.10 11345 Cycles
TS3.11 14006 Cycles
TS3.12 13102 Cycles
TS3.13 12650 Cycles
TS3.14 10601 Cycles
TS3.15 10962 Cycles
```

Description

Vector Description
TS3.1 "(TMFPrepCheckFlag_Cnt_M_lgc == FALSE)==>TRUE
&&
(SysFault3_Cnt_T_lgc == FALSE)=>TRUE"
TS3.2 (SysFault3_Cnt_T_lgc == FALSE)==>FALSE
TS3.3 "(TMFPrepCheckFlag_Cnt_M_lgc == FALSE)==>False
&&
(ElapsedTime_T_mS_u16 >= TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].StepTime_mS_u16)==>TRUE
((TmprlMonSt_Cnt_T_enum < TMPMON_OPERATE==>TRUE) &&
(TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].FetDrvCntlFdbk_lgc != FetDrvCntlFdbk_Cnt_T_lgc)=>TRUE ||
(TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].PwrSwitchEnFdbk_lgc != PwrSwitchEnFdbk_Cnt_T_lgc)==FALSE
(TMFTestStart_Cnt_T_lgc == TRUE))==>TRUE
&&
(InitTestStatus_Cnt_M_enum == NTC_STATUS_PASSED)==>FALSE"
TS3.4 "(TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].FetDrvCntlFdbk_lgc != FetDrvCntlFdbk_Cnt_T_lgc) ||
(TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].PwrSwitchEnFdbk_lgc != PwrSwitchEnFdbk_Cnt_T_lgc)==>FALSE"
TS3.5 "(ElapsedTime_T_mS_u16 >= TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].StepTime_mS_u16)==>FALSE ||
(((TmprlMonSt_Cnt_T_enum == TMPMON_INIT_PICINIT1)==>FALSE ||
(TmprlMonSt_Cnt_T_enum == TMPMON_INIT_PICINIT2) ==>FALSE) &&
(TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].FetDrvCntlFdbk_lgc == FetDrvCntlFdbk_Cnt_T_lgc) &&
(TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].PwrSwitchEnFdbk_lgc == PwrSwitchEnFdbk_Cnt_T_lgc)))"
TS3.6 "((TmprlMonSt_Cnt_T_enum < TMPMON_OPERATE)==>TRUE &&
(TMFTestStart_Cnt_T_lgc == TRUE)==FALSE)"
TS3.7 (InitTestStatus_Cnt_M_enum == NTC_STATUS_PASSED)==>TRUE
TS3.8 "((TmprlMonSt_Cnt_T_enum < TMPMON_OPERATE)==FALSE
&&
(TMFTestStart_Cnt_T_lgc == TRUE))"
TS3.9 "(ElapsedTime_T_mS_u16 >= TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].StepTime_mS_u16)==>FALSE ||
(((TmprlMonSt_Cnt_T_enum == TMPMON_INIT_PICINIT1)==>FALSE ||
(TmprlMonSt_Cnt_T_enum == TMPMON_INIT_PICINIT2) ==>TRUE) &&
(TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].FetDrvCntlFdbk_lgc == FetDrvCntlFdbk_Cnt_T_lgc)==FALSE &&
(TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].PwrSwitchEnFdbk_lgc == PwrSwitchEnFdbk_Cnt_T_lgc)))"
TS3.10 "(ElapsedTime_T_mS_u16 >= TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].StepTime_mS_u16)==>FALSE ||
(((TmprlMonSt_Cnt_T_enum == TMPMON_INIT_PICINIT1)==>FALSE ||
(TmprlMonSt_Cnt_T_enum == TMPMON_INIT_PICINIT2) ==>TRUE) &&
(TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].FetDrvCntlFdbk_lgc == FetDrvCntlFdbk_Cnt_T_lgc)==FALSE==TRUE &&
(TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].PwrSwitchEnFdbk_lgc == PwrSwitchEnFdbk_Cnt_T_lgc)==>FALSE))"
TS3.11 "(ElapsedTime_T_mS_u16 >= TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].StepTime_mS_u16)==>FALSE ||
(((TmprlMonSt_Cnt_T_enum == TMPMON_INIT_PICINIT1)==>FALSE ||
(TmprlMonSt_Cnt_T_enum == TMPMON_INIT_PICINIT2) ==>TRUE) &&
(TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].FetDrvCntlFdbk_lgc == FetDrvCntlFdbk_Cnt_T_lgc)==FALSE==TRUE &&
(TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].PwrSwitchEnFdbk_lgc == PwrSwitchEnFdbk_Cnt_T_lgc)==>TRUE))"
TS3.12 "(ElapsedTime_T_mS_u16 >= TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].StepTime_mS_u16)==>FALSE ||
(((TmprlMonSt_Cnt_T_enum == TMPMON_INIT_PICINIT1)==>TRUE ||
(TmprlMonSt_Cnt_T_enum == TMPMON_INIT_PICINIT2)) &&
(TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].FetDrvCntlFdbk_lgc == FetDrvCntlFdbk_Cnt_T_lgc)==FALSE==TRUE &&
(TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].PwrSwitchEnFdbk_lgc == PwrSwitchEnFdbk_Cnt_T_lgc)==>TRUE))"
TS3.13 "((TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].FetDrvCntlFdbk_lgc != FetDrvCntlFdbk_Cnt_T_lgc)==>TRUE ||
(TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].PwrSwitchEnFdbk_lgc != PwrSwitchEnFdbk_Cnt_T_lgc) "
TS3.14 "(ElapsedTime_T_mS_u16 >= TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].StepTime_mS_u16)==>FALSE ||
(((TmprlMonSt_Cnt_T_enum == TMPMON_INIT_PICINIT1)==>TRUE ||
(TmprlMonSt_Cnt_T_enum == TMPMON_INIT_PICINIT2)) &&
(TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].FetDrvCntlFdbk_lgc == FetDrvCntlFdbk_Cnt_T_lgc)==FALSE &&
(TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].PwrSwitchEnFdbk_lgc == PwrSwitchEnFdbk_Cnt_T_lgc)==>TRUE))"
TS3.15 "(ElapsedTime_T_mS_u16 >= TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].StepTime_mS_u16)==>FALSE ||
(((TmprlMonSt_Cnt_T_enum == TMPMON_INIT_PICINIT1)==>TRUE ||
(TmprlMonSt_Cnt_T_enum == TMPMON_INIT_PICINIT2)) &&
(TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].FetDrvCntlFdbk_lgc == FetDrvCntlFdbk_Cnt_T_lgc)==FALSE==TRUE &&
(TmprlMonStateTbl_Cnt_M_Str[TmprlMonSt_Cnt_T_enum].PwrSwitchEnFdbk_lgc == PwrSwitchEnFdbk_Cnt_T_lgc)==>False))"

Test Step 3.1 (Repeat Count = 1)

Name	Input Value
InitTestStatus_Cnt_M_enum	0
InitialTime_mS_M_u32	800
NTCStatusByte_Cnt_M_u08	4
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon

Name	Input Value
TMFPrepCheckFlag_Cnt_M_lgc	0
TMFTestComplete_Cnt_M_lgc	1
TmprlMonSt_Cnt_M_enum	TMPMON_RESET2
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	234
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	1000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	0

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	1000	1000 ± 1	✔
NTCStatusByte_Cnt_M_u08	240	240 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_RESET2	TMPMON_RESET2 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 3.2 (Repeat Count = 1) ✔

Name	Input Value
InitTestStatus_Cnt_M_enum	1
InitialTime_mS_M_u32	100
NTCStatusByte_Cnt_M_u08	1
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	1
TMFTestComplete_Cnt_M_lgc	1
TmprlMonSt_Cnt_M_enum	TMPMON_RESET1
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	123
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	1000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	1000	1000 ± 1	✔
NTCStatusByte_Cnt_M_u08	9	9 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_ALLOFF1	TMPMON_INIT_ALLOFF1 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

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Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 3.3 (Repeat Count = 1)			✔
Name	**Input Value**		
InitTestStatus_Cnt_M_enum	1		
InitialTime_mS_M_u32	500		
NTCStatusByte_Cnt_M_u08	5		
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal		
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela		
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren		
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon		
TMFPrepCheckFlag_Cnt_M_lgc	1		
TMFTestComplete_Cnt_M_lgc	1		
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_ALLOFF1		
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0		
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0		
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	345		
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	4000		
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc		
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc		
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1		
Name	**Actual Value**	**Expected Value**	**Result**
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	4000	4000 ± 1	✔
NTCStatusByte_Cnt_M_u08	13	13 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_TMOFF1	TMPMON_INIT_TMOFF1 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

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Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 3.4 (Repeat Count = 1)		✔
Name	**Input Value**	
InitTestStatus_Cnt_M_enum	1	
InitialTime_mS_M_u32	665	
NTCStatusByte_Cnt_M_u08	6	
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	

Name	Input Value
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	1
TMFTestComplete_Cnt_M_lgc	1
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_ALLOFF1
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	45
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	5000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	5000	5000 ± 1	✔
NTCStatusByte_Cnt_M_u08	6	6 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_TMOFF1	TMPMON_INIT_TMOFF1 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 3.5 (Repeat Count = 1) ✔

Name	Input Value
InitTestStatus_Cnt_M_enum	1
InitialTime_mS_M_u32	565
NTCStatusByte_Cnt_M_u08	7
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	1
TMFTestComplete_Cnt_M_lgc	1
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_ALLOFF1
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	15
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	6000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	565	565 ± 1	✔
NTCStatusByte_Cnt_M_u08	7	7 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_ALLOFF1	TMPMON_INIT_ALLOFF1 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 3.6 (Repeat Count = 1)			✔
Name	**Input Value**		
InitTestStatus_Cnt_M_enum	1		
InitialTime_mS_M_u32	450		
NTCStatusByte_Cnt_M_u08	8		
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal		
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela		
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren		
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon		
TMFPrepCheckFlag_Cnt_M_lgc	1		
TMFTestComplete_Cnt_M_lgc	1		
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_ALLOFF1		
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0		
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0		
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0		
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	15		
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	7000		
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc		
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc		
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	0		
Name	**Actual Value**	**Expected Value**	**Result**
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	7000	7000 ± 1	✔
NTCStatusByte_Cnt_M_u08	8	8 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_ALLOFF1	TMPMON_INIT_ALLOFF1 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 3.7 (Repeat Count = 1)		✔
Name	**Input Value**	
InitTestStatus_Cnt_M_enum	0	
InitialTime_mS_M_u32	500	
NTCStatusByte_Cnt_M_u08	5	
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon	

Name	Input Value
TMFPrepCheckFlag_Cnt_M_lgc	1
TMFTestComplete_Cnt_M_lgc	1
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_ALLOFF1
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	345
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	4000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	4000	4000 ± 1	✔
NTCStatusByte_Cnt_M_u08	29	29 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_TMOFF1	TMPMON_INIT_TMOFF1 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 3.8 (Repeat Count = 1) ✔

Name	Input Value
InitTestStatus_Cnt_M_enum	3
InitialTime_mS_M_u32	4294967295
NTCStatusByte_Cnt_M_u08	13
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	1
TMFTestComplete_Cnt_M_lgc	1
TmprlMonSt_Cnt_M_enum	TMPMON_OPERATE
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	65535
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	4294967295
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	3	3 ± 1	✔
InitialTime_mS_M_u32	4294967295	4294967295 ± 1	✔
NTCStatusByte_Cnt_M_u08	13	13 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_OPERATE	TMPMON_OPERATE ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 3.9 (Repeat Count = 1)			✔
Name	**Input Value**		
InitTestStatus_Cnt_M_enum	1		
InitialTime_mS_M_u32	565		
NTCStatusByte_Cnt_M_u08	7		
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal		
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela		
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren		
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon		
TMFPrepCheckFlag_Cnt_M_lgc	1		
TMFTestComplete_Cnt_M_lgc	1		
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2		
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0		
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0		
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0		
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	15		
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	6000		
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc		
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc		
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1		
Name	**Actual Value**	**Expected Value**	**Result**
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	565	565 ± 1	✔
NTCStatusByte_Cnt_M_u08	7	7 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2	TMPMON_INIT_PICINIT2 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 3.10 (Repeat Count = 1)		✔
Name	**Input Value**	
InitTestStatus_Cnt_M_enum	1	
InitialTime_mS_M_u32	565	
NTCStatusByte_Cnt_M_u08	7	
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon	

Name	Input Value
TMFPrepCheckFlag_Cnt_M_lgc	1
TMFTestComplete_Cnt_M_lgc	1
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	15
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	6000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	565	565 ± 1	✔
NTCStatusByte_Cnt_M_u08	7	7 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	0	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	0	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2	TMPMON_INIT_PICINIT2 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 3.11 (Repeat Count = 1) ✔

Name	Input Value
InitTestStatus_Cnt_M_enum	1
InitialTime_mS_M_u32	565
NTCStatusByte_Cnt_M_u08	7
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	1
TMFTestComplete_Cnt_M_lgc	1
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT2
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	15
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	6000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	6000	6000 ± 1	✔
NTCStatusByte_Cnt_M_u08	7	7 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	64	64	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	7	7	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	1	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_OPERATE	TMPMON_OPERATE ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 3.12 (Repeat Count = 1)			✔
Name	**Input Value**		
InitTestStatus_Cnt_M_enum	1		
InitialTime_mS_M_u32	565		
NTCStatusByte_Cnt_M_u08	7		
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal		
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal		
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela		
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren		
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon		
TMFPrepCheckFlag_Cnt_M_lgc	1		
TMFTestComplete_Cnt_M_lgc	1		
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT1		
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1		
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0		
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	15		
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	6000		
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc		
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc		
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1		
Name	**Actual Value**	**Expected Value**	**Result**
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	6000	6000 ± 1	✔
NTCStatusByte_Cnt_M_u08	7	7 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	64	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	7	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_SF2OFF	TMPMON_INIT_SF2OFF ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

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Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 3.13 (Repeat Count = 1)		✔
Name	**Input Value**	
InitTestStatus_Cnt_M_enum	1	
InitialTime_mS_M_u32	500	
NTCStatusByte_Cnt_M_u08	5	
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	

Name	Input Value
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	1
TMFTestComplete_Cnt_M_lgc	1
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_ALLOFF1
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	345
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	4000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	4000	4000 ± 1	✔
NTCStatusByte_Cnt_M_u08	13	13 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	64	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	7	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_TMOFF1	TMPMON_INIT_TMOFF1 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 3.14 (Repeat Count = 1) ✔

Name	Input Value
InitTestStatus_Cnt_M_enum	1
InitialTime_mS_M_u32	565
NTCStatusByte_Cnt_M_u08	7
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	1
TMFTestComplete_Cnt_M_lgc	1
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT1
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	15
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	6000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	565	565 ± 1	✔
NTCStatusByte_Cnt_M_u08	7	7 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	64	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	7	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT1	TMPMON_INIT_PICINIT1 ± 1	✔

Name	Actual Value	Expected Value	Result
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔

Test Step 3.15 (Repeat Count = 1) ✔

Name	Input Value
InitTestStatus_Cnt_M_enum	1
InitialTime_mS_M_u32	565
NTCStatusByte_Cnt_M_u08	7
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal
Rte_Call_Sa_TmprlMon_SysFault3_OP_GET(signal)	tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela
Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32(CurrentTime)	tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren
Rte_Inst_Sa_TmprlMon	tgt_Rte_Inst_Sa_TmprlMon
TMFPrepCheckFlag_Cnt_M_lgc	1
TMFTestComplete_Cnt_M_lgc	1
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT1
tgt_Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET_signal	1
tgt_Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SysFault3_OP_GET_signal	0
tgt_Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16_Ela	15
tgt_Rte_Call_Sa_TmprlMon_SystemTime_GetSystemTime_mS_u32_Curren	6000
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestComplete_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc
tgt_Rte_Inst_Sa_TmprlMon.TmprlMon_Per2_TMFTestStart_Cnt_lgc	tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc
tgt_TmprlMon_Per2_TMFTestStart_Cnt_lgc.value	1

Name	Actual Value	Expected Value	Result
InitTestStatus_Cnt_M_enum	1	1 ± 1	✔
InitialTime_mS_M_u32	565	565 ± 1	✔
NTCStatusByte_Cnt_M_u08	7	7 ± 1	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	64	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	7	*none*	✔
Rte_Call_Sa_TmprlMon_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	1	*none*	✔
TMFPrepCheckFlag_Cnt_M_lgc	1	1	✔
TMFTestComplete_Cnt_M_lgc	1	1 ± 1	✔
TmprlMonSt_Cnt_M_enum	TMPMON_INIT_PICINIT1	TMPMON_INIT_PICINIT1 ± 1	✔
tgt_TmprlMon_Per2_TMFTestComplete_Cnt_lgc.value	1	1	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP0_CheckpointReached	1	✔
Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	Rte_Call_Sa_TmprlMon_FetDrvCntl_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	Rte_Call_Sa_TmprlMon_PwrSwitchEn_OP_GET	1	✔
Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	Rte_Call_Sa_TmprlMon_SystemTime_DtrmnElapsedTime_mS_u16	1	✔
Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	Rte_Call_Sa_TmprlMon_WdReset_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault2_OP_SET	1	✔
Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	Rte_Call_Sa_TmprlMon_SysFault3_OP_SET	1	✔
Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	Rte_Call_TmprlMon_Per2_CP1_CheckpointReached	1	✔