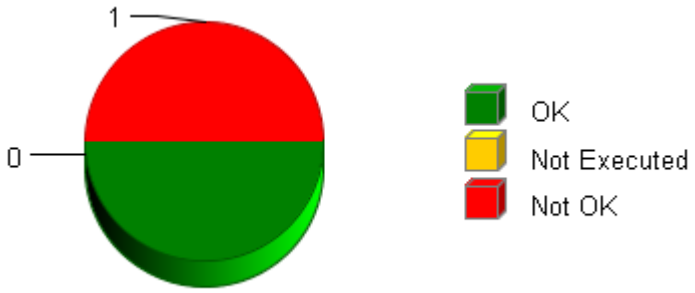
Summary

Total Test Objects:	2
Successful:	1
Failed:	1
Not Executed:	0
Date:	2018-05-18
Time:	13:32:19+0530

Overall Test Object Results (including Coverage)



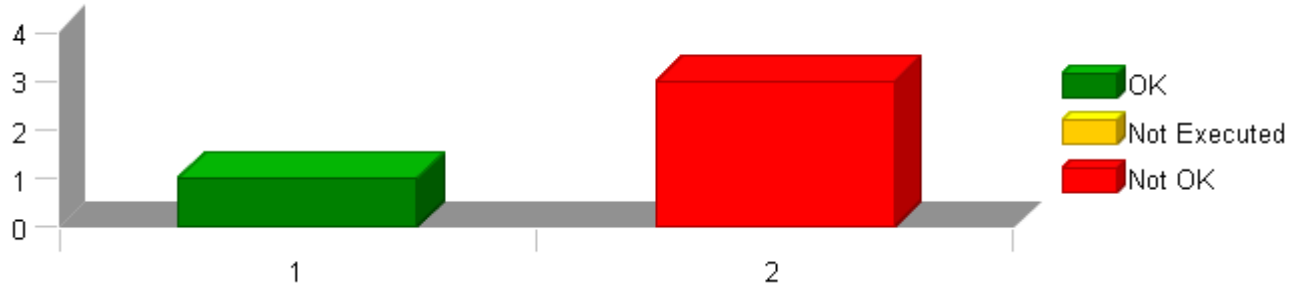
Selected Project Items

Test Object "CBD_Unittest/LoaMgr/LoaMgr_Init1"
Test Object "CBD_Unittest/LoaMgr/LoaMgr_Per1"

Used Test Environments

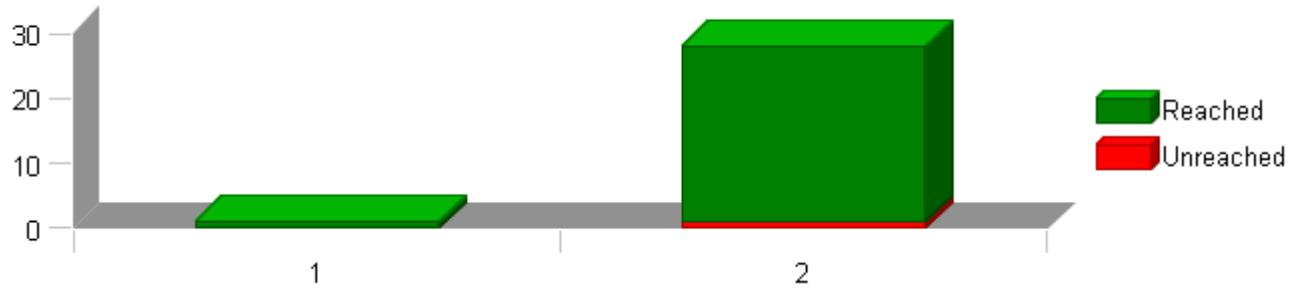
TI TMS 570 PLS UDE (Default)

Test Case Results for Each Test Object (without Coverage)



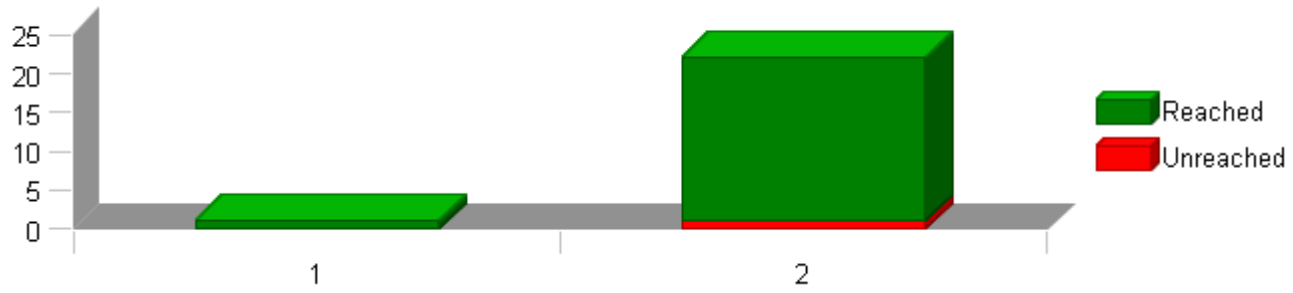
The table above shows each test object on the x axis and the number of test cases of the respective test object on the y axis. Each bar is divided into passed, not executed and failed test cases. The test case results do not take into account any coverage result (i.e. if all test cases of a test object are passed in this table but the coverage is failed, the overall test object result will be failed).

Statement (C0) Coverage: Total Statements for Each Test Object



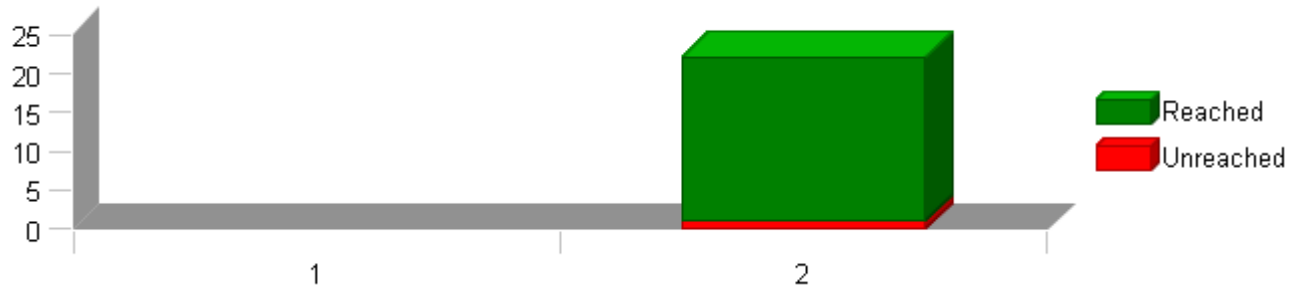
The table above shows each test object on the x axis and the number of statements of the respective test object on the y axis. Each bar is divided into reached statements (i.e. statements that have been executed during the test) and unreached statements.

Branch (C1) Coverage: Total Branches for Each Test Object



The table above shows each test object on the x axis and the number of branches of the respective test object on the y axis. Each bar is divided into reached branches (i.e. branches that have been executed during the test) and unreached branches.

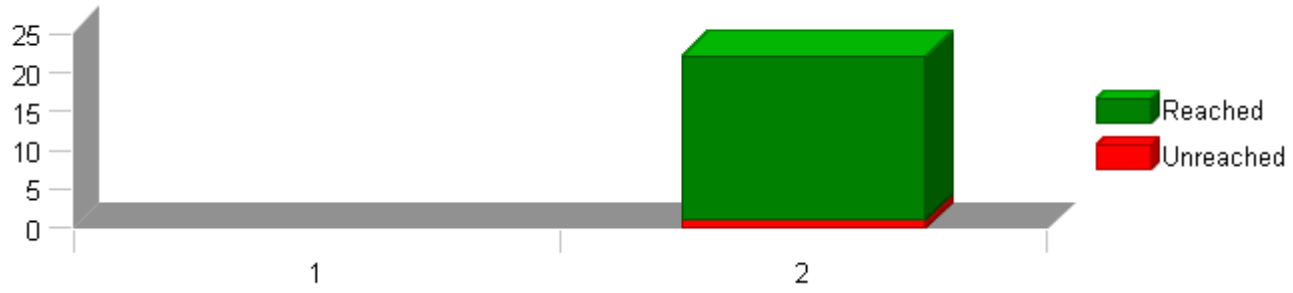
Decision Coverage: Total Decision Outcomes for Each Test Object



The table above shows test objects on the x axis and the number of possible outcomes of all decisions of the respective test object on the y axis. To achieve full DC coverage, each decision must evaluate to both true and false.

Each bar is divided into reached and unreached decision outcomes.

MC/DC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MC/DC coverage, each decision requires all contained atomic conditions to evaluate to both true and false independently of all other conditions. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

Test Object List

The following table lists all test objects with their test case and coverage results. The cumulated results for modules, folders and test collections are also displayed, the indentation within the name column indicates the parent relationship of the elements.

Please note that only test objects are numbered within the first column. This number is referenced on the x axis within the overview charts for test case and coverage results available on previous pages (if included into the report).

No.	Name	C0	C1	DC	MC/DC	Test Cases	Result
	LoaMgr	96.55 %	95.65 %	95.45 %	95.45 %	3 of 4 failed	✗
	CBD_Unittest	96.55 %	95.65 %	95.45 %	95.45 %	3 of 4 failed	✗
	LoaMgr	96.55 %	95.65 %	95.45 %	95.45 %	3 of 4 failed	✗
1	LoaMgr_Init1	100 %	100 %	-	-	1 of 1 passed	✓
2	LoaMgr_Per1	96.42 %	95.45 %	95.45 %	95.45 %	3 of 3 failed	✗

TEST DETAILS REPORT

LoaMgr_Init1

2018-05-18, 13:28:01+0530

Project	LoaMgr
Module	LoaMgr
Test Object	LoaMgr_Init1

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

Statistics

Total Testcases	1
Successful	1
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\LoaMgr_SF049A_4.3.0_0_NoUTP
Configuration File	D:\Synergy_Work_Area\LoaMgr_SF049A_4.3.0_0_NoUTP\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\LoaMgr\src\Ap_LoaMgr.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I$(PROJECTROOT)\LoaMgr\tools\contract -I$(PROJECTROOT)\LoaMgr\tools\contract\Ap_LoaMgr -I$(PROJECTROOT)\StdDef\include -I$(PROJECTROOT)\NxtrLib\include -I$(Compiler Install Path)\include

Comments/Description/Specification	
Name	**Text**

Module 'LoaMgr'	**********Unit Test Information********** Name of Tester:Pradnya Mhetre Code File(s) Under Test:Ap_LoaMgr.c Code File(s) Version:11 Module Design Version:9 Requirement Document Version:NA Data Dictionary Version:8 Unit Test Plan Version:5 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):2244 Total RAM Used (Bytes):27 Total CALS Used (Bytes):76 Special Test Requirements:NA Test Date:5/18/2018 Comments: Note1:Inline functions defined in 'globalmacro.h' are not unit tested. Note2:The Expected output calculated from MATLAB model. Note3:Local functions ""LatchInputs()"", ""RqstRespConds()"", ""ArbResp()"", ""AssignScale()"", ""RqstHwTqResp()"", ""ChooseFinalResp()"" and ""SwBasMtgtn()"" are not tested individually as they are tested in "LoaMgr_Per1" function. Please refer snapshot "LoaMgr_Per1_Coverage" for the same. Note4:In CSV_9 and CSV_10,value for boolean variable ""DiagcStsIvtr1Inactv"" given in "Simdata" is in float. Hence input values for "DiagcStsIvtr1Inactv" are captured from Matlab design and given in Tessy for those test steps. Note5: Out of range value is given to the variable ""HwTqIdptSig_Cnt_u08=5"" over the DD range {0,4}, to cover the path at src line no.908 in TS5.1 Note6: Out of range value is given to the variable ""MtrPosIdptSig_Cnt_u08=4"" over the DD range {0,3}, to cover the path at src line no.918 in TS5.2 Note7: Out of range value is given to the variable ""MotCurrIdptSig_Cnt_u08=3"" over the DD range {0,2}, to cover the path at src line no.928 in TS5.3 Note8:Output variable "LoaMgr_AgSV_Cnt_M_lgc" is failing because of Source Model Mismatch at src line no.1503 Anomaly EA3#20083 is logged for the same. Mote9:Parameter of "Rte_Call_NxtrDiagMgr_SetNTCStatus" "Param_Cnt_T_u08" is failing because of Source Model Mismatch. Anomaly EA3#20083 is logged for the same. Note10:Output variable "LoaMgr_VltgMdSrcSV_Cnt_M_u08" is going out of range as [0 3] over DD range [0 1] in PRM test vector TS4.103 Anomaly EA3#20083 is logged for the same. Note11:""CBD_Sandbox_dbg.map"" map file is embedded for reference. **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(ProgramFiles)\pls\UDE 4.4
Time Unit	cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\LoaMgr_SF049A_4.3.0_0_NoUTP\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: PRM Range Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:

TS1.1  2849.00 Cycles
TS1.2  2849.00 Cycles
```

Description Vector Description:

TS1.1k_LoaMgr_SnsrIsMotAgAvail_Cnt_lgc=>Min/Default
TS1.2k_LoaMgr_SnsrIsMotAgAvail_Cnt_lgc=>Max

Test Step 1.1 (Repeat Count = 1)

Name	Input Value
k_LoaMgr_SnsrIsMotAgAvail_Cnt_lgc	0

Name	Actual Value	Expected Value	Result
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	3	3	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	6	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	6	✔

Test Step 1.2 (Repeat Count = 1)

Name	Input Value
k_LoaMgr_SnsrIsMotAgAvail_Cnt_lgc	1

Name	Actual Value	Expected Value	Result
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	3	3	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1	1	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	6	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	6	✔

TEST DETAILS REPORT

LoaMgr_Per1

2018-05-18, 13:31:17+0530

Project	LoaMgr
Module	LoaMgr
Test Object	LoaMgr_Per1

Instrumentation: Test Object Only

Statement (C0) Coverage	96.42 %
Decision Coverage	95.45 %
Branch (C1) Coverage	95.45 %
MC/DC Coverage	95.45 %

Statistics

Total Testcases	3
Successful	0
Failed	3
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\LoaMgr_SF049A_4.3.0_0_NoUTP
Configuration File	D:\Synergy_Work_Area\LoaMgr_SF049A_4.3.0_0_NoUTP\UnitTestEnv\config \TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\LoaMgr\src\Ap_LoaMgr.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I$(PROJECTROOT)\LoaMgr\tools\contract -I$(PROJECTROOT)\LoaMgr\tools\contract\Ap_LoaMgr -I$ (PROJECTROOT)\StdDef\include -I$(PROJECTROOT)\NxtrLib\include -I$(Compiler Install Path)\include

Comments/Description/Specification

Name	Text
Module 'LoaMgr'	**********Unit Test Information********** Name of Tester:Pradnya Mhetre Code File(s) Under Test:Ap_LoaMgr.c Code File(s) Version:11 Module Design Version:9 Requirement Document Version:NA Data Dictionary Version:8 Unit Test Plan Version:5 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):2244 Total RAM Used (Bytes):27 Total CALS Used (Bytes):76 Special Test Requirements:NA Test Date:5/18/2018 Comments: Note1:Inline functions defined in 'globalmacro.h' are not unit tested. Note2:The Expected output calculated from MATLAB model. Note3:Local functions ""LatchInputs()"", ""RqstRespConds()"", ""ArbResp()"", ""AssignScale()"", ""RqstHwTqResp()"", ""ChooseFinalResp()"" and ""SwBasMtgtn()"" are not tested individually as they are tested in "LoaMgr_Per1" function. Please refer snapshot "LoaMgr_Per1_Coverage" for the same. Note4:In CSV_9 and CSV_10,value for boolean variable ""DiagcStsIvtr1Inactv"" given in "Simdata" is in float. Hence input values for "DiagcStsIvtr1Inactv" are captured from Matlab design and given in Tessy for those test steps. Note5: Out of range value is given to the variable ""HwTqIdptSig_Cnt_u08=5"" over the DD range {0,4}, to cover the path at src line no.908 in TS5.1 Note6: Out of range value is given to the variable ""MtrPosIdptSig_Cnt_u08=4"" over the DD range {0,3}, to cover the path at src line no.918 in TS5.2 Note7: Out of range value is given to the variable ""MotCurrIdptSig_Cnt_u08=3"" over the DD range {0,2}, to cover the path at src line no.928 in TS5.3 Note8:Output variable "LoaMgr_AgSV_Cnt_M_lgc" is failing because of Source Model Mismatch at src line no.1503 Anomaly EA3#20083 is logged for the same. Mote9:Parameter of "Rte_Call_NxtrDiagMgr_SetNTCStatus" "Param_Cnt_T_u08" is failing because of Source Model Mismatch. Anomaly EA3#20083 is logged for the same. Note10:Output variable "LoaMgr_VltgMdSrcSV_Cnt_M_u08" is going out of range as [0 3] over DD range [0 1] in PRM test vector TS4.103 Anomaly EA3#20083 is logged for the same. Note11:""CBD_Sandbox_dbg.map"" map file is embedded for reference. **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(ProgramFiles)\pls\UDE 4.4
Time Unit	cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\LoaMgr_SF049A_4.3.0_0_NoUTP\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Metric Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:

TS1.1 2849.00 Cycles
TS1.2 5486.00 Cycles
```

Description

Vector Description:

TS1.1Shortest Execution Path
if(LoaMgr_LOASt_State_M_enum == LOAST_RPDSHTDWNREQD)=>T
if(LoaScaDi_Cnt_T_lgc == TRUE)=>T
(LoaMgr_LoaRateLimit_UlspS_M_f32>=500.0f)=>T
(LoaMgr_LoaScaleFctr_Uls_M_f32>=1)=>T
if((HwTqResp_Cnt_T_u08 == D_LOASTSWMTGTN_CNT_U08)=>F||(LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc == TRUE)=>F)
if((MotAgResp_Cnt_T_u08 == D_LOASTSWMTGTN_CNT_U08)=>F||(LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc == TRUE)=>T)
if((MotCurrResp_Cnt_T_u08 == D_LOASTSWMTGTN_CNT_U08)=>F||(LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc == TRUE)=>F)
if((IvtrResp_Cnt_T_u08 == D_LOASTSWMTGTN_CNT_U08)=>F||(LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc == TRUE)=>F)
if (LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc == TRUE)=>T
if ((MtgtnCount_Cnt_T_u08 <= 1u))=>T
if(LoaMgr_LOASt_State_M_enum == LOAST_NORM)=>F
else if(LoaMgr_LOASt_State_M_enum == LOAST_REDCD)=>F
else if(LoaMgr_LOASt_State_M_enum == LOAST_SWBASDMTGTN)=>F
else if(LoaMgr_LOASt_State_M_enum == LOAST_FADEOUT)=>F
else if(LoaMgr_LOASt_State_M_enum == LOAST_CTRLDSHTDWNREQD)=>F
if (IvtrInactv_Cnt_T_logl == TRUE)=>F
Max_m(MultiMtgtnResp_Cnt_T_u08,Max_m(HwTqResp_Cnt_T_u08,
Max_m(MotAgResp_Cnt_T_u08,Max_m(MotCurrResp_Cnt_T_u08, IvtrResp_Cnt_T_u08))))=>F
switch (LoaMgr_MaxMtgtnResp_Cnt_M_u08)=>Default
if (HwTqIdptSig_Cnt_T_u08 > D_MAXHWTQIDPTSIGALLWD_CNT_U08)=>F
if (MtrPosIdptSig_Cnt_T_u08 > D_MAXMOTPOSNIDPTSIGALLWD_CNT_U08)=>F
if (MotCurrIdptSig_Cnt_T_u08 > D_MAXMOTCURRIDPTSIGALLWD_CNT_U08)=>F
Min_m(RngLimdHwTqIdptSig_Cnt_T_u08, LoaMgr_HwTqIdptSigSV_Cnt_M_u08)=>F
Min_m(RngLimdMtrPosIdptSig_Cnt_T_u08, LoaMgr_MotAgIdptSigSV_Cnt_M_u08)=>F
Min_m(RngLimdMtrCurrIdptSig_Cnt_T_u08, LoaMgr_MotCurrIdptSigSV_Cnt_M_u08)=>F
Min_m(IvtrIdptSig_Cnt_T_u08, LoaMgr_IvtrIdptSigSV_Cnt_M_u08)=>F
switch (HwTqIdptMin_Cnt_T_u08):Default =>if ((LoaMgr_TloaAvail_Cnt_M_lgc == TRUE)=F&& (LoaMgr_TloaDi_Cnt_M_lgc == FALSE))=>F
if (SteerMod_Cnt_T_enum == STEERMOD_FULLYATNMS)=>T
switch (MtrPosIdptMin_Cnt_T_u08):Default=>if (SmpAvail_Cnt_T_lgc == TRUE)=>F
switch (MtrCurrIdptMin_Cnt_T_u08):case1
switch (IvtrIdptMin_Cnt_T_u08):case2
Max_m(LoaMgr_MotAgRespSV_Cnt_M_u08, MotAgResp_Cnt_T_u08)=>T
Max_m(LoaMgr_MotCurrRespSV_Cnt_M_u08, MotCurrResp_Cnt_T_u08)=>T
Max_m(LoaMgr_IvtrRespSV_Cnt_M_u08, IvtrResp_Cnt_T_u08)=>T

TS1.2 Largest Execution Path

if(LoaMgr_LOASt_State_M_enum == LOAST_RPDSHTDWNREQD)>F
else if(LoaMgr_LOASt_State_M_enum == LOAST_CTRLDSHTDWNREQD)=>F
if(MtrPosIdptSig_Cnt_T_u08 <= k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08)=>T
if(MotCurrIdptSig_Cnt_T_u08 <= k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08)=>T
(LoaMgr_LoaRateLimit_UlspS_M_f32>=500.0f)=>F
(LoaMgr_LoaScaleFctr_Uls_M_f32>=1)=>F
if ((HwTqResp_Cnt_T_u08 == D_LOASTSWMTGTN_CNT_U08)=>F||(LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc == TRUE)=>F)=>F
if ((MotAgResp_Cnt_T_u08 == D_LOASTSWMTGTN_CNT_U08)=>F||(LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc == TRUE)=>F)=>F
if ((MotCurrResp_Cnt_T_u08 == D_LOASTSWMTGTN_CNT_U08)=>F||(LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc == TRUE)=>F)=>F
if ((IvtrResp_Cnt_T_u08 == D_LOASTSWMTGTN_CNT_U08)=>F||(LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc == TRUE)=>F)=>F
if ((MtgtnCount_Cnt_T_u08 <= 1u))=>T
if(LoaMgr_LOASt_State_M_enum == LOAST_NORM)=>F
else if(LoaMgr_LOASt_State_M_enum == LOAST_REDCD)=>T
else if(LoaMgr_LOASt_State_M_enum == LOAST_REDCD)=>F
if (IvtrInactv_Cnt_T_logl == TRUE)=>F
Max_m(MultiMtgtnResp_Cnt_T_u08,Max_m(HwTqResp_Cnt_T_u08,
Max_m(MotAgResp_Cnt_T_u08,Max_m(MotCurrResp_Cnt_T_u08, IvtrResp_Cnt_T_u08))))=>F
switch(LoaMgr_MaxMtgtnResp_Cnt_M_u08):case1
if (HwTqIdptSig_Cnt_T_u08 > D_MAXHWTQIDPTSIGALLWD_CNT_U08)=>F
if (MtrPosIdptSig_Cnt_T_u08 > D_MAXMOTPOSNIDPTSIGALLWD_CNT_U08)=>F
if (MotCurrIdptSig_Cnt_T_u08 > D_MAXMOTCURRIDPTSIGALLWD_CNT_U08)=>F
Min_m(RngLimdMtrPosIdptSig_Cnt_T_u08, LoaMgr_MotAgIdptSigSV_Cnt_M_u08)=>T
Min_m(RngLimdMtrCurrIdptSig_Cnt_T_u08, LoaMgr_MotCurrIdptSigSV_Cnt_M_u08)=>T
Min_m(IvtrIdptSig_Cnt_T_u08, LoaMgr_IvtrIdptSigSV_Cnt_M_u08)=>T
switch (HwTqIdptMin_Cnt_T_u08):case1=>if ((LoaMgr_TloaAvail_Cnt_M_lgc == TRUE)=>F
&& LoaMgr_TloaDi_Cnt_M_lgc == FALSE))=>F
if (SteerMod_Cnt_T_enum == STEERMOD_FULLYATNMS)=>F
Max_m(LoaMgr_HwTqRespSV_Cnt_M_u08, HwTqResp_Cnt_T_u08)=>F

Test Step 1.1 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	0
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_HwTqRespSV_Cnt_M_u08	0
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	2
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_IvtrRespSV_Cnt_M_u08	1
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1

TEST DETAILS REPORT

LoaMgr_Per1

2018-05-18, 13:31:17+0530

Name	Input Value
LoaMgr_MotAgRespSV_Cnt_M_u08	5
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotCurrRespSV_Cnt_M_u08	3
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	0
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	2
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Actual Value	Expected Value	Result
LoaMgr_IvtrRespSV_Cnt_M_u08	1	1	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	3	3	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170}	{170}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1}**	**{0, 0, 0, 0, 0}**	✘
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1}	{1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	1	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 1.2 (Repeat Count = 1) ✘

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	0
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_HwTqRespSV_Cnt_M_u08	0
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_IvtrRespSV_Cnt_M_u08	0
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotAgRespSV_Cnt_M_u08	1
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	2
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotCurrRespSV_Cnt_M_u08	1
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	0
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	0.123400003
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	0
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	1	1	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	0	0	✔
LoaMgr_LOASt_State_M_enum	1	1	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	1	1	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0.123400003	0.123400003	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	1	1	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	1	1	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	1	1	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{173, 174}	{173, 174}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1}	{1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	1	1 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0.123400003	0.123400003 ± 0.001	✔

Name	Actual Value	Expected Value	Result
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	1	1	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Case 2: Range Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:

TS2.1 5287.00 Cycles
TS2.2 5486.00 Cycles
TS2.3 5054.00 Cycles
TS2.4 5021.00 Cycles
TS2.5 5005.00 Cycles
TS2.6 5005.00 Cycles
TS2.7 5005.00 Cycles
TS2.8 5005.00 Cycles
TS2.9 5005.00 Cycles
TS2.10 5005.00 Cycles
TS2.11 5005.00 Cycles
TS2.12 5005.00 Cycles
TS2.13 5005.00 Cycles
TS2.14 5005.00 Cycles
TS2.15 5005.00 Cycles
TS2.16 5005.00 Cycles
TS2.17 5005.00 Cycles
TS2.18 5005.00 Cycles
TS2.19 5005.00 Cycles
TS2.20 5005.00 Cycles
TS2.21 5005.00 Cycles
TS2.22 5005.00 Cycles
TS2.23 5005.00 Cycles
TS2.24 5005.00 Cycles
```

Description

Vector Description:

TS2.1All Min
TS2.2All Max
TS2.3DiagcStsIvtr1Inactv_Cnt_lgc==>Min
TS2.4DiagcStsIvtr1Inactv_Cnt_lgc==>Max
TS2.5DiagcStsIvtr2Inactv_Cnt_lgc==>Min
TS2.6DiagcStsIvtr2Inactv_Cnt_lgc==>Max
TS2.7HwTqIdptSig_Cnt_u08==>Min
TS2.8HwTqIdptSig_Cnt_u08==>Max
TS2.9HwTqIdptSig_Cnt_u08==>Pos
TS2.10MotCurrIdptSig_Cnt_u08==>Min
TS2.11MotCurrIdptSig_Cnt_u08==>Max
TS2.12MotCurrIdptSig_Cnt_u08==>Pos
TS2.13MtrPosIdptSig_Cnt_u08==>Min
TS2.14MtrPosIdptSig_Cnt_u08==>Max
TS2.15MtrPosIdptSig_Cnt_u08==>Pos
TS2.16TloaAvail_Cnt_lgc==>Min
TS2.17TloaAvail_Cnt_lgc==>Max
TS2.18TloaDi_Cnt_lgc==>Min
TS2.19TloaDi_Cnt_lgc==>Max
TS2.20LoaScaDi_Cnt_lgc==>Min
TS2.21LoaScaDi_Cnt_lgc==>Max
TS2.22SteerMod_Cnt_enum==>STEERMOD_BASEPS
TS2.23SteerMod_Cnt_enum==>STEERMOD_SEMIATNMS
TS2.24SteerMod_Cnt_enum==>STEERMOD_FULLYATNMS

Test Step 2.1 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	0
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_HwTqRespSV_Cnt_M_u08	0

TEST DETAILS REPORT

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Name	Input Value
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_IvtrRespSV_Cnt_M_u08	0
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotAgRespSV_Cnt_M_u08	0
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotCurrRespSV_Cnt_M_u08	0
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	0
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	0.00999999978
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	0
k_LoaMgr_FadeOutStRate_UlspS_f32	0.00999999978
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	0
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	0.00999999978
k_LoaMgr_HwTqMtgtnSca_Uls_f32	0
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	0.00999999978
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	0
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	0
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	0.00999999978
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	0
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	0.00999999978
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	0
k_LoaMgr_RedcdStRate_UlspS_f32	0.00999999978
k_LoaMgr_RedcdStSca_Uls_f32	0
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	0
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔

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LoaMgr_Per1

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Name	Actual Value	Expected Value	Result
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	0	0	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172, 173, 174}	{170, 172, 173, 174}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1, 1}	{1, 1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	4	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	4	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 2.2 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	1
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	4
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_HwTqRespSV_Cnt_M_u08	5
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	2
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_IvtrRespSV_Cnt_M_u08	5
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	3
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotAgRespSV_Cnt_M_u08	5
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	2
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotCurrRespSV_Cnt_M_u08	5
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	500
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	500
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	5
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	5
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	5

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Name	Input Value
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	5
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	5
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	5
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	4
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	500
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	5
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	5
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	2
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	500
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	5
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	3
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	500
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	5
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	5
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	5
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	5
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	500
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	500
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	4
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	2
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	4	4	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	3	3	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1	1	✔

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LoaMgr_Per1

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Name	Actual Value	Expected Value	Result
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172, 173, 174, 175}	{170, 172, 173, 174, 175}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1, 1, 1}**	**{0, 0, 0, 0, 0}**	✘
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1, 1, 1}	{1, 1, 1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	5	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	5	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 2.3 (Repeat Count = 1) ✘

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	0
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_HwTqRespSV_Cnt_M_u08	0
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_IvtrRespSV_Cnt_M_u08	0
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotAgRespSV_Cnt_M_u08	0
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotCurrRespSV_Cnt_M_u08	0
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	0
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	1
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172}	{170, 172}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1}	{1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 2.4 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	*none*
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	*none*
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_HwTqRespSV_Cnt_M_u08	*none*
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_IvtrRespSV_Cnt_M_u08	*none*
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotAgRespSV_Cnt_M_u08	*none*
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotCurrRespSV_Cnt_M_u08	*none*
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	*none*
LoaMgr_VltgMdSrcSV_Cnt_M_u08	*none*
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	0
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172, 173, 174, 175}	{170, 172, 173, 174, 175}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1, 1, 1}	{1, 1, 1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	5	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	5	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 2.5 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	*none*
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	*none*
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_HwTqRespSV_Cnt_M_u08	*none*
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_IvtrRespSV_Cnt_M_u08	*none*
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotAgRespSV_Cnt_M_u08	*none*
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotCurrRespSV_Cnt_M_u08	*none*
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	*none*
LoaMgr_VltgMdSrcSV_Cnt_M_u08	*none*
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	2
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc

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Name	Input Value
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172}	{170, 172}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1}	{1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 2.6 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	*none*
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	*none*
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_HwTqRespSV_Cnt_M_u08	*none*
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_IvtrRespSV_Cnt_M_u08	*none*
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotAgRespSV_Cnt_M_u08	*none*
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotCurrRespSV_Cnt_M_u08	*none*
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	*none*
LoaMgr_VltgMdSrcSV_Cnt_M_u08	*none*
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1

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Name	Input Value
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	1
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔

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Name	Actual Value	Expected Value	Result
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173}	{170, 173}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1}	{1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 2.7 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	*none*
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	*none*
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_HwTqRespSV_Cnt_M_u08	*none*
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_IvtrRespSV_Cnt_M_u08	*none*
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotAgRespSV_Cnt_M_u08	*none*
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotCurrRespSV_Cnt_M_u08	*none*
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	*none*
LoaMgr_VltgMdSrcSV_Cnt_M_u08	*none*
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5

TEST DETAILS REPORT

LoaMgr_Per1

2018-05-18, 13:31:17+0530

Name	Input Value
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	0
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172, 173, 174}	{170, 172, 173, 174}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1, 1}	{1, 1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	4	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	4	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 2.8 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	*none*
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	*none*
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_HwTqRespSV_Cnt_M_u08	*none*
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_IvtrRespSV_Cnt_M_u08	*none*
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotAgRespSV_Cnt_M_u08	*none*
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotCurrRespSV_Cnt_M_u08	*none*
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	*none*
LoaMgr_VltgMdSrcSV_Cnt_M_u08	*none*
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1

Name	Input Value
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	4
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	1
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173}	{170, 173}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1}	{1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 2.9 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	*none*
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	*none*
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_HwTqRespSV_Cnt_M_u08	*none*
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_IvtrRespSV_Cnt_M_u08	*none*
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotAgRespSV_Cnt_M_u08	*none*
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotCurrRespSV_Cnt_M_u08	*none*
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	*none*
LoaMgr_VltgMdSrcSV_Cnt_M_u08	*none*
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	0
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc

TEST DETAILS REPORT

LoaMgr_Per1

2018-05-18, 13:31:17+0530

Name	Input Value
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 174}	{170, 174}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1}	{1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 2.10 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	*none*
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	*none*
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_HwTqRespSV_Cnt_M_u08	*none*
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_IvtrRespSV_Cnt_M_u08	*none*
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotAgRespSV_Cnt_M_u08	*none*
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotCurrRespSV_Cnt_M_u08	*none*
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	*none*
LoaMgr_VltgMdSrcSV_Cnt_M_u08	*none*
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1

Name	Input Value
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	4
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	0
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔

Name	Actual Value	Expected Value	Result
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 174}	{170, 174}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1}	{1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 2.11 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	*none*
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	*none*
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_HwTqRespSV_Cnt_M_u08	*none*
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_IvtrRespSV_Cnt_M_u08	*none*
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotAgRespSV_Cnt_M_u08	*none*
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotCurrRespSV_Cnt_M_u08	*none*
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	*none*
LoaMgr_VltgMdSrcSV_Cnt_M_u08	*none*
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5

Name	Input Value
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	2
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172, 173}	{170, 172, 173}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 2.12 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	*none*
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	*none*
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_HwTqRespSV_Cnt_M_u08	*none*
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_IvtrRespSV_Cnt_M_u08	*none*
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotAgRespSV_Cnt_M_u08	*none*
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotCurrRespSV_Cnt_M_u08	*none*
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	*none*
LoaMgr_VltgMdSrcSV_Cnt_M_u08	*none*
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1

Name	Input Value
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	1
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172, 173}	{170, 172, 173}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 2.13 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	*none*
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	*none*
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_HwTqRespSV_Cnt_M_u08	*none*
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_IvtrRespSV_Cnt_M_u08	*none*
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotAgRespSV_Cnt_M_u08	*none*
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotCurrRespSV_Cnt_M_u08	*none*
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	*none*
LoaMgr_VltgMdSrcSV_Cnt_M_u08	*none*
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	0
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc

TEST DETAILS REPORT

LoaMgr_Per1

2018-05-18, 13:31:17+0530

Name	Input Value
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172, 173, 174}	{170, 172, 173, 174}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1, 1}	{1, 1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	4	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	4	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 2.14 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	*none*
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	*none*
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_HwTqRespSV_Cnt_M_u08	*none*
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_IvtrRespSV_Cnt_M_u08	*none*
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotAgRespSV_Cnt_M_u08	*none*
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotCurrRespSV_Cnt_M_u08	*none*
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	*none*
LoaMgr_VltgMdSrcSV_Cnt_M_u08	*none*
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1

Name	Input Value
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	0
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔

Name	Actual Value	Expected Value	Result
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172, 174}	{170, 172, 174}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 2.15 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	*none*
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	*none*
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_HwTqRespSV_Cnt_M_u08	*none*
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_IvtrRespSV_Cnt_M_u08	*none*
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotAgRespSV_Cnt_M_u08	*none*
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotCurrRespSV_Cnt_M_u08	*none*
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	*none*
LoaMgr_VltgMdSrcSV_Cnt_M_u08	*none*
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5

TEST DETAILS REPORT

LoaMgr_Per1

2018-05-18, 13:31:17+0530

Name	Input Value
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	0
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173, 174, 175}	{170, 173, 174, 175}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1, 1}	{1, 1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	4	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	4	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 2.16 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	*none*
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	*none*
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_HwTqRespSV_Cnt_M_u08	*none*
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_IvtrRespSV_Cnt_M_u08	*none*
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotAgRespSV_Cnt_M_u08	*none*
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotCurrRespSV_Cnt_M_u08	*none*
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	*none*
LoaMgr_VltgMdSrcSV_Cnt_M_u08	*none*
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1

Name	Input Value
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	0
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172, 174}	{170, 172, 174}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 2.17 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	*none*
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	*none*
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_HwTqRespSV_Cnt_M_u08	*none*
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_IvtrRespSV_Cnt_M_u08	*none*
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotAgRespSV_Cnt_M_u08	*none*
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotCurrRespSV_Cnt_M_u08	*none*
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	*none*
LoaMgr_VltgMdSrcSV_Cnt_M_u08	*none*
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	1
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173}	{170, 173}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1}	{1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 2.18 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	*none*
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	*none*
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_HwTqRespSV_Cnt_M_u08	*none*
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_IvtrRespSV_Cnt_M_u08	*none*
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotAgRespSV_Cnt_M_u08	*none*
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotCurrRespSV_Cnt_M_u08	*none*
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	*none*
LoaMgr_VltgMdSrcSV_Cnt_M_u08	*none*
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Actual Value	Expected Value	Result
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173, 174}	{170, 173, 174}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 2.19 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	*none*
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	*none*
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_HwTqRespSV_Cnt_M_u08	*none*
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_IvtrRespSV_Cnt_M_u08	*none*
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotAgRespSV_Cnt_M_u08	*none*
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotCurrRespSV_Cnt_M_u08	*none*
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	*none*
LoaMgr_VltgMdSrcSV_Cnt_M_u08	*none*
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5

Name	Input Value
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	2
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173, 175}	{170, 173, 175}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 2.20 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	*none*
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	*none*
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_HwTqRespSV_Cnt_M_u08	*none*
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_IvtrRespSV_Cnt_M_u08	*none*
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotAgRespSV_Cnt_M_u08	*none*
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotCurrRespSV_Cnt_M_u08	*none*
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	*none*
LoaMgr_VltgMdSrcSV_Cnt_M_u08	*none*
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0

TEST DETAILS REPORT

LoaMgr_Per1

2018-05-18, 13:31:17+0530

Name	Input Value
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	4
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	2
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170}	{170}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1}	{1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	1	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 2.21 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	*none*
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	*none*
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_HwTqRespSV_Cnt_M_u08	*none*
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_IvtrRespSV_Cnt_M_u08	*none*
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotAgRespSV_Cnt_M_u08	*none*
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotCurrRespSV_Cnt_M_u08	*none*
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	*none*
LoaMgr_VltgMdSrcSV_Cnt_M_u08	*none*
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	1
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc

Name	Input Value
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173}	{170, 173}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1}	{1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 2.22 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	*none*
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	*none*
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_HwTqRespSV_Cnt_M_u08	*none*
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_IvtrRespSV_Cnt_M_u08	*none*
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotAgRespSV_Cnt_M_u08	*none*
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotCurrRespSV_Cnt_M_u08	*none*
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	*none*
LoaMgr_VltgMdSrcSV_Cnt_M_u08	*none*
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1

TEST DETAILS REPORT

LoaMgr_Per1

2018-05-18, 13:31:17+0530

Name	Input Value
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	0
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔

Name	Actual Value	Expected Value	Result
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173}	{170, 173}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1}	{1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 2.23 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	*none*
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	*none*
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_HwTqRespSV_Cnt_M_u08	*none*
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_IvtrRespSV_Cnt_M_u08	*none*
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotAgRespSV_Cnt_M_u08	*none*
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotCurrRespSV_Cnt_M_u08	*none*
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	*none*
LoaMgr_VltgMdSrcSV_Cnt_M_u08	*none*
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5

Name	Input Value
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	1
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173, 174}	{170, 173, 174}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 2.24 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	*none*
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	*none*
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_HwTqRespSV_Cnt_M_u08	*none*
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_IvtrRespSV_Cnt_M_u08	*none*
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotAgRespSV_Cnt_M_u08	*none*
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	*none*
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	*none*
LoaMgr_MotCurrRespSV_Cnt_M_u08	*none*
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	*none*
LoaMgr_VltgMdSrcSV_Cnt_M_u08	*none*
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	2
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172, 173, 174}	{170, 172, 173, 174}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1, 1}	{1, 1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	4	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	4	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Case 3: PIM_R Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:

TS3.1 5058.00 Cycles
TS3.2 4977.00 Cycles
TS3.3 4970.00 Cycles
TS3.4 5001.00 Cycles
TS3.5 5063.00 Cycles
TS3.6 5014.00 Cycles
TS3.7 4991.00 Cycles
TS3.8 5009.00 Cycles
TS3.9 4990.00 Cycles
TS3.10 4960.00 Cycles
TS3.11 5102.00 Cycles
TS3.12 5027.00 Cycles
TS3.13 5004.00 Cycles
TS3.14 4980.00 Cycles
TS3.15 4998.00 Cycles
TS3.16 4988.00 Cycles
TS3.17 5095.00 Cycles
TS3.18 5068.00 Cycles
TS3.19 4981.00 Cycles
TS3.20 5026.00 Cycles
TS3.21 4954.00 Cycles
TS3.22 5041.00 Cycles
TS3.23 5014.00 Cycles
TS3.24 4989.00 Cycles
TS3.25 5024.00 Cycles
TS3.26 4982.00 Cycles
TS3.27 5011.00 Cycles
TS3.28 4960.00 Cycles
TS3.29 5024.00 Cycles
TS3.30 5076.00 Cycles
TS3.31 5038.00 Cycles
TS3.32 5056.00 Cycles
TS3.33 4975.00 Cycles
TS3.34 5023.00 Cycles
TS3.35 4968.00 Cycles
TS3.36 5057.00 Cycles
TS3.37 5025.00 Cycles
TS3.38 5037.00 Cycles
```

Description

Vector Description:

TS3.1LoaMgr_HwTqIdptSigSV_Cnt_M_u08==>Min
TS3.2LoaMgr_HwTqIdptSigSV_Cnt_M_u08==>Max
TS3.3LoaMgr_HwTqIdptSigSV_Cnt_M_u08==>Pos
TS3.4LoaMgr_HwTqIdptSigSV_Cnt_M_u08==>Min
TS3.5LoaMgr_HwTqIdptSigSV_Cnt_M_u08==>Max
TS3.6LoaMgr_HwTqIdptSigSV_Cnt_M_u08==>Pos
TS3.7LoaMgr_MotCurrIdptSigSV_Cnt_M_u08==>Min
TS3.8LoaMgr_MotCurrIdptSigSV_Cnt_M_u08==>Max
TS3.9LoaMgr_MotCurrIdptSigSV_Cnt_M_u08==>Pos
TS3.10LoaMgr_IvtrIdptSigSV_Cnt_M_u08==>Min
TS3.11LoaMgr_IvtrIdptSigSV_Cnt_M_u08==>Max
TS3.12LoaMgr_IvtrIdptSigSV_Cnt_M_u08==>Pos
TS3.13LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc==>Min
TS3.14LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc==>Max
TS3.15LoaMgr_MotAgRespSV_Cnt_M_u08==>Min
TS3.16LoaMgr_MotAgRespSV_Cnt_M_u08==>Max
TS3.17LoaMgr_MotAgRespSV_Cnt_M_u08==>Pos
TS3.18LoaMgr_MotCurrRespSV_Cnt_M_u08==>Min
TS3.19LoaMgr_MotCurrRespSV_Cnt_M_u08==>Max
TS3.20LoaMgr_MotCurrRespSV_Cnt_M_u08==>Pos
TS3.21LoaMgr_IvtrRespSV_Cnt_M_u08==>Min
TS3.22LoaMgr_IvtrRespSV_Cnt_M_u08==>Max
TS3.23LoaMgr_IvtrRespSV_Cnt_M_u08==>Pos
TS3.24LoaMgr_TloaAvail_Cnt_M_lgc==>Min
TS3.25LoaMgr_HwTqRespSV_Cnt_M_u08==>Max
TS3.26LoaMgr_HwTqRespSV_Cnt_M_u08==>Pos
TS3.27LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc==>Min
TS3.28LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc==>Max
TS3.29LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc==>Min
TS3.30LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc==>Max
TS3.31LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc==>Min
TS3.32LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc==>Max
TS3.33LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc==>Min
TS3.34LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc==>Max
TS3.35LoaMgr_VltgMdSrcSV_Cnt_M_u08==>Max
TS3.36LoaMgr_VltgMdSrcSV_Cnt_M_u08==>Min
TS3.37LoaMgr_AgSV_Cnt_M_lgc==>Max
TS3.38LoaMgr_AgSV_Cnt_M_lgc==>Pos

Test Step 3.1 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	0
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_HwTqRespSV_Cnt_M_u08	1
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_IvtrRespSV_Cnt_M_u08	4
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
LoaMgr_MotAgRespSV_Cnt_M_u08	5
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotCurrRespSV_Cnt_M_u08	3
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	1
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	2	2	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Actual Value	Expected Value	Result
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	3	3	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172, 175}	{170, 172, 175}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
[redacted]		[redacted]	1	✔
RqstRespConds	1	RqstRespConds	1	

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	4
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	1
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	4	4	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	3	3	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	2	2	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173, 175}	{170, 173, 175}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Actual Value	Expected Value	Result
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.3 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	0
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_HwTqRespSV_Cnt_M_u08	3
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	2
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_IvtrRespSV_Cnt_M_u08	5
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotAgRespSV_Cnt_M_u08	2
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotCurrRespSV_Cnt_M_u08	2
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0

Name	Input Value
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	4
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	1
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	3	3	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	2	2	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170}	{170}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1}	{1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	1	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.4 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	0
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_HwTqRespSV_Cnt_M_u08	0
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	2
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_IvtrRespSV_Cnt_M_u08	1
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotAgRespSV_Cnt_M_u08	5
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotCurrRespSV_Cnt_M_u08	1
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1

Name	Input Value
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	1
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	1	1	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173, 175}	{170, 173, 175}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

TEST DETAILS REPORT

LoaMgr_Per1

2018-05-18, 13:31:17+0530

Name	Input Value
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	5	5	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	1	1	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	3	3	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	4	4	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173}	{170, 173}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1}	{1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.6 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	0
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_HwTqRespSV_Cnt_M_u08	5
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	2
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_IvtrRespSV_Cnt_M_u08	2
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	2
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotAgRespSV_Cnt_M_u08	5
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotCurrRespSV_Cnt_M_u08	4
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1

Name	Input Value
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	4
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	1
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	5	5	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔

Name	Actual Value	Expected Value	Result
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	4	4	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173}	{170, 173}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1}	{1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.7 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	1
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_HwTqRespSV_Cnt_M_u08	4
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_IvtrRespSV_Cnt_M_u08	2
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	2
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotAgRespSV_Cnt_M_u08	4
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotCurrRespSV_Cnt_M_u08	3
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5

TEST DETAILS REPORT

LoaMgr_Per1

2018-05-18, 13:31:17+0530

Name	Input Value
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	0
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	4	4	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	3	3	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173, 174}	{170, 173, 174}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.8 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	1
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_HwTqRespSV_Cnt_M_u08	3
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_IvtrRespSV_Cnt_M_u08	0
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	2
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotAgRespSV_Cnt_M_u08	5
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	2
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotCurrRespSV_Cnt_M_u08	1
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0

Name	Input Value
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	1
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	0	0	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	1	1	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172}	{170, 172}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1}	{1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.9 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	1
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_HwTqRespSV_Cnt_M_u08	2
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_IvtrRespSV_Cnt_M_u08	2
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	3
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotAgRespSV_Cnt_M_u08	2
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotCurrRespSV_Cnt_M_u08	2
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	0
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	4
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	0
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc

Name	Input Value
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	2	2	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173, 174}	{170, 173, 174}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.10 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	0
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_HwTqRespSV_Cnt_M_u08	2
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_IvtrRespSV_Cnt_M_u08	3
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotAgRespSV_Cnt_M_u08	5
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotCurrRespSV_Cnt_M_u08	4
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1

Name	Input Value
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	2
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔

Name	Actual Value	Expected Value	Result
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	4	4	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173, 175}	{170, 173, 175}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.11 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	0
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_HwTqRespSV_Cnt_M_u08	0
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	2
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_IvtrRespSV_Cnt_M_u08	1
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotAgRespSV_Cnt_M_u08	5
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotCurrRespSV_Cnt_M_u08	3
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	0
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5

TEST DETAILS REPORT

LoaMgr_Per1

2018-05-18, 13:31:17+0530

Name	Input Value
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	2
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	1	1	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	3	3	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170}	{170}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1}	{1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	1	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.12 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	0
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_HwTqRespSV_Cnt_M_u08	1
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_IvtrRespSV_Cnt_M_u08	5
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotAgRespSV_Cnt_M_u08	4
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotCurrRespSV_Cnt_M_u08	3
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	0
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1

Name	Input Value
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	2
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	3	3	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 175}	{170, 175}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1}	{1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.13 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	1
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_HwTqRespSV_Cnt_M_u08	1
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_IvtrRespSV_Cnt_M_u08	5
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotAgRespSV_Cnt_M_u08	3
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotCurrRespSV_Cnt_M_u08	0
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	0
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	2
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc

TEST DETAILS REPORT

LoaMgr_Per1

2018-05-18, 13:31:17+0530

Name	Input Value
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	0	0	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172, 173}	{170, 172, 173}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.14 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	1
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_HwTqRespSV_Cnt_M_u08	2
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_IvtrRespSV_Cnt_M_u08	3
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotAgRespSV_Cnt_M_u08	4
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotCurrRespSV_Cnt_M_u08	1
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1

Name	Input Value
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	1
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	3	3	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	4	4	✔

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Actual Value	Expected Value	Result
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	1	1	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172, 173}	{170, 172, 173}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.15 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	1
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_HwTqRespSV_Cnt_M_u08	1
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_IvtrRespSV_Cnt_M_u08	5
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	2
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotAgRespSV_Cnt_M_u08	0
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotCurrRespSV_Cnt_M_u08	3
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5

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LoaMgr_Per1

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Name	Input Value
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	2
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	2	2	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	3	3	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172, 173}	{170, 172, 173}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.16 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	1
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_HwTqRespSV_Cnt_M_u08	2
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_IvtrRespSV_Cnt_M_u08	3
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotAgRespSV_Cnt_M_u08	5
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotCurrRespSV_Cnt_M_u08	1
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	0
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0

Name	Input Value
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	2
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	1	1	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170}	{170}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1}	{1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	1	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.17 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	1
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_HwTqRespSV_Cnt_M_u08	1
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_IvtrRespSV_Cnt_M_u08	4
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotAgRespSV_Cnt_M_u08	3
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	2
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotCurrRespSV_Cnt_M_u08	4
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	0
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	4	4	✔
LoaMgr_LOASt_State_M_enum	4	4	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	4	4	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	3	3	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	4	4	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{171, 173, 174}	{171, 173, 174}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_LOASt_State_enum.value	4	4	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.18 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	1
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_HwTqRespSV_Cnt_M_u08	1
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_IvtrRespSV_Cnt_M_u08	2
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	2
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotAgRespSV_Cnt_M_u08	5
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotCurrRespSV_Cnt_M_u08	0
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	0
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	0
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔

Name	Actual Value	Expected Value	Result
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172, 173, 174}	{170, 172, 173, 174}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1, 1}	{1, 1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	4	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	4	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.19 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	1
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_HwTqRespSV_Cnt_M_u08	5
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_IvtrRespSV_Cnt_M_u08	1
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotAgRespSV_Cnt_M_u08	3
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotCurrRespSV_Cnt_M_u08	5
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	2
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	1	1	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	3	3	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172, 173}	{170, 172, 173}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.20 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	1
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_HwTqRespSV_Cnt_M_u08	0
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_IvtrRespSV_Cnt_M_u08	3
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	2
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotAgRespSV_Cnt_M_u08	3
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	2
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotCurrRespSV_Cnt_M_u08	4
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	0
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	0
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	3	3	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	3	3	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	4	4	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173, 174}	{170, 173, 174}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.21 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	0
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_HwTqRespSV_Cnt_M_u08	1
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_IvtrRespSV_Cnt_M_u08	0
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotAgRespSV_Cnt_M_u08	1
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotCurrRespSV_Cnt_M_u08	1
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	4
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	1
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	0	0	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	2	2	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	1	1	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170}	{170}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1}	{1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	1	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.22 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	0
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_HwTqRespSV_Cnt_M_u08	2
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_IvtrRespSV_Cnt_M_u08	5
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	3
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotAgRespSV_Cnt_M_u08	2
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotCurrRespSV_Cnt_M_u08	3
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	0
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	2
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	3	3	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	2	2	✔

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LoaMgr_Per1

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Name	Actual Value	Expected Value	Result
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	3	3	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 175}	{170, 175}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1}	{1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.23 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	1
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_HwTqRespSV_Cnt_M_u08	3
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	2
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_IvtrRespSV_Cnt_M_u08	3
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotAgRespSV_Cnt_M_u08	2
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	2
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotCurrRespSV_Cnt_M_u08	0
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5

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LoaMgr_Per1

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Name	Input Value
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	0
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	3	3	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	2	2	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172, 173, 174}	{170, 172, 173, 174}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1, 1}	{1, 1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	4	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	4	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.24 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	0
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_HwTqRespSV_Cnt_M_u08	3
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	2
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_IvtrRespSV_Cnt_M_u08	3
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	3
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotAgRespSV_Cnt_M_u08	2
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotCurrRespSV_Cnt_M_u08	3
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	4
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	0
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	3	3	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	3	3	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	3	3	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	2	2	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	3	3	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 174}	{170, 174}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1}	{1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.25 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	0
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_HwTqRespSV_Cnt_M_u08	5
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	2
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_IvtrRespSV_Cnt_M_u08	2
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	2
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotAgRespSV_Cnt_M_u08	4
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotCurrRespSV_Cnt_M_u08	5
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	0
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	5	5	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	4	4	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173, 174}	{170, 173, 174}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.26 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	0
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_HwTqRespSV_Cnt_M_u08	2
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_IvtrRespSV_Cnt_M_u08	1
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	3
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotAgRespSV_Cnt_M_u08	3
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	2
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotCurrRespSV_Cnt_M_u08	2
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	2
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	3	3	✔

Name	Actual Value	Expected Value	Result
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172, 173, 175}	{170, 172, 173, 175}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1, 1}	{1, 1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	4	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	4	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.27 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	0
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_HwTqRespSV_Cnt_M_u08	4
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_IvtrRespSV_Cnt_M_u08	2
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotAgRespSV_Cnt_M_u08	1
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotCurrRespSV_Cnt_M_u08	1
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	0
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	4
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	0
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173, 174}	{170, 173, 174}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.28 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	0
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_HwTqRespSV_Cnt_M_u08	2
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_IvtrRespSV_Cnt_M_u08	3
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotAgRespSV_Cnt_M_u08	1
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotCurrRespSV_Cnt_M_u08	4
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	0
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	1
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	2	2	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	3	3	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	4	4	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173}	{170, 173}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1}	{1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.29 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	1
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_HwTqRespSV_Cnt_M_u08	1
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_IvtrRespSV_Cnt_M_u08	1
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotAgRespSV_Cnt_M_u08	1
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotCurrRespSV_Cnt_M_u08	4
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	1
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	2	2	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	1	1	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	2	2	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	4	4	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172, 173}	{170, 172, 173}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.30 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	1
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_HwTqRespSV_Cnt_M_u08	3
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	2
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_IvtrRespSV_Cnt_M_u08	3
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	2
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotAgRespSV_Cnt_M_u08	5
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotCurrRespSV_Cnt_M_u08	3
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	0
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	2
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	3	3	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔

Name	Actual Value	Expected Value	Result
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	3	3	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172, 173}	{170, 172, 173}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.31 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	0
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_HwTqRespSV_Cnt_M_u08	3
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_IvtrRespSV_Cnt_M_u08	3
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotAgRespSV_Cnt_M_u08	1
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	2
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotCurrRespSV_Cnt_M_u08	0
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	4
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	1
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	2	2	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	0	0	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173}	{170, 173}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1}	{1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.32 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	0
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_HwTqRespSV_Cnt_M_u08	2
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	2
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_IvtrRespSV_Cnt_M_u08	0
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	2
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotAgRespSV_Cnt_M_u08	1
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotCurrRespSV_Cnt_M_u08	0
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	0
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	2
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	0	0	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	1	1	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173}	{170, 173}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1}	{1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.33 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	0
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	3
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_HwTqRespSV_Cnt_M_u08	2
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_IvtrRespSV_Cnt_M_u08	1
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotAgRespSV_Cnt_M_u08	0
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotCurrRespSV_Cnt_M_u08	0
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	4
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	3
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	1
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	3	3	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	1	1	✔
LoaMgr_LOASt_State_M_enum	4	4	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	4	4	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	2	2	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	0	0	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{171}	{171}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1}	{1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	4	4	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	1	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	1	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.34 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	1
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_HwTqRespSV_Cnt_M_u08	3
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_IvtrRespSV_Cnt_M_u08	4
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotAgRespSV_Cnt_M_u08	1
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	2
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotCurrRespSV_Cnt_M_u08	1
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	0
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	1
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	3	3	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔

Name	Actual Value	Expected Value	Result
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	1	1	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173, 175}	{170, 173, 175}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.35 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	1
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_HwTqRespSV_Cnt_M_u08	3
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_IvtrRespSV_Cnt_M_u08	4
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotAgRespSV_Cnt_M_u08	1
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	2
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotCurrRespSV_Cnt_M_u08	1
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	0
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	1
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	3	3	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	1	1	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173, 175}	{170, 173, 175}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.36 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	0
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_HwTqRespSV_Cnt_M_u08	1
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	2
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_IvtrRespSV_Cnt_M_u08	2
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	3
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotAgRespSV_Cnt_M_u08	5
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	2
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotCurrRespSV_Cnt_M_u08	0
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	2
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	2
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	1
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	0	0	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	5	5	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	2	2	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	0	0	✔
LoaMgr_TloaAvail_Cnt_M_lgc	1	1	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172, 173}	{170, 172, 173}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.37 (Repeat Count = 1)

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	0
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_HwTqRespSV_Cnt_M_u08	4
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_IvtrRespSV_Cnt_M_u08	5
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotAgRespSV_Cnt_M_u08	3
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotCurrRespSV_Cnt_M_u08	1
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	4
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	1
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	0
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	1
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	1
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	1	1	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0	0	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	3	3	✔
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	2	2	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	1	1	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	0	0	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 173}	{170, 173}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1}	{1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	1	1 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	0	0	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	2	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔

Test Step 3.38 (Repeat Count = 1) ✖

Name	Input Value
LoaMgr_AgSV_Cnt_M_lgc	1
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	2
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_HwTqRespSV_Cnt_M_u08	4
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	2
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_IvtrRespSV_Cnt_M_u08	5
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	3
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	0
LoaMgr_MotAgRespSV_Cnt_M_u08	1
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1
LoaMgr_MotCurrRespSV_Cnt_M_u08	3
LoaMgr_SnsrIsMotAgAvail_Cnt_M_lgc	1
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1
Rte_Inst_Ap_LoaMgr	target_Rte_Inst_Ap_LoaMgr
k_LoaMgr_CurrIvtrMtgtnRate_UlspS_f32	1

TEST DETAILS REPORT

LoaMgr_Per1

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Name	Input Value
k_LoaMgr_CurrIvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_CurrIvtrMtgtnSca_Uls_f32	1
k_LoaMgr_FadeOutStRate_UlspS_f32	1
k_LoaMgr_HwTqIdptSig0TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig1NoTloaResp_Cnt_u08	4
k_LoaMgr_HwTqIdptSig1TloaAvailResp_Cnt_u08	2
k_LoaMgr_HwTqIdptSig2TloaDiResp_Cnt_u08	1
k_LoaMgr_HwTqIdptSig2TloaEnaResp_Cnt_u08	0
k_LoaMgr_HwTqIdptSig4Resp_Cnt_u08	0
k_LoaMgr_HwTqIdptSigFltThd_Cnt_u08	1
k_LoaMgr_HwTqMtgtnRate_UlspS_f32	1
k_LoaMgr_HwTqMtgtnSca_Uls_f32	1
k_LoaMgr_IvtrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_IvtrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_IvtrMtgtnRate_UlspS_f32	1
k_LoaMgr_IvtrMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_IvtrMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgIdptSig1NoSmaResp_Cnt_u08	5
k_LoaMgr_MotAgIdptSig2Resp_Cnt_u08	1
k_LoaMgr_MotAgIdptSig3Resp_Cnt_u08	0
k_LoaMgr_MotAgIdptSigFltThd_Cnt_u08	2
k_LoaMgr_MotAgMtgtnRate_UlspS_f32	1
k_LoaMgr_MotAgMtgtnScaZeroEn_Cnt_lgc	0
k_LoaMgr_MotAgMtgtnSca_Uls_f32	1
k_LoaMgr_MotAgSmaAvailResp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig0Resp_Cnt_u08	2
k_LoaMgr_MotCurrIdptSig1Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSig2Resp_Cnt_u08	0
k_LoaMgr_MotCurrIdptSigFltThd_Cnt_u08	0
k_LoaMgr_MotCurrMtgtnRate_UlspS_f32	1
k_LoaMgr_MotCurrMtgtnScaZeroEn_Cnt_lgc	1
k_LoaMgr_MotCurrMtgtnSca_Uls_f32	1
k_LoaMgr_RedcdStRate_UlspS_f32	1
k_LoaMgr_RedcdStSca_Uls_f32	1
target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc.value	0
target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc.value	1
target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_LoaScaDi_Cnt_lgc.value	0
target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08.value	1
target_LoaMgr_Per1_SteerMod_Cnt_enum.value	1
target_LoaMgr_Per1_TloaAvail_Cnt_lgc.value	0
target_LoaMgr_Per1_TloaDi_Cnt_lgc.value	0
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr1Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc	target_LoaMgr_Per1_DiagcStsIvtr2Inactv_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqIdptSig_Cnt_u08	target_LoaMgr_Per1_HwTqIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LOASt_State_enum	target_LoaMgr_Per1_LOASt_State_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_LoaScaDi_Cnt_lgc	target_LoaMgr_Per1_LoaScaDi_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrIdptSig_Cnt_u08	target_LoaMgr_Per1_MotCurrIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc	target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_MtrPosIdptSig_Cnt_u08	target_LoaMgr_Per1_MtrPosIdptSig_Cnt_u08
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_SteerMod_Cnt_enum	target_LoaMgr_Per1_SteerMod_Cnt_enum
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaAvail_Cnt_lgc	target_LoaMgr_Per1_TloaAvail_Cnt_lgc
target_Rte_Inst_Ap_LoaMgr.LoaMgr_Per1_TloaDi_Cnt_lgc	target_LoaMgr_Per1_TloaDi_Cnt_lgc

Name	Actual Value	Expected Value	Result
LoaMgr_AgSV_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_HwTqLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_HwTqRespSV_Cnt_M_u08	4	4	✔
LoaMgr_IvtrIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_IvtrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_IvtrRespSV_Cnt_M_u08	5	5	✔
LoaMgr_LOASt_State_M_enum	5	5	✔
LoaMgr_LoaRateLimit_UlspS_M_f32	500	500	✔
LoaMgr_LoaScaleFctr_Uls_M_f32	0	0	✔
LoaMgr_MaxMtgtnResp_Cnt_M_u08	5	5	✔
LoaMgr_MotAgIdptSigSV_Cnt_M_u08	1	1	✔
LoaMgr_MotAgLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotAgRespSV_Cnt_M_u08	2	2	✔

TEST DETAILS REPORT

LoaMgr_Per1

2018-05-18, 13:31:17+0530

Name	Actual Value	Expected Value	Result
LoaMgr_MotCurrIdptSigSV_Cnt_M_u08	0	0	✔
LoaMgr_MotCurrLoaMtgtnEn_Cnt_M_lgc	1	1	✔
LoaMgr_MotCurrRespSV_Cnt_M_u08	3	3	✔
LoaMgr_TloaAvail_Cnt_M_lgc	0	0	✔
LoaMgr_TloaDi_Cnt_M_lgc	0	0	✔
LoaMgr_VltgMdSrcSV_Cnt_M_u08	1	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(NTC_Cnt_T_enum)	{170, 172, 173}	{170, 172, 173}	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Param_Cnt_T_u08)	**{1, 1, 1}**	**{0, 0, 0, 0, 0}**	✖
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus(Status_Cnt_T_enum)	{1, 1, 1}	{1, 1, 1}	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32(data)	500	500 ± 0.01	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32(data)	0	0 ± 0.001	✔
target_LoaMgr_Per1_HwTqLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_IvtrLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_LOASt_State_enum.value	5	5	✔
target_LoaMgr_Per1_MotAgLoaMtgtnEn_Cnt_lgc.value	1	1	✔
target_LoaMgr_Per1_MotCurrLoaMtgtnEn_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
CalcIvtrState	2	CalcIvtrState	2	✔
LatchInputs	1	LatchInputs	1	✔
RqstRespConds	1	RqstRespConds	1	✔
RqstHwTqResp	1	RqstHwTqResp	1	✔
ArbResp	1	ArbResp	1	✔
ChooseFinalResp	1	ChooseFinalResp	1	✔
Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	Rte_Call_Ap_LoaMgr_NxtrDiagMgr_SetNTCStatus	3	✔
AssignScale	1	AssignScale	1	✔
Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Enter_Ap_LoaMgr_EaLoaScaleAndRate	1	✔
Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	Rte_Write_Ap_LoaMgr_LoaRateLimit_UlspS_f32	1	✔
Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	Rte_Write_Ap_LoaMgr_LoaScaleFctr_Uls_f32	1	✔
Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	Rte_Exit_Ap_LoaMgr_EaLoaScaleAndRate	1	✔