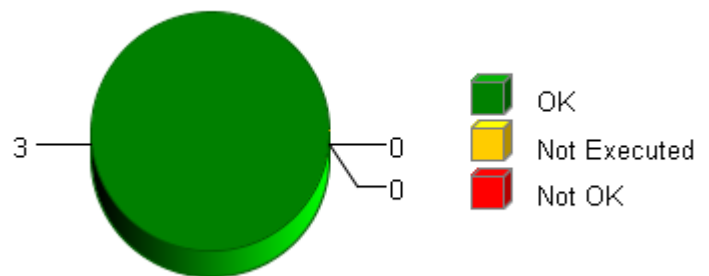


## Summary

Total Test Objects: 3  
Successful: 3  
Failed: 0  
Not Executed: 0  
Date: 2016-01-10  
Time: 16:35:38+0530

## Overall Test Object Results (including Coverage)



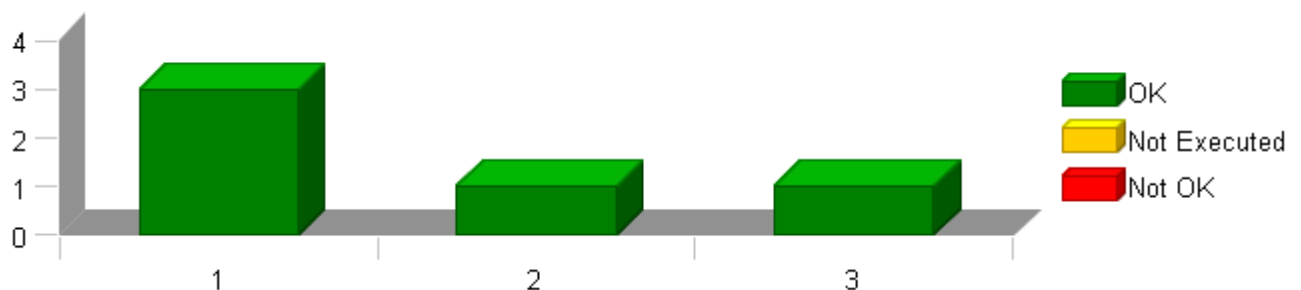
## Selected Project Items

Test Object "CBD\_UnitTest/MtrCtrl\_CM\_TrqCmdScl/TrqCmdScl\_Per1"  
Test Object "CBD\_UnitTest/MtrCtrl\_CM\_TrqCmdScl/TrqCmdScl\_SCom\_Get"  
Test Object "CBD\_UnitTest/MtrCtrl\_CM\_TrqCmdScl/TrqCmdScl\_SCom\_Set"

## Used Test Environments

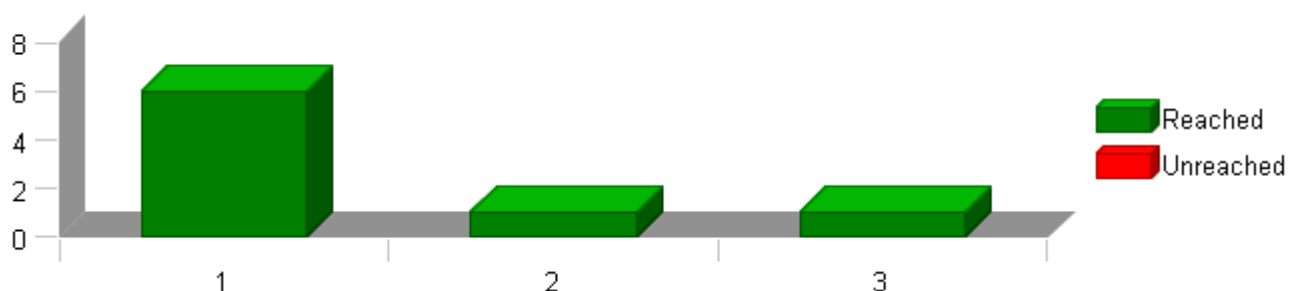
TI TMS 570 PLS UDE (Default)

## Test Case Results for Each Test Object (without Coverage)



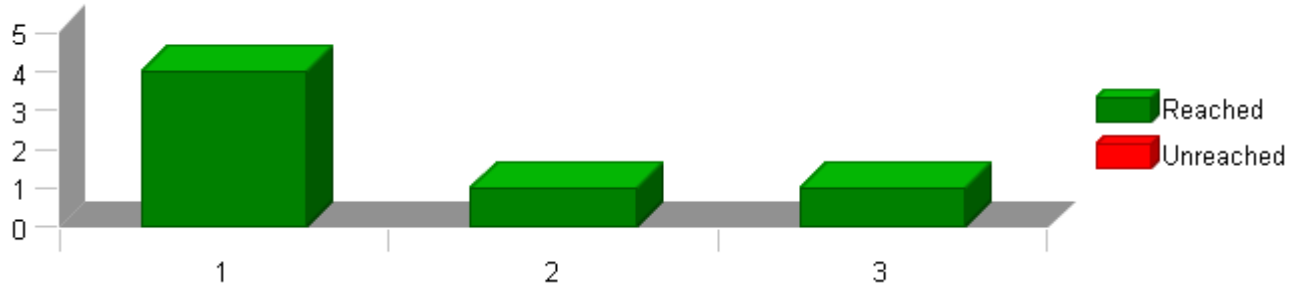
The table above shows each test object on the x axis and the number of test cases of the respective test object on the y axis. Each bar is divided into passed, not executed and failed test cases. The test case results do not take into account any coverage result (i.e. if all test cases of a test object are passed in this table but the coverage is failed, the overall test object result will be failed).

## Statement (C0) Coverage: Total Statements for Each Test Object



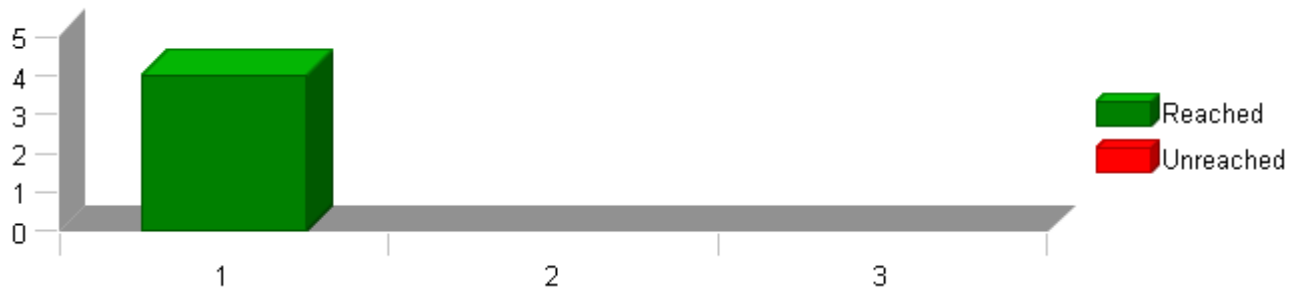
The table above shows each test object on the x axis and the number of statements of the respective test object on the y axis. Each bar is divided into reached statements (i.e. statements that have been executed during the test) and unreached statements.

### Branch (C1) Coverage: Total Branches for Each Test Object



The table above shows each test object on the x axis and the number of branches of the respective test object on the y axis. Each bar is divided into reached branches (i.e. branches that have been executed during the test) and unreached branches.

### Decision Coverage: Total Decision Outcomes for Each Test Object



The table above shows test objects on the x axis and the number of possible outcomes of all decisions of the respective test object on the y axis. To achieve full DC coverage, each decision must evaluate to both true and false.

Each bar is divided into reached and unreached decision outcomes.

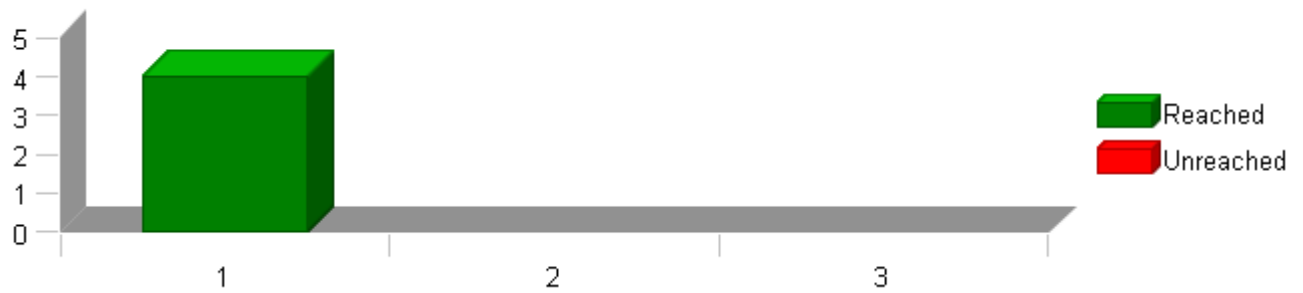
### MC/DC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MC/DC coverage, each decision requires all contained atomic conditions to evaluate to both true and false independently of all other conditions. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

## MCC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MCC coverage, each decision requires all contained atomic conditions to evaluate to all possible combinations of true and false values. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

## Test Object List

The following table lists all test objects with their test case and coverage results. The cumulated results for modules, folders and test collections are also displayed, the indentation within the name column indicates the parent relationship of the elements.

Please note that only test objects are numbered within the first column. This number is referenced on the x axis within the overview charts for test case and coverage results available on previous pages (if included into the report).

No.	Name	C0	C1	DC	MC/DC	MCC	Test Cases	Result
	MtrCtrl	100 %	100 %	100 %	100 %	100 %	5 of 5 passed	✓
	CBD_UnitTest	100 %	100 %	100 %	100 %	100 %	5 of 5 passed	✓
	MtrCtrl_CM_TrqCmdScl	100 %	100 %	100 %	100 %	100 %	5 of 5 passed	✓
1	<a href="#">TrqCmdScl_Per1</a>	100 %	100 %	100 %	100 %	100 %	3 of 3 passed	✓
2	<a href="#">TrqCmdScl_SCom_Get</a>	100 %	100 %	-	-	-	1 of 1 passed	✓
3	<a href="#">TrqCmdScl_SCom_Set</a>	100 %	100 %	-	-	-	1 of 1 passed	✓

MtrCtrl

MtrCtrl\_CM\_TrqCmdScl

TrqCmdScl\_SCom\_Set

100 %

100 %

	1
	1 ✓
	0
	0

	D:\Synergy_Work_Area\MtrCtrl_CM
	D:\Synergy_Work_Area\MtrCtrl_CM\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
	TI TMS 570 PLS UDE (Default)
	Unit Test
	\$(PROJECTROOT)\MtrCtrl_CM\src\Ap_TrqCmdScl.c
	-Dconst= -D_DATA_ACCESS= -I\$(PROJECTROOT)\StdDef\include -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\MtrCtrl_CM\utp\contract -I\$(PROJECTROOT)\MtrCtrl_CM\include -I\$(PROJECTROOT)\MtrCtrl_CM\utp\contract\Ap_TrqCmdScl -I\$(Compiler Install Path)\include

Module 'MtrCtrl_CM_TrqCmdScl'	*****Unit Test Information*****  Name of Tester:Priti Mangalekar Code File(s) Under Test:Ap_TrqCmdScl.c Code File(s) Version: 6 Module Design Document:TorqueCmdScaling_MDD.doc Module Design Document Version: 5 Data Dictionary Version:13 Unit Test Plan Version:1 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/ EPS Library 1.32 Total FLASH Used (Bytes):138 Total RAM Used (Bytes):0 Total CALS Used (Bytes):1026 Special Test Requirements: Test Date:01/10/2016 Comments:"NOTE1: INLINE functions defined in globalmacro.h are not unit-tested. NOTE2:""CBD_Sandbox_dbg.map"" map file is embedded for reference."  *****
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Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(ProgramFiles)\pls\UDE 3.2
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg

Workspace File	D:\Synergy_Work_Area\MtrCtrl_CM\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Performance Metrics :  
(With "None" instrumentation and WithPS  
Environment)

TS1.1 552.00 Cycles  
TS1.2 498.00 Cycles  
TS1.3 498.00 Cycles

Vector Description :

TS1.1 Par1\_f32=Min  
TS1.2 Par1\_f32=Max  
TS1.3 Par1\_f32=Pos

					✓
Par_f32	0.9				
Rte_Inst_Ap_TrqCmdScl	tgt_Rte_Inst_Ap_TrqCmdScl				
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32	tgt_Pim_TorqueCmdSF_Uls_f32				
tgt_Pim_TorqueCmdSF_Uls_f32	0.899999976	0.9			✓

T					✓
Rte_Call_Ap_TrqCmdScl_TrqCmdScl_WriteBlock	1	Rte_Call_Ap_TrqCmdScl_TrqCmdScl_WriteBlock	1		✓

					✓
Par_f32	1.1				
Rte_Inst_Ap_TrqCmdScl	tgt_Rte_Inst_Ap_TrqCmdScl				
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32	tgt_Pim_TorqueCmdSF_Uls_f32				
tgt_Pim_TorqueCmdSF_Uls_f32	1.10000002	1.1			✓

T					✓
Rte_Call_Ap_TrqCmdScl_TrqCmdScl_WriteBlock	1	Rte_Call_Ap_TrqCmdScl_TrqCmdScl_WriteBlock	1		✓

					✓
Par_f32	0.95				
Rte_Inst_Ap_TrqCmdScl	tgt_Rte_Inst_Ap_TrqCmdScl				
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32	tgt_Pim_TorqueCmdSF_Uls_f32				
tgt_Pim_TorqueCmdSF_Uls_f32	0.949999988	0.95			✓

T					✓
Rte_Call_Ap_TrqCmdScl_TrqCmdScl_WriteBlock	1	Rte_Call_Ap_TrqCmdScl_TrqCmdScl_WriteBlock	1		✓

# TEST DETAILS REPORT

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TrqCmdScl\_Per1



Project	MtrCtrl
Module	MtrCtrl_CM_TrqCmdScl
Test Object	TrqCmdScl_Per1

## Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MCC Coverage	100 %
MC/DC Coverage	100 %

## Statistics

Total Testcases	3
Successful	3 ✓
Failed	0
Not Executed	0

## Module Properties

Project Root Directory	D:\Synergy_Work_Area\MtrCtrl_CM
Configuration File	D:\Synergy_Work_Area\MtrCtrl_CM\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\MtrCtrl_CM\src\Ap_TrqCmdScl.c
Compiler Options	-Dconst= -D_DATA_ACCESS= -I\$(PROJECTROOT)\StdDef\include -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\MtrCtrl_CM\utpl\contract -I\$(PROJECTROOT)\MtrCtrl_CM\include -I\$(PROJECTROOT)\MtrCtrl_CM\utpl\contract\Ap_TrqCmdScl -I\$(Compiler Install Path)\include

## Comments/Description/Specification

Name	Text
Module 'MtrCtrl_CM_TrqCmdScl'	*****Unit Test Information*****  Name of Tester:Priti Mangalekar Code File(s) Under Test:Ap_TrqCmdScl.c Code File(s) Version: 6 Module Design Document:TorqueCmdScaling_MDD.doc Module Design Document Version: 5 Data Dictionary Version:13 Unit Test Plan Version:1 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/ EPS Library 1.32 Total FLASH Used (Bytes):138 Total RAM Used (Bytes):0 Total CALS Used (Bytes):1026 Special Test Requirements: Test Date:01/10/2016 Comments:"NOTE1: INLINE functions defined in globalmacro.h are not unit-tested. NOTE2:""CBD_Sandbox_dbg.map"" map file is embedded for reference."  *****

## Attributes

Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(ProgramFiles)\pls\UDE 3.2
Time Unit	Cycles
Timer Enabled	false



# TEST DETAILS REPORT

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TrqCmdScl\_Per1



Attributes	
Name	Value
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\MtrCtrl_CM\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

# TEST DETAILS REPORT

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TrqCmdScl\_Per1

## Test Case 1: Metrics Test

<b>Specification</b>	Performance Metrics : (With "None" instrumentation and WithPS Environment)
	TS1.1 1075.00 "Longest Execution Path" TS1.2 979.00 "Shortest Execution Path"
<b>Description</b>	Vector Description :
	TS1.1 "Longest Execution Path => ((TorqueCmdSF_Uls_T_f32) >= (k_MaxTrqCmdScl_Uls_f32))=FALSE ((TorqueCmdSF_Uls_T_f32) <= (k_MinTrqCmdScl_Uls_f32))=FALSE" TS1.2 "Shortest Execution Path => ((TorqueCmdSF_Uls_T_f32) >= (k_MaxTrqCmdScl_Uls_f32))=TRUE"

### Test Step 1.1 (Repeat Count = 1)

Name		Input Value		
Rte_Inst_Ap_TrqCmdScl		tgt_Rte_Inst_Ap_TrqCmdScl		
k_MaxTrqCmdScl_Uls_f32		1.1		
k_MinTrqCmdScl_Uls_f32		0.9		
tgt_Pim_TorqueCmdSF_Uls_f32		0.98		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32		tgt_Pim_TorqueCmdSF_Uls_f32		
tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32.value		2		
Name		Actual Value	Expected Value	Result
tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32.value		1.96000004	1.96 ± 0.0625	✓

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	✓
Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	✓

### Test Step 1.2 (Repeat Count = 1)

Name		Input Value		
Rte_Inst_Ap_TrqCmdScl		tgt_Rte_Inst_Ap_TrqCmdScl		
k_MaxTrqCmdScl_Uls_f32		0.98		
k_MinTrqCmdScl_Uls_f32		0.98		
tgt_Pim_TorqueCmdSF_Uls_f32		1		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32		tgt_Pim_TorqueCmdSF_Uls_f32		
tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32.value		3.2		
Name		Actual Value	Expected Value	Result
tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32.value		3.13600016	3.136 ± 0.0625	✓

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	✓
Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	✓

# TEST DETAILS REPORT

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TrqCmdScl\_Per1

## Test Case 2: Boundary Test

Specification	Performance Metrics : (With "None" instrumentation and WithPS Environment)
	TS2.1 1076.00 Cycles TS2.2 1013.00 Cycles TS2.3 995.00 Cycles TS2.4 995.00 Cycles TS2.5 994.00 Cycles TS2.6 994.00 Cycles TS2.7 1018.00 Cycles TS2.8 990.00 Cycles TS2.9 994.00 Cycles TS2.10 979.00 Cycles TS2.11 994.00 Cycles TS2.12 1018.00 Cycles TS2.13 990.00 Cycles TS2.14 994.00 Cycles TS2.15 979.00 Cycles TS2.16 995.00 Cycles
Description	Vector Description :
	TS2.1 MRFMtrTrqCmd_MtrNm_f32=Min TS2.2 MRFMtrTrqCmd_MtrNm_f32=Max TS2.3 MRFMtrTrqCmd_MtrNm_f32=Zero TS2.4 MRFMtrTrqCmd_MtrNm_f32=Pos TS2.5 MRFMtrTrqCmd_MtrNm_f32=Neg TS2.6 TorqueCmdSF_Uls_f32= Min TS2.7 TorqueCmdSF_Uls_f32= Max TS2.8 TorqueCmdSF_Uls_f32 =Pos TS2.9 k_MinTrqCmdScl_Uls_f32=Min/Default TS2.10 k_MinTrqCmdScl_Uls_f32=Max TS2.11 k_MinTrqCmdScl_Uls_f32=Pos TS2.12 k_MaxTrqCmdScl_Uls_f32=Min TS2.13 k_MaxTrqCmdScl_Uls_f32=Max/Default TS2.14 k_MaxTrqCmdScl_Uls_f32=Pos TS2.15 All Min TS2.16 All Max

### Test Step 2.1 (Repeat Count = 1)

Name	Input Value		
Rte_Inst_Ap_TrqCmdScl	tgt_Rte_Inst_Ap_TrqCmdScl		
k_MaxTrqCmdScl_Uls_f32	0.91		
k_MinTrqCmdScl_Uls_f32	0.91		
tgt_Pim_TorqueCmdSF_Uls_f32	0.91		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32	tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32	tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32	tgt_Pim_TorqueCmdSF_Uls_f32		
tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32.value	-8.8		
Name	Actual Value	Expected Value	Result
tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32.value	-8.00800037	-8.008 ± 0.0625	✔

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	✓
Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	✓

### Test Step 2.2 (Repeat Count = 1)

Name	Input Value		
Rte_Inst_Ap_TrqCmdScl	tgt_Rte_Inst_Ap_TrqCmdScl		
k_MaxTrqCmdScl_Uls_f32	0.92		
k_MinTrqCmdScl_Uls_f32	0.92		
tgt_Pim_TorqueCmdSF_Uls_f32	0.92		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32	tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32	tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32	tgt_Pim_TorqueCmdSF_Uls_f32		
tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32.value	8.8		
Name	Actual Value	Expected Value	Result
tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32.value	8.09600067	8.096 ± 0.0625	✔

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	✓
Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	✓

# TEST DETAILS REPORT

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TrqCmdScl\_Per1

Test Step 2.3 (Repeat Count = 1)				
Name		Input Value		
Rte_Inst_Ap_TrqCmdScl		tgt_Rte_Inst_Ap_TrqCmdScl		
k_MaxTrqCmdScl_Uls_f32		0.93		
k_MinTrqCmdScl_Uls_f32		0.93		
tgt_Pim_TorqueCmdSF_Uls_f32		0.93		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32		tgt_Pim_TorqueCmdSF_Uls_f32		
tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32.value		0		
Name		Actual Value	Expected Value	Result
tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32.value		0	0 ± 0.0625	✓

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	✓
Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	✓

Test Step 2.4 (Repeat Count = 1)				
Name		Input Value		
Rte_Inst_Ap_TrqCmdScl		tgt_Rte_Inst_Ap_TrqCmdScl		
k_MaxTrqCmdScl_Uls_f32		0.94		
k_MinTrqCmdScl_Uls_f32		0.94		
tgt_Pim_TorqueCmdSF_Uls_f32		0.94		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32		tgt_Pim_TorqueCmdSF_Uls_f32		
tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32.value		5.5		
Name		Actual Value	Expected Value	Result
tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32.value		5.17000008	5.17 ± 0.0625	✓

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	✓
Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	✓

Test Step 2.5 (Repeat Count = 1)				
Name		Input Value		
Rte_Inst_Ap_TrqCmdScl		tgt_Rte_Inst_Ap_TrqCmdScl		
k_MaxTrqCmdScl_Uls_f32		0.95		
k_MinTrqCmdScl_Uls_f32		0.95		
tgt_Pim_TorqueCmdSF_Uls_f32		0.95		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32		tgt_Pim_TorqueCmdSF_Uls_f32		
tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32.value		-5.5		
Name		Actual Value	Expected Value	Result
tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32.value		-5.2249999	-5.225 ± 0.0625	✓

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	✓
Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	✓

Test Step 2.6 (Repeat Count = 1)				
Name		Input Value		
Rte_Inst_Ap_TrqCmdScl		tgt_Rte_Inst_Ap_TrqCmdScl		
k_MaxTrqCmdScl_Uls_f32		0.96		
k_MinTrqCmdScl_Uls_f32		0.96		
tgt_Pim_TorqueCmdSF_Uls_f32		0.9		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32		tgt_Pim_TorqueCmdSF_Uls_f32		

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TrqCmdScl\_Per1

Name	Input Value		
tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32.value	4.2		
Name	Actual Value	Expected Value	Result
tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32.value	4.03199959	4.032 ± 0.0625	✔

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	✓
Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	✓

## Test Step 2.7 (Repeat Count = 1)

Name	Input Value		
Rte_Inst_Ap_TrqCmdScl	tgt_Rte_Inst_Ap_TrqCmdScl		
k_MaxTrqCmdScl_Uls_f32	0.97		
k_MinTrqCmdScl_Uls_f32	0.97		
tgt_Pim_TorqueCmdSF_Uls_f32	1.1		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32	tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32	tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32	tgt_Pim_TorqueCmdSF_Uls_f32		
tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32.value	-2.2		
Name	Actual Value	Expected Value	Result
tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32.value	-2.13400006	-2.134 ± 0.0625	✔

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	✓
Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	✓

## Test Step 2.8 (Repeat Count = 1)

Name	Input Value		
Rte_Inst_Ap_TrqCmdScl	tgt_Rte_Inst_Ap_TrqCmdScl		
k_MaxTrqCmdScl_Uls_f32	0.98		
k_MinTrqCmdScl_Uls_f32	0.98		
tgt_Pim_TorqueCmdSF_Uls_f32	0.96		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32	tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32	tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32	tgt_Pim_TorqueCmdSF_Uls_f32		
tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32.value	3.2		
Name	Actual Value	Expected Value	Result
tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32.value	3.13600016	3.136 ± 0.0625	✔

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	✓
Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	✓

## Test Step 2.9 (Repeat Count = 1)

Name	Input Value		
Rte_Inst_Ap_TrqCmdScl	tgt_Rte_Inst_Ap_TrqCmdScl		
k_MaxTrqCmdScl_Uls_f32	0.96		
k_MinTrqCmdScl_Uls_f32	0.9		
tgt_Pim_TorqueCmdSF_Uls_f32	0.99		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32	tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32	tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32	tgt_Pim_TorqueCmdSF_Uls_f32		
tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32.value	1.1		
Name	Actual Value	Expected Value	Result
tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32.value	1.05599999	1.056 ± 0.0625	✔

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	✓
Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	✓

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Test Step 2.10 (Repeat Count = 1)				
Name		Input Value		
Rte_Inst_Ap_TrqCmdScl		tgt_Rte_Inst_Ap_TrqCmdScl		
k_MaxTrqCmdScl_Uls_f32		0.97		
k_MinTrqCmdScl_Uls_f32		1.1		
tgt_Pim_TorqueCmdSF_Uls_f32		1		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32		tgt_Pim_TorqueCmdSF_Uls_f32		
tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32.value		-1.1		
Name		Actual Value	Expected Value	Result
tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32.value		-1.06700003	-1.067 ± 0.0625	✓

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	✓
Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	✓

Test Step 2.11 (Repeat Count = 1)				
Name		Input Value		
Rte_Inst_Ap_TrqCmdScl		tgt_Rte_Inst_Ap_TrqCmdScl		
k_MaxTrqCmdScl_Uls_f32		0.98		
k_MinTrqCmdScl_Uls_f32		0.96		
tgt_Pim_TorqueCmdSF_Uls_f32		1.1		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32		tgt_Pim_TorqueCmdSF_Uls_f32		
tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32.value		2.2		
Name		Actual Value	Expected Value	Result
tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32.value		2.15600014	2.156 ± 0.0625	✓

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	✓
Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	✓

Test Step 2.12 (Repeat Count = 1)				
Name		Input Value		
Rte_Inst_Ap_TrqCmdScl		tgt_Rte_Inst_Ap_TrqCmdScl		
k_MaxTrqCmdScl_Uls_f32		0.9		
k_MinTrqCmdScl_Uls_f32		0.99		
tgt_Pim_TorqueCmdSF_Uls_f32		0.96		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32		tgt_Pim_TorqueCmdSF_Uls_f32		
tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32.value		-2.2		
Name		Actual Value	Expected Value	Result
tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32.value		-1.98000002	-1.98 ± 0.0625	✓

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	✓
Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	✓

Test Step 2.13 (Repeat Count = 1)				
Name		Input Value		
Rte_Inst_Ap_TrqCmdScl		tgt_Rte_Inst_Ap_TrqCmdScl		
k_MaxTrqCmdScl_Uls_f32		1.1		
k_MinTrqCmdScl_Uls_f32		1		
tgt_Pim_TorqueCmdSF_Uls_f32		0.97		

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Name	Input Value		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32	tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32	tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32	tgt_Pim_TorqueCmdSF_Uls_f32		
tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32.value	3.3		
Name	Actual Value	Expected Value	Result
tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32.value	3.29999995	3.3 ± 0.0625	✔

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	✓
Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	✓

## Test Step 2.14 (Repeat Count = 1)

Name	Input Value		
Rte_Inst_Ap_TrqCmdScl	tgt_Rte_Inst_Ap_TrqCmdScl		
k_MaxTrqCmdScl_Uls_f32	0.96		
k_MinTrqCmdScl_Uls_f32	1.1		
tgt_Pim_TorqueCmdSF_Uls_f32	0.98		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32	tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32	tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32	tgt_Pim_TorqueCmdSF_Uls_f32		
tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32.value	-3.3		
Name	Actual Value	Expected Value	Result
tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32.value	-3.16799998	-3.168 ± 0.0625	✔

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	✓
Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	✓

## Test Step 2.15 (Repeat Count = 1)

Name	Input Value		
Rte_Inst_Ap_TrqCmdScl	tgt_Rte_Inst_Ap_TrqCmdScl		
k_MaxTrqCmdScl_Uls_f32	0.9		
k_MinTrqCmdScl_Uls_f32	0.9		
tgt_Pim_TorqueCmdSF_Uls_f32	0.9		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32	tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32	tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32	tgt_Pim_TorqueCmdSF_Uls_f32		
tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32.value	-8.8		
Name	Actual Value	Expected Value	Result
tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32.value	-7.92000008	-7.92 ± 0.0625	✔

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	✓
Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	✓

## Test Step 2.16 (Repeat Count = 1)

Name	Input Value		
Rte_Inst_Ap_TrqCmdScl	tgt_Rte_Inst_Ap_TrqCmdScl		
k_MaxTrqCmdScl_Uls_f32	1.1		
k_MinTrqCmdScl_Uls_f32	1.1		
tgt_Pim_TorqueCmdSF_Uls_f32	1.1		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32	tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32	tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32	tgt_Pim_TorqueCmdSF_Uls_f32		
tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32.value	8.8		
Name	Actual Value	Expected Value	Result
tat_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32.value	9.68000031	9.68 ± 0.0625	✔

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T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	✓
Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	✓

## Test Case 3: Path Test

Specification	Performance Metrics : (With "None" instrumentation and WithPS Environment)
	TS3.1 1075.00 Cycles TS3.2 1026.00 Cycles TS3.3 1009.00 Cycles
Description	Vector Description :  TS3.1 (TorqueCmdSF_Uls_T_f32 >= k_MaxTrqCmdScl_Uls_f32)=TRUE TS3.2 (TorqueCmdSF_Uls_T_f32 >= k_MaxTrqCmdScl_Uls_f32)=FALSE TS3.3 (TorqueCmdSF_Uls_T_f32 <= k_MinTrqCmdScl_Uls_f32)=FALSE

### Test Step 3.1 (Repeat Count = 1)

T			
Name	Input Value		
Rte_Inst_Ap_TrqCmdScl	tgt_Rte_Inst_Ap_TrqCmdScl		
k_MaxTrqCmdScl_Uls_f32	0.9		
k_MinTrqCmdScl_Uls_f32	0.9		
tgt_Pim_TorqueCmdSF_Uls_f32	1.1		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32	tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32	tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32	tgt_Pim_TorqueCmdSF_Uls_f32		
tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32.value	1		
Name	Actual Value	Expected Value	Result
tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32.value	0.899999976	0.9 ± 0.0625	✓

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	✓
Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	✓

### Test Step 3.2 (Repeat Count = 1)

T			
Name	Input Value		
Rte_Inst_Ap_TrqCmdScl	tgt_Rte_Inst_Ap_TrqCmdScl		
k_MaxTrqCmdScl_Uls_f32	1.1		
k_MinTrqCmdScl_Uls_f32	0.9		
tgt_Pim_TorqueCmdSF_Uls_f32	0.9		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32	tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32	tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32		
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32	tgt_Pim_TorqueCmdSF_Uls_f32		
tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32.value	2		
Name	Actual Value	Expected Value	Result
tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32.value	1.79999995	1.8 ± 0.0625	✓

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	✓
Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	✓

### Test Step 3.3 (Repeat Count = 1)

T	
Name	Input Value
Rte_Inst_Ap_TrqCmdScl	tgt_Rte_Inst_Ap_TrqCmdScl
k_MaxTrqCmdScl_Uls_f32	1.1
k_MinTrqCmdScl_Uls_f32	0.9
tgt_Pim_TorqueCmdSF_Uls_f32	0.98
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32	tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32
tgt_Rte_Inst_Ap_TrqCmdScl.TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32	tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32	tgt_Pim_TorqueCmdSF_Uls_f32



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Name	Input Value		
tgt_TrqCmdScl_Per1_MRFMtrTrqCmd_MtrNm_f32.value	2		
Name	Actual Value	Expected Value	Result
tgt_TrqCmdScl_Per1_MRFMtrTrqCmdScl_MtrNm_f32.value	1.96000004	1.96 ± 0.0625	✓

T					✓
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP0_CheckpointReached	1	✓	
Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	Rte_Call_TrqCmdScl_Per1_CP1_CheckpointReached	1	✓	

MtrCtrl

MtrCtrl\_CM\_TrqCmdScl

TrqCmdScl\_SCom\_Get

100 %

100 %

	1
	1 ✓
	0
	0

	D:\Synergy_Work_Area\MtrCtrl_CM
	D:\Synergy_Work_Area\MtrCtrl_CM\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
	TI TMS 570 PLS UDE (Default)
	Unit Test
	\$(PROJECTROOT)\MtrCtrl_CM\src\Ap_TrqCmdScl.c
	-Dconst= -D_DATA_ACCESS= -I\$(PROJECTROOT)\StdDef\include -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\MtrCtrl_CM\utp\contract -I\$(PROJECTROOT)\MtrCtrl_CM\include -I\$(PROJECTROOT)\MtrCtrl_CM\utp\contract\Ap_TrqCmdScl -I\$(Compiler Install Path)\include

Module 'MtrCtrl_CM_TrqCmdScl'	*****Unit Test Information*****  Name of Tester:Priti Mangalekar Code File(s) Under Test:Ap_TrqCmdScl.c Code File(s) Version: 6 Module Design Document:TorqueCmdScaling_MDD.doc Module Design Document Version: 5 Data Dictionary Version:13 Unit Test Plan Version:1 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/ EPS Library 1.32 Total FLASH Used (Bytes):138 Total RAM Used (Bytes):0 Total CALS Used (Bytes):1026 Special Test Requirements: Test Date:01/10/2016 Comments:"NOTE1: INLINE functions defined in globalmacro.h are not unit-tested. NOTE2:""CBD_Sandbox_dbg.map"" map file is embedded for reference."  *****
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Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(ProgramFiles)\pls\UDE 3.2
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg



Workspace File	D:\Synergy_Work_Area\MtrCtrl_CM\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Performance Metrics :  
(With "None" instrumentation and WithPS  
Environment)

TS1.1 16.00 Cycles  
TS1.2 16.00 Cycles  
TS1.3 16.00 Cycles

Vector Description :

TS1.1 Rte\_Pim\_TorqueCmdSF\_Uls\_f32=Min  
TS1.2 Rte\_Pim\_TorqueCmdSF\_Uls\_f32=Max  
TS1.3 Rte\_Pim\_TorqueCmdSF\_Uls\_f32=Pos

				✓
Par_f32	tgt_Par_f32			
Rte_Inst_Ap_TrqCmdScl	tgt_Rte_Inst_Ap_TrqCmdScl			
tgt_Pim_TorqueCmdSF_Uls_f32	0.9			
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32	tgt_Pim_TorqueCmdSF_Uls_f32			
tgt_Par_f32	0.899999976	0.9		✓

				✓
Par_f32	tgt_Par_f32			
Rte_Inst_Ap_TrqCmdScl	tgt_Rte_Inst_Ap_TrqCmdScl			
tgt_Pim_TorqueCmdSF_Uls_f32	1.1			
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32	tgt_Pim_TorqueCmdSF_Uls_f32			
tgt_Par_f32	1.10000002	1.1		✓

				✓
Par_f32	tgt_Par_f32			
Rte_Inst_Ap_TrqCmdScl	tgt_Rte_Inst_Ap_TrqCmdScl			
tgt_Pim_TorqueCmdSF_Uls_f32	0.95			
tgt_Rte_Inst_Ap_TrqCmdScl.Pim_TorqueCmdSF_Uls_f32	tgt_Pim_TorqueCmdSF_Uls_f32			
tgt_Par_f32	0.949999988	0.95		✓