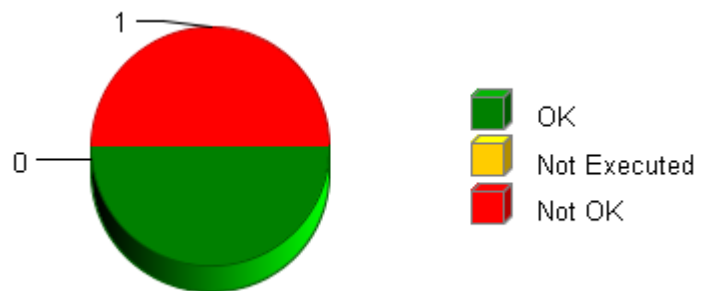


## Summary

<b>Total Test Objects:</b>	2
<b>Successful:</b>	1
<b>Failed:</b>	1
<b>Not Executed:</b>	0
<b>Date:</b>	2018-03-12
<b>Time:</b>	13:21:04+0530

## Overall Test Object Results (including Coverage)



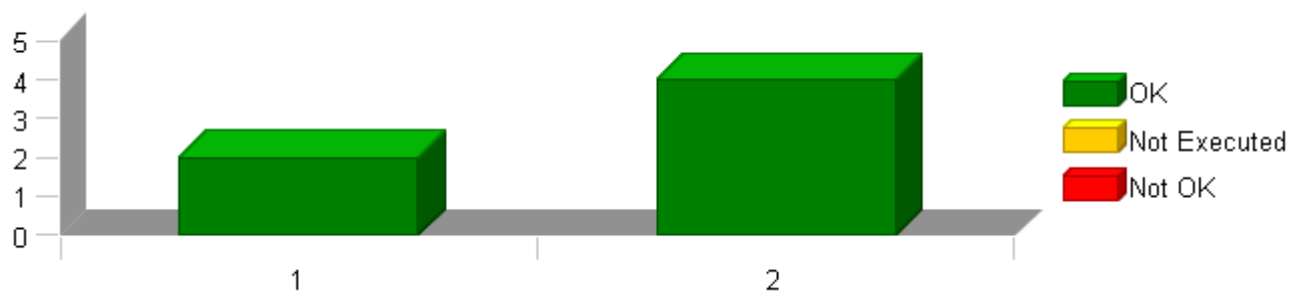
## Selected Project Items

Test Collection "CBD\_UnitTest"

## Used Test Environments

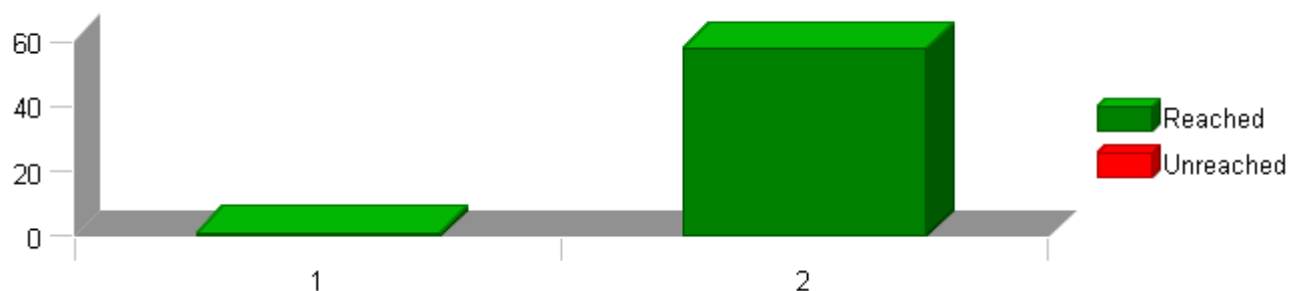
TI TMS 570 PLS UDE (Default)

## Test Case Results for Each Test Object (without Coverage)



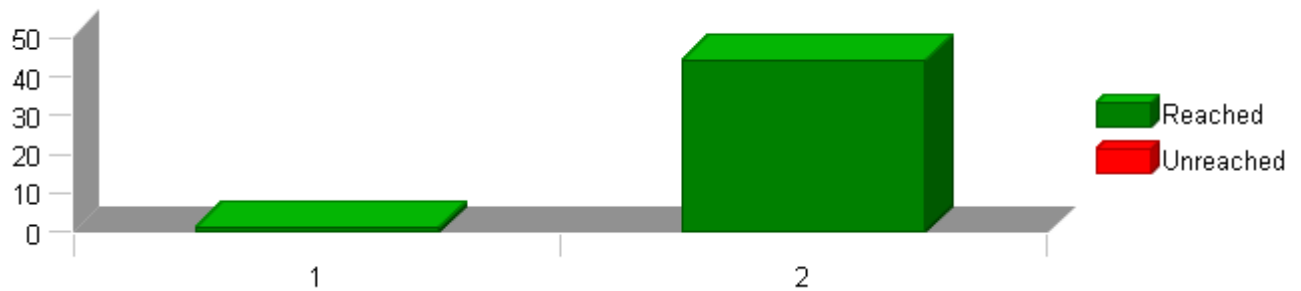
The table above shows each test object on the x axis and the number of test cases of the respective test object on the y axis. Each bar is divided into passed, not executed and failed test cases. The test case results do not take into account any coverage result (i.e. if all test cases of a test object are passed in this table but the coverage is failed, the overall test object result will be failed).

## Statement (C0) Coverage: Total Statements for Each Test Object



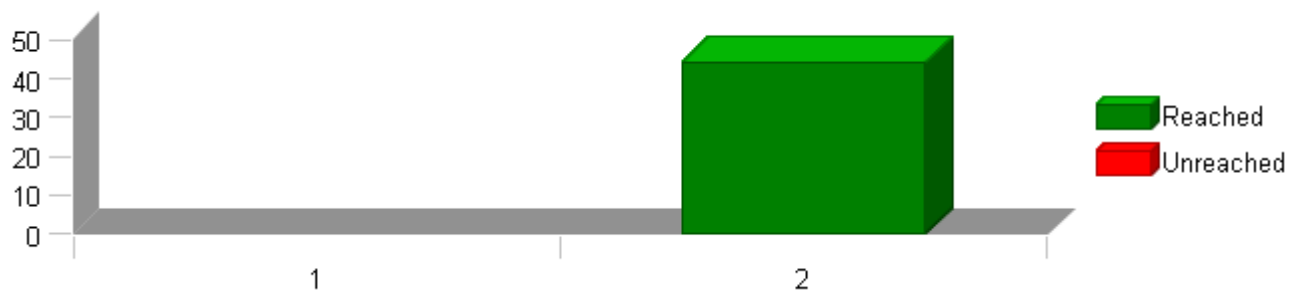
The table above shows each test object on the x axis and the number of statements of the respective test object on the y axis. Each bar is divided into reached statements (i.e. statements that have been executed during the test) and unreached statements.

### Branch (C1) Coverage: Total Branches for Each Test Object



The table above shows each test object on the x axis and the number of branches of the respective test object on the y axis. Each bar is divided into reached branches (i.e. branches that have been executed during the test) and unreached branches.

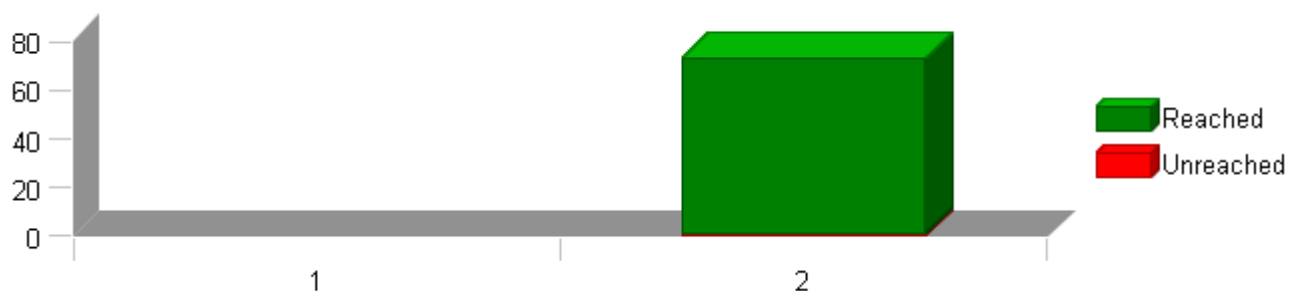
### Decision Coverage: Total Decision Outcomes for Each Test Object



The table above shows test objects on the x axis and the number of possible outcomes of all decisions of the respective test object on the y axis. To achieve full DC coverage, each decision must evaluate to both true and false.

Each bar is divided into reached and unreached decision outcomes.

### MC/DC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MC/DC coverage, each decision requires all contained atomic conditions to evaluate to both true and false independently of all other conditions. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

## TEST OVERVIEW REPORT

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Project VehPwrMd



### Test Object List

The following table lists all test objects with their test case and coverage results. The cumulated results for modules, folders and test collections are also displayed, the indentation within the name column indicates the parent relationship of the elements.

Please note that only test objects are numbered within the first column. This number is referenced on the x axis within the overview charts for test case and coverage results available on previous pages (if included into the report).

No.	Name	C0	C1	DC	MC/DC	Test Cases	Result
	VehPwrMd	100 %	100 %	100 %	98.63 %	6 of 6 passed	✖
	CBD_UnitTest	100 %	100 %	100 %	98.63 %	6 of 6 passed	✖
	VehPwrMd	100 %	100 %	100 %	98.63 %	6 of 6 passed	✖
1	<a href="#">VehPwrMd_Init1</a>	100 %	100 %	-	-	2 of 2 passed	✔
2	<a href="#">VehPwrMd_Per1</a>	100 %	100 %	100 %	98.63 %	4 of 4 passed	✖

# TEST DETAILS REPORT

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VehPwrMd\_Per1



Project	
Module	
Test Object	

## Instrumentation: Test Object Only

Statement (C0) Coverage	
Decision Coverage	
Branch (C1) Coverage	
MC/DC Coverage	98.63 %

## Statistics

Total Testcases	
Successful	✓
Failed	
Not Executed	

## Module Properties

Project Root Directory	
Configuration File	
Target Environment	
Kind of Test	
Linker Options	
Source File(s)	
File	
Compiler Options	

## Comments/Description/Specification

Name	Text

## Attributes

Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570.tpl
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4
Time Unit	cycles

# TEST DETAILS REPORT

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VehPwrMd\_Per1



Attributes	
Name	Value
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\VehPwrMd\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

## VehPwrMd\_Per1



Performance Metrics:

CPU Cycles:

```
TS1.1 1731.00 Cycles
TS1.2 1812.00 Cycles
```

### Description



## VehPwrMd\_Per1

[illegible]

## Test Step 1.2 (Repeat Count = 1) ✔

[illegible]

## VehPwrMd\_Per1

[illegible]

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓
				✓





Test Case 2: Range Test

Specification	Performance Metrics:  (With "None" Instrumentation and "WithPS" Environment)  CPU Cycles:  TS2.1 1732.00 Cycles TS2.2 1713.00 Cycles TS2.3 1791.00 Cycles TS2.4 1733.00 Cycles TS2.5 1729.00 Cycles TS2.6 1695.00 Cycles TS2.7 1662.00 Cycles TS2.8 1682.00 Cycles TS2.9 1723.00 Cycles TS2.10 1682.00 Cycles TS2.11 1662.00 Cycles TS2.12 1718.00 Cycles TS2.13 1682.00 Cycles TS2.14 2242.00 Cycles TS2.15 1748.00 Cycles TS2.16 1764.00 Cycles TS2.17 1716.00 Cycles TS2.18 1741.00 Cycles TS2.19 1713.00 Cycles TS2.20 1718.00 Cycles TS2.21 1718.00 Cycles TS2.22 1698.00 Cycles TS2.23 1666.00 Cycles TS2.24 1705.00 Cycles TS2.25 1735.00 Cycles TS2.26 1705.00 Cycles TS2.27 1701.00 Cycles TS2.28 1735.00 Cycles TS2.29 1666.00 Cycles TS2.30 1666.00 Cycles TS2.31 1701.00 Cycles TS2.32 1666.00 Cycles TS2.33 1666.00 Cycles TS2.34 2242.00 Cycles TS2.35 1716.00 Cycles TS2.36 1714.00 Cycles TS2.37 1741.00 Cycles TS2.38 1666.00 Cycles TS2.39 2260.00 Cycles TS2.40 1712.00 Cycles TS2.41 1734.00 Cycles
Description	

Test Step 2.1 (Repeat Count = 1)

Name	Input Value

## VehPwrMd\_Per1

[illegible]

Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓

## VehPwrMd\_Per1

[illegible]

## VehPwrMd\_Per1

[illegible]



*VehPwrMd\_Per1*



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓
			✓

## VehPwrMd\_Per1



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓

TEST DETAILS REPORT

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VehPwrMd\_Per1

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓
			✓
			✓
			✓

Test Step Call Trace					✓
Actual Function	Count	Expected Function	Count	Result	
					✓
					✓
					✓





## VehPwrMd\_Per1

[illegible]

*VehPwrMd\_Per1*



5



---

*VehPwrMd\_Per1*



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓
			✓

*VehPwrMd\_Per1*



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓

TEST DETAILS REPORT

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VehPwrMd\_Per1

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓
			✓
			✓
			✓

Test Step Call Trace

					✓
Actual Function	Count	Expected Function	Count	Result	
					✓
					✓
					✓

## VehPwrMd\_Per1

[illegible]

## VehPwrMd\_Per1



5





TEST DETAILS REPORT

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VehPwrMd\_Per1

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓

## VehPwrMd\_Per1

[illegible]

*VehPwrMd\_Per1*



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓
				✓

## VehPwrMd\_Per1



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓

[illegible]

## VehPwrMd\_Per1



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓

[illegible]



*VehPwrMd\_Per1*

[illegible]

## VehPwrMd\_Per1

[illegible]



*VehPwrMd\_Per1*

[illegible]

*VehPwrMd\_Per1*

[illegible][illegible]

## VehPwrMd\_Per1

[illegible]

5



*VehPwrMd\_Per1*

[illegible][illegible]

*VehPwrMd\_Per1*

[illegible]

*VehPwrMd\_Per1*

[illegible]

5

TEST DETAILS REPORT

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VehPwrMd\_Per1

Name	Input Value



## VehPwrMd\_Per1

[illegible]

## Test Step 2.30 (Repeat Count = 1) ✔

## VehPwrMd\_Per1

[illegible]

Test Step 2.31 (Repeat Count = 1)	
Name	Input Value

## VehPwrMd\_Per1

[illegible]

Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓
				✓

## VehPwrMd\_Per1

[illegible]

## VehPwrMd\_Per1

[illegible]



## VehPwrMd\_Per1



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓
				✓

[illegible]

TEST DETAILS REPORT

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VehPwrMd\_Per1

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓
			✓
			✓

Test Step Call Trace ✓

Actual Function	Count	Expected Function	Count	Result
-----------------	-------	-------------------	-------	--------



TEST DETAILS REPORT

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VehPwrMd\_Per1

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓
			✓
			✓
			✓

Test Step Call Trace

					✓
Actual Function	Count	Expected Function	Count	Result	
					✓
					✓
					✓

## VehPwrMd\_Per1

[illegible]

## VehPwrMd\_Per1

[illegible]



*VehPwrMd\_Per1*



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓
				✓

[illegible]

## VehPwrMd\_Per1

[illegible]

*VehPwrMd\_Per1*



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓

Specification	Performance Metrics:
	(With "None" Instrumentation and "WithPS" Environment)
	CPU Cycles:
TS3.1	1700.00 Cycles
TS3.2	1714.00 Cycles
TS3.3	1700.00 Cycles
TS3.4	1710.00 Cycles
TS3.5	1734.00 Cycles
TS3.6	2210.00 Cycles
TS3.7	1716.00 Cycles
TS3.8	1775.00 Cycles
TS3.9	1692.00 Cycles
TS3.10	1719.00 Cycles
TS3.11	1712.00 Cycles
TS3.12	1767.00 Cycles
TS3.13	1752.00 Cycles
TS3.14	1752.00 Cycles
TS3.15	1759.00 Cycles
TS3.16	1696.00 Cycles
TS3.17	1719.00 Cycles
TS3.18	1743.00 Cycles
TS3.19	1719.00 Cycles

### Description

[illegible]





## VehPwrMd\_Per1

[illegible]

Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓
				✓

Name	Input Value

## VehPwrMd\_Per1

[illegible]

Test Step 3.4 (Repeat Count = 1)	
Name	Input Value

## VehPwrMd\_Per1

[illegible]

Test Step 3.5 (Repeat Count = 1)	
Name	Input Value

## VehPwrMd\_Per1

[illegible]

Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓

## VehPwrMd\_Per1

[illegible]

## VehPwrMd\_Per1

[illegible]

## VehPwrMd\_Per1



## Test Step Call Trace

### Test Step 3.8 (Repeat Count = 1)

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓

## VehPwrMd\_Per1

[illegible]



TEST DETAILS REPORT

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VehPwrMd\_Per1

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓
			✓
			✓
			✓

Test Step Call Trace

					✓
Actual Function	Count	Expected Function	Count	Result	
					✓
					✓
					✓



## VehPwrMd\_Per1

[illegible]



## VehPwrMd\_Per1



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓
				✓

[illegible]

*VehPwrMd\_Per1*

[illegible]

*VehPwrMd\_Per1*



### Test Step Call Trace

### Test Step 3.15 (Repeat Count = 1)

*VehPwrMd\_Per1*



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓

[illegible]



## VehPwrMd\_Per1



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓

[illegible]

## VehPwrMd\_Per1

[illegible]

## VehPwrMd\_Per1

[illegible]

TEST DETAILS REPORT

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VehPwrMd\_Per1

Name	Input Value

TEST DETAILS REPORT

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VehPwrMd\_Per1



Test Case 4: PRM Range Test

Specification	Performance Metrics:  (With "None" Instrumentation and "WithPS" Environment)  CPU Cycles:  TS4.1 1733.00 Cycles TS4.2 1733.00 Cycles TS4.3 1722.00 Cycles TS4.4 1722.00 Cycles TS4.5 2336.00 Cycles TS4.6 2239.00 Cycles TS4.7 2313.00 Cycles TS4.8 2208.00 Cycles TS4.9 2228.00 Cycles TS4.10 2235.00 Cycles TS4.11 1808.00 Cycles TS4.12 1779.00 Cycles TS4.13 1751.00 Cycles TS4.14 1751.00 Cycles TS4.15 1749.00 Cycles TS4.16 1692.00 Cycles TS4.17 1803.00 Cycles TS4.18 1773.00 Cycles TS4.19 1693.00 Cycles TS4.20 1735.00 Cycles TS4.21 1728.00 Cycles TS4.22 1760.00 Cycles TS4.23 1751.00 Cycles TS4.24 1789.00 Cycles TS4.25 1745.00 Cycles TS4.26 1775.00 Cycles TS4.27 1780.00 Cycles TS4.28 1775.00 Cycles TS4.29 1832.00 Cycles TS4.30 1720.00 Cycles TS4.31 1782.00 Cycles TS4.32 1749.00 Cycles TS4.33 1735.00 Cycles TS4.34 1745.00 Cycles TS4.35 1719.00 Cycles TS4.36 1719.00 Cycles TS4.37 1775.00 Cycles TS4.38 1760.00 Cycles TS4.39 1751.00 Cycles TS4.40 1828.00 Cycles TS4.41 1753.00 Cycles TS4.42 1740.00 Cycles
Description	

Test Step 4.1 (Repeat Count = 1)

Name	Input Value

## VehPwrMd\_Per1

[illegible]

Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓
				✓

## VehPwrMd\_Per1

[illegible]

*VehPwrMd\_Per1*

[illegible]



## VehPwrMd\_Per1



## Test Step Call Trace

### Test Step 4.4 (Repeat Count = 1)

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓

TEST DETAILS REPORT

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VehPwrMd\_Per1

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓
			✓
			✓

Test Step Call Trace					✓
Actual Function	Count	Expected Function	Count	Result	
					✓
					✓
					✓
					✓

## VehPwrMd\_Per1

[illegible]

## VehPwrMd\_Per1

[illegible]

## VehPwrMd\_Per1



## Test Step Call Trace

### Test Step 4.7 (Repeat Count = 1)

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓

TEST DETAILS REPORT

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VehPwrMd\_Per1

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓
			✓
			✓

Test Step Call Trace

					✓
Actual Function	Count	Expected Function	Count	Result	
					✓
					✓
					✓
					✓

## VehPwrMd\_Per1

[illegible]

*VehPwrMd\_Per1*





## VehPwrMd\_Per1



## Test Step Call Trace

### Test Step 4.10 (Repeat Count = 1)

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓

TEST DETAILS REPORT

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VehPwrMd\_Per1

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓
			✓
			✓

Test Step Call Trace					✓
Actual Function	Count	Expected Function	Count	Result	
					✓
					✓
					✓
					✓

*VehPwrMd\_Per1*

[illegible]

## VehPwrMd\_Per1



1

## VehPwrMd\_Per1



## Test Step Call Trace

### Test Step 4.13 (Repeat Count = 1)

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓

TEST DETAILS REPORT

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VehPwrMd\_Per1

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓
			✓
			✓

Test Step Call Trace					✓
Actual Function	Count	Expected Function	Count	Result	
					✓
					✓
					✓
					✓

## VehPwrMd\_Per1

[illegible]

## VehPwrMd\_Per1





## VehPwrMd\_Per1



Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓

Name	Input Value
------	-------------

[illegible]

## VehPwrMd\_Per1



Name	Actual Value	Expected Value	Result
			✓
			✓

TEST DETAILS REPORT

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VehPwrMd\_Per1

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓
			✓
			✓
			✓

Test Step Call Trace

					✓
Actual Function	Count	Expected Function	Count	Result	
					✓
					✓
					✓

TEST DETAILS REPORT

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VehPwrMd\_Per1



Test Step 4.18 (Repeat Count = 1)		✓
Name	Input Value	

## VehPwrMd\_Per1

[illegible]

## VehPwrMd\_Per1



10



## VehPwrMd\_Per1



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓
			✓

## VehPwrMd\_Per1



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓



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VehPwrMd\_Per1

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓
			✓
			✓
			✓

Test Step Call Trace

					✓
Actual Function	Count	Expected Function	Count	Result	
					✓
					✓
					✓

## VehPwrMd\_Per1



**Input Value**

## VehPwrMd\_Per1

[illegible]



## VehPwrMd\_Per1



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓
			✓

## VehPwrMd\_Per1



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓

TEST DETAILS REPORT

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VehPwrMd\_Per1

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓
			✓
			✓
			✓

Test Step Call Trace

					✓
Actual Function	Count	Expected Function	Count	Result	
					✓
					✓
					✓

## VehPwrMd\_Per1



**Input Value**



## VehPwrMd\_Per1

[illegible]

## VehPwrMd\_Per1



100



## VehPwrMd\_Per1



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓
			✓



TEST DETAILS REPORT

2018-03-12, 13:20:40+0530



VehPwrMd\_Per1

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓
			✓
			✓
			✓

Test Step Call Trace

					✓
Actual Function	Count	Expected Function	Count	Result	
					✓
					✓
					✓



## VehPwrMd\_Per1

[illegible]

## VehPwrMd\_Per1



1





## VehPwrMd\_Per1



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓
			✓

## VehPwrMd\_Per1



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓

TEST DETAILS REPORT

2018-03-12, 13:20:40+0530



VehPwrMd\_Per1

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓
			✓
			✓
			✓

Test Step Call Trace					✓
Actual Function	Count	Expected Function	Count	Result	
					✓
					✓
					✓



## VehPwrMd\_Per1

[illegible]

## VehPwrMd\_Per1



1



## VehPwrMd\_Per1



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
				✓
				✓
				✓

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓
			✓

TEST DETAILS REPORT

2018-03-12, 13:20:40+0530



VehPwrMd\_Per1

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓

Test Step Call Trace



Actual Function	Count	Expected Function	Count	Result
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TEST DETAILS REPORT

2018-03-12, 13:20:40+0530



VehPwrMd\_Per1

Name	Actual Value	Expected Value	Result
			✓
			✓
			✓
			✓
			✓
			✓
			✓

Test Step Call Trace

					✓
Actual Function	Count	Expected Function	Count	Result	
					✓
					✓
					✓

# TEST DETAILS REPORT



Project	VehPwrMd
Module	VehPwrMd
Test Object	VehPwrMd_Init1

## Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

## Statistics

Total Testcases	2
Successful	2 ✓
Failed	0
Not Executed	0

## Module Properties

Project Root Directory	D:\Synergy_Work_Area\VehPwrMd
Configuration File	D:\Synergy_Work_Area\VehPwrMd\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\VehPwrMd\src\Ap_VehPwrMd.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I\$(PROJECTROOT)\VehPwrMd\utp\contract -I\$(PROJECTROOT)\VehPwrMd\utp\contract\Ap_VehPwrMd -I\$(PROJECTROOT)\NtrLib\include -I\$(PROJECTROOT)\StdDef\include -I\$(Compiler Install Path)\include

## Comments/Description/Specification

Name	Text
Module 'VehPwrMd'	***** Unit Test Information *****  Name of Tester: Sachin Kamate Code File(s) Under Test: Ap_VehPwrMd.c Code File(s) Version: 2 Module Design Document: VehPwrMd_MDD.doc Module Design Document Version: 6 Data Dictionary Version: 6 Unit Test Plan Version: 3 Optimization Level: Ogeneral Compiler (CodeGen) Version: TMS470_4.9.5 Model Type: None Model Version: Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes): 978 Total RAM Used (Bytes): 19 Total CALS Used (Bytes): 36 Special Test Requirements: NA Test Date: 3/12/2018 Comments: Note1: Inline functions defined in "Globalmacro.h" are not unit tested. Note2: "CBD_Sandbox_dbg.map" file is embedded for reference. Note3: In Function "VehPwrMd_Per1", 100% MC/DC coverage is not possible at Src Line No. 955. Anomaly needs to be logged for the same. Note4: In Function "VehPwrMd_Per1", the PIM variable "RampStatus_Cnt_M_u08" is going Out of range [0, 3] over the DD range [0, 2]. Anomaly needs to be logged for the same.  *****

## Attributes

Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570.tpl
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4
Time Unit	cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1

Attributes	
Name	Value
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\VehPwrMd\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

## Test Case 1: Range Test

## Specification

Performance Metrics:

(With "None" Instrumentation and  
"WithPS" Environment)

CPU Cycles:

TS1.1 566.00 Cycles  
TS1.2 529.00 Cycles  
TS1.3 529.00 Cycles  
TS1.4 529.00 Cycles  
TS1.5 529.00 Cycles

## Description

Vector Description:

TS1.1All Min  
TS1.2All Max  
TS1.3Rte\_Call\_SystemTime\_GetSystemTime\_mS\_u32==>Min  
TS1.4Rte\_Call\_SystemTime\_GetSystemTime\_mS\_u32==>Max  
TS1.5Rte\_Call\_SystemTime\_GetSystemTime\_mS\_u32==>Pos

## Test Step 1.1 (Repeat Count = 1)

Name	Input Value		
Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32_CurrentTime		
Rte_Inst_Ap_VehPwrMd	target_Rte_Inst_Ap_VehPwrMd		
k_RampDnRt_UlspmS_f32	9.99999975e-005		
target_Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32_CurrentTime	0		
target_Rte_Inst_Ap_VehPwrMd.VehPwrMd_Init1_OperRampRate_XpmS_f32	target_VehPwrMd_Init1_OperRampRate_XpmS_f32		
target_Rte_Inst_Ap_VehPwrMd.VehPwrMd_Init1_OperRampValue_Uls_f32	target_VehPwrMd_Init1_OperRampValue_Uls_f32		
Name	Actual Value	Expected Value	Result
ATermTimer_mS_M_u32	0	0	✓
CTermIgnOffTimer_mS_M_u32	0	0	✓
CTermIgnOnTimer_mS_M_u32	0	0	✓
CTermVehSpdInvalidTimer_mS_M_u32	0	0	✓
target_VehPwrMd_Init1_OperRampRate_XpmS_f32.value	9.99999975e-005	9.99999975e-005 ± 0.015625	✓
target_VehPwrMd_Init1_OperRampValue_Uls_f32.value	0	0 ± 0.00006103515625	✓

## Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32	1	✓

## Test Step 1.2 (Repeat Count = 1)

Name	Input Value		
Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32_CurrentTime		
Rte_Inst_Ap_VehPwrMd	target_Rte_Inst_Ap_VehPwrMd		
k_RampDnRt_UlspmS_f32	0.00499999989		
target_Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32_CurrentTime	4294967295		
target_Rte_Inst_Ap_VehPwrMd.VehPwrMd_Init1_OperRampRate_XpmS_f32	target_VehPwrMd_Init1_OperRampRate_XpmS_f32		
target_Rte_Inst_Ap_VehPwrMd.VehPwrMd_Init1_OperRampValue_Uls_f32	target_VehPwrMd_Init1_OperRampValue_Uls_f32		
Name	Actual Value	Expected Value	Result
ATermTimer_mS_M_u32	4294967295	4294967295	✓
CTermIgnOffTimer_mS_M_u32	4294967295	4294967295	✓
CTermIgnOnTimer_mS_M_u32	4294967295	4294967295	✓
CTermVehSpdInvalidTimer_mS_M_u32	4294967295	4294967295	✓
target_VehPwrMd_Init1_OperRampRate_XpmS_f32.value	0.00499999989	0.00499999989 ± 0.015625	✓
target_VehPwrMd_Init1_OperRampValue_Uls_f32.value	0	0 ± 0.00006103515625	✓

## Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32	1	✓

# TEST DETAILS REPORT



## Test Step 1.3 (Repeat Count = 1) ✓

Name	Input Value		
Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32_CurrentTime		
Rte_Inst_Ap_VehPwrMd	target_Rte_Inst_Ap_VehPwrMd		
k_RampDnRt_UlspmS_f32	0.001667		
target_Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32_CurrentTime	0		
target_Rte_Inst_Ap_VehPwrMd.VehPwrMd_Init1_OperRampRate_XpmS_f32	target_VehPwrMd_Init1_OperRampRate_XpmS_f32		
target_Rte_Inst_Ap_VehPwrMd.VehPwrMd_Init1_OperRampValue_Uls_f32	target_VehPwrMd_Init1_OperRampValue_Uls_f32		
Name	Actual Value	Expected Value	Result
ATermTimer_mS_M_u32	0	0	✔
CTermIgnOffTimer_mS_M_u32	0	0	✔
CTermIgnOnTimer_mS_M_u32	0	0	✔
CTermVehSpdInvalidTimer_mS_M_u32	0	0	✔
target_VehPwrMd_Init1_OperRampRate_XpmS_f32.value	0.001667	0.001667 ± 0.015625	✔
target_VehPwrMd_Init1_OperRampValue_Uls_f32.value	0	0 ± 0.00006103515625	✔

## Test Step Call Trace ✓

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32	1	✓

## Test Step 1.4 (Repeat Count = 1) ✓

Name	Input Value		
Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32_CurrentTime		
Rte_Inst_Ap_VehPwrMd	target_Rte_Inst_Ap_VehPwrMd		
k_RampDnRt_UlspmS_f32	0.001667		
target_Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32_CurrentTime	4294967295		
target_Rte_Inst_Ap_VehPwrMd.VehPwrMd_Init1_OperRampRate_XpmS_f32	target_VehPwrMd_Init1_OperRampRate_XpmS_f32		
target_Rte_Inst_Ap_VehPwrMd.VehPwrMd_Init1_OperRampValue_Uls_f32	target_VehPwrMd_Init1_OperRampValue_Uls_f32		
Name	Actual Value	Expected Value	Result
ATermTimer_mS_M_u32	4294967295	4294967295	✓
CTermIgnOffTimer_mS_M_u32	4294967295	4294967295	✓
CTermIgnOnTimer_mS_M_u32	4294967295	4294967295	✓
CTermVehSpdInvalidTimer_mS_M_u32	4294967295	4294967295	✓
target_VehPwrMd_Init1_OperRampRate_XpmS_f32.value	0.001667	0.001667 ± 0.015625	✓
target_VehPwrMd_Init1_OperRampValue_Uls_f32.value	0	0 ± 0.00006103515625	✓

## Test Step Call Trace ✓

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32	1	✓

## Test Step 1.5 (Repeat Count = 1) ✓

Name		Input Value		
Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32(CurrentTime)		target_Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32_CurrentTime		
Rte_Inst_Ap_VehPwrMd		target_Rte_Inst_Ap_VehPwrMd		
k_RampDnRt_UlspmS_f32		0.001667		
target_Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32_CurrentTime		1604325632		
target_Rte_Inst_Ap_VehPwrMd.VehPwrMd_Init1_OperRampRate_XpmS_f32		target_VehPwrMd_Init1_OperRampRate_XpmS_f32		
target_Rte_Inst_Ap_VehPwrMd.VehPwrMd_Init1_OperRampValue_Uls_f32		target_VehPwrMd_Init1_OperRampValue_Uls_f32		
Name	Actual Value	Expected Value	Result	
ATermTimer_mS_M_u32	1604325632	1604325632	✔	
CTermIgnOffTimer_mS_M_u32	1604325632	1604325632	✔	
CTermIgnOnTimer_mS_M_u32	1604325632	1604325632	✔	
CTermVehSpdInvalidTimer_mS_M_u32	1604325632	1604325632	✔	
target_VehPwrMd_Init1_OperRampRate_XpmS_f32.value	0.001667	0.001667 ± 0.015625	✔	
target_VehPwrMd_Init1_OperRampValue_Uls_f32.value	0	0 ± 0.00006103515625	✔	

## Test Step Call Trace ✓

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32	1	✓

# TEST DETAILS REPORT



## Test Case 2: PRM Range Test

Specification	Performance Metrics:
	(With "None" Instrumentation and "WithPS" Environment)
Description	CPU Cycles:
	TS2.1 529.00 Cycles TS2.2 529.00 Cycles TS2.3 529.00 Cycles TS2.4 529.00 Cycles
Description	Vector Description:
	TS2.1k_RampDnRt_UlspmS_f32==>Min TS2.2k_RampDnRt_UlspmS_f32==>Max TS2.3k_RampDnRt_UlspmS_f32==>Pos TS2.4k_RampDnRt_UlspmS_f32==>Default

### Test Step 2.1 (Repeat Count = 1)

Name	Input Value		
Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32_CurrentTime		
Rte_Inst_Ap_VehPwrMd	target_Rte_Inst_Ap_VehPwrMd		
k_RampDnRt_UlspmS_f32	9.99999975e-005		
target_Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32_CurrentTime	60205312		
target_Rte_Inst_Ap_VehPwrMd.VehPwrMd_Init1_OperRampRate_XpmS_f32	target_VehPwrMd_Init1_OperRampRate_XpmS_f32		
target_Rte_Inst_Ap_VehPwrMd.VehPwrMd_Init1_OperRampValue_Uls_f32	target_VehPwrMd_Init1_OperRampValue_Uls_f32		
Name	Actual Value	Expected Value	Result
ATermTimer_mS_M_u32	60205312	60205312	✓
CTermIgnOffTimer_mS_M_u32	60205312	60205312	✓
CTermIgnOnTimer_mS_M_u32	60205312	60205312	✓
CTermVehSpdInvalidTimer_mS_M_u32	60205312	60205312	✓
target_VehPwrMd_Init1_OperRampRate_XpmS_f32.value	9.99999975e-005	9.99999975e-005 ± 0.015625	✓
target_VehPwrMd_Init1_OperRampValue_Uls_f32.value	0	0 ± 0.00006103515625	✓

### Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32	1	✓

### Test Step 2.2 (Repeat Count = 1)

Name	Input Value		
Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32_CurrentTime		
Rte_Inst_Ap_VehPwrMd	target_Rte_Inst_Ap_VehPwrMd		
k_RampDnRt_UlspmS_f32	0.00499999989		
target_Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32_CurrentTime	3267282944		
target_Rte_Inst_Ap_VehPwrMd.VehPwrMd_Init1_OperRampRate_XpmS_f32	target_VehPwrMd_Init1_OperRampRate_XpmS_f32		
target_Rte_Inst_Ap_VehPwrMd.VehPwrMd_Init1_OperRampValue_Uls_f32	target_VehPwrMd_Init1_OperRampValue_Uls_f32		
Name	Actual Value	Expected Value	Result
ATermTimer_mS_M_u32	3267282944	3267282944	✓
CTermIgnOffTimer_mS_M_u32	3267282944	3267282944	✓
CTermIgnOnTimer_mS_M_u32	3267282944	3267282944	✓
CTermVehSpdInvalidTimer_mS_M_u32	3267282944	3267282944	✓
target_VehPwrMd_Init1_OperRampRate_XpmS_f32.value	0.00499999989	0.00499999989 ± 0.015625	✓
target_VehPwrMd_Init1_OperRampValue_Uls_f32.value	0	0 ± 0.00006103515625	✓

### Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32	1	✓

### Test Step 2.3 (Repeat Count = 1)

Name		Input Value	
Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32(CurrentTime)		target_Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32_CurrentTime	
Rte_Inst_Ap_VehPwrMd		target_Rte_Inst_Ap_VehPwrMd	
k_RampDnRt_UlspmS_f32		0.00350000011	
target_Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32_CurrentTime		3498208000	
target_Rte_Inst_Ap_VehPwrMd.VehPwrMd_Init1_OperRampRate_XpmS_f32		target_VehPwrMd_Init1_OperRampRate_XpmS_f32	
target_Rte_Inst_Ap_VehPwrMd.VehPwrMd_Init1_OperRampValue_Uls_f32		target_VehPwrMd_Init1_OperRampValue_Uls_f32	
Name	Actual Value	Expected Value	Result
ATermTimer_mS_M_u32	3498208000	3498208000	✓
CTermIgnOffTimer_mS_M_u32	3498208000	3498208000	✓

# TEST DETAILS REPORT



Name	Actual Value	Expected Value	Result
CTermIgnOnTimer_mS_M_u32	3498208000	3498208000	✓
CTermVehSpdInvalidTimer_mS_M_u32	3498208000	3498208000	✓
target_VehPwrMd_Init1_OperRampRate_XpmS_f32.value	0.00350000011	0.00350000011 ± 0.015625	✓
target_VehPwrMd_Init1_OperRampValue_Uls_f32.value	0	0 ± 0.00006103515625	✓

## Test Step Call Trace ✓

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32	1	✓

## Test Step 2.4 (Repeat Count = 1) ✓

Name	Input Value		
Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32_CurrentTime		
Rte_Inst_Ap_VehPwrMd	target_Rte_Inst_Ap_VehPwrMd		
k_RampDnRt_UlspmS_f32	0.001667		
target_Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32_CurrentTime	379133056		
target_Rte_Inst_Ap_VehPwrMd.VehPwrMd_Init1_OperRampRate_XpmS_f32	target_VehPwrMd_Init1_OperRampRate_XpmS_f32		
target_Rte_Inst_Ap_VehPwrMd.VehPwrMd_Init1_OperRampValue_Uls_f32	target_VehPwrMd_Init1_OperRampValue_Uls_f32		
Name	Actual Value	Expected Value	Result
ATermTimer_mS_M_u32	379133056	379133056	✓
CTermIgnOffTimer_mS_M_u32	379133056	379133056	✓
CTermIgnOnTimer_mS_M_u32	379133056	379133056	✓
CTermVehSpdInvalidTimer_mS_M_u32	379133056	379133056	✓
target_VehPwrMd_Init1_OperRampRate_XpmS_f32.value	0.001667	0.001667 ± 0.015625	✓
target_VehPwrMd_Init1_OperRampValue_Uls_f32.value	0	0 ± 0.00006103515625	✓

## Test Step Call Trace ✓

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_VehPwrMd_SystemTime_GetSystemTime_mS_u32	1	✓