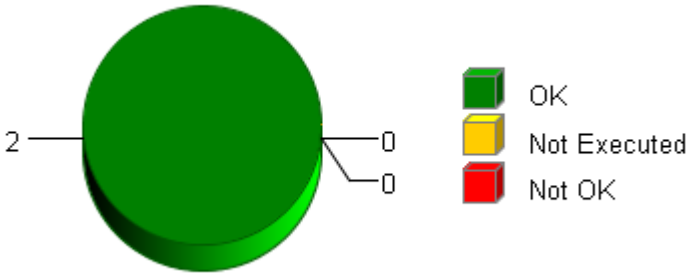
Summary

Total Test Objects:	2
Successful:	2
Failed:	0
Not Executed:	0
Date:	2015-12-21
Time:	17:40:38+0530

Overall Test Object Results (including Coverage)



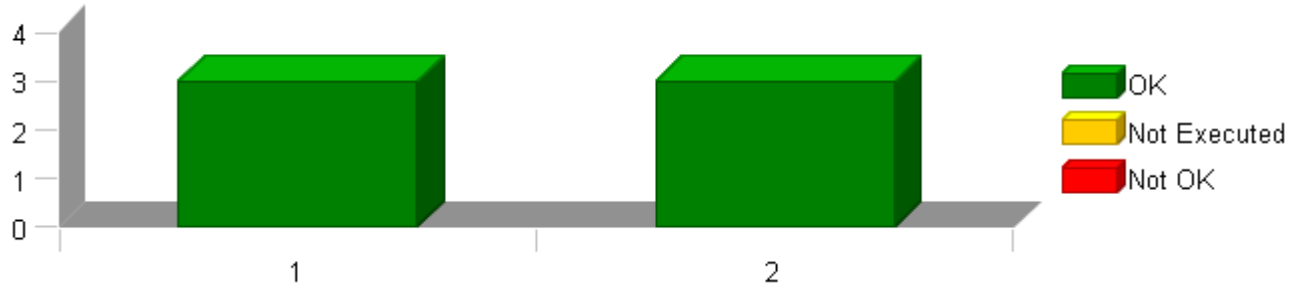
Selected Project Items

Test Object "CBD_UnitTest/DiagMgr_FailAction/DiagMgr_Per1"
Test Object "CBD_UnitTest/DiagMgr_FailAction/ReadBit_u16"

Used Test Environments

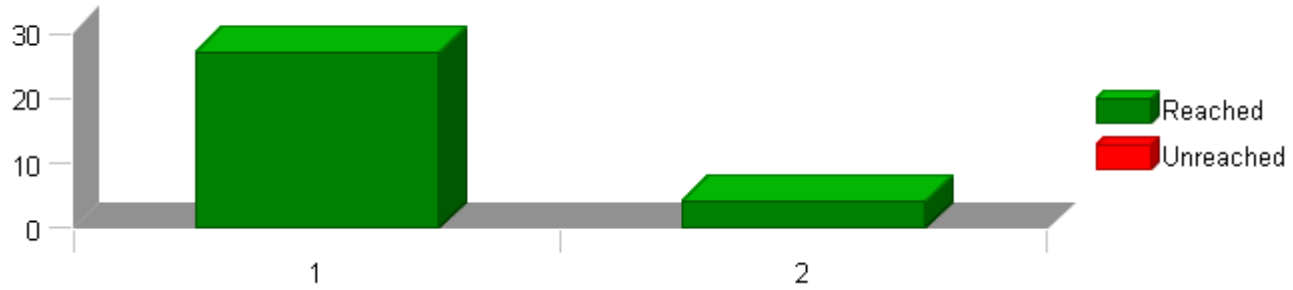
TI TMS 570 PLS UDE (Default)

Test Case Results for Each Test Object (without Coverage)



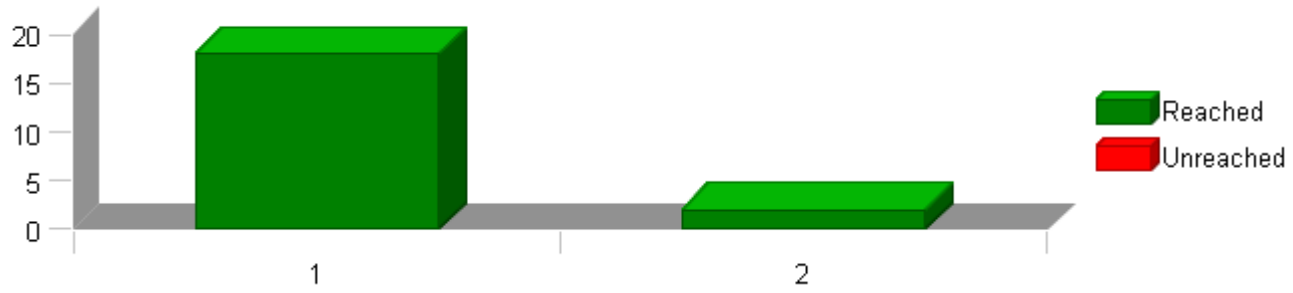
The table above shows each test object on the x axis and the number of test cases of the respective test object on the y axis. Each bar is divided into passed, not executed and failed test cases. The test case results do not take into account any coverage result (i.e. if all test cases of a test object are passed in this table but the coverage is failed, the overall test object result will be failed).

Statement (C0) Coverage: Total Statements for Each Test Object



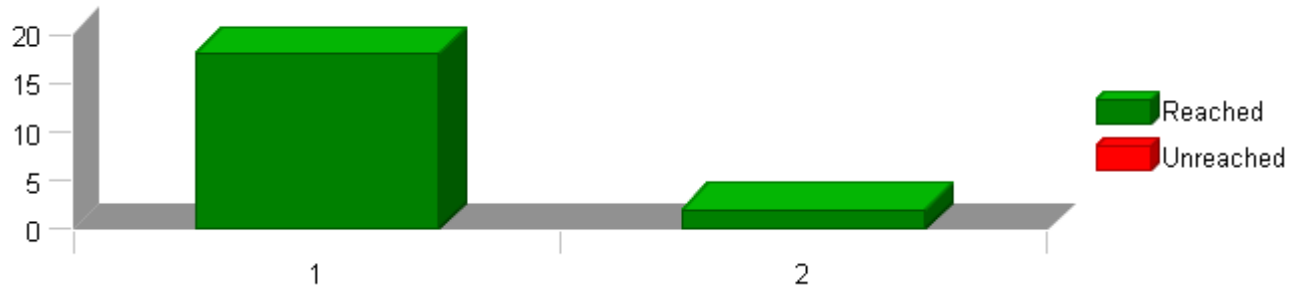
The table above shows each test object on the x axis and the number of statements of the respective test object on the y axis. Each bar is divided into reached statements (i.e. statements that have been executed during the test) and unreached statements.

Branch (C1) Coverage: Total Branches for Each Test Object



The table above shows each test object on the x axis and the number of branches of the respective test object on the y axis. Each bar is divided into reached branches (i.e. branches that have been executed during the test) and unreached branches.

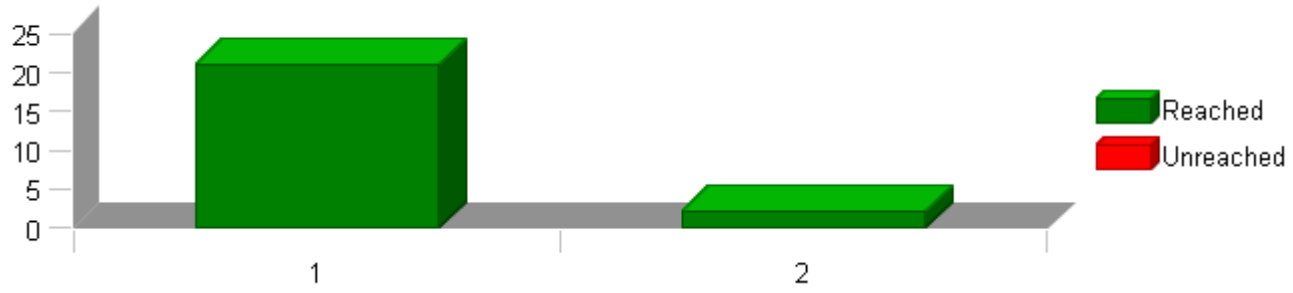
Decision Coverage: Total Decision Outcomes for Each Test Object



The table above shows test objects on the x axis and the number of possible outcomes of all decisions of the respective test object on the y axis. To achieve full DC coverage, each decision must evaluate to both true and false.

Each bar is divided into reached and unreached decision outcomes.

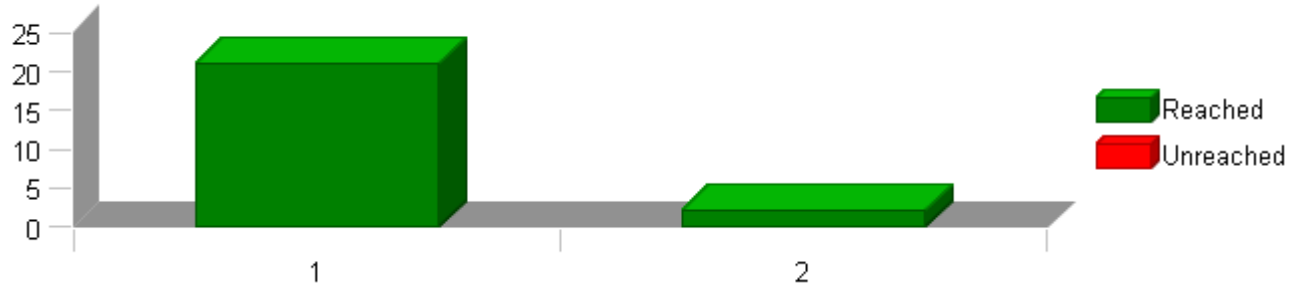
MC/DC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MC/DC coverage, each decision requires all contained atomic conditions to evaluate to both true and false independently of all other conditions. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

MCC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MCC coverage, each decision requires all contained atomic conditions to evaluate to all possible combinations of true and false values. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

Test Object List

The following table lists all test objects with their test case and coverage results. The cumulated results for modules, folders and test collections are also displayed, the indentation within the name column indicates the parent relationship of the elements.

Please note that only test objects are numbered within the first column. This number is referenced on the x axis within the overview charts for test case and coverage results available on previous pages (if included into the report).

No.	Name	C0	C1	DC	MC/DC	MCC	Test Cases	Result
	DiagMgr_failaction	100 %	100 %	100 %	100 %	100 %	6 of 6 passed	✔
	CBD_UnitTest	100 %	100 %	100 %	100 %	100 %	6 of 6 passed	✔
	DiagMgr_FailAction	100 %	100 %	100 %	100 %	100 %	6 of 6 passed	✔
1	DiagMgr_Per1	100 %	100 %	100 %	100 %	100 %	3 of 3 passed	✔
2	ReadBit_u16	100 %	100 %	100 %	100 %	100 %	3 of 3 passed	✔

TEST DETAILS REPORT

DiagMgr_Per1

2015-12-21, 17:36:44+0530

Project	DiagMgr_failaction
Module	DiagMgr_FailAction
Test Object	DiagMgr_Per1

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MCC Coverage	100 %
MC/DC Coverage	100 %

Statistics

Total Testcases	3
Successful	3
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\DiagMgr_Failaction
Configuration File	D:\Synergy_Work_Area\DiagMgr_Failaction\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\DiagMgr\src\Ap_DiagMgr_FailAction.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -Dstatic= -DSKIP_MAGIC_NUMBER= -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef \include -I$(PROJECTROOT)\DiagMgr\utp\contract -I$(PROJECTROOT)\DiagMgr\utp\contract\Test_CFG -I$(PROJECTROOT)\DiagMgr \include -I$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5\include

Comments/Description/Specification

Name	Text
Module 'DiagMgr_FailAction'	**********Unit Test Description********** Name of Tester:Namrata Morbale Code File(s) Under Test:Ap_DiagMgr_FailAction.c Code File(s) Version:3 Module Design Document:Diagnostics_Manager_FailAction_MDD.docx Module Design Document Version:3 Data Dictionary Version:11 Unit Test Plan Version:2 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS570_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.32 Total FLASH Used (Bytes):290 Total RAM Used (Bytes):0 Total CALS Used (Bytes):2760 Special Test Requirements: Test Date:12/21/2015 Comments:"Note 1: Inline Function defined in GlobalMacro.h is not unit tested. NOTE 2:""CBD_Sandbox_dbg.map"" map file is embedded for reference. NOTE 3: Constant D_NOOFACTIVEINVERTER_CNT_U08 is configurable variable and which is configured as per program so instead of declaring this variable as constant it is declared as variable for testing purpose and added same in Input. **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570.tpl
Target Install Path	$(ProgramFiles)\pls\UDE 3.2
Timer Enabled	false

Attributes

Name	Value
Timer Prescale	0
Timer Resolution	1
Timer Unit	Cycles
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\DiagMgr_Failaction\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Metrics Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:

TS1.1 7533.00 Cycles
TS1.2 7675.00 Cycles
```

Description

Vector Description:

TS 1.1Shortest Execution Path:(i<2u)=TRUE/FALSE && ((T_DiagMgrRmpRate_Ptr_f32[i])[0]>=(T_DiagMgrRmpRate_Ptr_f32[i])[1])=TRUE && ((DiagMgrRmpRate_UlspmS_T_f32>=AppRmpRate_UlspmS_T_f32)=FALSE && (TRUE == DiagStsNonRecRmpToZeroFltPres_Cnt_T_lgc)=FALSE && (TRUE == DiagStsRecRmpToZeroFltPres_Cnt_T_lgc)=FALSE && (D_NOOFACTIVEINVERTER_CNT_U08 == 2U)=TRUE && (DiagStsInverter1Inactive_Cnt_T_lgc==FALSE)=TRUE && (DiagStsInverter2Inactive_Cnt_T_lgc==FALSE)=TRUE
TS 1.2Longest Execution Path:(DiagStsInverter1Inactive_Cnt_T_lgc==FALSE)=FALSE && (DiagStsInverter2Inactive_Cnt_T_lgc==FALSE)=TRUE && (DiagStsInverter1Inactive_Cnt_T_lgc==TRUE)=FALSE && (DiagStsInverter1Inactive_Cnt_T_lgc==FALSE)=TRUE

Test Step 1.1 (Repeat Count = 1)

Name	Input Value
D_NOOFACTIVEINVERTER_CNT_U08	2
T_DiagMgrDiagSts_Ptr_b16[0]	tgt_0
T_DiagMgrDiagSts_Ptr_b16[1]	tgt_1
T_DiagMgrRmpRate_Ptr_f32[0]	tgt_rmp0
T_DiagMgrRmpRate_Ptr_f32[1]	tgt_rmp1
tgt_0[0]	0
tgt_0[1]	0
tgt_1[0]	0
tgt_1[1]	0
tgt_rmp0[0]	0.100000001
tgt_rmp0[1]	0.100000001
tgt_rmp1[0]	0.449999988
tgt_rmp1[1]	0.449999988

Name	Actual Value	Expected Value	Result
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32(data)	0.449999988	0.449999988	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc(data)	0	0	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08(data)	2	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc(data)	0	0	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc(data)	0	0	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	✔
Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	✔

Test Step 1.2 (Repeat Count = 1)			✔
Name	**Input Value**		
D_NOOFACTIVEINVERTER_CNT_U08	2		
T_DiagMgrDiagSts_Ptr_b16[0]	tgt_0		
T_DiagMgrDiagSts_Ptr_b16[1]	tgt_1		
T_DiagMgrRmpRate_Ptr_f32[0]	tgt_rmp0		
T_DiagMgrRmpRate_Ptr_f32[1]	tgt_rmp1		
tgt_0[0]	65535		
tgt_0[1]	65535		
tgt_1[0]	65535		
tgt_1[1]	65535		
tgt_rmp0[0]	0.5		
tgt_rmp0[1]	0.5		
tgt_rmp1[0]	0.5		
tgt_rmp1[1]	0.5		
Name	**Actual Value**	**Expected Value**	**Result**
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32(data)	0.5	0.5	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc(data)	1	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08(data)	0	0	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc(data)	1	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc(data)	1	1	✔

T				
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	✔
Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	✔

Test Case 2: Boundary Test ✔

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:

TS2.1 7675.00 Cycles
TS2.2 7612.00 Cycles
TS2.3 7582.00 Cycles
TS2.4 7601.00 Cycles
TS2.5 7567.00 Cycles
TS2.6 7550.00 Cycles
TS2.7 7578.00 Cycles
TS2.8 7556.00 Cycles
TS2.9 7617.00 Cycles
TS2.10 7578.00 Cycles
TS2.11 7578.00 Cycles
TS2.12 7625.00 Cycles
TS2.13 7647.00 Cycles
TS2.14 7556.00 Cycles
```

Description

Vector Description:

TS 2.1DiagSts10_Cnt_M_b16 =min
TS 2.2DiagSts10_Cnt_M_b16 =max
TS 2.3DiagSts10_Cnt_M_b16 =pos
TS 2.4DiagSts9_Cnt_M_b16 =min
TS 2.5DiagSts9_Cnt_M_b16 = max
TS 2.6DiagSts9_Cnt_M_b16 = pos
TS 2.7ActiveRmpRate10_UlspmS_M_f32 =min
TS 2.8ActiveRmpRate10_UlspmS_M_f32= max
TS 2.9ActiveRmpRate10_UlspmS_M_f32 = pos
TS 2.10ActiveRmpRate9_UlspmS_M_f32 =min
TS 2.11ActiveRmpRate9_UlspmS_M_f32 =max
TS 2.12ActiveRmpRate9_UlspmS_M_f32 = pos
TS 2.13All Min
TS 2.14All Max

Test Step 2.1 (Repeat Count = 1) ✔

Name	Input Value
D_NOOFACTIVEINVERTER_CNT_U08	2
T_DiagMgrDiagSts_Ptr_b16[0]	tgt_0
T_DiagMgrDiagSts_Ptr_b16[1]	tgt_1
T_DiagMgrRmpRate_Ptr_f32[0]	tgt_rmp0
T_DiagMgrRmpRate_Ptr_f32[1]	tgt_rmp1
tgt_0[0]	0
tgt_0[1]	0
tgt_1[0]	25
tgt_1[1]	50
tgt_rmp0[0]	0.100000001
tgt_rmp0[1]	0.100000001
tgt_rmp1[0]	0.449999988

Name	Input Value
tgt_rmp1[1]	0.449999988

Name	Actual Value	Expected Value	Result
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32(data)	0.449999988	0.449999988	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc(data)	0	0	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08(data)	2	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc(data)	0	0	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc(data)	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	✔
Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	✔

Test Step 2.2 (Repeat Count = 1) ✔

Name	Input Value
D_NOOFACTIVEINVERTER_CNT_U08	2
T_DiagMgrDiagSts_Ptr_b16[0]	tgt_0
T_DiagMgrDiagSts_Ptr_b16[1]	tgt_1
T_DiagMgrRmpRate_Ptr_f32[0]	tgt_rmp0
T_DiagMgrRmpRate_Ptr_f32[1]	tgt_rmp1
tgt_0[0]	65535
tgt_0[1]	65535
tgt_1[0]	89
tgt_1[1]	500
tgt_rmp0[0]	0.200000003
tgt_rmp0[1]	0.200000003
tgt_rmp1[0]	0.0199999996
tgt_rmp1[1]	0.0199999996

Name	Actual Value	Expected Value	Result
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32(data)	0.200000003	0.200000003	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc(data)	1	1	✔

Name	Actual Value	Expected Value	Result
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc(data)	1	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08(data)	0	0	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc(data)	1	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc(data)	1	1	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	✔
Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	✔

Test Step 2.3 (Repeat Count = 1) ✔

Name	Input Value
D_NOOFACTIVEINVERTER_CNT_U08	2
T_DiagMgrDiagSts_Ptr_b16[0]	tgt_0
T_DiagMgrDiagSts_Ptr_b16[1]	tgt_1
T_DiagMgrRmpRate_Ptr_f32[0]	tgt_rmp0
T_DiagMgrRmpRate_Ptr_f32[1]	tgt_rmp1
tgt_0[0]	2000
tgt_0[1]	5000
tgt_1[0]	62
tgt_1[1]	756
tgt_rmp0[0]	0.300000012
tgt_rmp0[1]	0.300000012
tgt_rmp1[0]	0.155000001
tgt_rmp1[1]	0.155000001

Name	Actual Value	Expected Value	Result
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32(data)	0.300000012	0.300000012	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc(data)	1	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08(data)	1	1	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc(data)	1	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc(data)	0	0	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	✔
Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	✔

Test Step 2.4 (Repeat Count = 1)			✔
Name	**Input Value**		
D_NOOFACTIVEINVERTER_CNT_U08	2		
T_DiagMgrDiagSts_Ptr_b16[0]	tgt_0		
T_DiagMgrDiagSts_Ptr_b16[1]	tgt_1		
T_DiagMgrRmpRate_Ptr_f32[0]	tgt_rmp0		
T_DiagMgrRmpRate_Ptr_f32[1]	tgt_rmp1		
tgt_0[0]	56		
tgt_0[1]	548		
tgt_1[0]	0		
tgt_1[1]	0		
tgt_rmp0[0]	0.150000006		
tgt_rmp0[1]	0.150000006		
tgt_rmp1[0]	0.100000001		
tgt_rmp1[1]	0.100000001		
Name	**Actual Value**	**Expected Value**	**Result**
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32(data)	0.150000006	0.150000006	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc(data)	0	0	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08(data)	2	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc(data)	0	0	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc(data)	0	0	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	✔
Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	✔

Test Step 2.5 (Repeat Count = 1)			✔
Name	**Input Value**		
D_NOOFACTIVEINVERTER_CNT_U08	2		
T_DiagMgrDiagSts_Ptr_b16[0]	tgt_0		
T_DiagMgrDiagSts_Ptr_b16[1]	tgt_1		
T_DiagMgrRmpRate_Ptr_f32[0]	tgt_rmp0		
T_DiagMgrRmpRate_Ptr_f32[1]	tgt_rmp1		
tgt_0[0]	548		
tgt_0[1]	6254		
tgt_1[0]	65535		
tgt_1[1]	65535		
tgt_rmp0[0]	0.25		
tgt_rmp0[1]	0.25		
tgt_rmp1[0]	0.200000003		
tgt_rmp1[1]	0.200000003		
Name	**Actual Value**	**Expected Value**	**Result**
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32(data)	0.25	0.25	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc(data)	1	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08(data)	0	0	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc(data)	1	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc(data)	1	1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	✔
Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	✔

Test Step 2.6 (Repeat Count = 1)			✔
Name	**Input Value**		
D_NOOFACTIVEINVERTER_CNT_U08	2		
T_DiagMgrDiagSts_Ptr_b16[0]	tgt_0		
T_DiagMgrDiagSts_Ptr_b16[1]	tgt_1		
T_DiagMgrRmpRate_Ptr_f32[0]	tgt_rmp0		
T_DiagMgrRmpRate_Ptr_f32[1]	tgt_rmp1		
tgt_0[0]	264		
tgt_0[1]	7		
tgt_1[0]	2000		
tgt_1[1]	5000		
tgt_rmp0[0]	0.349999994		
tgt_rmp0[1]	0.349999994		
tgt_rmp1[0]	0.300000012		
tgt_rmp1[1]	0.300000012		
Name	**Actual Value**	**Expected Value**	**Result**
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32(data)	0.349999994	0.349999994	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc(data)	1	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08(data)	1	1	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc(data)	1	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc(data)	0	0	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	✔
Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	✔

Test Step 2.7 (Repeat Count = 1)			✔
Name	**Input Value**		
D_NOOFACTIVEINVERTER_CNT_U08	2		
T_DiagMgrDiagSts_Ptr_b16[0]	tgt_0		
T_DiagMgrDiagSts_Ptr_b16[1]	tgt_1		
T_DiagMgrRmpRate_Ptr_f32[0]	tgt_rmp0		
T_DiagMgrRmpRate_Ptr_f32[1]	tgt_rmp1		
tgt_0[0]	25		
tgt_0[1]	50		
tgt_1[0]	56		
tgt_1[1]	548		
tgt_rmp0[0]	9.99999975e-005		
tgt_rmp0[1]	9.99999975e-005		
tgt_rmp1[0]	0.150000006		
tgt_rmp1[1]	0.150000006		
Name	**Actual Value**	**Expected Value**	**Result**
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32(data)	0.150000006	0.150000006	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc(data)	0	0	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08(data)	2	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc(data)	0	0	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc(data)	0	0	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	✔
Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	✔

Test Step 2.8 (Repeat Count = 1)			✔
Name	**Input Value**		
D_NOOFACTIVEINVERTER_CNT_U08	2		
T_DiagMgrDiagSts_Ptr_b16[0]	tgt_0		
T_DiagMgrDiagSts_Ptr_b16[1]	tgt_1		
T_DiagMgrRmpRate_Ptr_f32[0]	tgt_rmp0		
T_DiagMgrRmpRate_Ptr_f32[1]	tgt_rmp1		
tgt_0[0]	89		
tgt_0[1]	500		
tgt_1[0]	548		
tgt_1[1]	6254		
tgt_rmp0[0]	0.5		
tgt_rmp0[1]	0.5		
tgt_rmp1[0]	0.25		
tgt_rmp1[1]	0.25		
Name	**Actual Value**	**Expected Value**	**Result**
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32(data)	0.5	0.5	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc(data)	1	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08(data)	0	0	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc(data)	1	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc(data)	1	1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	✔
Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	✔

Test Step 2.9 (Repeat Count = 1)			✔
Name	**Input Value**		
D_NOOFACTIVEINVERTER_CNT_U08	2		
T_DiagMgrDiagSts_Ptr_b16[0]	tgt_0		
T_DiagMgrDiagSts_Ptr_b16[1]	tgt_1		
T_DiagMgrRmpRate_Ptr_f32[0]	tgt_rmp0		
T_DiagMgrRmpRate_Ptr_f32[1]	tgt_rmp1		
tgt_0[0]	62		
tgt_0[1]	756		
tgt_1[0]	264		
tgt_1[1]	7		
tgt_rmp0[0]	0.300000012		
tgt_rmp0[1]	0.400000006		
tgt_rmp1[0]	0.349999994		
tgt_rmp1[1]	0.349999994		
Name	**Actual Value**	**Expected Value**	**Result**
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32(data)	0.400000006	0.400000006	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc(data)	1	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08(data)	2	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc(data)	0	0	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc(data)	0	0	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	✔
Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	✔

Test Step 2.10 (Repeat Count = 1)			✔
Name	**Input Value**		
D_NOOFACTIVEINVERTER_CNT_U08	2		
T_DiagMgrDiagSts_Ptr_b16[0]	tgt_0		
T_DiagMgrDiagSts_Ptr_b16[1]	tgt_1		
T_DiagMgrRmpRate_Ptr_f32[0]	tgt_rmp0		
T_DiagMgrRmpRate_Ptr_f32[1]	tgt_rmp1		
tgt_0[0]	136		
tgt_0[1]	789		
tgt_1[0]	147		
tgt_1[1]	852		
tgt_rmp0[0]	0.449999988		
tgt_rmp0[1]	0.449999988		
tgt_rmp1[0]	9.99999975e-005		
tgt_rmp1[1]	9.99999975e-005		
Name	**Actual Value**	**Expected Value**	**Result**
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32(data)	0.449999988	0.449999988	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc(data)	1	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08(data)	2	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc(data)	0	0	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc(data)	0	0	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	✔
Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	✔

Test Step 2.11 (Repeat Count = 1)			✔
Name	**Input Value**		
D_NOOFACTIVEINVERTER_CNT_U08	2		
T_DiagMgrDiagSts_Ptr_b16[0]	tgt_0		
T_DiagMgrDiagSts_Ptr_b16[1]	tgt_1		
T_DiagMgrRmpRate_Ptr_f32[0]	tgt_rmp0		
T_DiagMgrRmpRate_Ptr_f32[1]	tgt_rmp1		
tgt_0[0]	456		
tgt_0[1]	987		
tgt_1[0]	951		
tgt_1[1]	753		
tgt_rmp0[0]	0.0199999996		
tgt_rmp0[1]	0.0199999996		
tgt_rmp1[0]	0.5		
tgt_rmp1[1]	0.5		
Name	**Actual Value**	**Expected Value**	**Result**
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32(data)	0.5	0.5	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc(data)	1	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08(data)	2	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc(data)	0	0	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc(data)	0	0	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	✔
Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	✔

Test Step 2.12 (Repeat Count = 1)			✔
Name	**Input Value**		
D_NOOFACTIVEINVERTER_CNT_U08	2		
T_DiagMgrDiagSts_Ptr_b16[0]	tgt_0		
T_DiagMgrDiagSts_Ptr_b16[1]	tgt_1		
T_DiagMgrRmpRate_Ptr_f32[0]	tgt_rmp0		
T_DiagMgrRmpRate_Ptr_f32[1]	tgt_rmp1		
tgt_0[0]	318		
tgt_0[1]	963		
tgt_1[0]	751		
tgt_1[1]	359		
tgt_rmp0[0]	0.155000001		
tgt_rmp0[1]	0.155000001		
tgt_rmp1[0]	0.300000012		
tgt_rmp1[1]	0.400000006		
Name	**Actual Value**	**Expected Value**	**Result**
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32(data)	0.400000006	0.400000006	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc(data)	1	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08(data)	2	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc(data)	0	0	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc(data)	0	0	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	✔
Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	✔

Test Step 2.13 (Repeat Count = 1)			✔
Name	**Input Value**		
D_NOOFACTIVEINVERTER_CNT_U08	2		
T_DiagMgrDiagSts_Ptr_b16[0]	tgt_0		
T_DiagMgrDiagSts_Ptr_b16[1]	tgt_1		
T_DiagMgrRmpRate_Ptr_f32[0]	tgt_rmp0		
T_DiagMgrRmpRate_Ptr_f32[1]	tgt_rmp1		
tgt_0[0]	0		
tgt_0[1]	0		
tgt_1[0]	0		
tgt_1[1]	0		
tgt_rmp0[0]	9.99999975e-005		
tgt_rmp0[1]	9.99999975e-005		
tgt_rmp1[0]	9.99999975e-005		
tgt_rmp1[1]	9.99999975e-005		
Name	**Actual Value**	**Expected Value**	**Result**
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32(data)	9.99999975e-005	9.99999975e-005	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc(data)	0	0	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08(data)	2	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc(data)	0	0	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc(data)	0	0	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	✔
Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	✔

Test Step 2.14 (Repeat Count = 1)			✔
Name	**Input Value**		
D_NOOFACTIVEINVERTER_CNT_U08	2		
T_DiagMgrDiagSts_Ptr_b16[0]	tgt_0		
T_DiagMgrDiagSts_Ptr_b16[1]	tgt_1		
T_DiagMgrRmpRate_Ptr_f32[0]	tgt_rmp0		
T_DiagMgrRmpRate_Ptr_f32[1]	tgt_rmp1		
tgt_0[0]	65535		
tgt_0[1]	65535		
tgt_1[0]	65535		
tgt_1[1]	65535		
tgt_rmp0[0]	0.5		
tgt_rmp0[1]	0.5		
tgt_rmp1[0]	0.5		
tgt_rmp1[1]	0.5		
Name	**Actual Value**	**Expected Value**	**Result**
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32(data)	0.5	0.5	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc(data)	1	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08(data)	0	0	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc(data)	1	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc(data)	1	1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	✔
Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	✔

Test Case 3: Path Test ✔

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:

TS3.1 7675.00 Cycles
TS3.2 7649.00 Cycles
TS3.3 7611.00 Cycles
TS3.4 7651.00 Cycles
TS3.5 7549.00 Cycles
TS3.6 7533.00 Cycles
```

Description

Vector Description:

TS 3.1"if ((TRUE == DiagStsNonRecRmpToZeroFltPres_Cnt_T_lgc) || (TRUE == DiagStsRecRmpToZeroFltPres_Cnt_T_lgc))
= TRUE"
TS 3.2"if ((TRUE == DiagStsNonRecRmpToZeroFltPres_Cnt_T_lgc) || (TRUE == DiagStsRecRmpToZeroFltPres_Cnt_T_lgc))
= FALSE"
TS 3.3"(TRUE == DiagStsNonRecRmpToZeroFltPres_Cnt_T_lgc)FALSE
and (TRUE == DiagStsRecRmpToZeroFltPres_Cnt_T_lgc))=>TRUE"
TS 3.4"(DiagStsInverter1Inactive_Cnt_T_lgc==FALSE)=TRUE && (DiagStsInverter2Inactive_Cnt_T_lgc==FALSE)=FALSE &&
(DiagStsInverter1Inactive_Cnt_T_lgc==TRUE)=FALSE
&& (DiagStsInverter1Inactive_Cnt_T_lgc==FALSE)=TRUE"
TS 3.5"((TRUE == DiagStsNonRecRmpToZeroFltPres_Cnt_T_lgc) || (TRUE == DiagStsRecRmpToZeroFltPres_Cnt_T_lgc)) = False;
(D_NOOFACTIVEINVERTER_CNT_U08 == 2U) = False
DiagStsInverter1Inactive_Cnt_T_lgc== TRUE) = False;"
TS 3.6"((TRUE == DiagStsNonRecRmpToZeroFltPres_Cnt_T_lgc) || (TRUE == DiagStsRecRmpToZeroFltPres_Cnt_T_lgc)) = False;
(D_NOOFACTIVEINVERTER_CNT_U08 == 2U) = False
(DiagStsInverter1Inactive_Cnt_T_lgc== TRUE) = True;"

Test Step 3.1 (Repeat Count = 1) ✔

Name	**Input Value**
D_NOOFACTIVEINVERTER_CNT_U08	2
T_DiagMgrDiagSts_Ptr_b16[0]	tgt_0
T_DiagMgrDiagSts_Ptr_b16[1]	tgt_1
T_DiagMgrRmpRate_Ptr_f32[0]	tgt_rmp0
T_DiagMgrRmpRate_Ptr_f32[1]	tgt_rmp1
tgt_0[0]	0
tgt_0[1]	0
tgt_1[0]	25
tgt_1[1]	50
tgt_rmp0[0]	0.100000001
tgt_rmp0[1]	0.100000001
tgt_rmp1[0]	0.449999988
tgt_rmp1[1]	0.449999988

Name	**Actual Value**	**Expected Value**	**Result**
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32(data)	0.449999988	0.449999988	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc(data)	1	1	✔

Name	Actual Value	Expected Value	Result
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc(data)	0	0	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08(data)	2	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc(data)	0	0	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc(data)	0	0	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	✔
Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	✔

Test Step 3.2 (Repeat Count = 1) ✔

Name	Input Value
D_NOOFACTIVEINVERTER_CNT_U08	2
T_DiagMgrDiagSts_Ptr_b16[0]	tgt_0
T_DiagMgrDiagSts_Ptr_b16[1]	tgt_1
T_DiagMgrRmpRate_Ptr_f32[0]	tgt_rmp0
T_DiagMgrRmpRate_Ptr_f32[1]	tgt_rmp1
tgt_0[0]	0
tgt_0[1]	0
tgt_1[0]	0
tgt_1[1]	0
tgt_rmp0[0]	9.99999975e-005
tgt_rmp0[1]	9.99999975e-005
tgt_rmp1[0]	9.99999975e-005
tgt_rmp1[1]	9.99999975e-005

Name	Actual Value	Expected Value	Result
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32(data)	9.99999975e-005	9.99999975e-005	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc(data)	0	0	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08(data)	2	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc(data)	0	0	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc(data)	0	0	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	✔
Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	✔

Test Step 3.3 (Repeat Count = 1)			✔
Name	**Input Value**		
D_NOOFACTIVEINVERTER_CNT_U08	2		
T_DiagMgrDiagSts_Ptr_b16[0]	tgt_0		
T_DiagMgrDiagSts_Ptr_b16[1]	tgt_1		
T_DiagMgrRmpRate_Ptr_f32[0]	tgt_rmp0		
T_DiagMgrRmpRate_Ptr_f32[1]	tgt_rmp1		
tgt_0[0]	0		
tgt_0[1]	0		
tgt_1[0]	0		
tgt_1[1]	0		
tgt_rmp0[0]	0.100000001		
tgt_rmp0[1]	0.100000001		
tgt_rmp1[0]	0.449999988		
tgt_rmp1[1]	0.449999988		
Name	**Actual Value**	**Expected Value**	**Result**
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32(data)	0.449999988	0.449999988	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc(data)	0	0	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08(data)	2	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc(data)	0	0	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc(data)	0	0	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	✔
Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	✔

Test Step 3.4 (Repeat Count = 1)			✔
Name	**Input Value**		
D_NOOFACTIVEINVERTER_CNT_U08	2		
T_DiagMgrDiagSts_Ptr_b16[0]	tgt_0		
T_DiagMgrDiagSts_Ptr_b16[1]	tgt_1		
T_DiagMgrRmpRate_Ptr_f32[0]	tgt_rmp0		
T_DiagMgrRmpRate_Ptr_f32[1]	tgt_rmp1		
tgt_0[0]	2048		
tgt_0[1]	2048		
tgt_1[0]	2048		
tgt_1[1]	2048		
tgt_rmp0[0]	0.100000001		
tgt_rmp0[1]	0.100000001		
tgt_rmp1[0]	0.449999988		
tgt_rmp1[1]	0.449999988		
Name	**Actual Value**	**Expected Value**	**Result**
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32(data)	0.449999988	0.449999988	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc(data)	0	0	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08(data)	1	1	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc(data)	0	0	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc(data)	1	1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	✔
Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	✔

Test Step 3.5 (Repeat Count = 1)			✔
Name	**Input Value**		
D_NOOFACTIVEINVERTER_CNT_U08	1		
T_DiagMgrDiagSts_Ptr_b16[0]	tgt_0		
T_DiagMgrDiagSts_Ptr_b16[1]	tgt_1		
T_DiagMgrRmpRate_Ptr_f32[0]	tgt_rmp0		
T_DiagMgrRmpRate_Ptr_f32[1]	tgt_rmp1		
tgt_0[0]	2048		
tgt_0[1]	2048		
tgt_1[0]	2048		
tgt_1[1]	2048		
tgt_rmp0[0]	0.100000001		
tgt_rmp0[1]	0.100000001		
tgt_rmp1[0]	0.449999988		
tgt_rmp1[1]	0.449999988		
Name	**Actual Value**	**Expected Value**	**Result**
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32(data)	0.449999988	0.449999988	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc(data)	0	0	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08(data)	1	1	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc(data)	0	0	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc(data)	1	1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	✔
Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	✔

Test Step 3.6 (Repeat Count = 1)			✔
Name	**Input Value**		
D_NOOFACTIVEINVERTER_CNT_U08	1		
T_DiagMgrDiagSts_Ptr_b16[0]	tgt_0		
T_DiagMgrDiagSts_Ptr_b16[1]	tgt_1		
T_DiagMgrRmpRate_Ptr_f32[0]	tgt_rmp0		
T_DiagMgrRmpRate_Ptr_f32[1]	tgt_rmp1		
tgt_0[0]	65535		
tgt_0[1]	65535		
tgt_1[0]	89		
tgt_1[1]	500		
tgt_rmp0[0]	0.200000003		
tgt_rmp0[1]	0.200000003		
tgt_rmp1[0]	0.0199999996		
tgt_rmp1[1]	0.0199999996		
Name	**Actual Value**	**Expected Value**	**Result**
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32(data)	0.200000003	0.200000003	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32(data)	0	0	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc(data)	1	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc(data)	1	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08(data)	0	0	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc(data)	1	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc(data)	1	1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP0_CheckpointReached	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsNonRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsCtrldDisRmpPres_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsRecRmpToZeroFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsHWASbSystmFltPres_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefVehSpd_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsDefTemp_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsScomHWANotValid_Cnt_lgc	1	✔
ReadBit_u16	1	ReadBit_u16	1	✔
Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagStsWIRDisable_Cnt_lgc	1	✔
ReadBit_u16	2	ReadBit_u16	2	✔
Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter1Inactive_Cnt_lgc	1	✔
Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	Rte_Write_DiagStsInverter2Inactive_Cnt_lgc	1	✔
Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	Rte_Write_Ap_DiagMgr_DiagRampRate_XpmS_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	Rte_Write_Ap_DiagMgr_DiagRampValue_Uls_f32	1	✔
Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	Rte_Write_Ap_DiagMgr_DiagRmpToZeroActive_Cnt_lgc	1	✔
Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	Rte_Write_DiagNoofActiveInverter_Cnt_u08	1	✔
Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	Rte_Call_DiagMgr_Per1_CP1_CheckpointReached	1	✔

TEST DETAILS REPORT

ReadBit_u16

2015-12-21, 17:40:00+0530

Project	DiagMgr_failaction
Module	DiagMgr_FailAction
Test Object	ReadBit_u16

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MCC Coverage	100 %
MC/DC Coverage	100 %

Statistics

Total Testcases	3
Successful	3
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\DiagMgr_Failaction
Configuration File	D:\Synergy_Work_Area\DiagMgr_Failaction\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\DiagMgr\src\Ap_DiagMgr_FailAction.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -Dstatic= -DSKIP_MAGIC_NUMBER= -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef \include -I$(PROJECTROOT)\DiagMgr\utp\contract -I$(PROJECTROOT)\DiagMgr\utp\contract\Test_CFG -I$(PROJECTROOT)\DiagMgr \include -I$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5\include

Comments/Description/Specification

Name	Text
Module 'DiagMgr_FailAction'	**********Unit Test Description********** Name of Tester:Namrata Morbale Code File(s) Under Test:Ap_DiagMgr_FailAction.c Code File(s) Version:3 Module Design Document:Diagnostics_Manager_FailAction_MDD.docx Module Design Document Version:3 Data Dictionary Version:11 Unit Test Plan Version:2 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS570_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.32 Total FLASH Used (Bytes):290 Total RAM Used (Bytes):0 Total CALS Used (Bytes):2760 Special Test Requirements: Test Date:12/21/2015 Comments:"Note 1: Inline Function defined in GlobalMacro.h is not unit tested. NOTE 2:""CBD_Sandbox_dbg.map"" map file is embedded for reference. NOTE 3: Constant D_NOOFACTIVEINVERTER_CNT_U08 is configurable variable and which is configured as per program so instead of declaring this variable as constant it is declared as variable for testing purpose and added same in Input. **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570.tpl
Target Install Path	$(ProgramFiles)\pls\UDE 3.2
Timer Enabled	false

Attributes

Name	Value
Timer Prescale	0
Timer Resolution	1
Timer Unit	Cycles
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\DiagMgr_Failaction\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Metrics Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:

TS1.1 25.00 Cycles
TS1.2 25.00 Cycles
```

Description

Vector Description:

TS 1.1Shortest Execution Path:(Data & BitMask) == 0U)=TRUE
TS 1.2Longest Execution Path:(Data & BitMask) == 0U)=FALSE

Test Step 1.1 (Repeat Count = 1)

Name	Input Value
BitMask	1
Data	0

Name	Actual Value	Expected Value	Result
ReadBit_u16()	0	0	✔

T

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 1.2 (Repeat Count = 1)

Name	Input Value
BitMask	1
Data	1

Name	Actual Value	Expected Value	Result
ReadBit_u16()	1	1	✔

T

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Case 2: Boundary Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:

TS2.1 25.00 Cycles
TS2.2 25.00 Cycles
TS2.3 25.00 Cycles
TS2.4 25.00 Cycles
TS2.5 25.00 Cycles
TS2.6 25.00 Cycles
TS2.7 25.00 Cycles
TS2.8 25.00 Cycles
```

Description

Vector Description:

TS 2.1data= min
TS 2.2data =max
TS 2.3data =pos
TS 2.4bitmask =min
TS 2.5bitmask =max
TS 2.6bitmask =Pos
TS 2.7all min
TS 2.8all max

Test Step 2.1 (Repeat Count = 1)

Name	Input Value
BitMask	500
Data	0

Name	Actual Value	Expected Value	Result
ReadBit_u16()	0	0	✔

T

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.2 (Repeat Count = 1)			✔
Name	**Input Value**		
BitMask	3568		
Data	65535		
Name	**Actual Value**	**Expected Value**	**Result**
ReadBit_u16()	1	1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
none	0	*** No Call Expected ***	0	✔

Test Step 2.3 (Repeat Count = 1)			✔
Name	**Input Value**		
BitMask	789		
Data	400		
Name	**Actual Value**	**Expected Value**	**Result**
ReadBit_u16()	1	1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
none	0	*** No Call Expected ***	0	✔

Test Step 2.4 (Repeat Count = 1)			✔
Name	**Input Value**		
BitMask	0		
Data	123		
Name	**Actual Value**	**Expected Value**	**Result**
ReadBit_u16()	0	0	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
none	0	*** No Call Expected ***	0	✔

Test Step 2.5 (Repeat Count = 1)			✔
Name	**Input Value**		
BitMask	65535		
Data	456		
Name	**Actual Value**	**Expected Value**	**Result**
ReadBit_u16()	1	1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
none	0	*** No Call Expected ***	0	✔

Test Step 2.6 (Repeat Count = 1)			✔
Name	**Input Value**		
BitMask	4000		
Data	789		
Name	**Actual Value**	**Expected Value**	**Result**
ReadBit_u16()	1	1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
none	0	*** No Call Expected ***	0	✔

Test Step 2.7 (Repeat Count = 1)

Name	Input Value		
BitMask	0		
Data	0		
Name	**Actual Value**	**Expected Value**	**Result**
ReadBit_u16()	0	0	✔

T

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.8 (Repeat Count = 1)

Name	Input Value		
BitMask	65535		
Data	65535		
Name	**Actual Value**	**Expected Value**	**Result**
ReadBit_u16()	1	1	✔

T

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Case 3: Path Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:

TS3.1 25.00 Cycles
TS3.2 25.00 Cycles
```

Description Vector Description:

TS 3.1Return= FALSE
TS 3.2Return= TRUE

Test Step 3.1 (Repeat Count = 1)

Name	Input Value		
BitMask	1		
Data	0		
Name	**Actual Value**	**Expected Value**	**Result**
ReadBit_u16()	0	0	✔

T

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 3.2 (Repeat Count = 1)

Name	Input Value		
BitMask	1		
Data	1		
Name	**Actual Value**	**Expected Value**	**Result**
ReadBit_u16()	1	1	✔

T

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔