Integration Manual – Thermal Duty Cycle

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# Dependencies

## SWCs

|  |  |
| --- | --- |
| Module | Required Feature |
| None |  |

## Global Functions(Non RTE) to be provided to Integration Project

## 

None

# Configuration

## Build Time Config

|  |  |  |
| --- | --- | --- |
| Modules | Notes |  |
| None |  |  |

## Configuration Files to be provided by Integration Project

Ap\_ThrmlDutyCycle\_Cfg.h to be generated by ThrmlDutyCycle\_Cfg.h.tt for checkpoint enables

### Da Vinci Parameter Configuration Changes

|  |  |  |
| --- | --- | --- |
| Parameter | Notes | SWC |
| ThrmDutyCycleGeneral/ThrmDutyCycleCPEnable | Enable checkpoints as needed | ThrmDutyCycle |

### DaVinci Interrupt Configuration Changes

|  |  |  |  |
| --- | --- | --- | --- |
| ISR Name | VIM # | Priority Dependency | Notes |
| <None> |  |  |  |

### Manual Configuration Changes

|  |  |  |
| --- | --- | --- |
| Constant | Notes | SWC |
| <None> |  |  |

# Integration

## Required Global Data Inputs

CuTempEst\_DegC\_f32

DefeatDutySvc\_Cnt\_lgc

FiltMeasTemp\_DegC\_f32

FilteredPkCurr\_AmpSq\_f32

IgnTimeOff\_Cnt\_u32

MagTempEst\_DegC\_f32

MotorVelCRF\_MtrRadpS\_f32

MtrPkCurr\_AmpSq\_f32

SiTempEst\_DegC\_f32

VehTimeValid\_Cnt\_lgc

## Required Global Data Outputs

DutyCycleLevel\_Uls\_f32

ThermLimitPerc\_Uls\_f32

ThermalLimit\_MtrNm\_f32

## Specific Include Path present

No

# Runnable Scheduling

This section specifies the required runnable scheduling.

|  |  |  |
| --- | --- | --- |
| Init | Scheduling Requirements | Trigger |
| ThrmlDutyCycle\_Init1 | After starting RTE, before first call of periodic functions | RTE (init) |

|  |  |  |
| --- | --- | --- |
| Runnable | Scheduling Requirements | Trigger |
| ThrmlDutyCycle\_Per1 | None | RTE (100ms) |
| ThrmlDutyCycle\_Trns1 | None | RTE transition to OFF state |

# Memory Mapping

## Mapping

|  |  |  |
| --- | --- | --- |
| Memory Section | Contents | Notes |
| THRMLDUTYCYCLE\_START\_SEC\_VAR\_CLEARED\_16 |  |  |
| THRMLDUTYCYCLE\_START\_SEC\_VAR\_CLEARED\_32 |  |  |
| THRMLDUTYCYCLE\_START\_SEC\_VAR\_CLEARED\_8 |  |  |
| THRMLDUTYCYCLE\_START\_SEC\_VAR\_CLEARED\_UNSPECIFIED |  |  |
| THRMLDUTYCYCLE\_STARTP\_SEC\_VAR\_CLEARED\_BOOLEAN |  |  |

\* Each …START\_SEC… constant is terminated by a …STOP\_SEC… constant as specified in the AUTOSAR Memory Mapping requirements.

## Usage

|  |  |  |
| --- | --- | --- |
| Feature | RAM | ROM |
|  |  |  |

Table 1: ARM Cortex R4 Memory Usage

## Non RTE NvM Blocks

|  |
| --- |
| Block Name |
| <NVM block used Non RTE functions > |

Note : Size of the NVM block if configured in developer

## RTE NvM Blocks

|  |
| --- |
| Block Name |
| Rte\_NvmBlock\_ThrmlDutyCycle\_ThrmlDutyCycle\_FltStVal (4 Bytes) |

Note : Size of the NVM block if configured in developer

# Compiler Settings

## Preprocessor MACRO

<Define all the preprocessor Macros needed and conditions when needed>.

## Optimization Settings

<Define Optimization levels that are needed and conditions when needed>.

# Revision Control Log

|  |  |  |  |
| --- | --- | --- | --- |
| **Rev #** | **Change Description** | **Date** | **Author** |
| 1 | Initial version | 25-Mar-13 | Selva |
| 2 | Updated to latest integration manual template | 1-Oct-13 | KMC |
| 3 | Updated NvM blocks and memory mapping for latest revision | 22-Nov-13 | KJS |
| 4 | Updated per anomaly EA3#3092 fix | 28-Oct-15 | Rijvi |