MICROSAR

Document Information

History

Author	Date	Version	Remarks
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Reference Documents

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1 Introduction

1.1 Purpose

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1.2 Scope

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1.3 Definitions

No.	Term	Description
		-

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1.4 Overview

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2 Functional safety on system level

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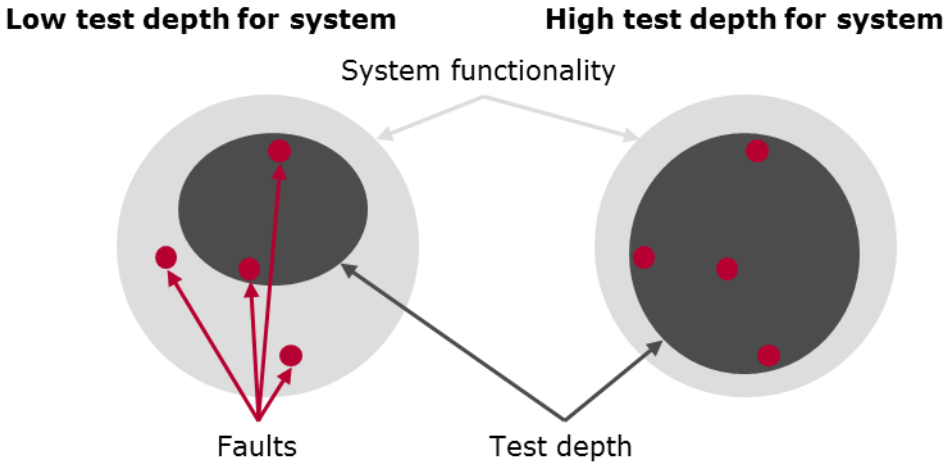
functional safety *absence of unreasonable risk due to hazards caused by malfunctioning behavior of E/E systems*

Malfunctioning behavior *failure or unintended behavior of an item with respect to its design intent*

Thus, a functionally safe system has to mitigate the risk associated with a failure and prevent unintended behavior.

2.1 Prevention of unintended behavior



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Thus, the system should be as simple as possible to keep it testable.

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Thus, the system should be as deterministic as possible to ease verification.

2.2 Mitigation of risk associated with a failure

failure
fault Faults *random hardware faults*
technical safety requirements
fault **detect** *random hardware faults* **act**
safe state
Random hardware faults *permanent faults* *transient faults*

random hardware faults

permanent faults
hardware components
transient faults

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Thus, we recommend the consideration of transient faults starting from ASIL B. For ASIL C systems transient faults must be handled appropriately.

fault *hardware component*

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2.3 Fail-safe and fail-operational systems

- *random hardware fault* *safe state* *random hardware faults*

safe state *failure*

Thus, only fail-safe systems are considered in this guide.

faults *fail-operational*

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3 Recommendations on safety mechanisms

3.1 Integrity of the microcontroller

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3.1.1 Operation in lock-step mode

enabling lock-step as early as possible in the boot process

diagnostic coverage

latent fault

3.1.2 Monitoring the temperature of the microcontrollers

3.1.3 Self-test of the microcontroller components

Thus, the requirements on self-tests are defined by the required ASIL.

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3.2 Integrity of volatile data

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3.2.1 Static tests of volatile memory

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latent fault

3.2.1.1 Initial test of volatile memory

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Caution

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3.2.1.2 Periodic tests of volatile memory

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3.2.2 Protection of volatile memory through error correcting codes (ECC)

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enabling the use of ECC-mechanisms as early as possible in the boot process

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3.2.2.1 Redundant storage of data

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Redundant storage of data is not supported by the Vector MICROSAR stack.

3.3 Integrity of non-volatile data

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diagnostic coverage

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diagnostic coverage

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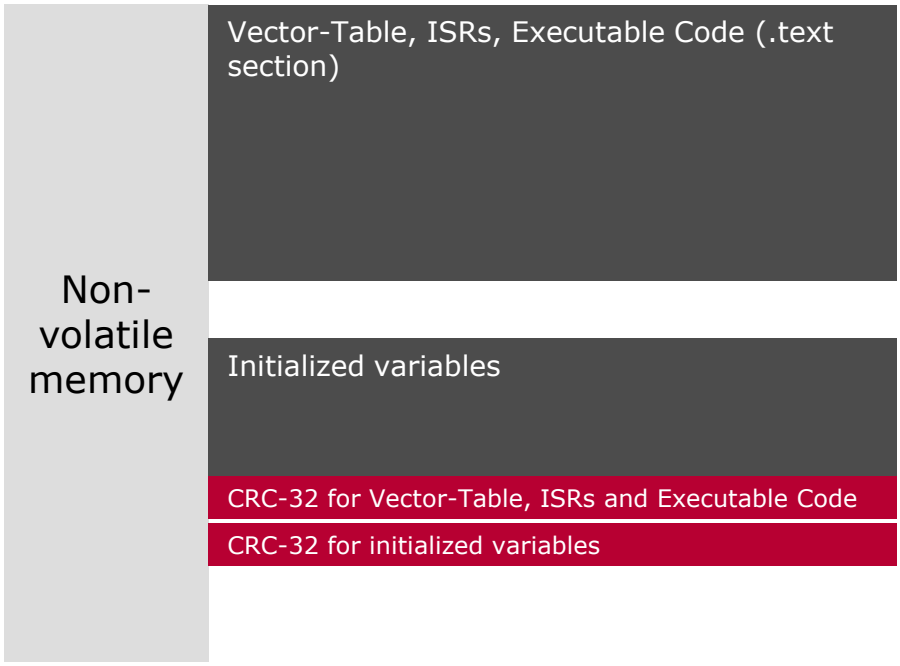

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3.3.1 Consistency of configuration and calibration data

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3.3.2 Securing non-volatile data with use of NVRAM Manager

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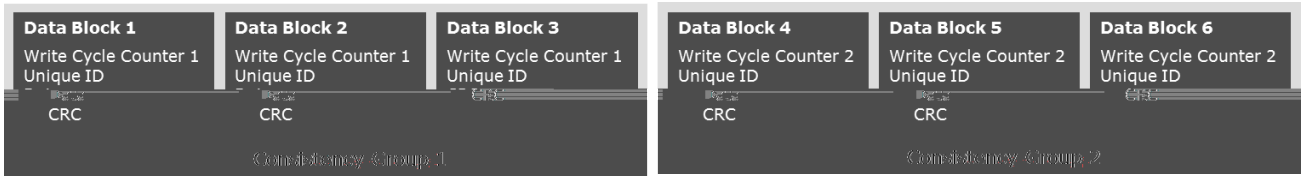

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3.4 Initialization of the microcontroller

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`StartOS()`

fault reaction

time

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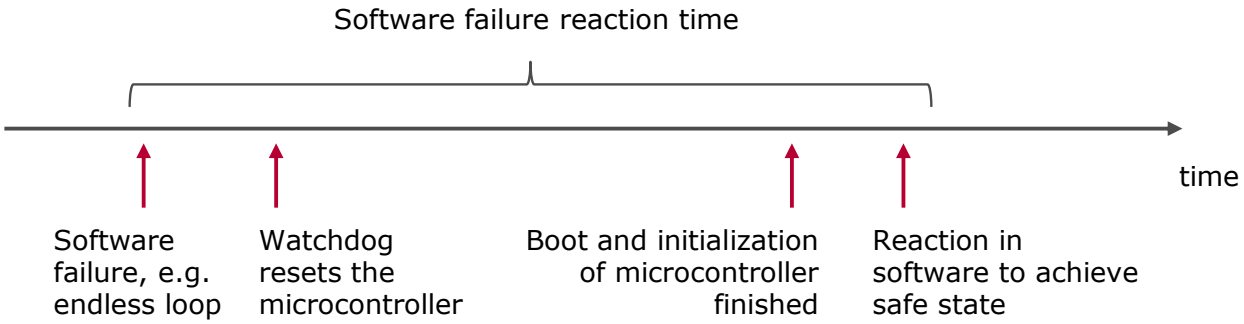

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3.5 Separation in memory

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freedom from interference

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freedom from interference

3.6 Separation in time

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3.7 Scheduling

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3.8 Communication

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3.9 Input and output

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4 Example use-cases

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4.1 ECU with direct I/O

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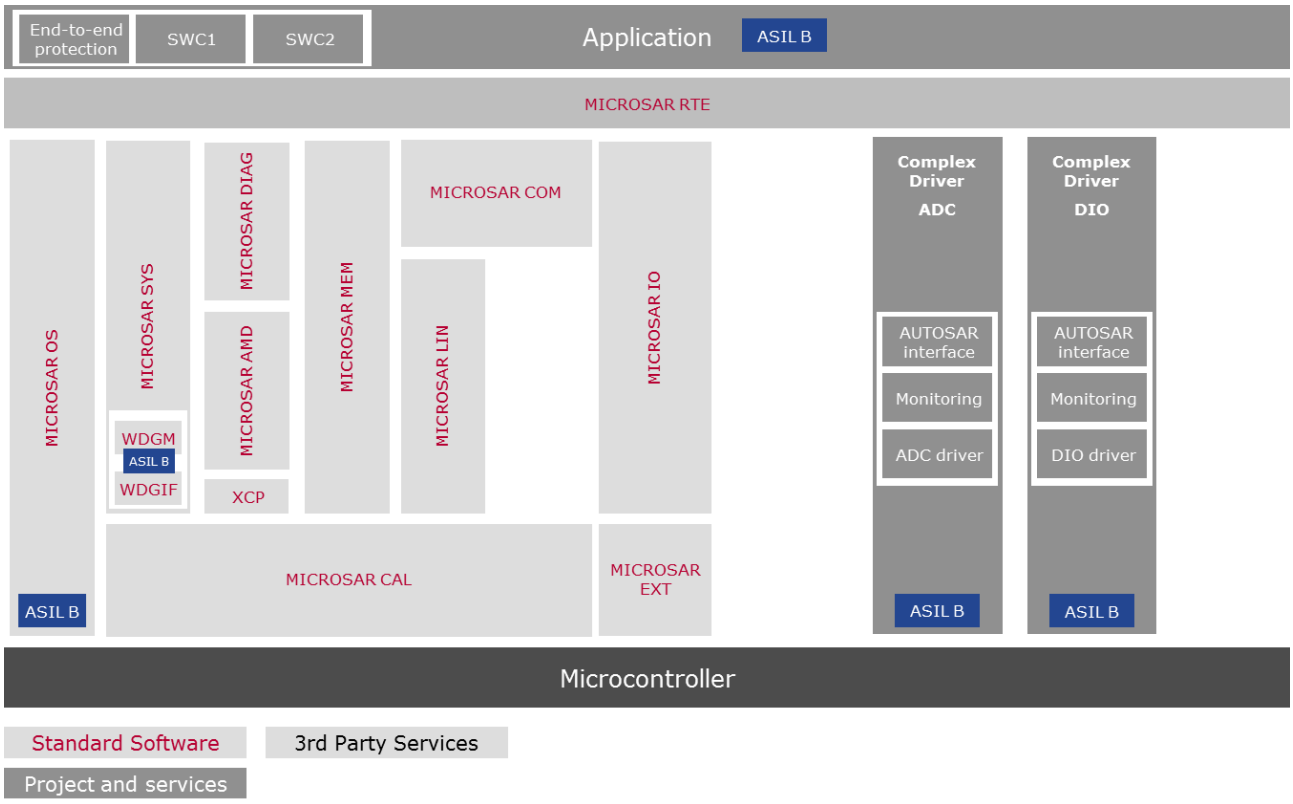

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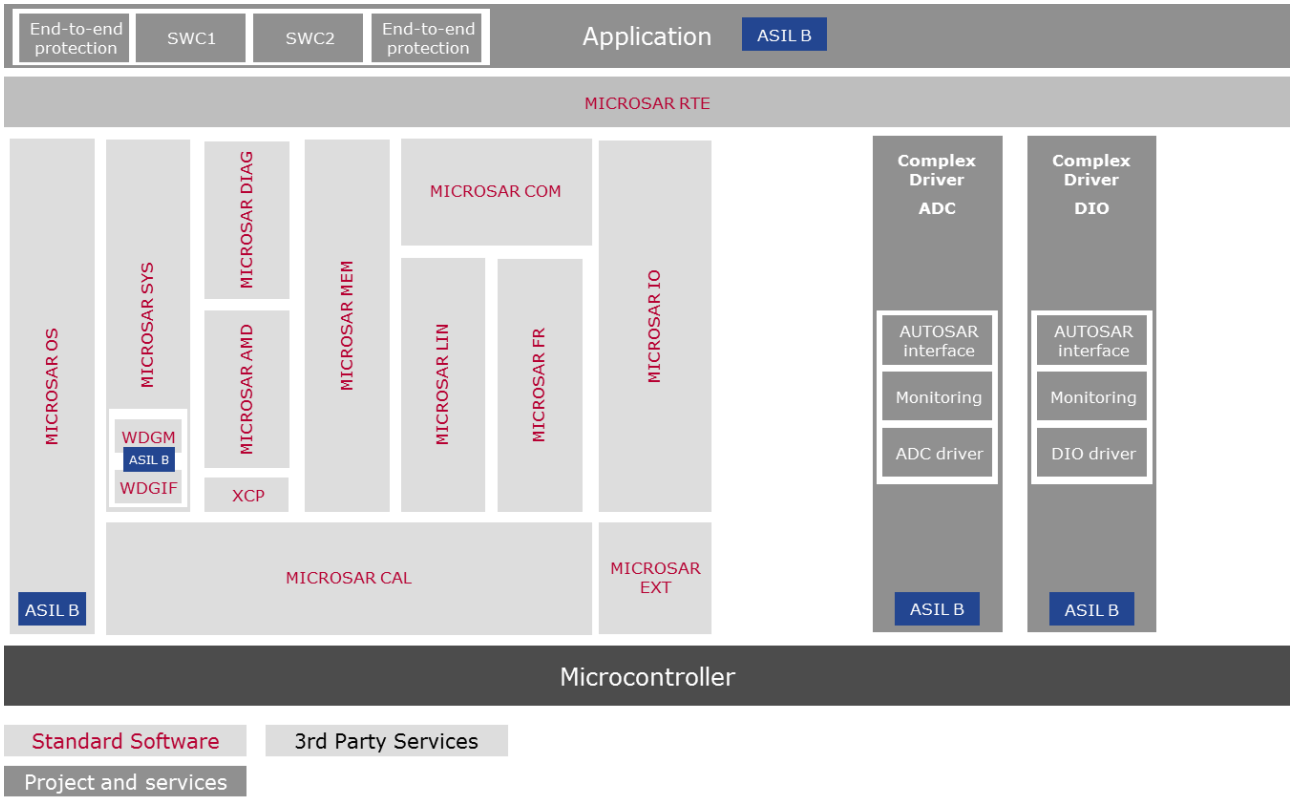
4.2 ECU with direct I/O and safety-related bus communication



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4.3 Mixed ASIL SWCs with safety-related bus communication

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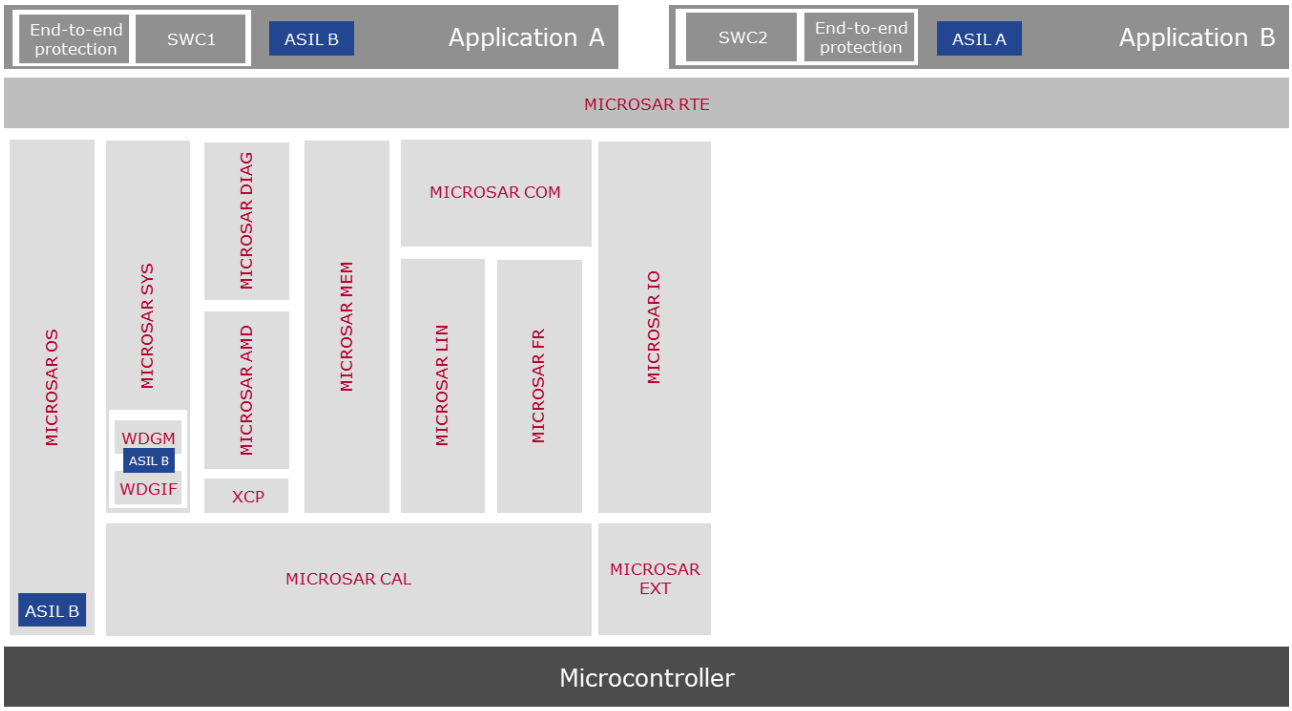

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5 Recommendations for the MICROSAR stack

5.1 Initialization

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3. -

5.2 ECU State Manager (EcuM)

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5.3 Basic Software Mode Manager (BswM)

5.4 Development Error Tracer (Det)

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5.5 Diagnostic Event Manager (Dem)

5.6 NVRAM Manager

5.7 Run-Time Environment (RTE)

5.8 End-to-End Protection (E2E)

5.9 Operating System (OS)

diagnostic coverage

5.10 Interrupt service routines (ISRs)

5.11 Microcontroller Abstraction Layer (MCAL)

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6 Procedural requirements

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7 Assumptions of Vector's safety solution

7.1 Assumptions of RTE

Assumption	Description	Can be shown by
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Assumption	Description	Can be shown by
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Assumption	Description	Can be shown by
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7.2 Assumptions of SafeWatchdog

Assumption	Description	Can be shown by
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Assumption	Description	Can be shown by
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8 Glossary and Abbreviations

8.1 Glossary

8.2 Abbreviations

Abbreviation	Description
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9 Contact

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