Modulation, demodulation, sampling, sampling theorem

Types of modulation

communication

CW modulation, Pulse modulation

AM & FM, RF

PAM, PDM, PPM, PCM.

Techiques of analog & digital

Idode, transistor, IC,

Resistor, Conductor, Inductor, semiconductor

Amplifier, Oscillator, repeater. rheostat, +ve f/B, -ve f/B

Capacitor, rectifier

Advantages of resistor

cutoff freq, pass band, stop band, base station

FeedBack, types < +ve, -ve, bipolar

Handover

Crosstalk

Bluetooth

CDMA

TDMA

FDMA.

op-amp

instrumentational amplifier

DIGITAL ELECTRONICS

1) Number system
- Decimal (with decimal eg)
- Binary
- Hexadecimal
- Octal

2) Laws => Moore law
- => Commutative law
- =>duality =>Associative
- Theorem =>distributive
- =>Demorgan
- => Idempotent
- => Law of complement
- => Law of Negation con Inclusion
- => Law of absorption
- => Consensus Law con Included factor law.

3) Forms of Boolean expression
- => MIN terms
- => Max terms
- => SOP
- => POS

4) Race condition

5) Eqn of HA, FA, HS, FS.

6) Basic gates & universal gates

7) MUX & DEMUX

8) ENCODER & DECODER, Priority encoder

9) K map, Quine MC Clusky

10) Flipflop & Latches → storage element in seq circuit
(1)

single bit storage (synchronous ckt)
edge triggering

Bistable multivibrator
2 stages

SR FF $Q(n+1) = S + R Q(n)$

D FF $Q(n+1) = D$

JK FF $Q(n+1) = J Q'(n) + K' Q(n)$

T FF $Q(n+1) = T \oplus Q(n)$

App of FF
⇒ data storage
⇒ transfer register
⇒ Counter, register
⇒ memory
⇒ freq division

Real time app of FF
⇒ Counter display at bank
⇒ token counters
⇒ microwave oven timer
⇒ fuel pump
⇒ weighing machine
⇒ Vending machine

Because counter act oly bang on FF function and it will count the value based on no. of FF used.

App of IC's
⇒ Computer
⇒ microwave
⇒ play station
⇒ camera
⇒ laptop
⇒ memory device
⇒ Wrist watches
⇒ TV, juice maker

App of Encoder & decoder
⇒ Health monitoring machine
⇒ RF based home automation system.
⇒ Robotic vehicle with metal detector.
⇒ used in communication syst. like telecommunication
⇒ networking, to transfer data from one end to another.

Priority encoder

It compresses multiple binary I/Ps into a smaller no. of O/P. In encoder, no of ~~~~ I/p lines but only one of them get activated at time. In PE, more than one I/P get activated at same time, register ⟹ shift register

App of shift reg

⇒ to store binary data,

⇒ data transfer & manipulation

⇒ SISO ⇒ time delay to ckt.

⇒ convert serial data to parallel data comm. lines. & parallel to serial.

SIPO ⇒ used in communication (demultiplexing of data lines)

PISO ⇒ convert parallel data to serial data (MUX)

PIPO ⇒ used as temporary storage

Bidirectional shift reg ⇒ Shift by left (×2). " " right (÷ 2)

mode = 1 - right
0 - left

Shift registers Counters ⇒ are the shift reg in which O/P are connected back to I/P in order to produce particular sequence.

Ring Counter — Johnson Counters

⇒ It is basically a shift register counter in which the O/P of FF is connected to next FF and so on. and O/P of last FF is feedback into 1st FF.

⇒ It is self decoding, No extra decoding is needed to determine what state the counter is in.

⇒ data pattern with in shift reg will circulate as long as clock pulse are applied

⇒ data pattern will repeat after every 4 clk pulses.

JOHNSON (TWISTED RING COUNTERS)

⇒ O/P of FF is connected to Next FF and so on, but O/P of last FF is inverted and again feedback to 1st FF.

⇒ data pattern will repeat every 8 clk pulse.

Ad

it only need n no. of FF compared to ring counter to circulate a given data to generate sequence of 2n states

COUNTERS

⇒ stores & displays the no. of times a particular event (or) process has occured.

⇒ Counting purpose

⇒ Asynchronous counter (ripple counter) / Synchronous counter (parallel clk)

In asynchronous, we don't use universal clk, only first FF is driven by clk. & clk I/P of rest of the following FF is drive by O/P of previous FF.

→ In synchronous, has one global clk which drives each FF, so O/P changes parallely.

⇒ Ad ⇒ does not have delay because same clk is given to each FF.

⇒ operate at high freq than asynchronous counters

- up counter
- down
- up/down
- mod counter ($2^n \geq N$) n = no of FF used, N = no of counter
- counting seq

Decade counter. (mod counter (or) synchronous BCD counter)

It counts ten different state & then reset to its initial state. will count from 0–9 (i.e. simple counter also count (0 to 15) (for 4 bit counter).

App of counter

⇒ digital clk

⇒ freq counters

= A to digital convertor

⇒ design digital Δ wave by using counter

⇒ Oven,

⇒ washing machine } calculating timer.

Conversion

- BCD. (Normal
- Gray (EXOR)
- Excess (+3)
- ASCII
- EBCDIC
- Error detecting code.
- Alpha numeric code

Binary → Bcd.

→ parity checker and generator (even, odd)

⇒ Complements (to substracting the numbers complements is used)

⇒ Conversion of FF

⇒ NAND / NOR implementation

⇒ 3 state buffer

Reducing method
⇒ K map (Karnaugh)
⇒ Tabulation method (Quin Mc Cluskey)

⇒ seq detector
⇒ 4 bit parallel adder/subtr or ripple carry adder/sub
⇒ carry look ahead adder
⇒ BCD adder
⇒ 4 bit magnitude comparator

Memory — RAM
ROM — PROM, EPROM, EEPROM

Programmable Logic devices		AND array	OR array
	PROM	fixed	programmable
	PAL	programmable	fixed
	PLA	programmable	...

IC — Combination, sequential ckt

⇒ Analysis of synchronous seq ckt
⇒ state eqn (or Characteristic eqn)
⇒ state diagram
⇒ state table
⇒ Mealy / Moore Model

state assignments
⇒ Binary code
⇒ Gray code
⇒ One hot assignment
⇒ universal register
⇒ serial adder

1) Combinal & sequential circuits

Combinational	sequential
⇒ O/P depends only on I/P.	⇒ O/P depends on both present & past I/PS.
⇒ Clk is not required.	⇒ Clk req
⇒ Easy to design	⇒ difficult
⇒ faster in speed	⇒ slower
⇒ memory not req	⇒ memory req to store previous I/Ps.
⇒ Eg: MUX, demux, encoder, decoder, adders, subtractor	Memory — FF — sync ckt — Latch — Asy ckt Eg: Register, Counter

syn ckt	Asy ckt
⇒ digital circuits are governed by clock signal	digital circuits are not driven by clk signal. They are self timed circuits
⇒ O/P depends on I/P at discrete time.	O/P depends on sequence in which the I/P changes.
⇒ Memory elements are used like clocked FF.	Memory elements are used like unclocked FF (or) time delay elements
⇒ Time variable is discrete	Time variable is continuous.
⇒ Easy to design but slow in operation	Difficult to design but faster in operation.
⇒ No timing prblm in feedback path	Prblm involved in feedback path.
⇒ complex circuit, more expensive.	has few components, less expensive (economical).
⇒ In these circuit, change in state occurs in response to clock puls	In these circuits, state changes occurs whenever I/P variable change
Eg: Counter, Shift reg, memory unit	Eg: Low power & high speed operation like simple microprocessor, digital signal processing units, in communi system for email application, internet access & networking.

Synchoronus Counter	Asynchronous Counter
=> All FF are triggered with same clock simultaneously.	=> different FF are triggered with different clock not simultan....
=> Faster in operater than any counter	=> slower.
=> Does not produce any decoding errors.	=> produce decoding error
=> Also called as parallel counter	=> serial counter
=> Designing & implementation are complex due to increasing no. of states.	=> Very easy
=> will operate in any desired count sequence.	=> will operate only in fixed count sequence (up/down)
=> Eg: ring, Johnson counter	Eg: Ripple up counter, ripple down.
=> propagation delay is less	=> High propagation delay.