Lab07 Interrupt & Timer

PIC18F4520 Datasheet

MicroChip - PIC18F4520 Datasheet

(https://ww1.microchip.com/downloads/en/DeviceDoc/39631E.pdf)

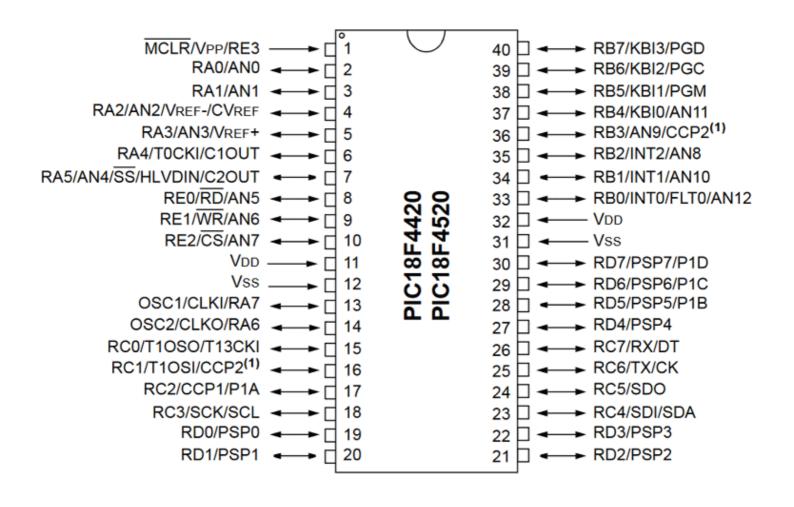
Interrupt用

Register名稱	在第幾頁	用途
RCON	第44頁	IPEN: 設定Interrupt優先度
INTCON	第95頁	GIE、INTO的[Flag bit, Enable Bit]
ADCON1	第226頁	設定數位類比

Timer用

Register名稱	在第幾頁	用途
OSCCON	第32頁	調整時脈 (可以玩看看)
T2CON	第135頁	設定Timer2的啟動、預除器後除器
PIR1	第98頁	TMR2IF、TMR1IF等
PIE1	第100頁	TMR2IE、TMR1IE等
IPR1	第102頁	TMR2IP、TMR1IP等

PIC18F4520 架構圖



Interrupt 範例程式碼

```
1
     #include "p18f4520.inc"
 2
 3
     ; CONFIG1H
                                      ; Oscillator Selection bits (Internal (
 4
       CONFIG OSC = INTIO67
 5
       CONFIG FCMEN = OFF
                                      : Fail-Safe Clock Monitor Enable bit (I
                                      ; Internal/External Oscillator Switchov
 6
       CONFIG IESO = OFF
 7
 8
     ; CONFIG2L
 9
       CONFIG PWRT = OFF
                                      ; Power-up Timer Enable bit (PWRT disal
       CONFIG
               BOREN = SBORDIS
                                      ; Brown-out Reset Enable bits (Brown-out)
10
               BORV = 3
                                      ; Brown Out Reset Voltage bits (Minimur
       CONFIG
11
12
13
     ; CONFIG2H
                                      ; Watchdog Timer Enable bit (WDT disab
14
       CONFIG WDT = OFF
       CONFIG WDTPS = 32768
                                      ; Watchdog Timer Postscale Select bits
15
16
17
     ; CONFIG3H
18
       CONFIG CCP2MX = PORTC
                                      ; CCP2 MUX bit (CCP2 input/output is mu
       CONFIG PBADEN = ON
                                      ; PORTB A/D Enable bit (PORTB<4:0> pins
19
       CONFIG LPT10SC = 0FF
                                      ; Low-Power Timer1 Oscillator Enable b:
20
                                      ; MCLR Pin Enable bit (MCLR pin enabled
       CONFIG MCLRE = ON
21
```

```
22
23
     ; CONFIG4L
                                      ; Stack Full/Underflow Reset Enable bit
24
       CONFIG STVREN = ON
                                      ; Single-Supply ICSP Enable bit (Single
25
       CONFIG LVP = OFF
26
       CONFIG XINST = OFF
                                      ; Extended Instruction Set Enable bit
27
28
     ; CONFIG5L
       CONFIG CP0 = OFF
                                      ; Code Protection bit (Block 0 (000800-
29
30
       CONFIG CP1 = OFF
                                      ; Code Protection bit (Block 1 (002000-
31
       CONFIG CP2 = OFF
                                      ; Code Protection bit (Block 2 (004000-
32
       CONFIG CP3 = OFF
                                      ; Code Protection bit (Block 3 (006000-
33
34
     ; CONFIG5H
       CONFIG CPB = OFF
35
                                      ; Boot Block Code Protection bit (Boot
       CONFIG CPD = OFF
                                      ; Data EEPROM Code Protection bit (Data
36
37
38
     ; CONFIG6L
       CONFIG WRT0 = OFF
                                      ; Write Protection bit (Block 0 (00080)
39
       CONFIG WRT1 = OFF
                                      ; Write Protection bit (Block 1 (00200)
40
                                      ; Write Protection bit (Block 2 (00400)
41
       CONFIG WRT2 = OFF
       CONFIG WRT3 = OFF
                                      : Write Protection bit (Block 3 (00600)
42
43
     ; CONFIG6H
44
       CONFIG WRTC = OFF
45
                                      ; Configuration Register Write Protect:
46
       CONFIG WRTB = OFF
                                      ; Boot Block Write Protection bit (Boot
47
       CONFIG WRTD = OFF
                                      ; Data EEPROM Write Protection bit (Dat
48
49
     ; CONFIG7L
50
                                      ; Table Read Protection bit (Block 0 (
       CONFIG EBTR0 = OFF
51
       CONFIG EBTR1 = OFF
                                      ; Table Read Protection bit (Block 1 (
                                      ; Table Read Protection bit (Block 2 (
52
       CONFIG EBTR2 = OFF
53
       CONFIG EBTR3 = OFF
                                      ; Table Read Protection bit (Block 3 (
54
55
     ; CONFIG7H
       CONFIG EBTRB = OFF
56
                                      ; Boot Block Table Read Protection bit
57
58
         L1 EQU 0x14
59
         L2 EQU 0x15
60
         org 0x00
61
     DELAY macro num1, num2
62
63
         local LOOP1
64
         local LOOP2
65
         MOVLW num2
         MOVWF L2
66
67
         L00P2:
             MOVLW num1
68
             MOVWF L1
69
70
         L00P1:
71
             N<sub>0</sub>P
72
             N<sub>0</sub>P
```

73

N₀P

```
74
            N<sub>0</sub>P
75
            N<sub>0</sub>P
76
            N0P
77
            DECFSZ L1, 1
            BRA LOOP1
78
79
            DECFSZ L2, 1
80
             BRA LOOP2
81
     endm
82
83
     ; 程式邏輯:會一直卡在main裡面做無限迴圈,按下RBO的按鈕後會觸發interrupt,跳到ISR:
     ; ISR裡的內容會亮起所有在RA上的燈泡, Delay約0.5秒後熄滅。
84
85
86
     goto Initial
                                   ; 避免程式一開始就會執行到ISR這一段,要跳過。
     ISR:
87
                                   ; Interrupt發生時,會跳到這裡執行。
88
         org 0x08
89
         SETF LATA
90
         DELAY d'350', d'180'
                                   ; 約500_000cycles數, 在1MHz的情況下大約會D\epsilon
91
         CLRF LATA
92
         BCF INTCON, INT0IF
93
         RETFIE
                                  ; 離開ISR,回到原本程式執行的位址,同時會將GIE設
94
95
96
     Initial:
                                          ; 初始化的相關設定
97
         MOVLW 0x0F
         MOVWF ADCON1
98
                                  ; 設定成要用數位的方式, Digitial I/0
99
         CLRF TRISA
100
         CLRF LATA
101
102
         BSF TRISB,
         BCF RCON, IPEN
103
         BCF INTCON, INT0IF
                                ; 先將Interrupt flag bit清空
104
         BSF INTCON, GIE
                                  ; 將Global interrupt enable bit打開
105
         BSF INTCON, INTOIE
                                 ; 將interrupt0 enable bit 打開 (INT0與RB0
106
107
108
     main:
109
         bra main
110
     end
```

Timer2 範例程式碼

```
1
    #include "p18f4520.inc"
2
3
    ; CONFIG1H
                                     ; Oscillator Selection bits (Internal o
4
      CONFIG OSC = INTIO67
5
      CONFIG FCMEN = OFF
                                     ; Fail-Safe Clock Monitor Enable bit (F
      CONFIG IESO = OFF
                                     ; Internal/External Oscillator Switchov
6
7

    CONFTG2L
```

```
9
              PWRT = OFF
                                     ; Power-up Timer Enable bit (PWRT disab
       CONFIG
10
       CONFIG BOREN = SBORDIS
                                     ; Brown-out Reset Enable bits (Brown-ou
       CONFIG BORV = 3
                                     ; Brown Out Reset Voltage bits (Minimum
11
12
13
     ; CONFIG2H
14
       CONFIG
              WDT = OFF
                                     ; Watchdog Timer Enable bit (WDT disabl
       CONFIG WDTPS = 32768
15
                                     ; Watchdog Timer Postscale Select bits
16
17
     ; CONFIG3H
18
       CONFIG CCP2MX = PORTC
                                     ; CCP2 MUX bit (CCP2 input/output is mu
19
       CONFIG PBADEN = ON
                                     ; PORTB A/D Enable bit (PORTB<4:0> pins
20
       CONFIG LPT10SC = 0FF
                                     ; Low-Power Timer1 Oscillator Enable bi
21
       CONFIG MCLRE = ON
                                     ; MCLR Pin Enable bit (MCLR pin enabled
22
23
     ; CONFIG4L
24
       CONFIG STVREN = 0N
                                     ; Stack Full/Underflow Reset Enable bit
25
       CONFIG LVP = OFF
                                     ; Single-Supply ICSP Enable bit (Single
26
       CONFIG XINST = OFF
                                     ; Extended Instruction Set Enable bit (
27
28
     ; CONFIG5L
29
       CONFIG CP0 = OFF
                                     ; Code Protection bit (Block 0 (000800-
30
       CONFIG CP1 = OFF
                                     ; Code Protection bit (Block 1 (002000-
                                     ; Code Protection bit (Block 2 (004000-
31
       CONFIG CP2 = OFF
       CONFIG CP3 = OFF
32
                                     ; Code Protection bit (Block 3 (006000-
33
34
     ; CONFIG5H
35
       CONFIG CPB = OFF
                                     ; Boot Block Code Protection bit (Boot
36
       CONFIG CPD = OFF
                                     ; Data EEPROM Code Protection bit (Data
37
38
     ; CONFIG6L
39
       CONFIG WRT0 = OFF
                                     ; Write Protection bit (Block 0 (000800
40
       CONFIG WRT1 = OFF
                                     ; Write Protection bit (Block 1 (002000
       CONFIG WRT2 = OFF
41
                                     ; Write Protection bit (Block 2 (004000
42
       CONFIG WRT3 = OFF
                                     ; Write Protection bit (Block 3 (006000
43
44
     ; CONFIG6H
45
       CONFIG WRTC = OFF
                                     ; Configuration Register Write Protecti
46
       CONFIG
              WRTB = OFF
                                     ; Boot Block Write Protection bit (Boot
47
       CONFIG WRTD = OFF
                                     ; Data EEPROM Write Protection bit (Dat
48
49
     ; CONFIG7L
50
       CONFIG
              EBTR0 = OFF
                                     ; Table Read Protection bit (Block 0 (0
51
       CONFIG EBTR1 = 0FF
                                     ; Table Read Protection bit (Block 1 (0
52
       CONFIG EBTR2 = OFF
                                     ; Table Read Protection bit (Block 2 (0
53
       CONFIG EBTR3 = OFF
                                     ; Table Read Protection bit (Block 3 (0
54
55
     ; CONFIG7H
56
       CONFIG EBTRB = OFF
                                     ; Boot Block Table Read Protection bit
57
58
         org 0x00
```

, CONTINUEL

59

```
60
    goto Initial
61
    ISR:
62
        org 0x08
                               ; 大致效果: 每0.5秒會進入一次interrupt
        COMF LATA
                               ; interrupt會開關LATA一次
63
64
        BCF PIR1, TMR2IF
                               ; 離開前記得把TMR2IF清空 (清空flag bit)
65
        RETFIE
66
    Initial:
67
68
        MOVLW 0x0F
        MOVWF ADCON1
69
70
        CLRF TRISA
71
        CLRF LATA
72
        BSF RCON, IPEN
73
        BSF INTCON, GIE
74
        BCF PIR1, TMR2IF
                                  ; 為了使用TIMER2,所以要設定好相關的TMR2IF、T№
        BSF IPR1, TMR2IP
75
76
        BSF PIE1 , TMR2IE
77
        MOVLW b'11111111'
                                  ; 將Prescale與Postscale都設為1:16, 意思是之行
        MOVWF T2CON
                                  ; 而由於TIMER本身會是以系統時脈/4所得到的時脈為
78
79
        MOVLW D'122'
                                  ; 因此每256 * 4 = 1024個cycles才會將TIMER2
80
        MOVWF PR2
                                  ; 若目前時脈為250khz, 想要Delay 0.5秒的話,代:
81
                                  ; 因此PR2應設為 125000 / 1024 = 122.070312
82
        MOVLW D'00100000'
83
        MOVWF OSCCON
                                  ; 記得將系統時脈調整成250kHz
84
85
    main:
86
        bra main
87
88
89
    end
90
```