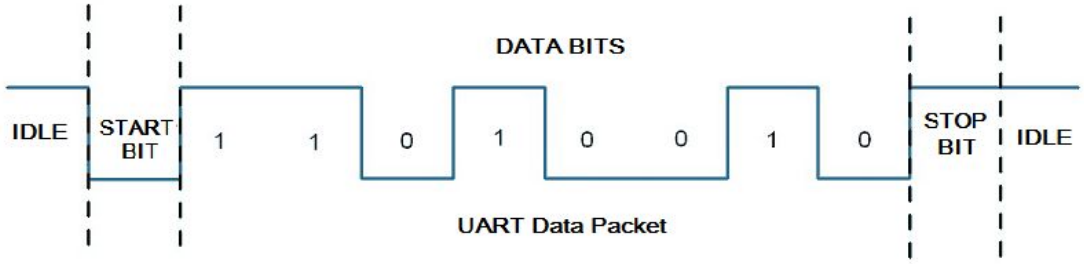
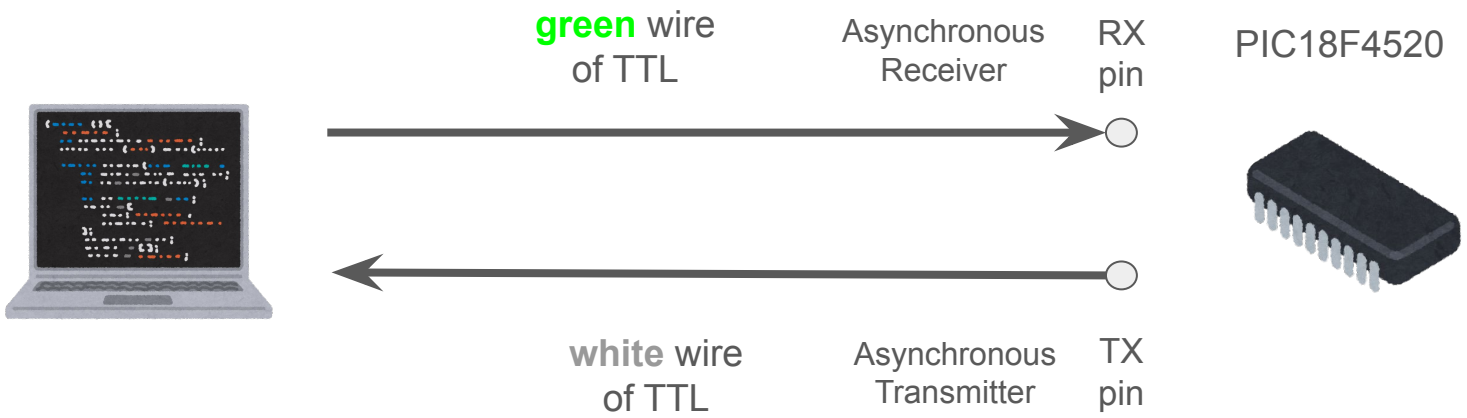
Lab 10 - UART

Introduction - UART

- **U**niversal **A**synchronous **R**eceiver **T**ransmitter
- Each character (data byte) is placed in between the start and stop bits. The start bit is always 0 (low) and the stop bit is always 1 (high).
- 3 important components:
  - Asynchronous transmitter
  - Asynchronous receiver
  - Baud rate generator



Experiment Setup



Asynchronous transmitter

Register bit needed to set:

1. TXEN (TXSTA<5>): Enable transmission.
2. SPEN (RCSTA<7>): Enable asynchronous serial port.

Register bit will set while transmit:

1. TRMT (TXSTA<7>): Read only, which is set when the TSR register is empty.
2. TXIF (PIR1<4>): Set when TXREG is empty

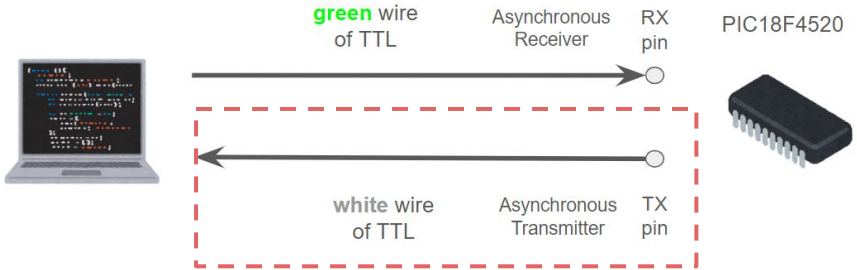
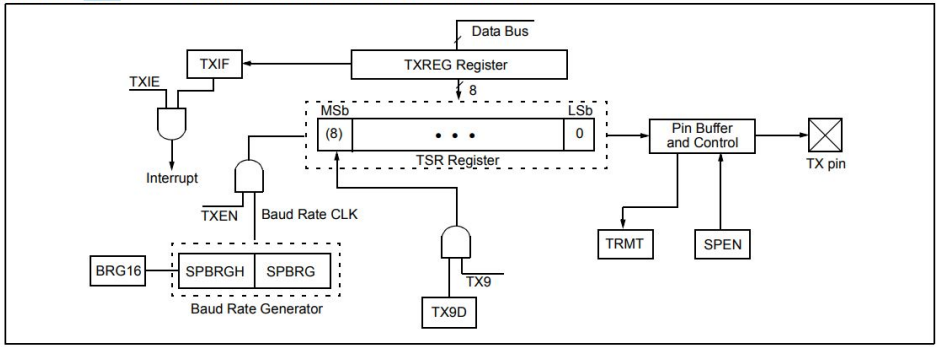


FIGURE 18-3: EUSART TRANSMIT BLOCK DIAGRAM



Reference: Datasheet p.211 FIGURE 18-3

Asynchronous transmitter

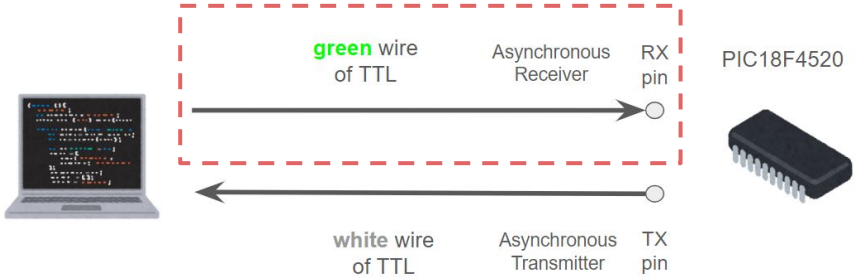
Set up asynchronous transmission:

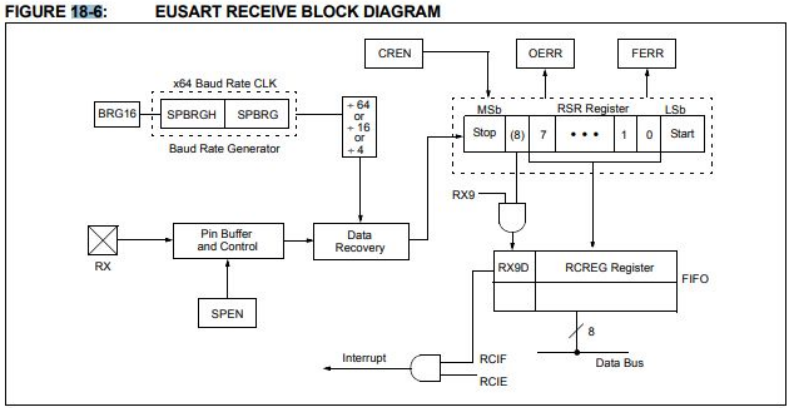
1. Set the baud rate correctly
2. Enable the asynchronous serial port by clearing **SYNC** (TXSTA<4>), and setting **SPEN** (RCSTA<7>)
3. If interrupt is desired, set **TXIE** (PIE<4>)
4. Enable the transmission by setting **TXEN** (TXSTA<5>), which will also set **TXIF** bit.
5. Load data to **TXREG** register to start transmission.

Reference: Datasheet p.214

Asynchronous receiver

1. RCIF (RIR1<5>): will set when reception is complete
2. SPEN (RCSTA<7>): enable asynchronous serial port
3. OERR, FERR: error detect
4. CREN: continuous receive enable bit, will be cleared when error occurred





Reference: Datasheet p.213 FIGURE 18-6

Asynchronous receiver

Set up asynchronous reception:

1. Set the baud rate correctly
2. Enable the asynchronous serial port by clearing **SYNC** (TXSTA<4>), and setting **SPEN** (RCSTA<7>)
3. If interrupt is desired, set **RCIE** (PIE<4>)
4. Enable the reception by setting bit, **CREN** (RCSTA<4>)
5. Read the 8-bit received data by reading the **RCREG** register

Reference: Datasheet p.216

Baud Rate

1. BRG16 (BAUDCON<3>): choose 16-bit or 8-bit baud rate generator
   a. 16-bit: SPBRGH and SPBRG
   b. 8-bit: SPBRG only
2. SYNC (TXSTA<4>): EUSART Mode Select bit, we use async mode
3. BRGH (TXSTA<2>): High Baud Rate Select bit
4. SPBRGH : SPBRG: controls the period of a free-running timer

EXAMPLE 18-1: CALCULATING BAUD RATE ERROR

For a device with FOSC of 16 MHz, desired baud rate of 9600, Asynchronous mode, 8-bit BRG:

Desired Baud Rate = FOSC/(64 ([SPBRGH:SPBRG] + 1))

Solving for SPBRGH:SPBRG:

X = ((FOSC/Desired Baud Rate)/64) – 1
= ((16000000/9600)/64) – 1
= [25.042] = 25

Calculated Baud Rate = 16000000/(64 (25 + 1))
= 9615

Error = (Calculated Baud Rate – Desired Baud Rate)/Desired Baud Rate
= (9615 – 9600)/9600 = 0.16%

Reference: Datasheet p.206 EXAMPLE 18-1

Baud Rate (Cont')

TABLE 18-1: BAUD RATE FORMULAS

Configuration Bits			BRG/EUSART Mode	Baud Rate Formula
SYNC	BRG16	BRGH		
0	0	0	8-Bit/Asynchronous	Fosc/[64 (n + 1)]
0	0	1	8-Bit/Asynchronous	Fosc/[16 (n + 1)]
0	1	0	16-Bit/Asynchronous	
0	1	1	16-Bit/Asynchronous	Fosc/[4 (n + 1)]
1	0	x	8-Bit/Synchronous	
1	1	x	16-Bit/Synchronous	

Legend: x = Don't care, n = value of SPBRGH:SPBRG register pair

Reference: Datasheet p.206 - 208

TABLE 18-3: BAUD RATES FOR ASYNCHRONOUS MODES

BAUD RATE (K)	SYNC = 0, BRGH = 0, BRG16 = 0											
	Fosc = 40.000 MHz			Fosc = 20.000 MHz			Fosc = 10.000 MHz			Fosc = 8.000 MHz		
	Actual Rate (K)	% Error	SPBRG Value (decimal)	Actual Rate (K)	% Error	SPBRG Value (decimal)	Actual Rate (K)	% Error	SPBRG Value (decimal)	Actual Rate (K)	% Error	SPBRG Value (decimal)
0.3	—	—	—	—	—	—	—	—	—	—	—	—
1.2	—	—	—	1.221	1.73	255	1.202	0.16	129	1.201	-0.16	103
2.4	2.441	1.73	255	2.404	0.16	129	2.404	0.16	64	2.403	-0.16	51
9.6	9.615	0.16	64	9.766	1.73	31	9.766	1.73	15	9.615	-0.16	12
19.2	19.531	1.73	31	19.531	1.73	15	19.531	1.73	7	—	—	—
57.6	56.818	-1.36	10	62.500	8.51	4	52.083	-9.58	2	—	—	—
115.2	125.000	8.51	4	104.167	-9.58	2	78.125	-32.18	1	—	—	—

BAUD RATE (K)	SYNC = 0, BRGH = 0, BRG16 = 0								
	Fosc = 4.000 MHz			Fosc = 2.000 MHz			Fosc = 1.000 MHz		
	Actual Rate (K)	% Error	SPBRG Value (decimal)	Actual Rate (K)	% Error	SPBRG Value (decimal)	Actual Rate (K)	% Error	SPBRG Value (decimal)
0.3	0.300	0.16	207	0.300	-0.16	103	0.300	-0.16	51
1.2	1.202	0.16	51	1.201	-0.16	25	1.201	-0.16	12
2.4	2.404	0.16	25	2.403	-0.16	12	—	—	—
9.6	8.929	-6.99	6	—	—	—	—	—	—
19.2	20.833	8.51	2	—	—	—	—	—	—
57.6	62.500	8.51	0	—	—	—	—	—	—
115.2	62.500	-45.75	0	—	—	—	—	—	—

BAUD RATE (K)	SYNC = 0, BRGH = 1, BRG16 = 0											
	Fosc = 40.000 MHz			Fosc = 20.000 MHz			Fosc = 10.000 MHz			Fosc = 8.000 MHz		
	Actual Rate (K)	% Error	SPBRG Value (decimal)	Actual Rate (K)	% Error	SPBRG Value (decimal)	Actual Rate (K)	% Error	SPBRG Value (decimal)	Actual Rate (K)	% Error	SPBRG Value (decimal)
0.3	—	—	—	—	—	—	—	—	—	—	—	—
1.2	—	—	—	—	—	—	—	—	—	—	—	—
2.4	—	—	—	—	—	—	2.441	1.73	255	2.403	-0.16	207
9.6	9.766	1.73	255	9.615	0.16	129	9.615	0.16	64	9.615	-0.16	51
19.2	19.231	0.16	129	19.231	0.16	64	19.531	1.73	31	19.230	-0.16	25
57.6	58.140	0.94	42	56.818	-1.36	21	56.818	-1.36	10	55.555	3.55	8
115.2	113.636	-1.36	21	113.636	-1.36	10	125.000	8.51	4	—	—	—

BAUD RATE (K)	SYNC = 0, BRGH = 1, BRG16 = 0								
	Fosc = 4.000 MHz			Fosc = 2.000 MHz			Fosc = 1.000 MHz		
	Actual Rate (K)	% Error	SPBRG Value (decimal)	Actual Rate (K)	% Error	SPBRG Value (decimal)	Actual Rate (K)	% Error	SPBRG Value (decimal)
0.3	—	—	—	—	—	—	0.300	-0.16	207
1.2	1.202	0.16	207	1.201	-0.16	103	1.201	-0.16	51
2.4	2.404	0.16	103	2.403	-0.16	51	2.403	-0.16	25
9.6	9.615	0.16	25	9.615	-0.16	12	—	—	—
19.2	19.231	0.16	12	—	—	—	—	—	—
57.6	62.500	8.51	3	—	—	—	—	—	—
115.2	125.000	8.51	1	—	—	—	—	—	—

Setting UART pin

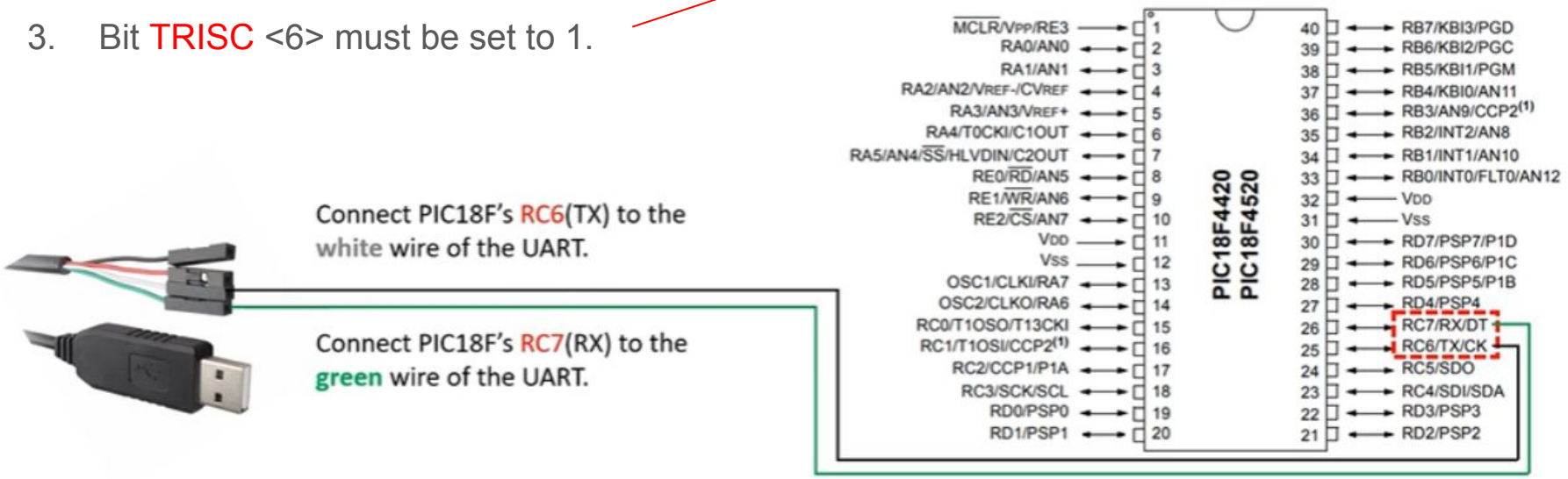
Reference: Datasheet p.112 TABLE10-5

RC6/TX/CK	RC6	0	O	DIG	LATC<6> data output.
		1	I	ST	PORTC<6> data input.
	TX	1	O	DIG	Asynchronous serial transmit data output (EUSART module); takes priority over port data. User must configure as output.
	CK	1	O	DIG	Synchronous serial clock output (EUSART module); takes priority over port data.
		1	I	ST	Synchronous serial clock input (EUSART module).
RC7/RX/DT	RC7	0	O	DIG	LATC<7> data output.
		1	I	ST	PORTC<7> data input.
	RX	1	I	ST	Asynchronous serial receive data input (EUSART module).
	DT	1	O	DIG	Synchronous serial data output (EUSART module); takes priority over port data.
		1	I	ST	Synchronous serial data input (EUSART module). User must configure as an input.

The pins of the Enhanced UART are multiplexed with PORTC.

In order to configure RC6/TX/CK and RC7/TX/DT as a UART:

1. Bit SPEN (RCSTA<7>) must be set to 1
2. Bit TRISC <7> must be set to 1
3. Bit TRISC <6> must be set to 1.



Reference

PIC18F4520 Datasheet: https://ww1.microchip.com/downloads/en/DeviceDoc/39631E.pdf