

# Operators (1/3)

- Operators perform an operation on one or more operands within an expression. An expression combines operands with appropriate operators to produce the desired function expression.

Name	Operator
bit-select or part-select	[ ]
parenthesis	( )
<b>Arithmetic Operators</b>	
multiplication	*
division	/
addition	+
subtraction	-
modulus	%
<b>Sign Operators</b>	
identity	+
negation	-

# Keywords (2/2)

- All keywords are defined in lower case.

always	and	assign	attribute	begin
buf	bufif0	bufif1	case	casex
casez	cmos	deassign	default	defparam
disable	edge	else	end	endattribute
endcase	endfunction	endmodule	endprimitive	endspecify
endtable	endtask	event	for	force

forever	fork	function	highz0	highz1
if	initial	inout	input	integer
join	large	macromodule	medium	module
nand	negedge	nmos	nor	not
notif0	notif1	or	output	parameter
pmos	posedge	primitive	pull0	pull1
pulldown	pullup	rcmos	real	realtime
reg	release	repeat	rnmos	rpmos
rtran	rtranif0	rtranif1	scalared	signed
small	specify	specparam	strength	strong0
strong1	supply0	supply1	table	task
time	tran	tranif0	tranif1	tri
tri0	tri1	triand	trior	triereg
unsigned	vectored	wait	wand	weak0
weak1	while	wire	wor	xnor
xor				



## Data type - net (wire)

接線種類	功能	能否合成
wire, tri	For standard interconnection wires (default)	可
wor, trior	For multiple drivers that are wire-ORed	wor 可, trior 否
wand, triand	For multiple drivers that are wire-ANDed	wand 可, triand 否
triereg	For nets with capacitive storage	否
tri0	For nets which pull down when not driven	否
tri1	For nets which pull up when not driven	否
supply0	For power rails	可
supply1	For ground rails	可

# Operators (2/3)

Name	Operator
<b>Relational Operators</b> less than less than or equal to greater than greater than or equal to	$<$ $<=$ $>$ $>=$
<b>Equality Operators</b> logic equality logic inequality case equality case inequality	$==$ $!=$ $===$ $!==$
<b>Logical Comparison Operators</b> NOT AND OR	$!$ $\&\&$ $  $
<b>Logical Bit-Wise Operators</b> unary negation NOT binary AND binary OR binary XOR binary XNOR	$\sim$ $\&$ $ $ $\wedge$ $\wedge\sim$ or $\sim\wedge$

# Operators (3/3)

Name	Operator
<b>Shift Operators</b> logical shift left logical shift right	<< >>
<b>Concatenation &amp; Replication Operators</b> concatenation replication	{ } { { } }
<b>Reduction Operators</b> AND OR NAND NOR XOR XNOR	&   ~& ~  ^ ^~ or ~^
<b>Conditional Operator</b> conditional	?: