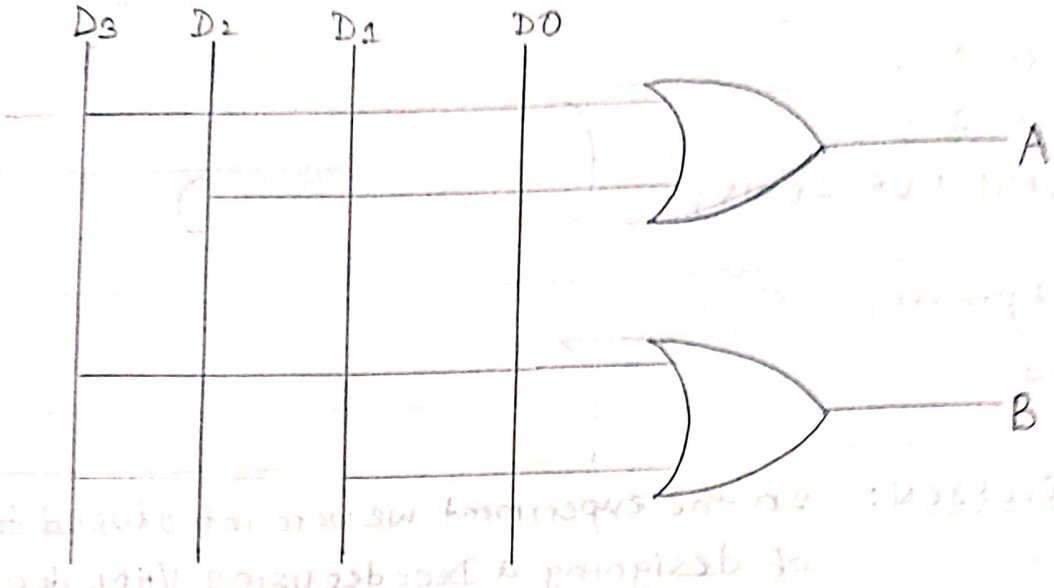
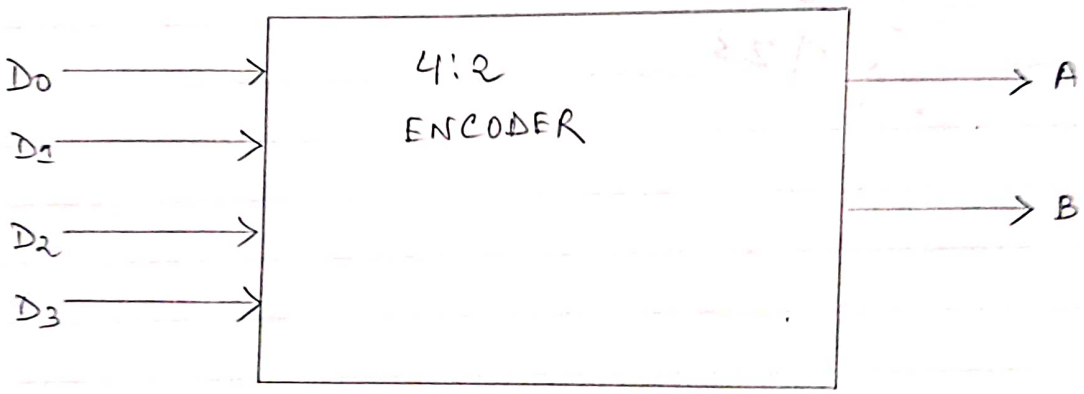



CIRCUIT DIAGRAM OF 4:2 ENCODER




BLOCK DIAGRAM

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# EXPERIMENT NO-11

**TITLE:** Design of Encoder using VHDL Code

**OBJECTIVE:** To design a 4:2 Encoder using VHDL CODE

**Software Used:-** Xilinx ISE Project Navigator

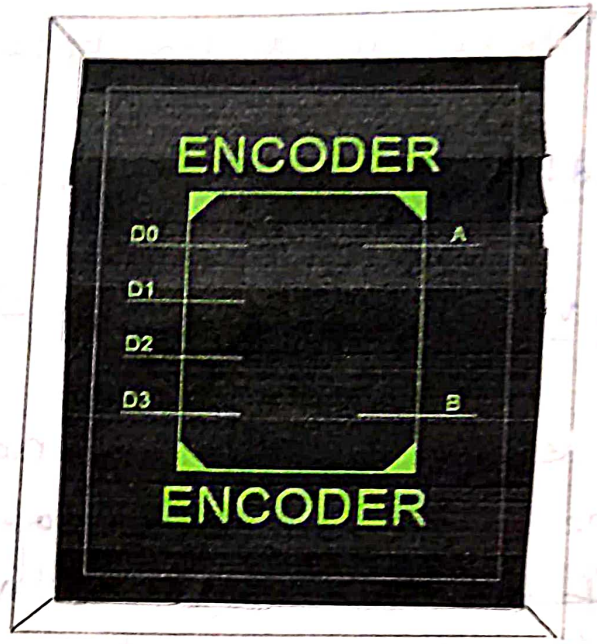
**Software Tools used:-** ISE 14.7 Simulator

**THEORY:-** An encoder is a combinational circuit that performed the reverse operation of Decoder. It has maximum of $2^n$ input lines and 'n' output lines, A $2^n$ to n encoder has n number of transmission lines and can be compared to a multiplexer. Only one of the inputs become 'high' at a time.

## Truth Table for 4:2 Encoder.

| INPUT | | | | OUTPUT | |
|---|---|---|---|---|---|
| $D_3$ | $D_2$ | $D_1$ | $D_0$ | A | B |
| 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 |

Teacher's Signature .....


ENCODER
D0
D1
D2
D3
A
B
ENCODER

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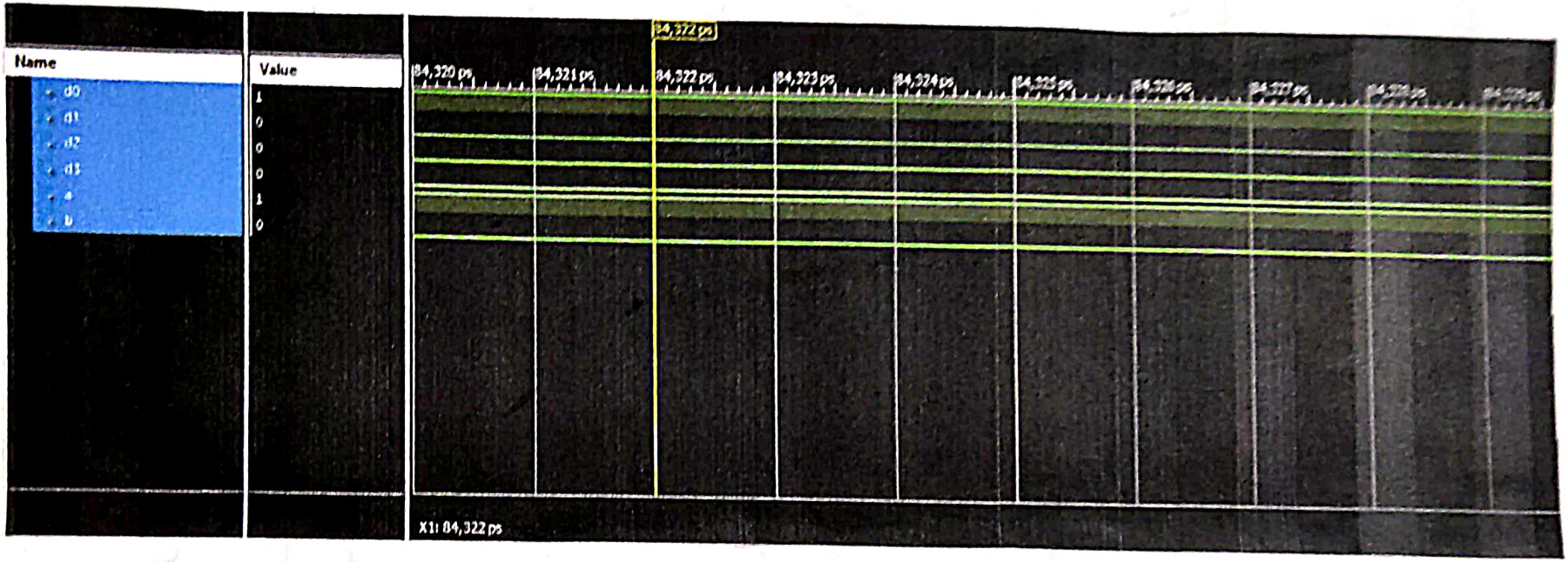
## VHDL CODE for 4:2 ENCODER

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity ENCODER is
    Port ( A: out STD_LOGIC;
           B: out STD_LOGIC;
           D0: in STD_LOGIC;
           D1: in STD_LOGIC;
           D2: in STD_LOGIC;
           D3: in STD_LOGIC);
end ENCODER;
architecture Behavioral of ENCODER is

begin
A<= D0 OR D1;
B<= D2 OR D3;

end Behavioral;
```

OXFORD

Teacher's Signature .....


Name
Value
d0
d1
d2
d3
a
b
1
0
0
0
1
0
84,320 ps
84,321 ps
84,322 ps
84,323 ps
84,324 ps
X1: 84,322 ps

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# VHDL TESTBENCH CODE for 4:2 ENCODER.

```
LIBRARY ieee;
use ieee.std_logic_1164.ALL
use ieee.std_logic_ARITH.ALL
use ieee.std_logic_unsigned.ALL

ENTITY ENCODER_TESTBENCH IS
END ENCODER_TESTBENCH;

ARCHITECTURE behavior OF ENCODER_TESTBENCH IS

  COMPONENT ENCODER
  PORT (
        A : OUT std_logic;
        B : OUT std_logic;
        D0 : IN std_logic;
        D1 : IN std_logic;
        D2 : IN std_logic;
        D3 : IN std_logic
    );
END COMPONENT;
```

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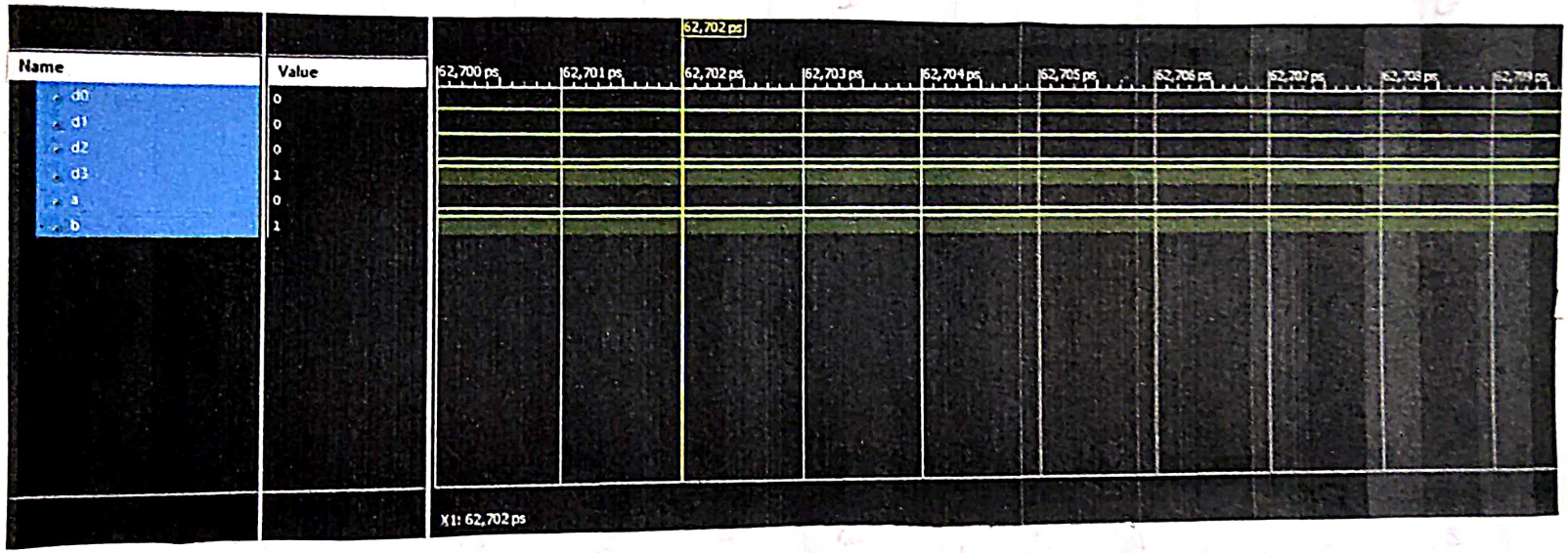
Name
Value
d0
d1
d2
d3
a
b
0
0
0
1
0
1
62,702 ps
62,700 ps
62,701 ps
62,702 ps
62,703 ps
62,704 ps
62,705 ps
62,706 ps
62,707 ps
62,708 ps
62,709 ps
X1: 62,702 ps

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```
signal D0: std_logic := '0';
signal D1: std_logic := '0';
signal D2: std_logic := '0';
signal D3: std_logic := '0';

signal A: std_logic;
signal B: std_logic;

BEGIN
   uut: ENCODER PORT MAP (
          A => A,
          B => B,
          D0 => D0,
          D1 => D1,
          D2 => D2,
          D3 => D3
       );
stim_proc: process
begin
    D0 <= '1';
    D1 <= '0';
    D2 <= '0';
    D3 <= '0';
    WAIT FOR 20 NS;
```

OXFORD©

Teacher's Signature .....

```
D0 <= '0';
D1 <= '1';
D2 <= '0';
D3 <= '0';
WAIT FOR 20NS;
D0 <= '0';
D1 <= '0';
D2 <= '1';
D3 <= '0';
WAIT FOR 20NS;
D0 <= '0';
D1 <= '0';
D2 <= '0';
D3 <= '1';
WAIT FOR 20NS;
end process;
END;
```

CONCLUSION: IN this experiment we are introduced to procedure of designing a Encoder using VHDL. Encoder being a combinational circuit. we have to use the statement in VHDL. We also have written the corresponding VHDL Test Bench and successfully verified the simulation result with the help of truth table.



Teacher's Signature .....