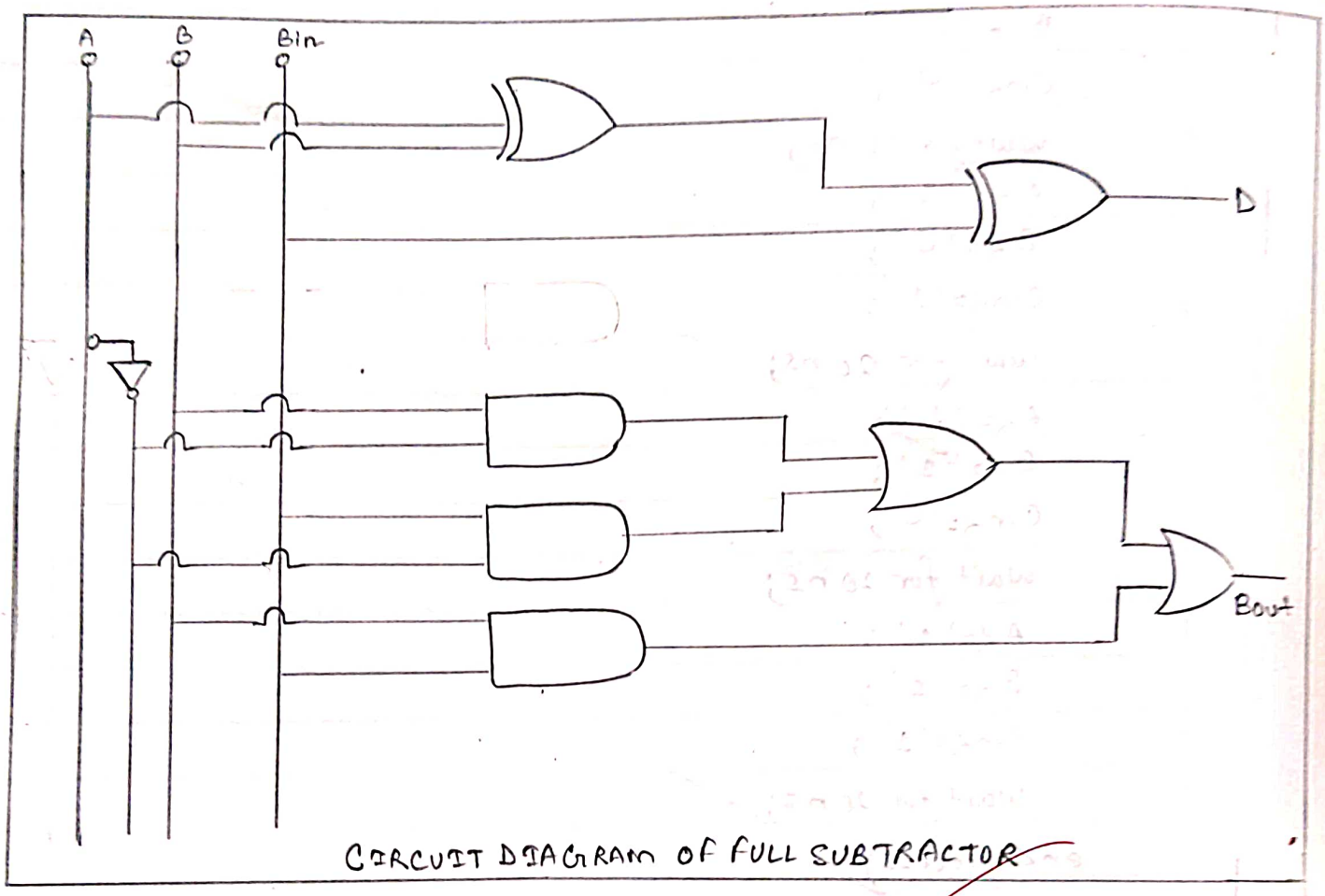

CIRCUIT DIAGRAM OF FULL SUBTRACTOR

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Date./ 23/03/23

EXPERIMENT NO: 8

TITLE: Design of Full Subtractor using VHDL Code

OBJECTIVE: To design a full subtractor using VHDL code

Software Used: Xilinx · ISE Project Navigator

Software tools used: ISE 14.7 simulator

THEORY: A full Subtractor is a combinational circuit that perform subtraction of two bits, one is minvend & other is subtratend, taking into account borrow of the previous adjacent lower minvend bit. The circuit has three input & two output. The three inputs A, B & Bin, denoted the minvend, subtractend & previous borrow, respectively. The two outputs, D & Bout represent the difference & output borrow respectively.

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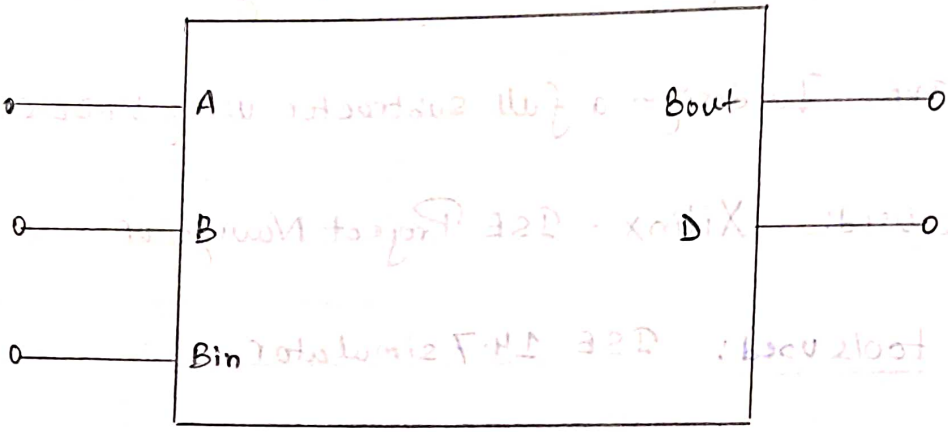

BLOCK DIAGRAM OF FULL SUBTRACTOR

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Truth Table of Full Subtractor

INPUT			OUTPUT	
A	B	Bin	Bout	D
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

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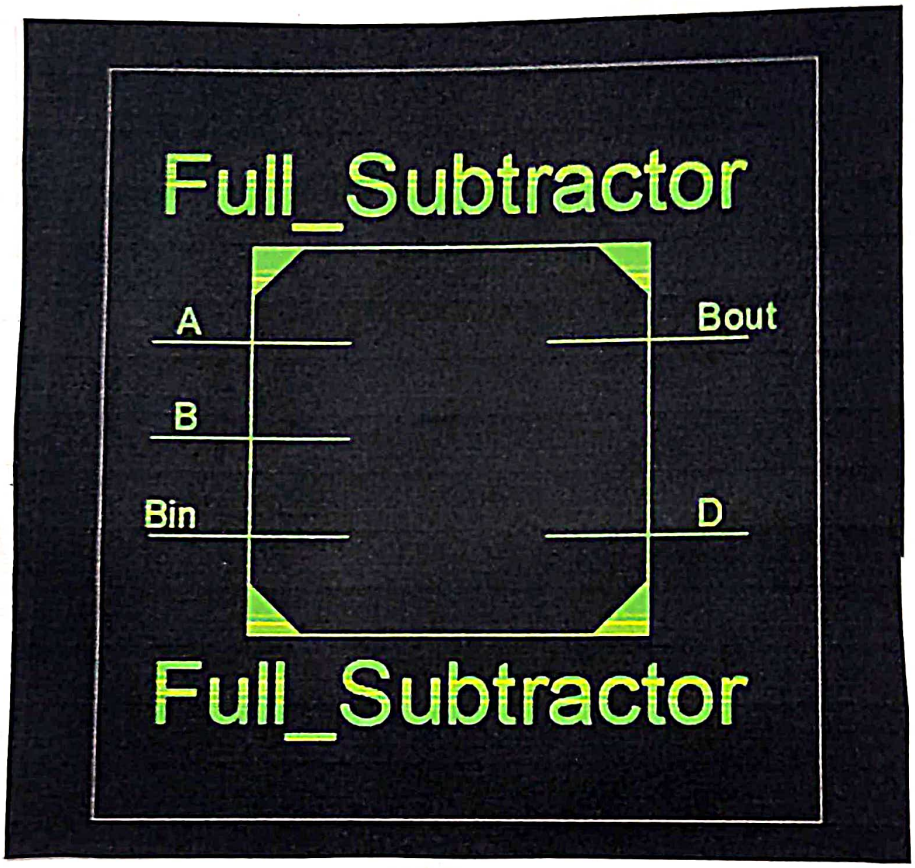
Full_Subtractor
A
B
Bin
Bout
D
Full_Subtractor

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VHDL CODE for FULL SUBTRACTOR

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity full_subtractor is
    Port ( A : in STD_LOGIC;
           B : in STD_LOGIC;
           Bin : in STD_LOGIC;
           Bout : out STD_LOGIC;
           D : out STD_LOGIC);
end full_subtractor;

architecture Behavioral of full_subtractor is

begin
D <= A XOR B XOR Bin;
Bout <= ((B XOR Bin) AND (NOT A)) OR (B AND Bin);
end Behavioral;
```

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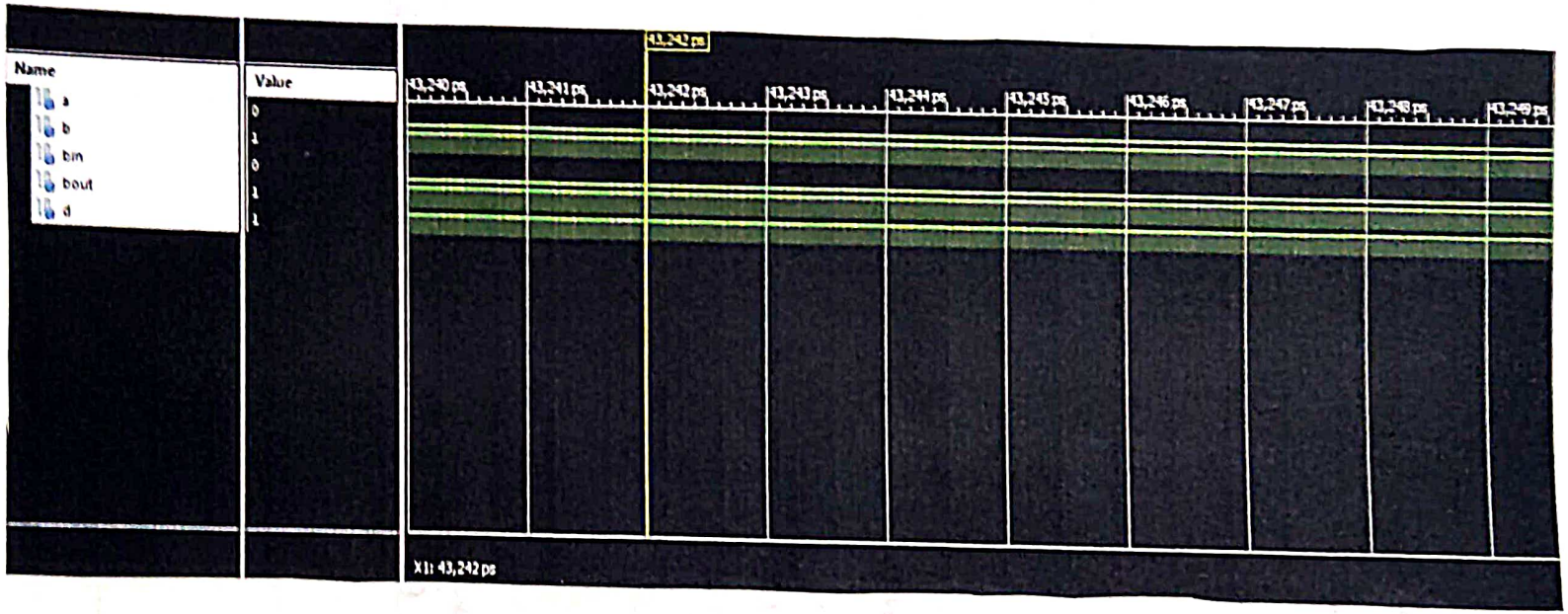
Name
a
b
bin
bout
d
Value
0
1
0
1
1
43,242 ps
43,240 ps
43,241 ps
43,242 ps
43,243 ps
43,244 ps
43,245 ps
43,246 ps
43,247 ps
43,248 ps
43,249 ps
X1: 43,242 ps

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VHDL TESTBENCH CODE for FULL SUBTRACTOR

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY Sub_Testbench IS
END Sub_Testbench;

ARCHITECTURE behavior OF Sub_Testbench IS
    COMPONENT Full_Subtractor
    PORT (
        A: IN std_logic;
        B: IN std_logic;
        Bin: IN std_logic;
        Bout: OUT std_logic;
        D: OUT std_logic
    );
    END COMPONENT;
signal A: std_logic := '0';
signal B: std_logic := '0';
signal Bin: std_logic := '0';
signal Bout: std_logic;
signal D: std_logic;

BEGIN
    uut: full_Subtractor PORTMAP(
```

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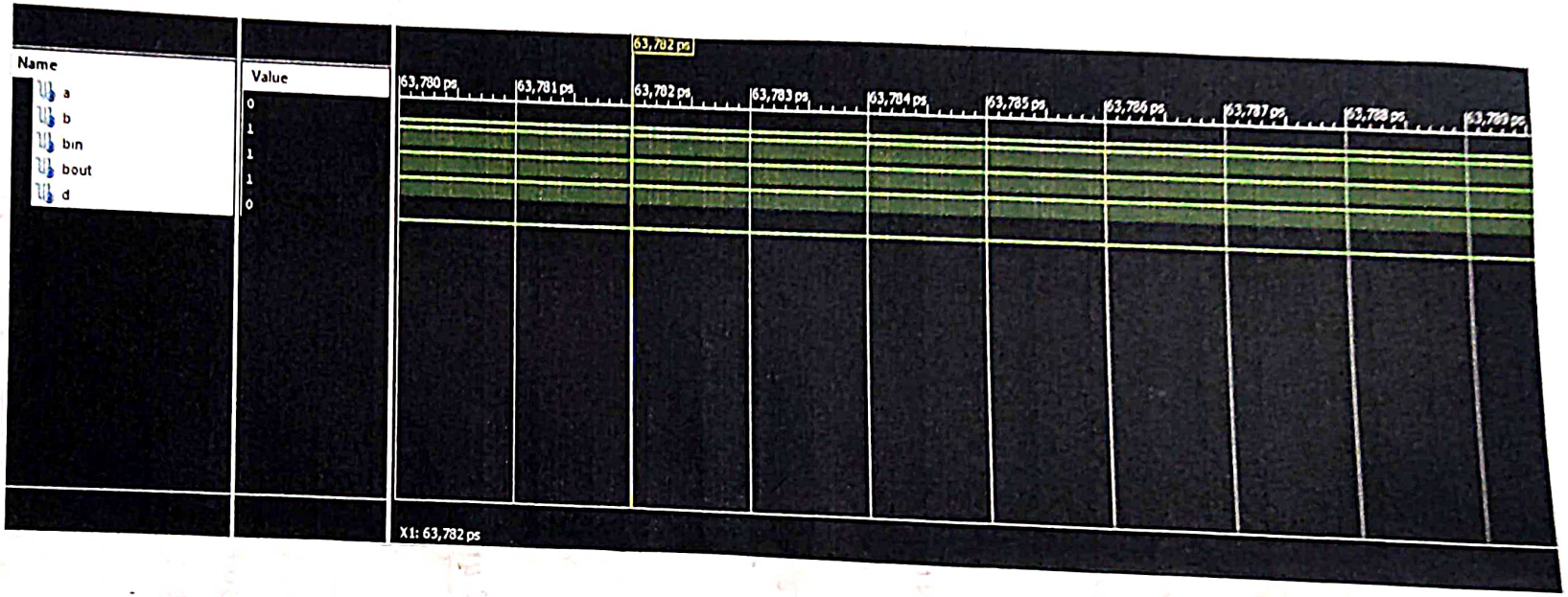
Name
a
b
bin
bout
d
Value
0
1
1
1
0
63,780 ps
63,781 ps
63,782 ps
63,783 ps
63,784 ps
63,785 ps
63,786 ps
63,787 ps
63,788 ps
63,789 ps
X1: 63,782 ps

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```
A => A,
B => B,
Bin => Bin,
Bout => Bout,
D => D
);

stim_proc: process
begin
A <= '0';
B <= '0';
Bin <= '0';
wait for 20 ns;
A <= '0';
B <= '0';
Bin <= '1';
wait for 20 ns;
A <= '0';
B <= '1';
Bin <= '0';
wait for 20 ns;
A <= '0';
B <= '1';
Bin <= '1';
wait for 20 ns;
A <= '1';
B <= '0';
```

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```
Bin<='0';
wait for 20 ns;
A<='1';
B<='0';
Bin<='1';
wait for 20 ns;
A<='1';
B<='1';
Bin<='0';
wait for 20 ns;
A<='1';
B<='1';
Bin<='1';
wait for 20 ns;
    end process;
END;
```

CONCLUSION: In this experiment we were introduced with the procedure of designing a full subtractor using VHDL logic in this experiment. We also have written the corresponding VHDL testbench & successfully verified the simulation result with the help of truth table.

4/4/23

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