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EXPERIMENT NO-13

TITLE: Design of Arithmetic-Logic Unit (ALU) using VHDL CODE

OBJECTIVE: To design a Arithmetic-logic Unit (ALU) using VHDL CODE

Software Used: Xilinx ISE Project Navigator

Software tools used: ISE 14.7 Simulator

THEORY: An arithmetic logic Unit (ALU) is a combinational digital circuit that performs, arithmetic and bitwise operations on integer binary numbers. This is in contrast to a floating point unit, which operates on floating point numbers, it is a fundamental building block of many types of computing circuits, including the central processing Unit (CPU) of computer, FPUs and graphis processing Unit (GPUs)

The inputs to an ALU are the data to be operated on called operands and a code indicating the operation to be performed. The ALU's output is the result of performed operation

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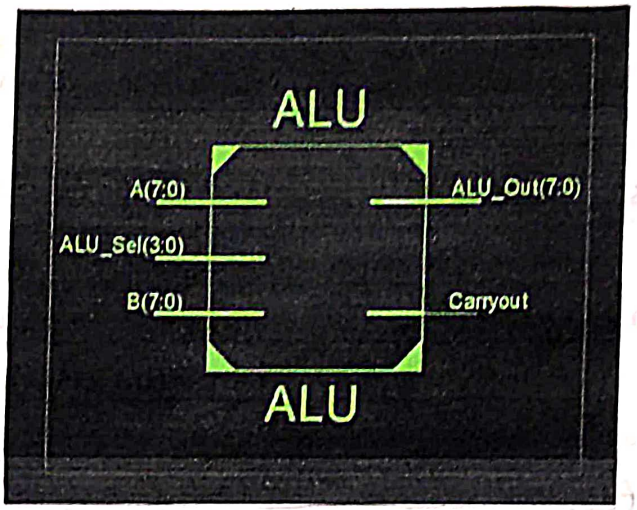
ALU
A(7:0)
ALU_Sel(3:0)
B(7:0)
ALU_Out(7:0)
Carryout
ALU

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VHDL CODE for ALU

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
use ieee.Numeric_STD.ALL;

entity ALU is
  generic (
      Constant N: natural := 1
    );
    Port (
      A, B  : in STD_LOGIC_VECTOR (7 downto 0);
      ALU_Sel : in STD_LOGIC_VECTOR (3 downto 0);
      ALU_Out: Out STD_LOGIC_VECTOR (7 downto 0);
      Carryout: OUT Std_logic
    );
end ALU
architecture Behavioral of ALU is

signal ALU_Result: std_logic_vector (7 downto 0);
signal tmp: std_logic_vector (8 downto 0);

begin
    process (A, B, ALU_Sel)
```

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```
begin
  case (ALU_Sel) is
  when "0000" =>
  ALU_Result <= A+B;
  when "0001" =>
  ALU_Result <= A - B;
  when "0010" =>
  ALU_Result <= std_logic_vector(to_unsigned((to_integer(unsigned(A))
                                  * to_integer(unsigned(B))),8));
  when "0010" =>
  ALU_Result <= std_logic_vector(to_unsigned(to_integer(unsigned
                                  (A)) / to_integer(unsigned(B)),8));
  when "0100" =>
  ALU_Result <= std_logic_vector(unsigned(A) sll N);
  when "0101" =>
  ALU_Result <= std_logic_vector(unsigned(A) srl N);
  when "0110" =>
  ALU_Result <= std_logic_vector(unsigned(A) rol N);
  when "0111" =>
  ALU_Result <= std_logic_vector(unsigned(A) ror N);
  when "1000" =>
  ALU_Result <= A and B;
  when "1001" =>
  ALU_Result <= A or B;
  when "1010" =>
  ALU_Result <= A xor B;
```

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```
when "1011" =>
ALU_Result <= A nor B;
when "1100" =>
ALU_Result <= A nand B;
when "1101" =>
ALU_Result <= A xnor B;
when "1110" =>
  if (A>B) then
    ALU_Result <= x"01";
  else
    ALU_Result <= x"00";
  end if;
when "1111" =>
  if (A=B) then
    ALU_Result <= x"01";
  else
    ALU_Result <= x"00";
  end if;
When others => ALU_Result <= A+B
end case;
end process;
ALU_Out <= ALU_Result;
tmp <= ('0' & A) + ('0' & B);
Carryout <= tmp(8);
end Behavioral;
```

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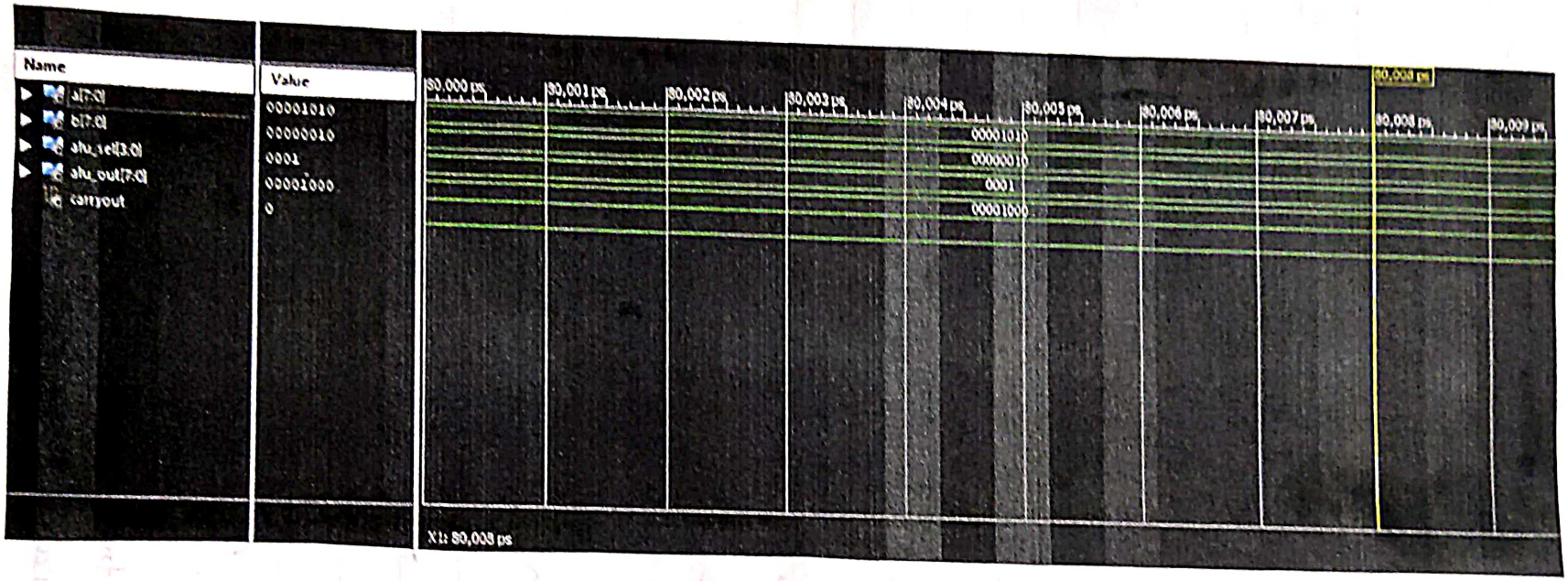
Name
Value
a[7:0]
b[7:0]
alu_sel[3:0]
alu_out[7:0]
carryout
00001010
00000010
0001
00001000
0
80,000 ps
80,001 ps
80,002 ps
80,003 ps
80,004 ps
80,005 ps
80,006 ps
80,007 ps
80,008 ps
80,009 ps
00001010
00000010
0001
00001000
X1: 80,008 ps

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VHDL TESTBENCH CODE for ALU

```
LIBRARY ieee;
use ieee.std_logic_1164.ALL;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_STD.all;

ENTITY tb_ALU IS
END tb_ALU;

ARCHITECTURE behavior OF tb_ALU IS
    COMPONENT ALU
    PORT (
        A: IN Std_logic_vector (7 downto 0);
        B: IN Std_logic_vector (7 downto 0);
        ALU_Sel: IN Std_logic_vector (3 downto 0);
        ALU_Out: OUT Std_logic_vector (7 downto 0);
        Carryout: OUT std_logic_vector
    );
    END COMPONENT;

Signal A: std_logic_vector (7 downto 0) := (others => '0');
Signal B: Std_logic_vector (7 downto 0) := (others => '0');
Signal ALU_sel: Std_logicvector(3 downto 0) := (others => '0');
```

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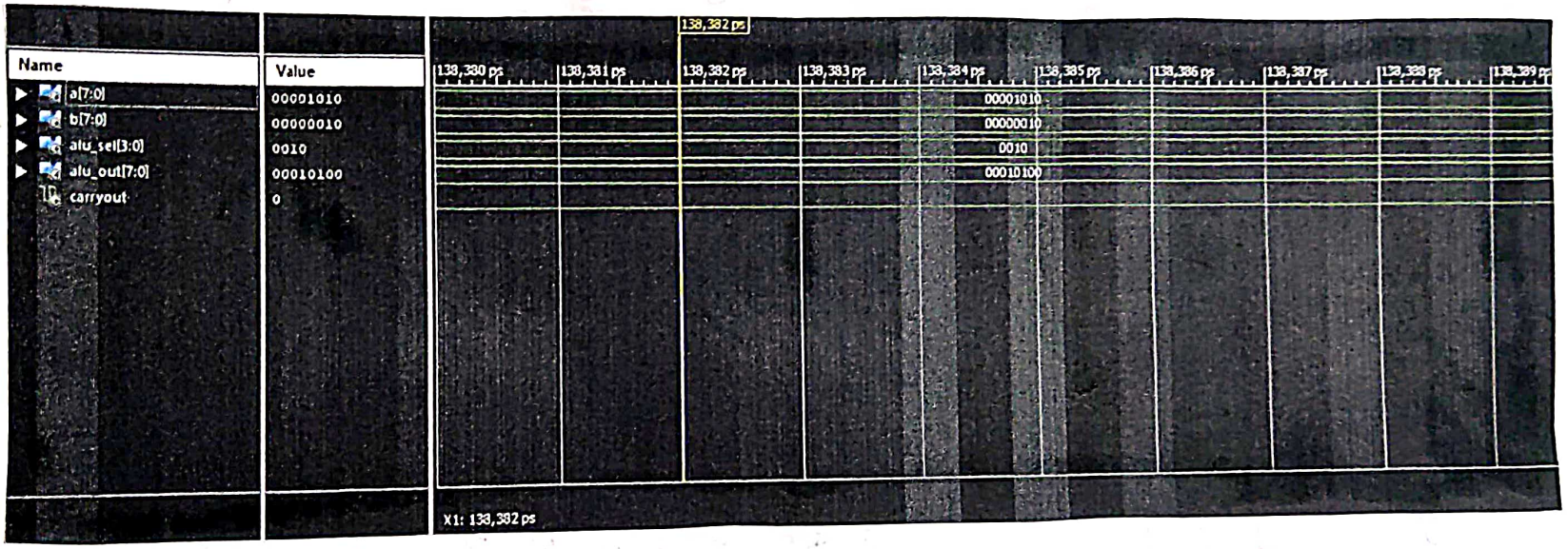
Name
Value
a[7:0]
00001010
b[7:0]
00000010
alu_sel[3:0]
0010
alu_out[7:0]
00010100
carryout
0
138,382 ps
138,380 ps
138,381 ps
138,382 ps
138,383 ps
138,384 ps
138,385 ps
138,386 ps
138,387 ps
138,388 ps
138,389 ps
00001010
00000010
0010
00010100
X1: 138,382 ps

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```
signal ALU_Out: std_logic_vector(7 downto 0);
signal Carryout: std_logic;

signal i: integer;

BEGIN
    uut: ALU PORT MAP(
            A => A,
            B => B,
            ALU_Sel => ALU_Sel,
            ALU_Out => ALU_Out,
            Carryout => Carryout
        );

stim_proc: process
begin
    A <= x"0A";
    B <= x"02";
    ALU_Sel <= x"0";
    for i in 0 to 15 loop
        ALU_Sel <= ALU_sel + x"1";
        wait for 100 ns;
    end loop
            A <= x"F6";
            B <= x"0A";
```

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wait;
end process;
END;

CONCLUSION: In this experiment we are introduced to procedure of designing a Arithmetic Logic Unit (ALU) using VHDL. ALU is a combinational digital circuit. We have to use the Statement in VHDL. We also have written the corresponding Test Bench and successfully verified the Simulation result with help of Truth Table.

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