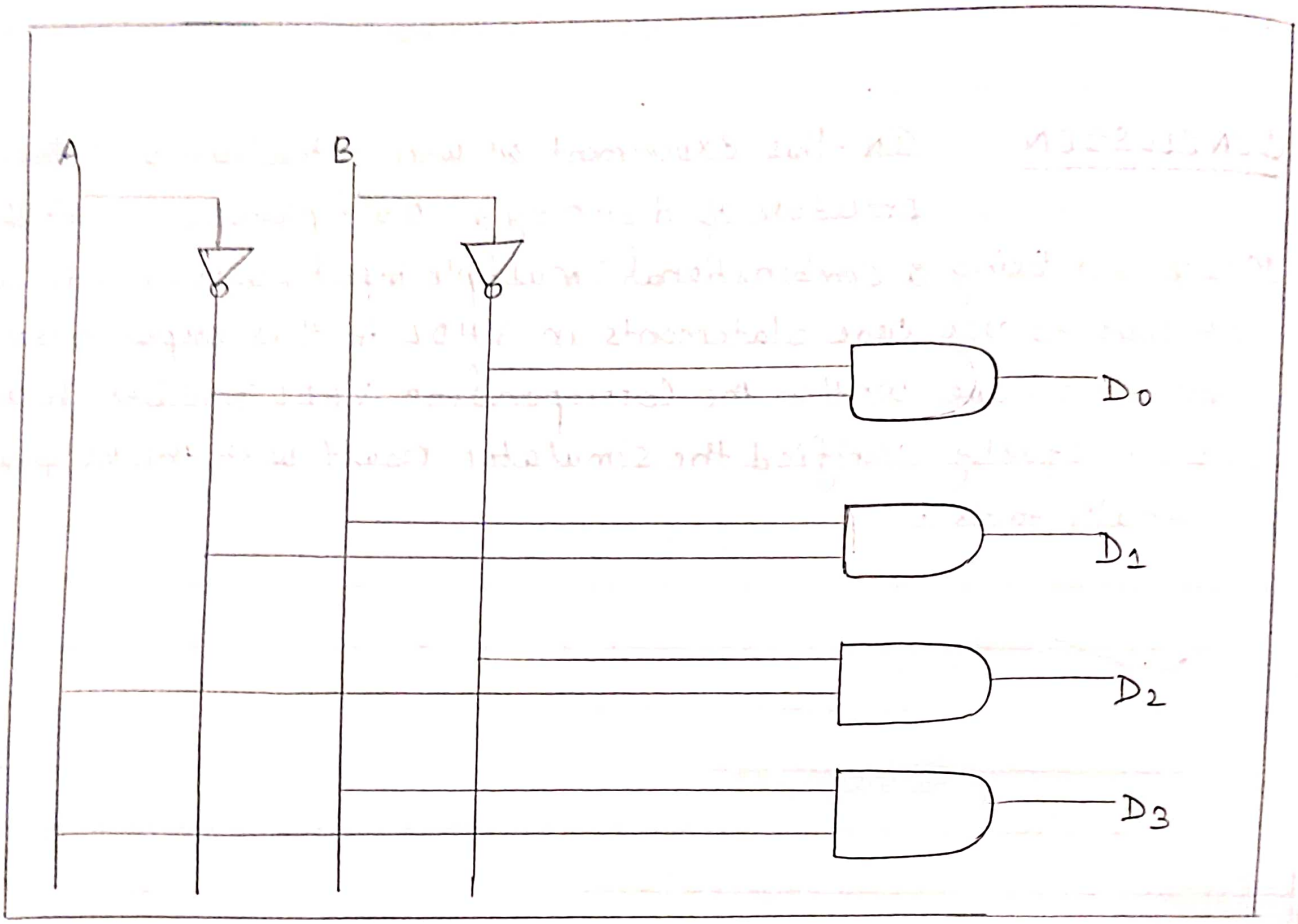

2:4 DECODER CIRCUIT

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EXPERIMENT NO:- 10

TITLE: Design of Decoder using VHDL code

OBJECTIVE: To design a 2:4 Decoder using VHDL code.

Software Used: Xilinx ISE Project Navigator

Software Tools used:- ISE 14.7 Simulator

THEORY: Decoder is a combinational logic circuit that converts binary information from the n coded input to a minimum 2^n unique output. A Binary Decoder will convert binary information from 2^n output signals for n number of input signal. Some Decoder in such cases, at least one output pattern will be repeated for different input values.

In this type of Decoders, decoders have two inputs name a, b and four outputs denoted by D_0, D_1, D_2, D_3.

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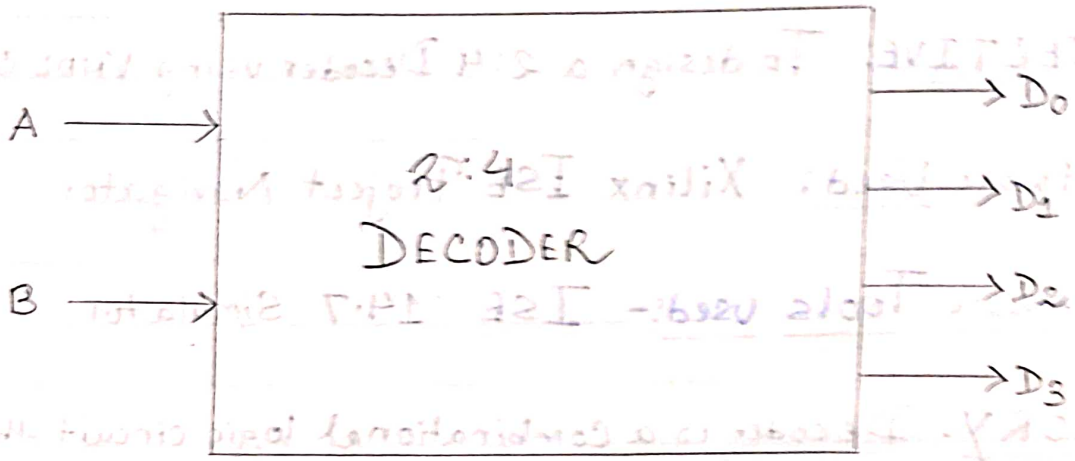

BLOCK DIAGRAM

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Truth Table for 2:4 Decoder

INPUT		OUTPUT			
A	B	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

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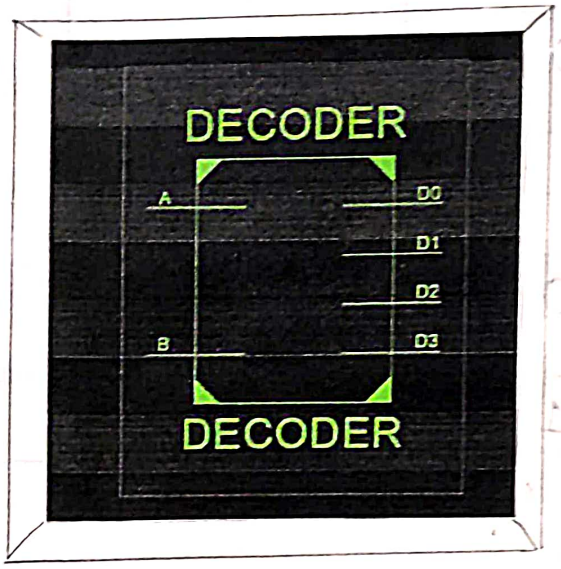
DECODER
A
B
D0
D1
D2
D3
DECODER

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VHDL CODE for 2:4 DECODER

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity DECODER is
    Port ( A: in STD_LOGIC;
           B: in STD_LOGIC;
           D0, D1, D2, D3: out STD_LOGIC);
end DECODER;

architecture Behavioral of DECODER is

begin

D0 <= (NOT A) AND (NOT B);
D1 <= (NOT A) AND (B);
D2 <= (A) AND (NOT B);
D3 <= (A) AND (B);

end Behavioral;
```

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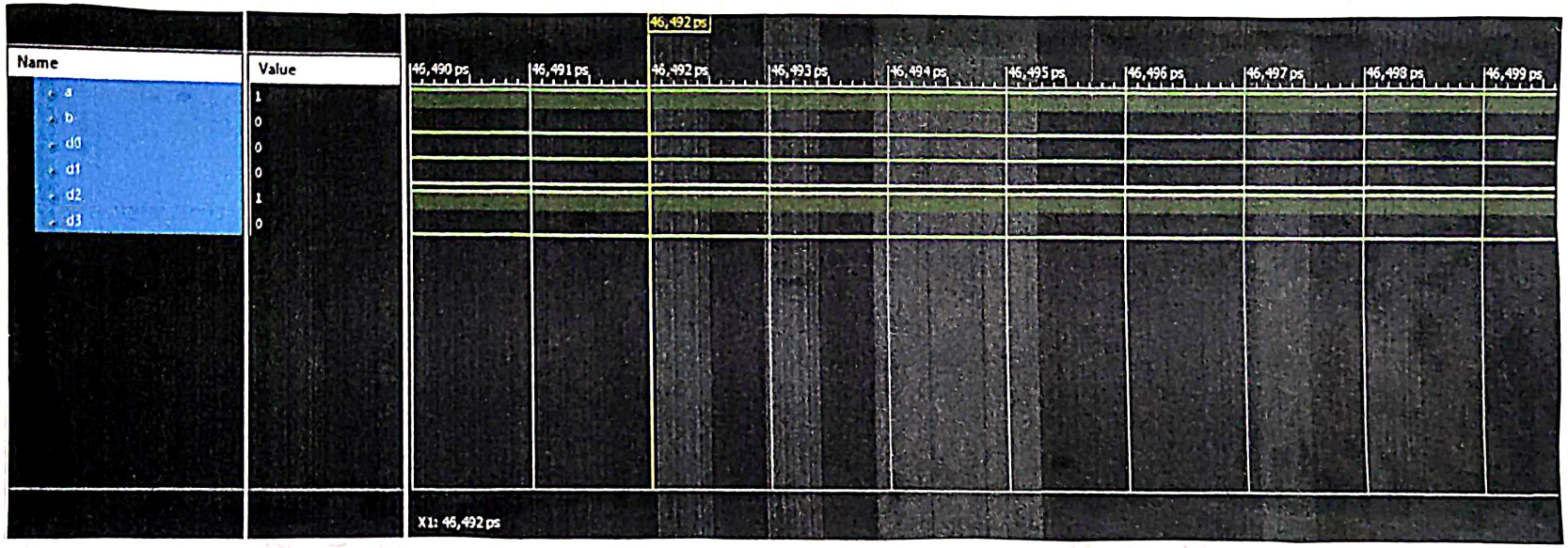
Name
a
b
d0
d1
d2
d3
Value
1
0
0
0
1
0
46,492 ps
46,490 ps
46,491 ps
46,492 ps
46,493 ps
46,494 ps
46,495 ps
46,496 ps
46,497 ps
46,498 ps
46,499 ps
X1: 46,492 ps

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VHDL TESTBENCH for 2:4 DECODER

```
LIBRARY ieee;
use ieee.std_logic_1164.ALL;
use ieee.std_logic_unsigned.ALL;
use ieee.std_logic_arith.ALL;

ENTITY DECODER_TESTBENCH IS
END DECODER_TESTBENCH

ARCHITECTURE behavior OF DECODER_TESTBENCH IS
COMPONENT DECODER
PORT (
        A: IN std_logic;
        B: IN std_logic;
        D0: OUT std_logic;
        D1: OUT std_logic;
        D2: OUT std_logic;
        D3: OUT std_logic;
    );
END COMPONENT;

    signal A: std_logic := '0';
    signal B: std_logic := '0';
```

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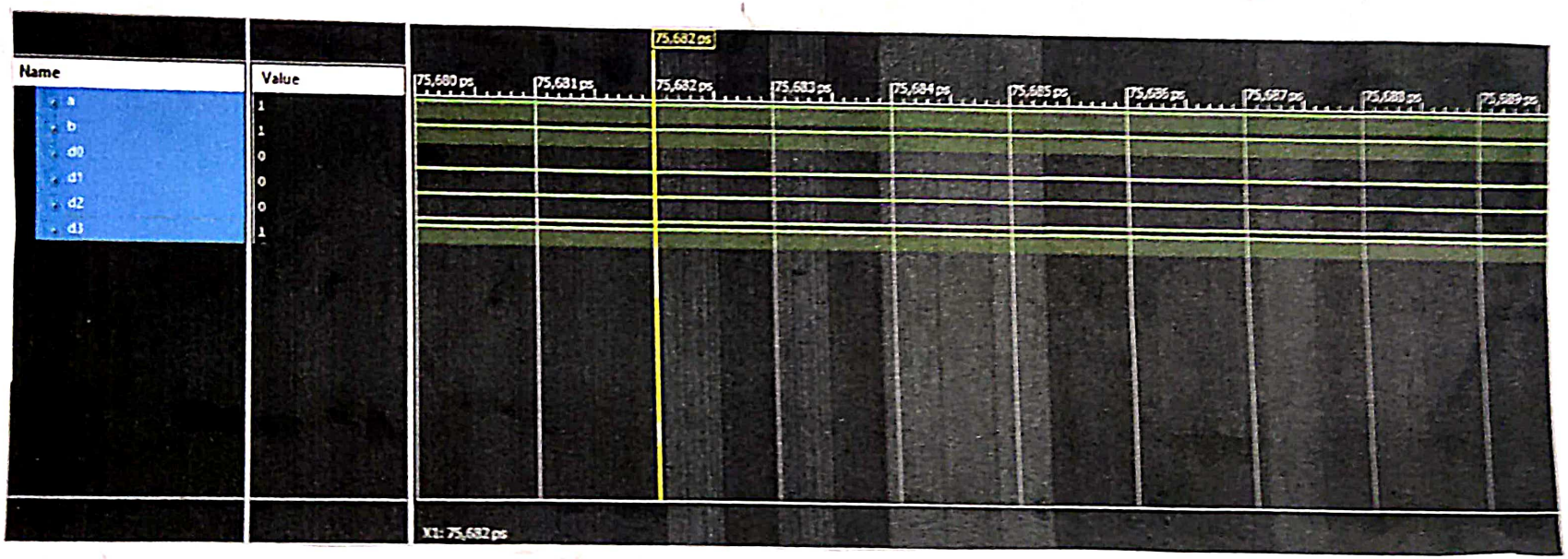
Name
Value
a
b
d0
d1
d2
d3
1
1
0
0
0
1
75,682 ps
75,680 ps
75,681 ps
75,682 ps
75,683 ps
75,684 ps
75,685 ps
75,686 ps
75,687 ps
75,688 ps
75,689 ps
X1: 75,682 ps

```
signal D0 : std_logic := '0';
signal D1 : std_logic := '0';
signal D2 : std_logic := '0';
signal D3 : std_logic := '0';

BEGIN
    uut : DECODER PORT MAP (
            A => A,
            B => B,
            D0 => D0,
            D1 => D1,
            D2 => D2,
            D3 => D3
        );
stim_proc : process
 begin
    A <= '0';
    B <= '0';
    WAIT FOR 20 NS;
    A <= '0';
    B <= '1';
    WAIT FOR 20 NS;
    A <= '1';
    B <= '0';
    WAIT FOR 20 NS;
```

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```
A <= '1';
B <= '1';
WAIT FOR 20 NS;

end process;
END;
```

CONCLUSION: In the experiment we were introduced to procedure of designing a Decoder using VHDL decoder being a combinational circuit we have to use the statement in VHDL. IN this experiment we have written the corresponding VHDL Test Bench and successfully verified the simulation result with the help of truth table.

29/5/23

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