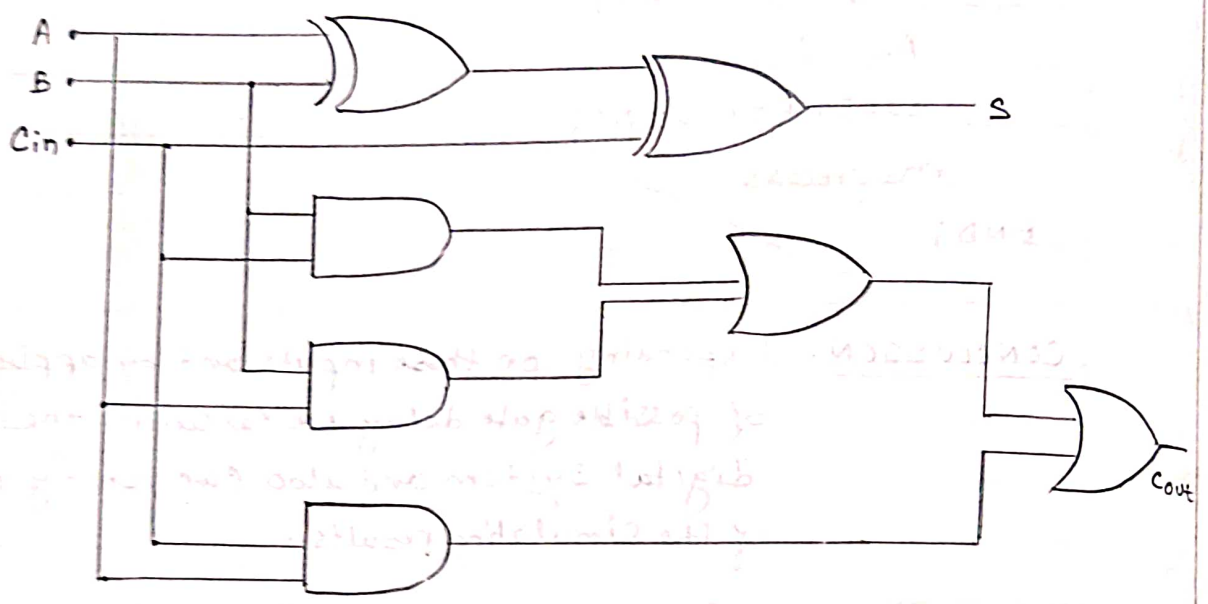

CIRCUIT DIAGRAM OF FULL ADDER

Expt.No.

Page No./ 24
Date./16/03/23

EXPERIMENT No: 7

TITLE: Design of Full Adder using VHDL Code

OBJECTIVE: To design a full adder using VHDL code

Software used: Xilinx ISE Project Navigator

Software tools used: ISE 14.7 Simulator

THEORY: A full adder is a combinational circuit that performed the arithmetic sum of 3 inputs bits. It consist of 3 inputs & 2 output. Those of the input variables can be defined as A, B, C i.e & the two output vaciables can be defined earlier Cout & B. The two input variable that are defined earlier A & B represent the carry bit. The 2 input significant bits to be added. The 3rd input Cin represent the carry bit. We have to use two digit because the arithmetic sum of the 3 binary digits needs two digits. The two output represent for sum & cost for carry.

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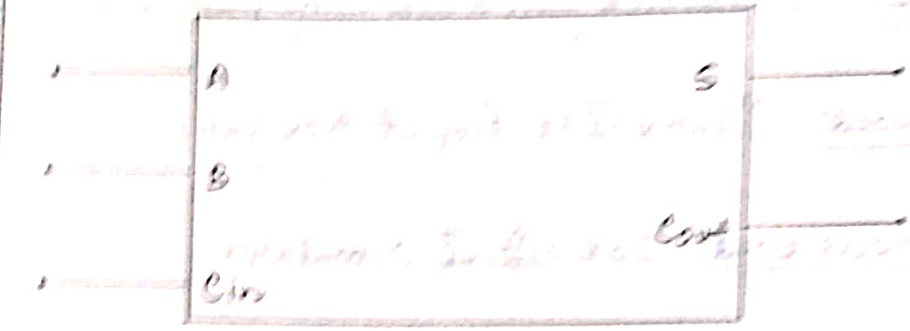

BLOCK DIAGRAM OF FULL ADDER

Expt.No.

Page No. 25
Date.

Truth Table of FULL ADDER

INPUT			OUTPUT	
A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

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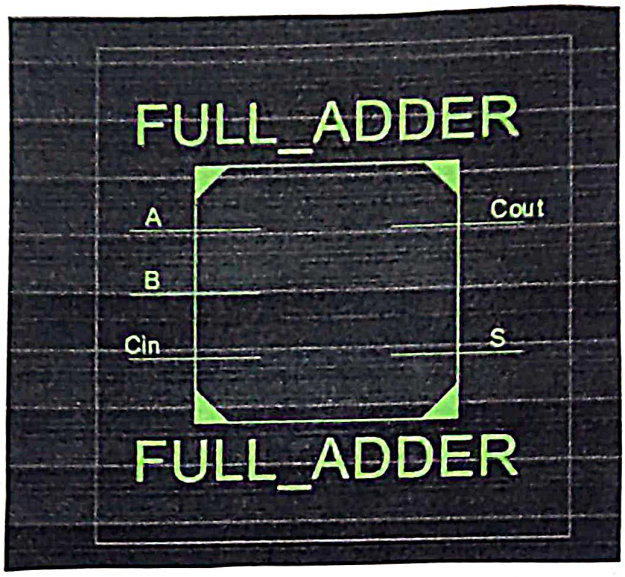
FULL_ADDER
A
B
Cin
Cout
S
FULL_ADDER

Expt.No.

Page No. 26
Date.

VHDL Code for FULL ADDER

```
Library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity FULL_ADDER is
    Port ( A: in STD_LOGIC;
           B: in STD_LOGIC;
           Cin: in STD_LOGIC;
           S: out STD_LOGIC;
           Cout: out STD_LOGIC);
end FULL_ADDER;

architecture Behavioral of FULL_ADDER is

begin
  S <= A XOR B XOR Cin;
  Cout <= ((A AND B) OR (B AND Cin) OR (A AND Cin));

end Behavioral;
```

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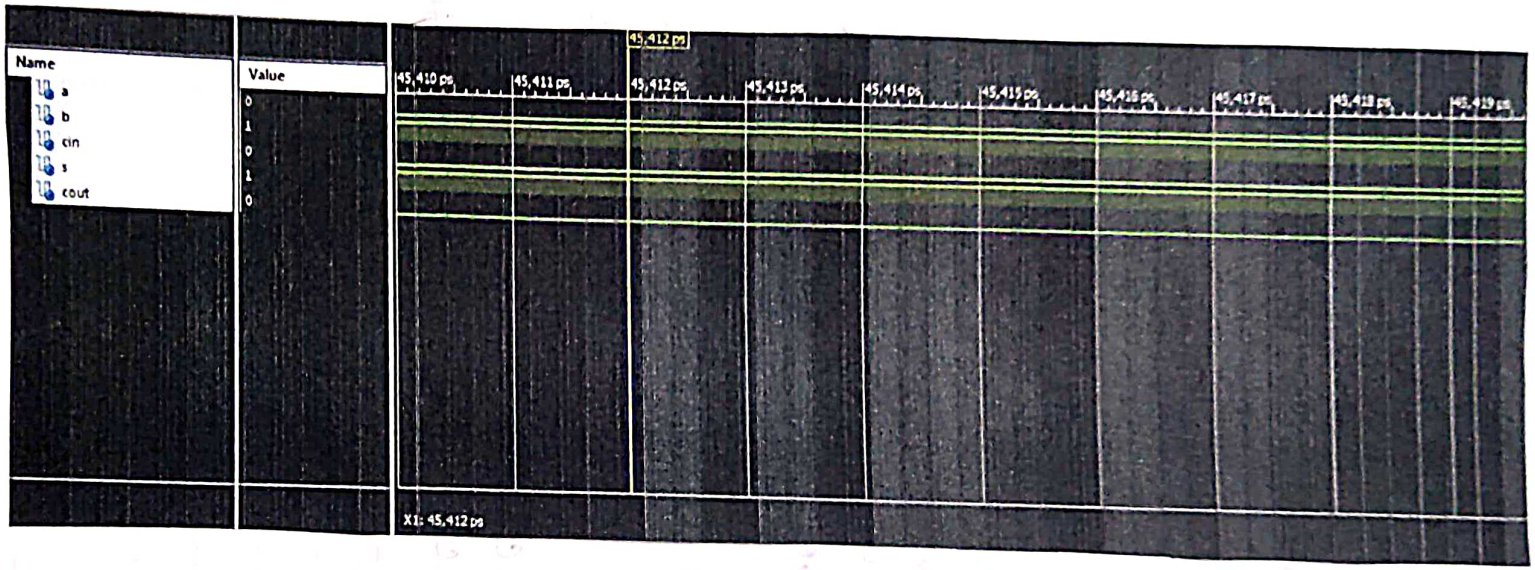
Name
a
b
cin
s
cout
Value
0
1
0
1
0
45,412 ps
45,410 ps
45,411 ps
45,412 ps
45,413 ps
45,414 ps
45,415 ps
45,416 ps
45,417 ps
45,418 ps
45,419 ps
X1: 45,412 ps

Expt.No.

Page No. 27
Date.

VHDL TESTBENCH Code for FULL ADDER :-

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY FULLADDER_TESTBENCH IS
END FULLADDER_TESTBENCH;

ARCHITECTURE behavior OF FULLADDER_TESTBENCH IS
    COMPONENT FULL_ADDER
        PORT (
            A: IN std_logic;
            B: IN std_logic;
            Cin: IN std_logic;
            S : OUT std_logic;
            Cout: OUT std_logic
            );
    END COMPONENT;

    signal A: std_logic := '0';
    Signal B: std_logic := '0';
    Signal Cin: std_logic := '0';
    signal S: std_logic;
    signal Cout: std_logic;
```

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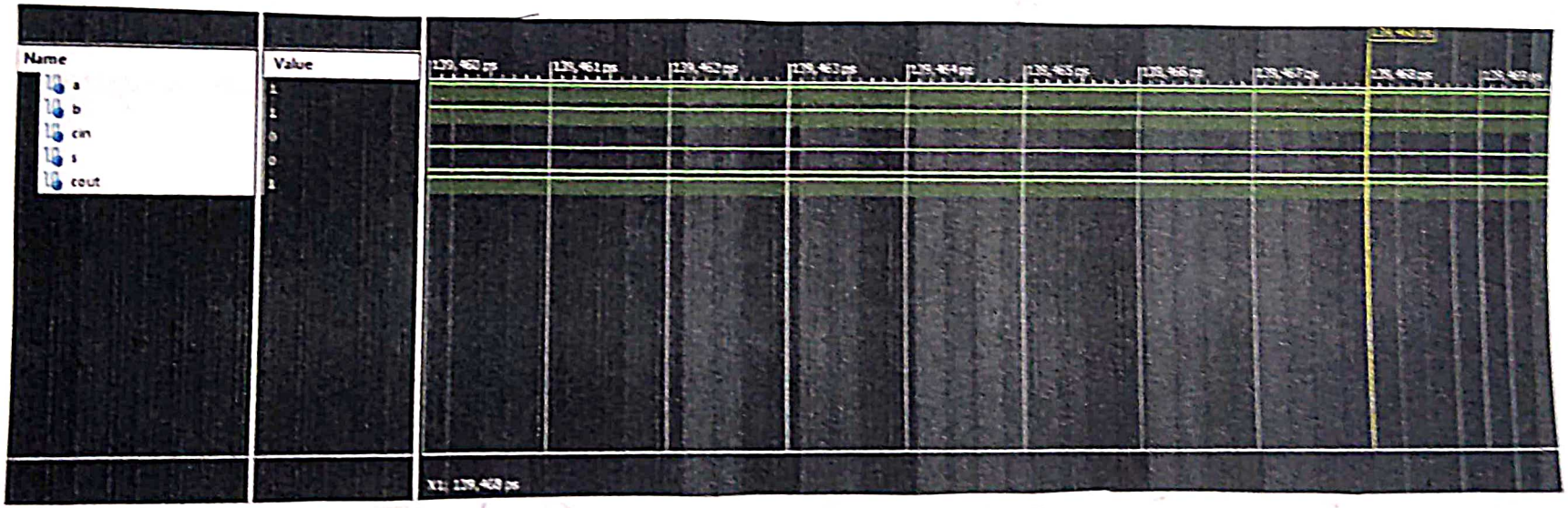
Name
a
b
cin
s
cout
Value
1
1
0
0
1

Expt.No.

Page No. 28
Date.

```
BEGIN
  uut: FULL_ADDER PORT MAP (
                A => A1
                B => B1
                Cin => cin
                S => S1
                Cout => Cout
                );

stim_proc : process
  begin
  A <= '0';
  B <= '0';
  Cin <= '0';
  wait for 20 ns;
  A <= '0' ;
  B <= '0' ;
  Cin <= '1' ;
  wait for 20 ns;
  A <= '0' ;
  B <= '1' ;
  Cin <= '0' ;
  wait for 20 ns
  A <= '0' ;
  B <= '1' ;
  Cin <= '1' ;
```

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```
wait for 20 ns;
A <= '1';
B <= '0';
Cin <= '0';
wait for 20 ns;
A <= '1';
B <= '0';
Cin <= '1';
wait for 20 ns;
A <= '1';
B <= '1';
Cin <= '0';
wait for 20 ns;
A <= '1';
B <= '1';
Cin <= '1';
wait for 20 ns;
end process;
END;
```

CONCLUSION: In this experiment we were introduced with the produce of designing a full adder using VHDL. It is a combinational circuit we have touse the logic in VHDL in this experiment. We also have written the corresponding VHDL Testbench & successfully verified the simulation result with the help of truthtable.

Date 23/3

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