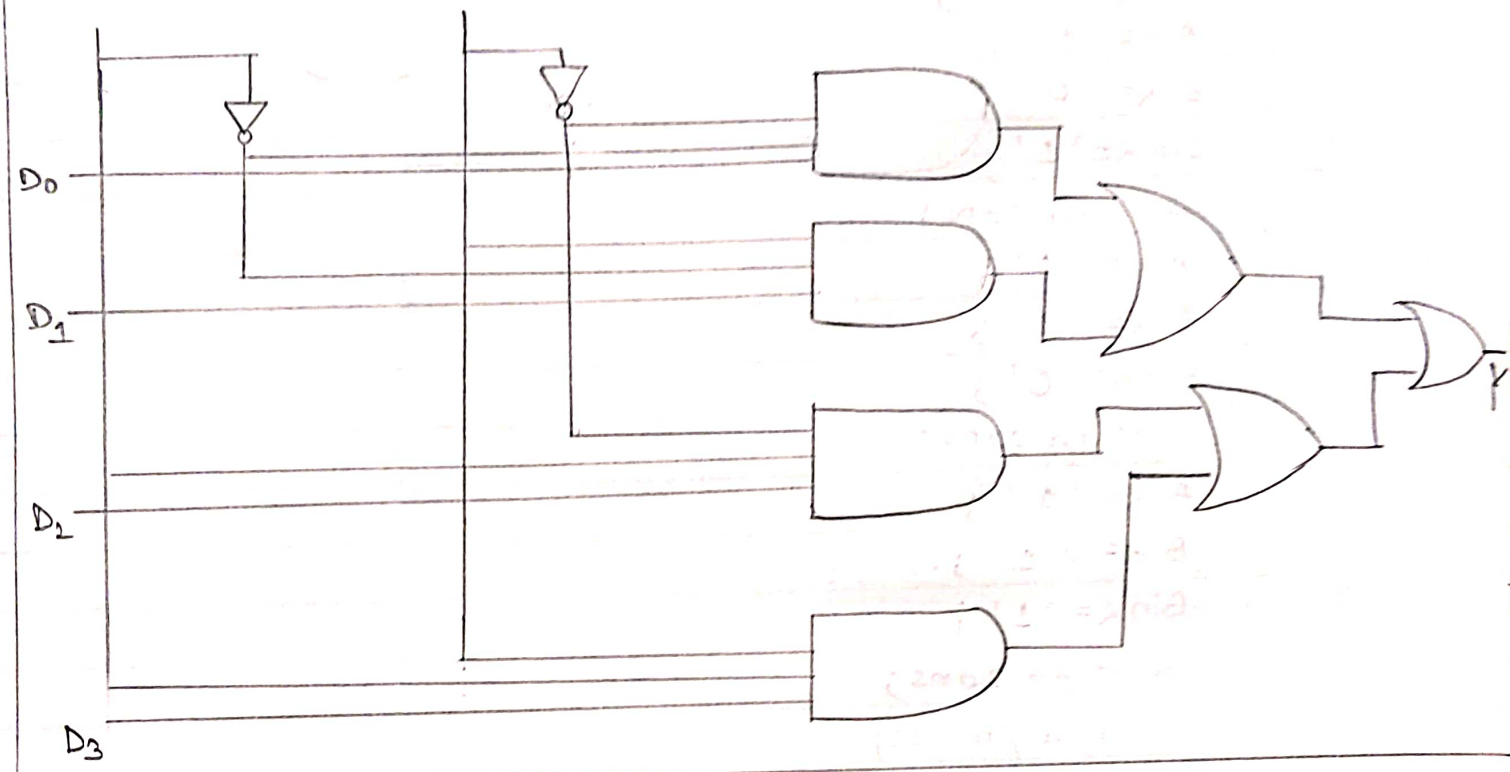

CIRCUIT DIAGRAM OF MULTIPLEXER

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EXPERIMENT NO: 9

TITLE: Design of Multiplexer using VHDL code.

OBJECTIVE: To design a 4:1 multiplexer using VHDL code.

Software used: Xilinx ISE Project Navigator

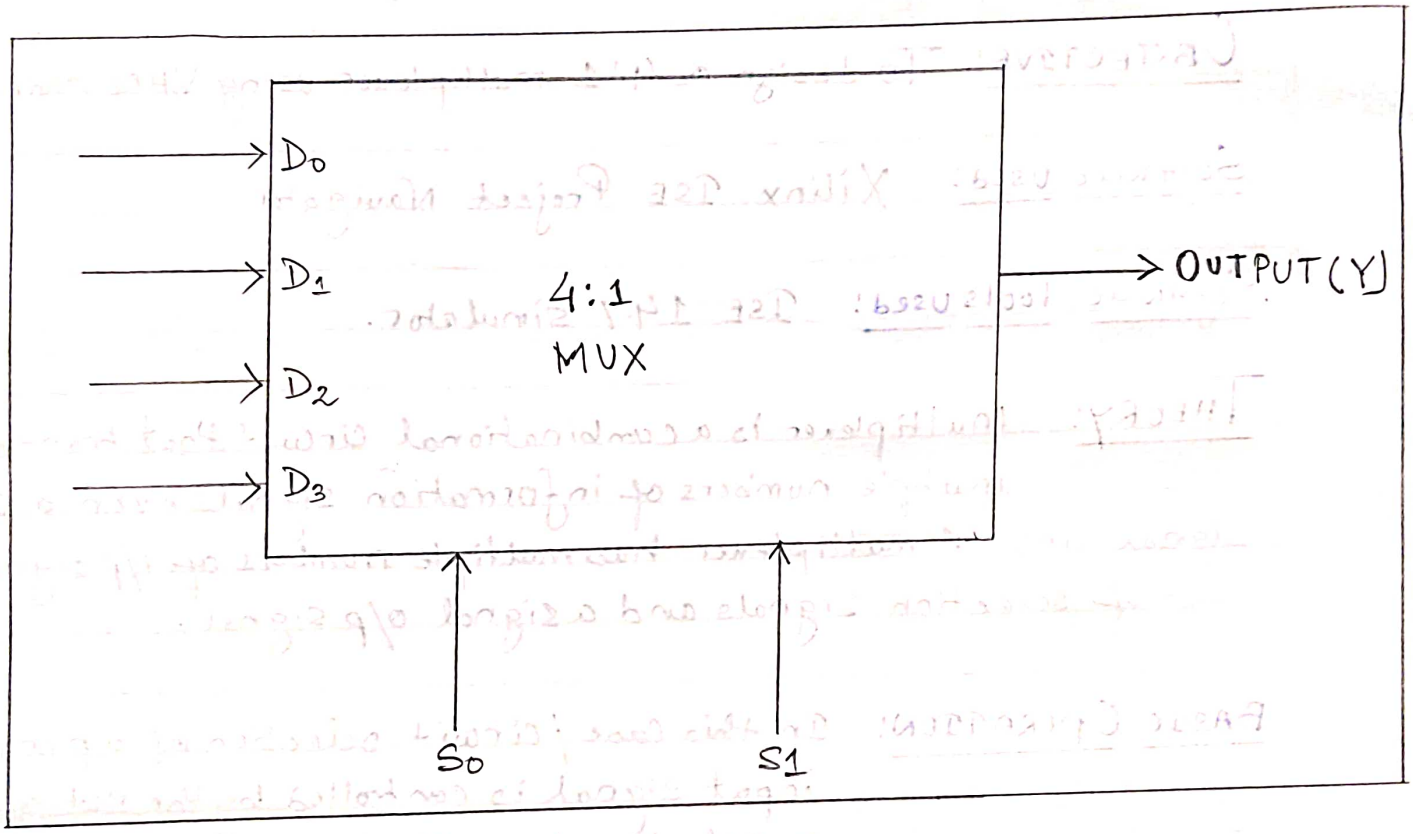
Software Tools used: ISE 14.7 simulator.

THEORY: Multiplexer is a combinational circuit that transmits multiple numbers of information signals over a single signal line. A multiplexer has multiple numbers of i/p signals set of selection signals and a signal o/p signal.

BASIC OPERATION: In this case / circuit selection of a particular input signal is controlled by the set of i/p signals given through selection lines. Since there are 2 Select lines then they can have 2^2 i.e 4 possible combinations & thus they can identify 4 i/p lines. The o/p at any line is dependent on input line given to the selection lines as well as on corresponding 'selected' i/p line.

OXFORD

Teacher's Signature .....



BLOCK DIAGRAM OF 4:1 MULTIPLEXER

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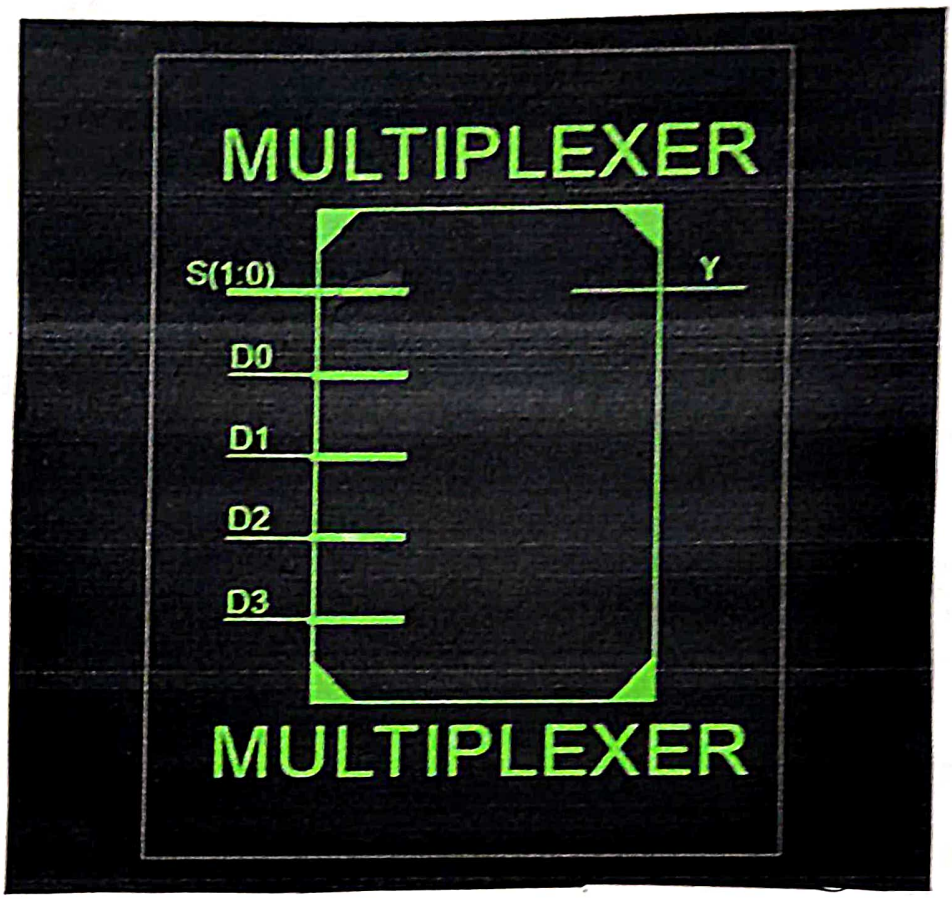
Truth Table for 4:1 Multiplexer

INPUT		OUTPUT
S_0	S_1	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

Teacher's Signature .....


MULTIPLEXER
S(1:0)
Y
D0
D1
D2
D3
MULTIPLEXER

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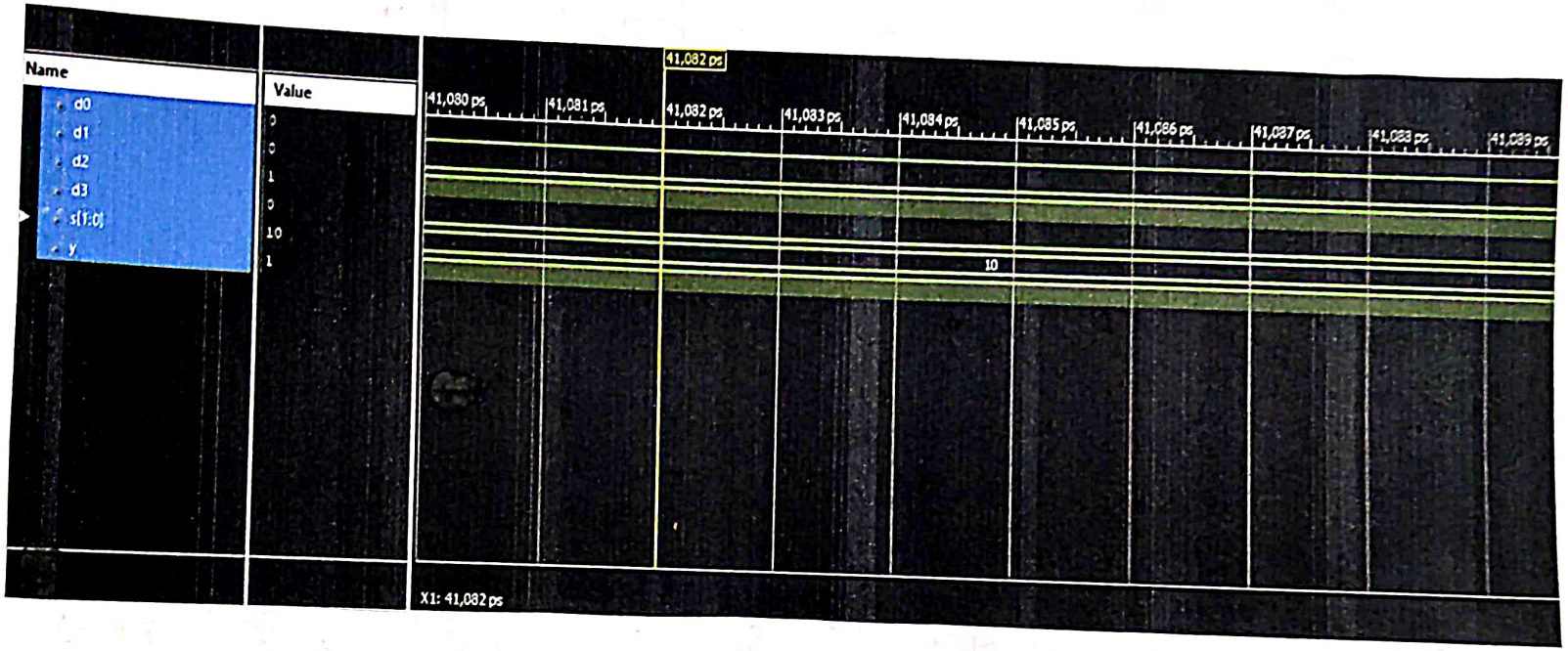
VHDL CODE for 4:1 MULTIPLEXER

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity MULTIPLEXER is
    Port ( D0: in STD_LOGIC;
           D1: in STD_LOGIC;
           D2: in STD_LOGIC;
           D3: in STD_LOGIC;
           S: in STD_LOGIC_VECTOR(1 DOWNTO 0);
           Y: out STD_LOGIC);
end MULTIPLEXER;

architecture Behavioral of MULTIPLEXER is

begin
with S Select

Y <= D0 when "00";
     D1 when "01";
     D2 when "10";
     D3 when Others;

end Behavioral;
```

OXFORD

Teacher's Signature .....


Name
d0
d1
d2
d3
s[1:0]
y
Value
0
0
1
0
10
1
41,082 ps
41,080 ps
41,081 ps
41,082 ps
41,083 ps
41,084 ps
41,085 ps
41,086 ps
41,087 ps
41,088 ps
41,089 ps
10
X1: 41,082 ps

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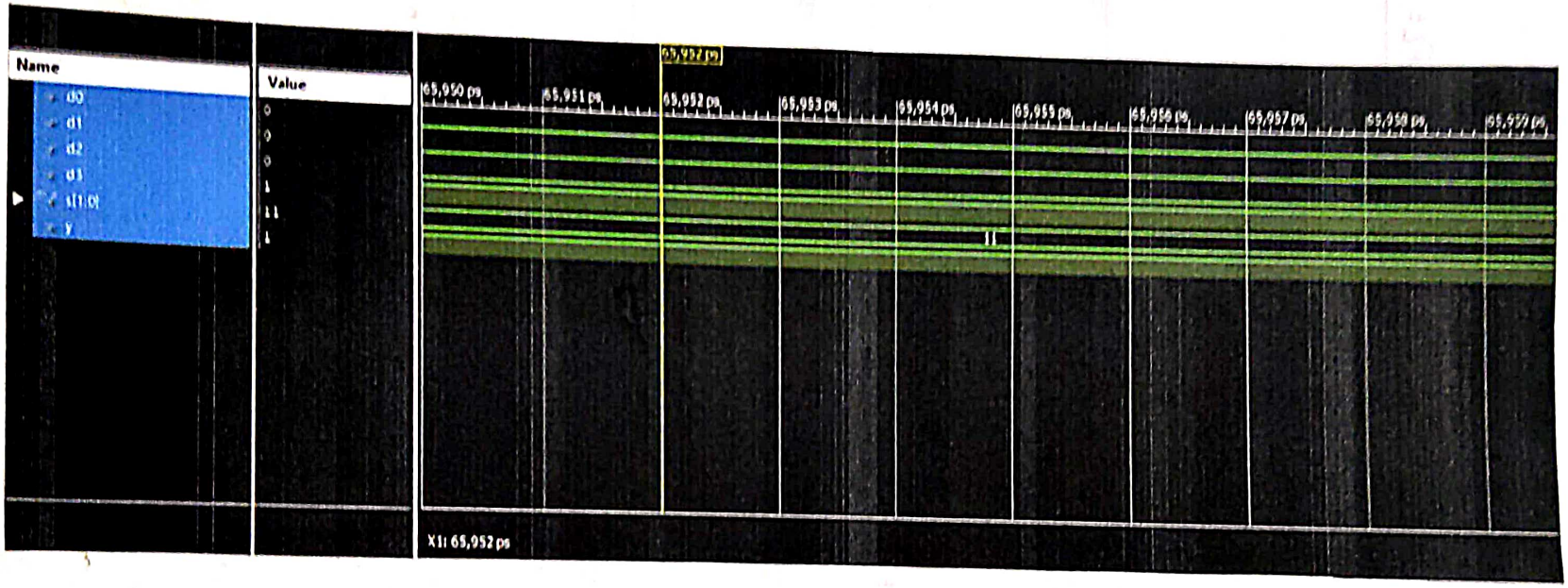
VHDL TESTBENCH CODE for 4:1 MULTIPLEXER

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY MULTI_TESTBENCH IS
END MULTI_TESTBENCH;

ARCHITECTURE behavior OF
MULTI_TESTBENCH IS

COMPONENT MULTIPLEXER
 PORT (
        D0: IN std_logic;
        D1: IN std_logic;
        D2: IN std_logic;
        D3: IN std_logic;
         S: IN std_logic_vector(1 downto 0);
         Y: OUT std_logic
      );
 END COMPONENT
```

OXFORD

Teacher's Signature .....


Name
d0
d1
d2
d3
s[1:0]
y
Value
65,950 ps
65,951 ps
65,952 ps
65,953 ps
65,954 ps
65,955 ps
65,956 ps
65,957 ps
65,958 ps
65,959 ps
X1: 65,952 ps

```
signal D0: std_logic := '0';
signal D1: std_logic := '0';
signal D2: std_logic := '0';
signal D3: std_logic := '0';
signal S: std_logic_vector (1 downto 0) := (others => '0');

signal Y: std_logic

BEGIN
 uut: MULTIPLEXER PORT MAP
  (
      D0 => D0,
      D1 => D1,
      D2 => D2,
      D3 => D3,
      S => S,
      Y => Y
  );

  stim_proc: process
  begin
      D3 <= '0';
      D1 <= '1';
      wait for 20 ns;
      D0 <= '0';
      D1 <= '1';
      wait for 20 ns;
```

```
D1 <= '0';
D2 <= '1';
wait for 20 ns;
D2 <= '0';
D3 <= '1';
wait for 20ns;
end process;

t2 : process
 begin
  S <= "00";
  wait for 20ns;
  S <= "01";
  wait for 20ns;
  S <= "10";
  wait for 20 ns;
  S <= "11";
  wait for 20 ns;

  end process;

END;
```

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CONCLUSION: In this experiment we were introduced with the procedure of designing a Multiplexer using VHDL. Multiplexer being a combinational multiple input switching circuit we have to use case statements in VHDL in this experiment. We also have written the corresponding VHDL Test bench and successfully verified the simulator result with the help of truth table.

Teacher's Signature .....