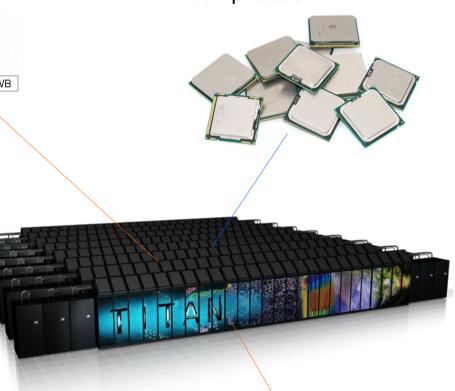
Pipeline

Take care of the order of the instructions

IF	ID	EX	MEM	WB				
i	IF	ID	EX	MEM	WB			
t ,		IF	ID	EX	MEM	WB		
			IF	ID	EX	MEM	WB	
				IF	ID	EX	MEM	WB

Many cores

Efficient parallelism is complicated



Memory hierarchy

Data locallity → memory access patterns

