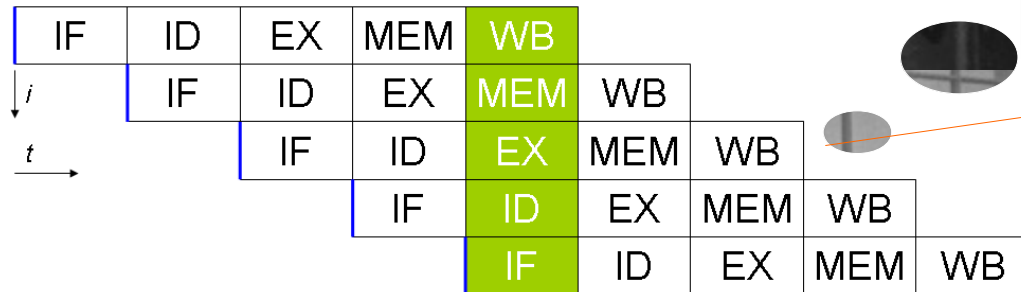


Pipeline

- Instructions divided in steps Multiple instructions in the pipeline but at different steps
- **Importance of the order** of the instructions



Many cores



Memory hierarchy

