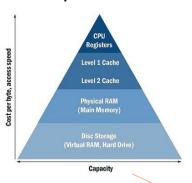
Memory hierarchy

Data locallity → memory access patterns



Many cores

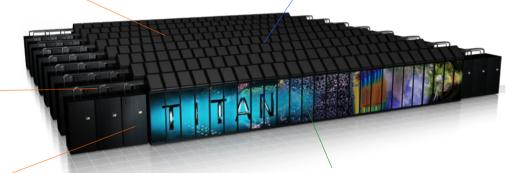
Efficient parallelism is complicated



Pipeline

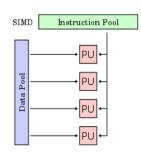
Take care of the order of the instructions

IF	ID	EX	MEM	WB				
i	IF	ID	EX	MEM	WB			
<i>t</i>		IF	ID	EX	MEM	WB		
			IF	ID	EX	MEM	WB	
				IF	ID	EX	MEM	WB



Vector support

Manipulate vector instead of scalar variables



GPUs

Different architecture and paradigm than CPUs

