Pipeline

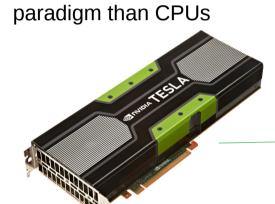
Take care of the order of the instructions

IF	ID	EX	MEM	WB				
j	IF	ID	EX	MEM	WB			
<i>t</i>		IF	ID	EX	MEM	WB		
			IF	ID	EX	MEM	WB	
				IF	ID	EX	MEM	WB

Many cores

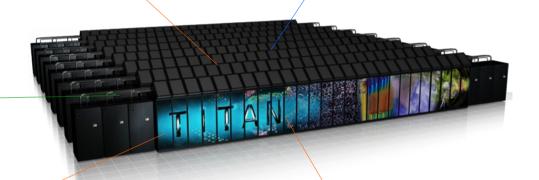
Efficient parallelism is complicated





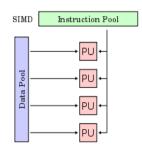
Different architecture and

GPUs



Vector support

Manipulate vector instead of scalar variables



Memory hierarchy

Data locallity → memory access patterns

