REGULATORS

T2K ASUM TEST - Regulators.SCHDOC

VREF_2.5V
EN_AN_+5V
EN_AN_-5V

VREF_2.5V
EN_AN_+5V
EN_AN_-5V

+6V_Analog_VMon
-6V_Analog_VMon
+6V_Dig_VMon
+6V_Analog_IMon
-6V_Analog_IMon
+6V_Dig_IMon

+6V_Analog_VMon
-6V_Analog_VMon
+6V_Dig_VMon
+6V_Analog_IMon
-6V_Analog_IMon
+6V_Dig_IMon

J1

POWER

6	AN_-6V_IN
5	AN_+6V_IN
4	GND
3	GND
2	SLO_+5V
1	DIG_+6V_IN

MIDAS_CPU

T2K ASUM TEST - MIDAS Slow Control.SCHDOC

MIDAS_RS485A
MIDAS_RS485B
SMB_CLK
SMB_DAT

BiasCurrentSense
Reference_Current
Bias_Readback
+6V_Analog_VMon
-6V_Analog_VMon
+6V_Dig_VMon
+6V_Analog_IMon
-6V_Analog_IMon
+6V_Dig_IMon

RS485-A
RS485-B
SMB_CLK
SMB_DAT

BiasCurrentSense
Reference_Current
Bias_Readback
+6V_Analog_VMon
-6V_Analog_VMon
+6V_Dig_VMon
+6V_Analog_IMon
-6V_Analog_IMon
+6V_Dig_IMon

SPI_MOSI
SPI_SCK
BIAS_DAC_CSn
SUM_DAC_CSn
ResetN

VREF_2.5V
Dcb1
De1

EN_AN_+5V
EN_AN_-5V
CEX0_CHG_PMP

SPI_MOSI
SPI_SCK
BIAS_DAC_CSn
SUM_DAC_CSn
ResetN

VREF_2.5V
Dcb1
De1

EN_AN_+5V
EN_AN_-5V
CEX0_CHG_PMP

J3

Amplifier Input

APDa1	1	2	APDk1
	3	4	
APDa2	5	6	APDk2
	7	8	
APDa3	9	10	APDk3
	11	12	
APDa4	13	14	APDk4
	15	16	
APDa5	17	18	APDk5
	19	20	
APDa6	21	22	APDk6
	23	24	
APDa7	25	26	APDk7
	27	28	
APDa8	29	30	APDk8
	31	32	
Dcb1	33	34	De1

GND GND

J4

SCA OUTPUT

APD_HATTN8	34	33	
APD_LATTN8	32	31	
APD_HATTN7	30	29	
APD_LATTN7	28	27	
APD_HATTN6	26	25	
APD_LATTN6	24	23	
APD_HATTN5	22	21	
APD_LATTN5	20	19	
APD_HATTN4	18	17	
APD_LATTN4	16	15	
APD_HATTN3	14	13	
APD_LATTN3	12	11	
APD_HATTN2	10	9	
APD_LATTN2	8	7	
APD_HATTN1	6	5	
APD_LATTN1	4	3	
ASUM_OUT	2	1	

GND

BIAS_DAC

T2K ASUM TEST - 8 Channel Bias Control.SCHDOC

BIAS_DAC_CSn
SPI_SCK
SPI_MOSI
ResetN

BIAS_DAC_CSn
BIAS_DAC_SCK
BIAS_DAC_DIN
BIAS_DAC_CLRn

BIAS_DAC[8..1]

BIAS_DAC[8..1]

BIAS_DAC

REPEAT(FIL,1,8)

T2K ASUM TEST- DAC Filter.SCHDOC

REPEAT(IN)

REPEAT(OUT)

APDk

APDk[8..1]

BIAS_EN

T2K ASUM TEST - Bias Enable.SCHDOC

ResetN
SMB_DAT
SMB_CLK

BiasEnable_RSTn
SMB_DAT
SMB_CLK

EN_BIASn[8..1]

EN_BIASn[8..1]

BIAS_SW

T2K ASUM TEST - 8 Channel MOSFET Switch.SCHDOC

EN_BIASn[8..1]

SW_BIAS[8..1]

+80V_Bias

APDa[8..1]

APDa

Repeat(DIV,1,8)

T2K ASUM TEST - APD Inputs - Charge Division.SCHDOC

REPEAT(APD_IN)

REPEAT(APD_HATTN)
REPEAT(APD_LATTN)
REPEAT(ASUM)

APD_HATTN
APD_LATTN
ASUM

APD_HATTN[8..1]
APD_LATTN[8..1]
ASUM[8..1]

CHRG_PUMP

T2K ASUM TEST - 80 Volt Charge Pump.SCHDOC

CEX0_CHG_PMP
SMB_CLK
SMB_DAT

CEX0_CHG_PMP
SCL
SDA

+80V_Bias
BiasCurrentSense
Reference_Current
Bias_Readback

+80V_Bias
BiasCurrentSense
Reference_Current
Bias_Readback

APD_SUM

T2K ASUM TEST - SUM.SCHDOC

ASUM[8..1]
SUM_DAC_CSn
SPI_SCK
SPI_MOSI
ResetN

APD_SUM[8..1]
SUM_DAC_CSn
SUM_DAC_SCK
SUM_DAC_DIN
SUM_DAC_CLRn

ASUM_OUT
LVDS_ASum_p
LVDS_ASum_n

ASUM_OUT
LVDS_ASum_p
LVDS_ASum

J2

ASUM

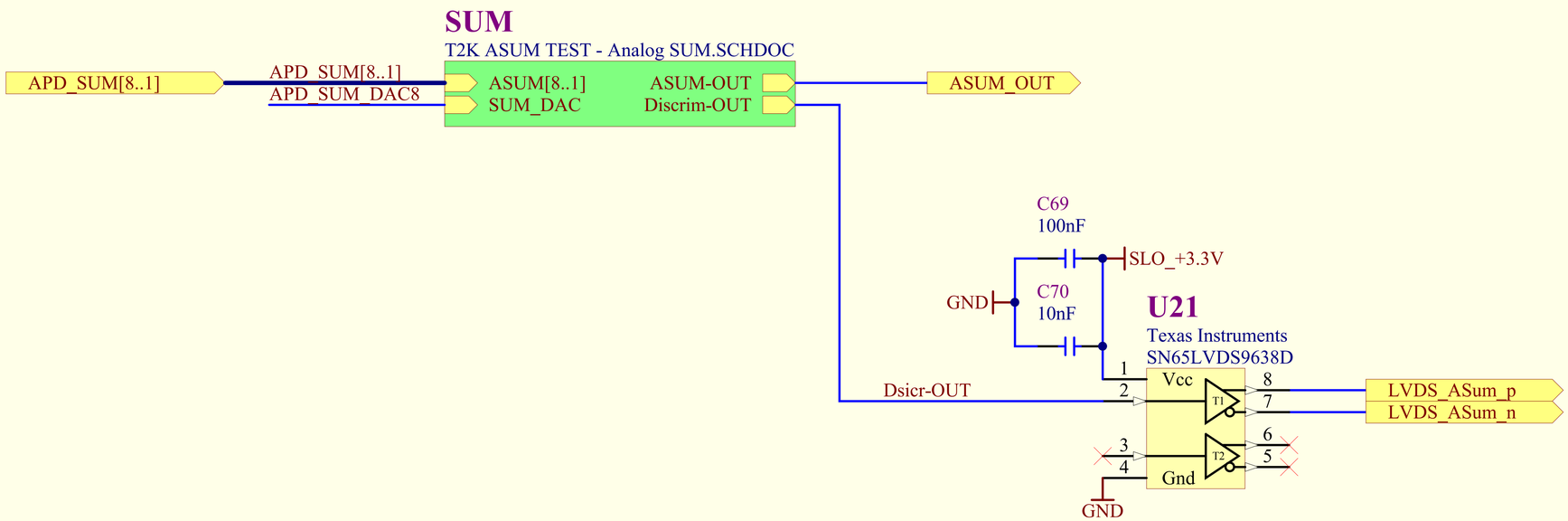
ADAPTER

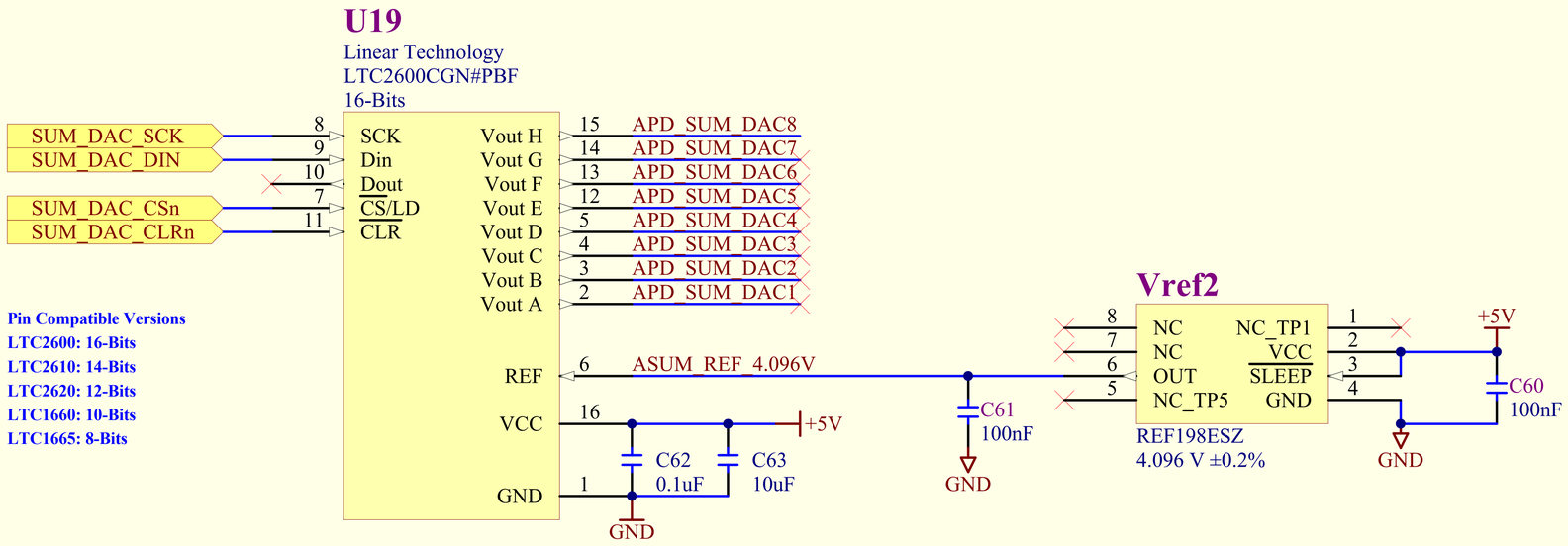
T2K ASUM TEST - ADAPTER.SCHDOC

T2K ASUM TEST - Top Level

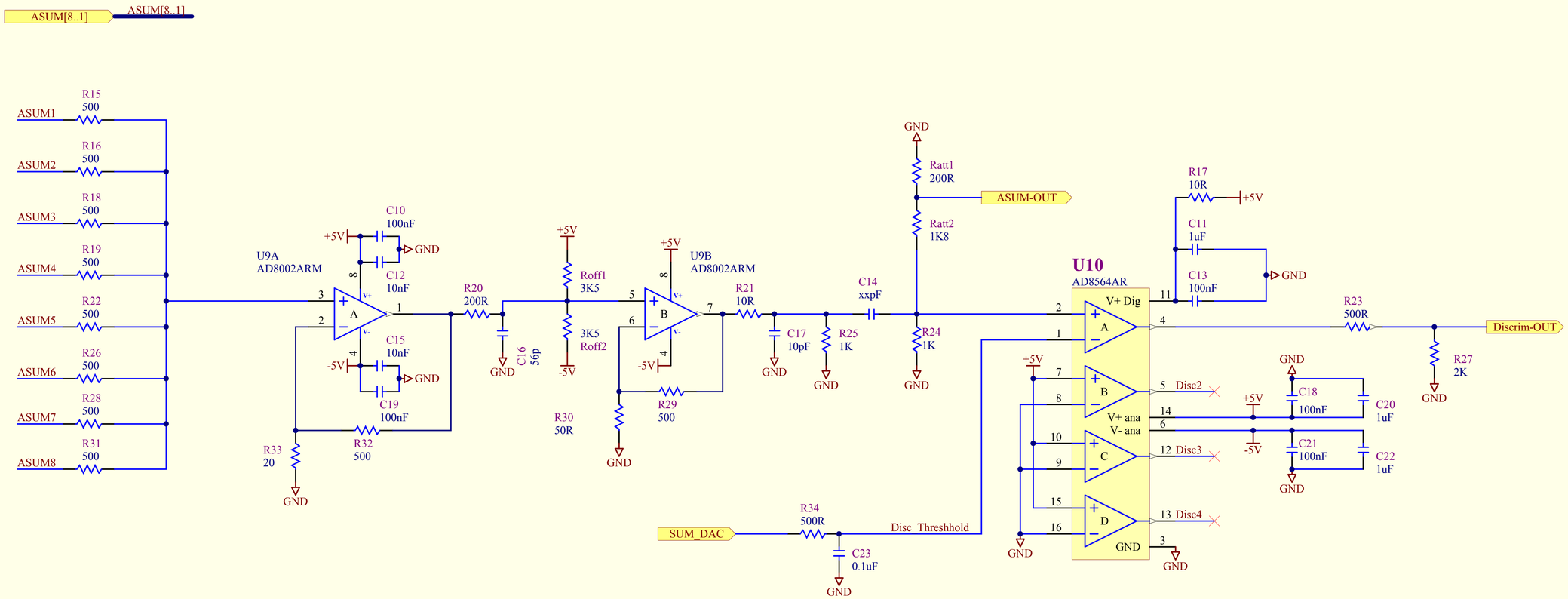
TRIUMF LOGO

Revision 0	Drawing #: 3		*TRIUMF* 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 3 of 12	Size: B	
	Drawn by: D.BIshop	Date: 5/23/2007	
File: G:\AHW\T2K\T2K - ASUM TEST\T2K ASUM TEST - Top Level.SCHDOC			8:05:33 PM



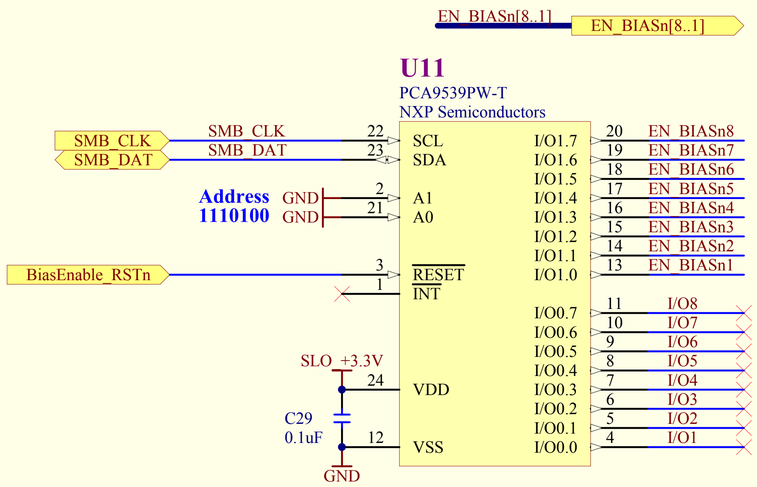


T2K ASUM TEST - APD SUM			
Revision **0**	Drawing #: 4		*TRIUMF* 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 4 of 12	Size: A	
	Drawn by: D.Bishop	Date: 5/23/2007	
File: G:\AHW\T2K\T2K - ASUM TEST\T2K_ASUM TEST - SUM.SCHDOC			8:05:33 PM



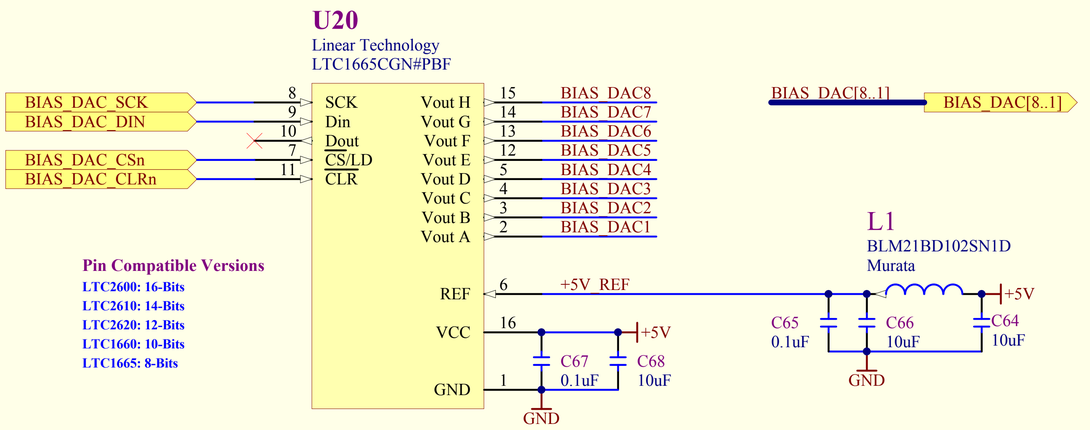
T2K ASUM TEST- OP Amps / Discriminator

Revision **0**	Drawing #: 9		*TRIUMF* 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 9 of 12	Size: B	
	Drawn by: D. Bishop	Date: 5/23/2007	
File: G:\AHW\T2K\T2K - ASUM TEST\T2K ASUM TEST - Analog SUM.SCHDOC			8:05:33 PM



T2K ASUM TEST - Channel Bias Enable

Revision **0**	Drawing #: 10		*TRIUMF* 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 10 of 12	Size: A	
	Drawn by: D.Bishop	Date: 5/23/2007	
File: G:\AHW\T2K\T2K - ASUM TEST\T2K ASUM TEST - Bias Enable.SCHDOC			8:05:34 PM



T2K ASUM TEST - 8 Channel Bias Control

Revision	Drawing #: 7		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3	
0	Sheet #: 7 of 12	Size: A		
	Drawn by: D.Bishop	Date: 5/23/2007		

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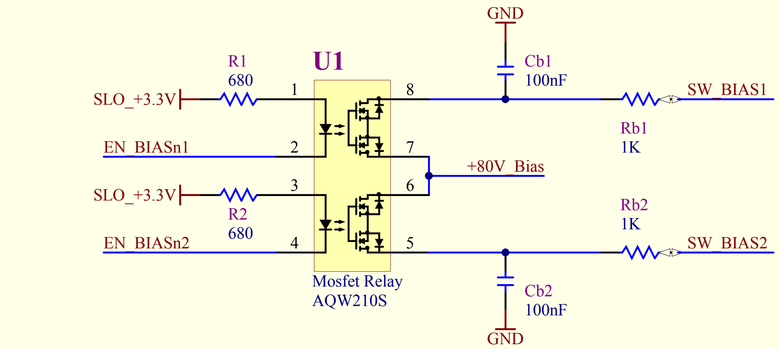

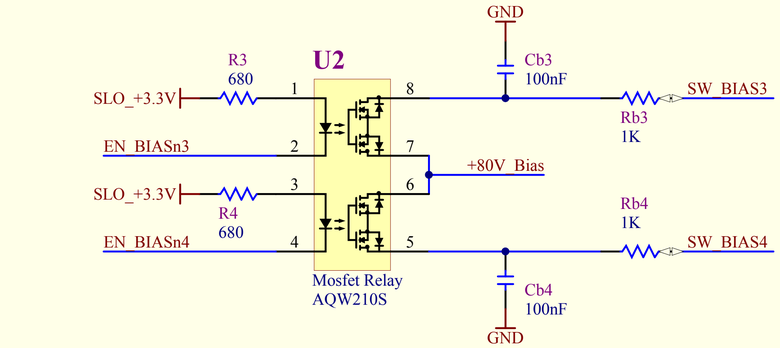

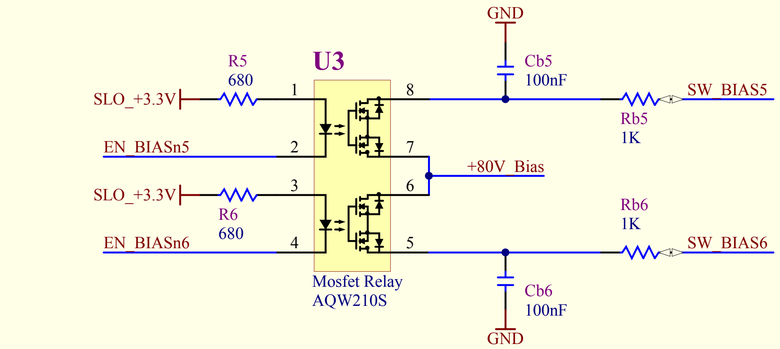

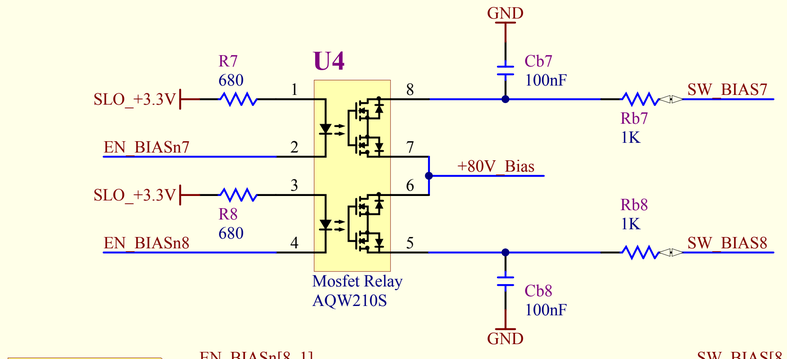

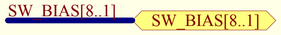

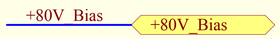

T2K ASUM TEST - 8 Channel Mosfet Switch

Revision	Drawing #: 8		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
0	Sheet #: 8 of 12	Size: A	
	Drawn by: D.Bishop	Date: 5/23/2007	

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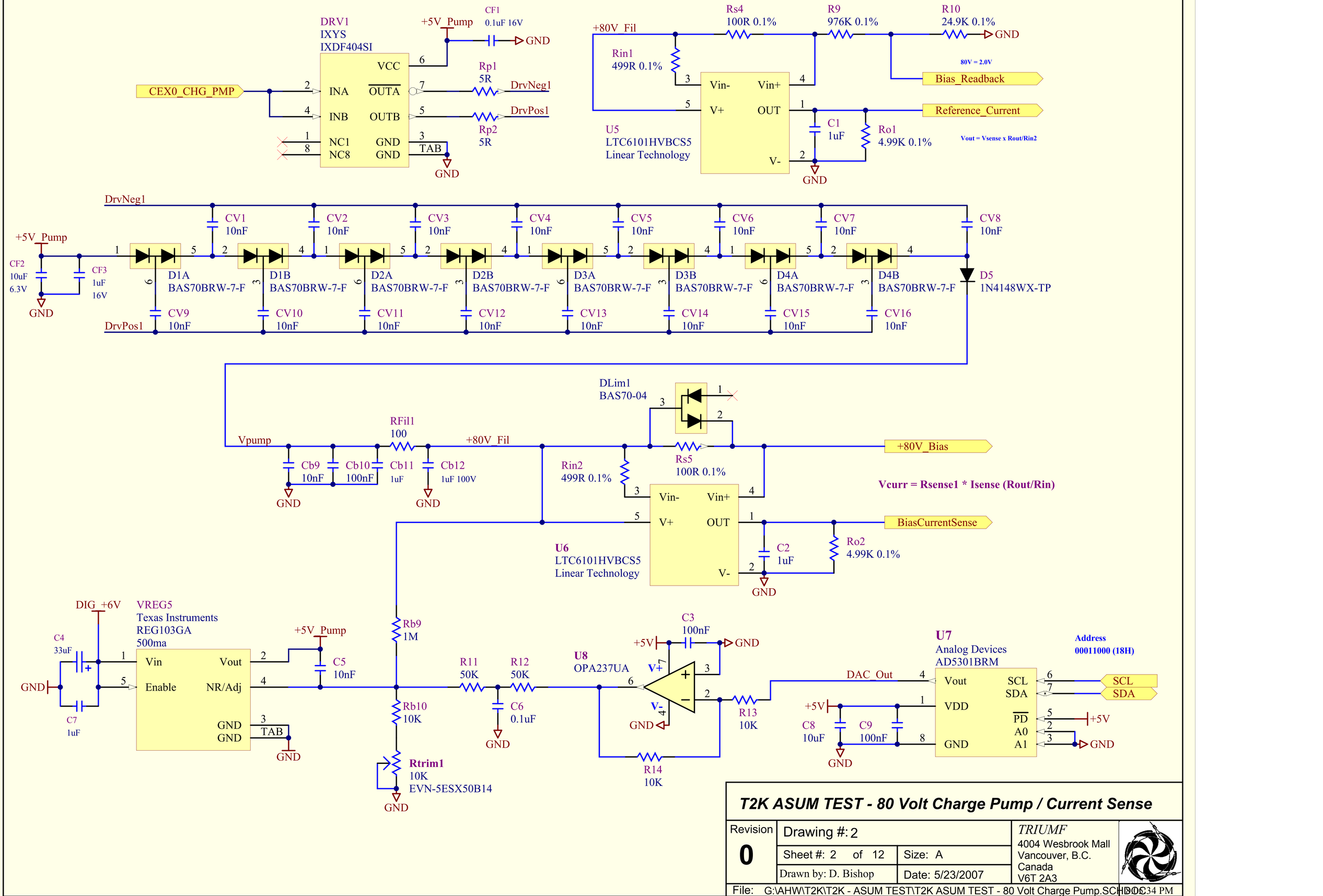
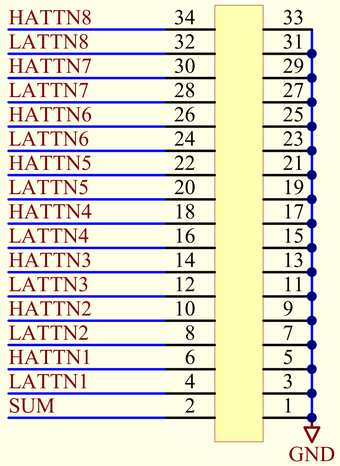

DRV1
IXYS
IXDF404SI
VCC
INA
INB
NC1
NC8
OUTA
OUTB
GND
GND
TAB
CEX0_CHG_PMP
+5V_Pump
CF1
0.1uF 16V
GND
Rp1
5R
DrvNeg1
DrvPos1
Rp2
5R
GND
+80V_Fil
Rs4
100R 0.1%
R9
976K 0.1%
R10
24.9K 0.1%
GND
80V = 2.0V
Bias_Readback
Rin1
499R 0.1%
U5
LTC6101HVBCS5
Linear Technology
Vin-
Vin+
V+
OUT
V-
C1
1uF
Ro1
4.99K 0.1%
Reference_Current
Vout = Vsense x Rout/Rin2
GND
DrvNeg1
DrvPos1
CV1 10nF
CV2 10nF
CV3 10nF
CV4 10nF
CV5 10nF
CV6 10nF
CV7 10nF
CV8 10nF
CV9 10nF
CV10 10nF
CV11 10nF
CV12 10nF
CV13 10nF
CV14 10nF
CV15 10nF
CV16 10nF
+5V_Pump
CF2
10uF
6.3V
CF3
1uF
16V
GND
D1A BAS70BRW-7-F
D1B BAS70BRW-7-F
D2A BAS70BRW-7-F
D2B BAS70BRW-7-F
D3A BAS70BRW-7-F
D3B BAS70BRW-7-F
D4A BAS70BRW-7-F
D4B BAS70BRW-7-F
D5
1N4148WX-TP
DLim1
BAS70-04
RFil1
100
Vpump
+80V_Fil
Cb9 10nF
Cb10 100nF
Cb11 1uF
Cb12 1uF 100V
GND
GND
Rin2
499R 0.1%
Rs5
100R 0.1%
+80V_Bias
Vcurr = Rsense1 * Isense (Rout/Rin)
U6
LTC6101HVBCS5
Linear Technology
BiasCurrentSense
C2
1uF
Ro2
4.99K 0.1%
GND
DIG_+6V
VREG5
Texas Instruments
REG103GA
500ma
C4
33uF
Vin
Vout
Enable
NR/Adj
GND
GND
TAB
C7
1uF
GND
+5V_Pump
C5
10nF
Rb9
1M
Rb10
10K
Rtrim1
10K
EVN-5ESX50B14
GND
R11
50K
R12
50K
C6
0.1uF
GND
U8
OPA237UA
C3
100nF
+5V
GND
V+
V-
GND
R13
10K
R14
10K
U7
Analog Devices
AD5301BRM
Address
00011000 (18H)
DAC_Out
Vout
VDD
GND
SCL
SDA
PD
A0
A1
SCL
SDA
+5V
GND
C8
10uF
C9
100nF
+5V
GND
T2K ASUM TEST - 80 Volt Charge Pump / Current Sense
Revision
0
Drawing #: 2
Sheet #: 2 of 12
Size: A
Drawn by: D. Bishop
Date: 5/23/2007
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
File: G:\AHW\T2K\T2K - ASUM TEST\T2K ASUM TEST - 80 Volt Charge Pump.SCHDOC
3:01:34 PM

S1

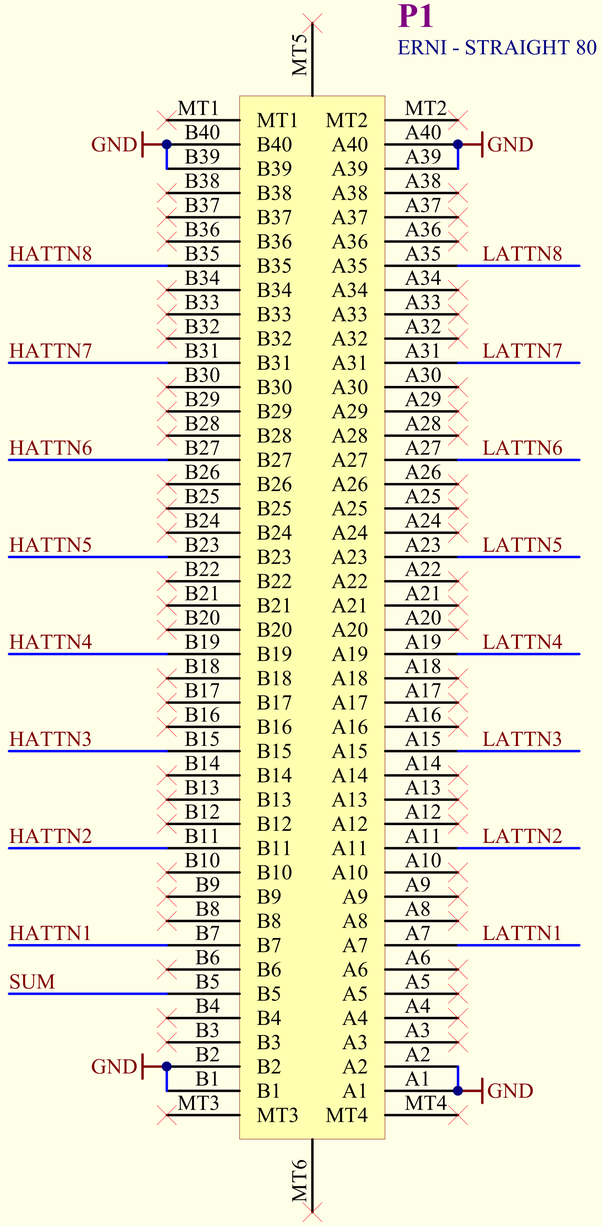
SCA INPUT

34 Pin Header 0.1" Pitch



P1

ERNI - STRAIGHT 80 PIN



T2K ASUM TEST - ADAPTER

Revision	Drawing #: 12		*TRIUMF* 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
0	Sheet #: 12 of 12	Size: A	
	Drawn by: D.BISHOP	Date: 5/23/2007	
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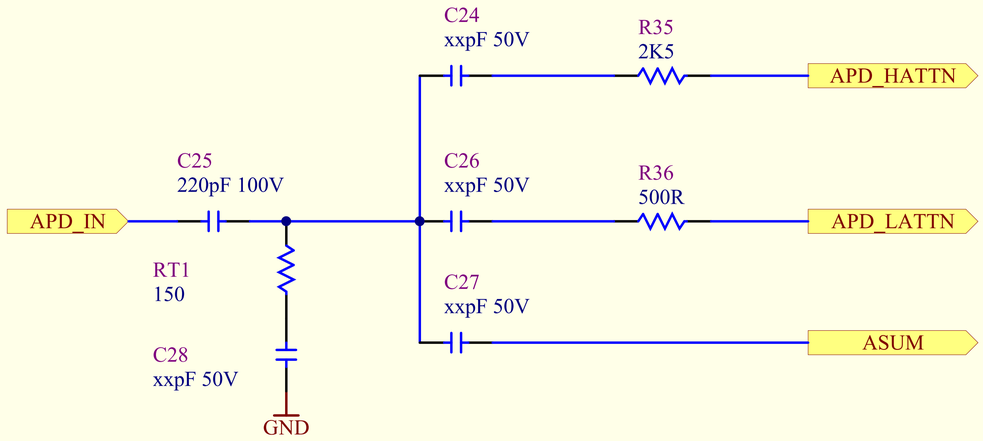

T2K ASUM TEST - APD Input - Charge Division

Revision 0	Drawing #: 5		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 5 of 12	Size: A	
	Drawn by: D.Bishop	Date: 5/23/2007	
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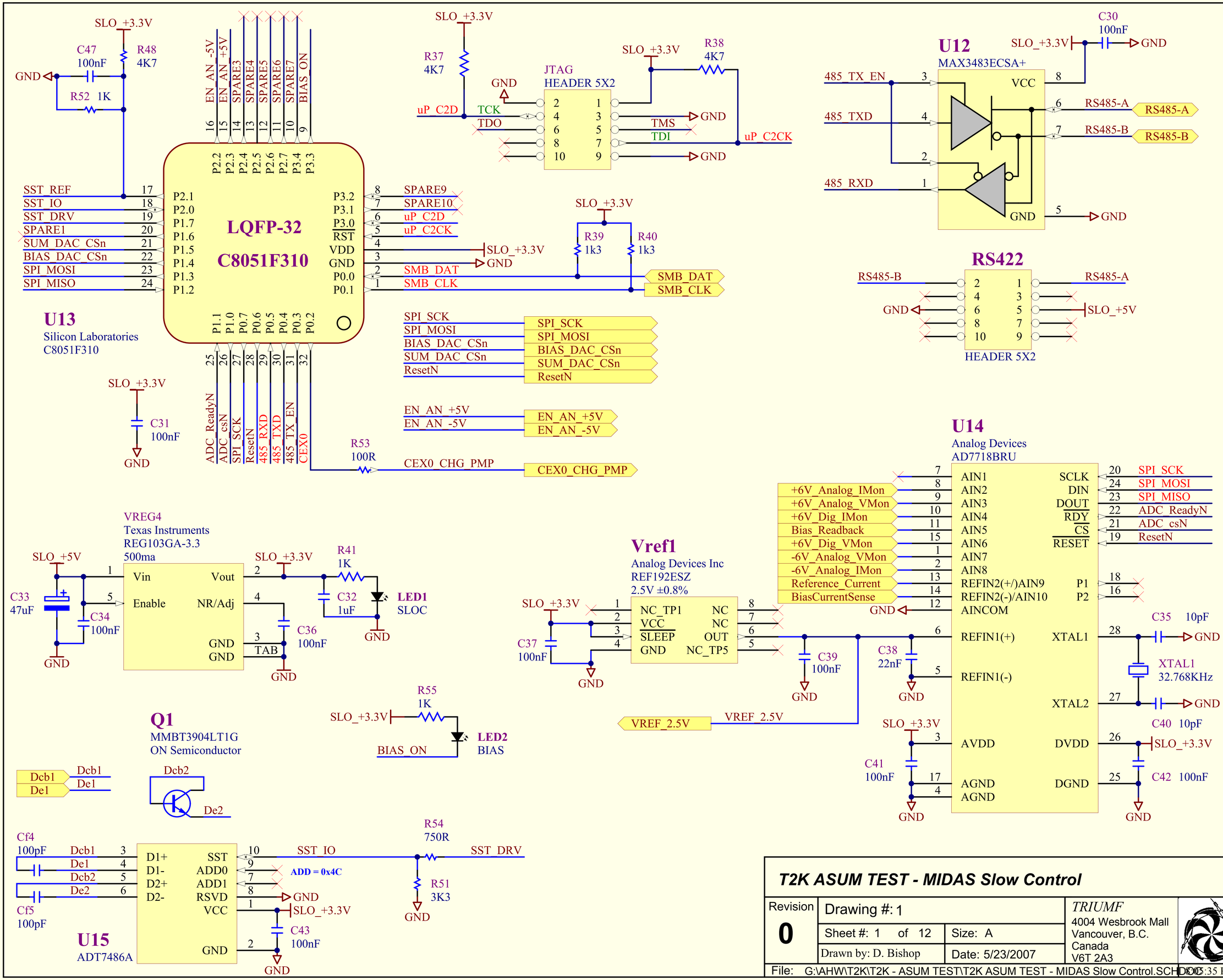
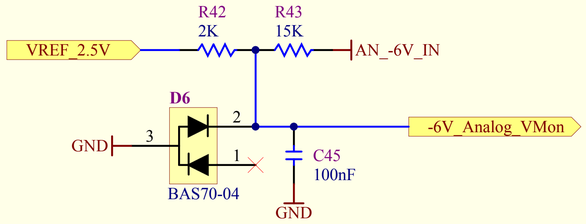
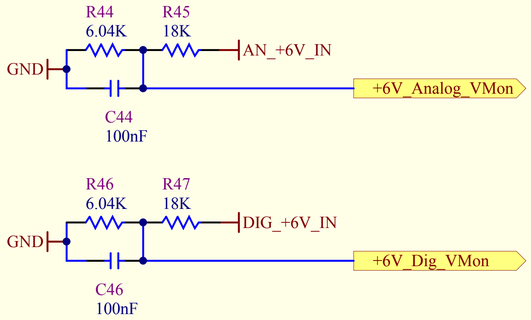


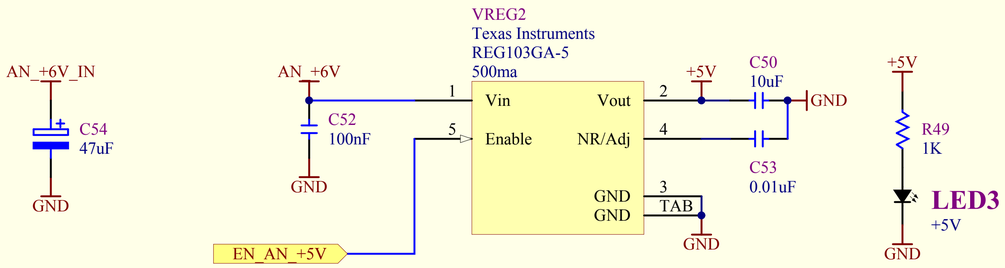
T2K ASUM TEST - MIDAS Slow Control

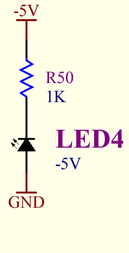
Revision	Drawing #: 1		TRIUMF
0	Sheet #: 1 of 12	Size: A	4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Drawn by: D. Bishop	Date: 5/23/2007	

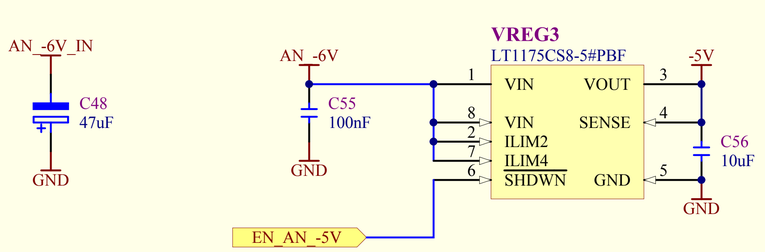
File: G:\AHW\T2K\T2K - ASUM TEST\T2K ASUM TEST - MIDAS Slow Control.SCHDOC 5:35 PM

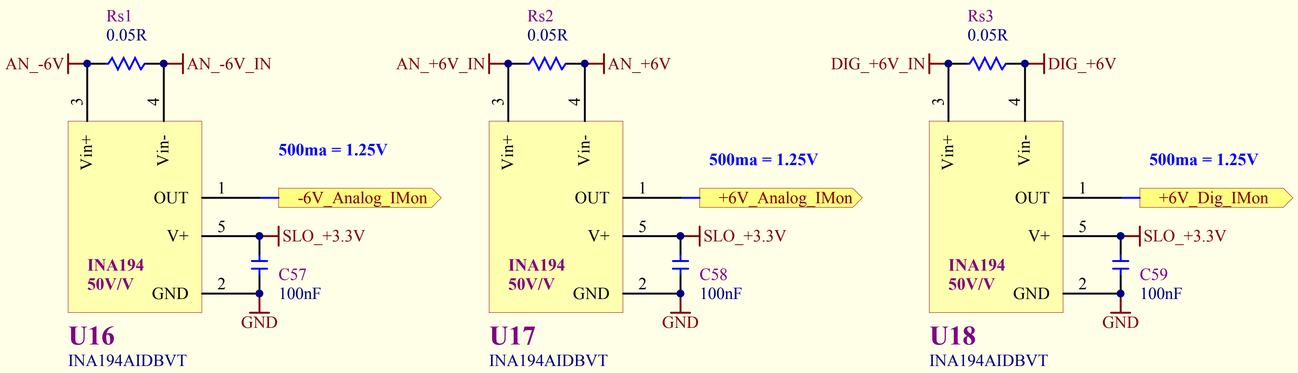






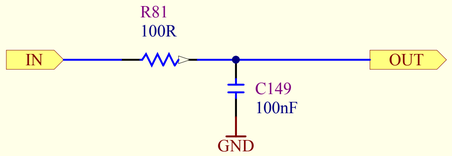






T2K ASUM TEST - Voltage Regulators - Volt/Curr Monitor

Revision	Drawing #: 11		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3	
0	Sheet #: 11 of 12	Size: A		
	Drawn by: D. Bishop	Date: 5/23/2007		
File: G:\AHW\T2K\T2K - ASUM TEST\T2K ASUM TEST - Regulators.SCHDOC				8:05:35 PM



T2K ASUM TEST - DAC Filter

Revision: 0	Drawing #: 6		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 6 of 12	Size: A	
	Drawn by: D.Bishop	Date: 5/23/2007	
File: G:\AHW\T2K\T2K - ASUM TEST\T2K ASUM TEST- DAC Filter.SCHDOC			8:05:35 PM