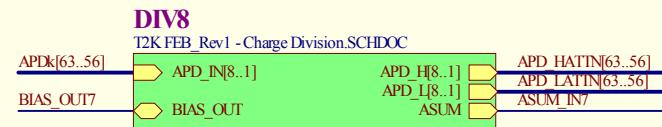
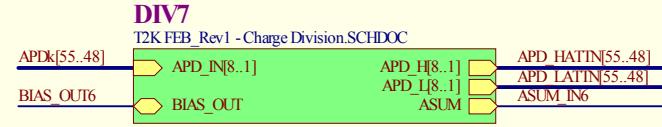
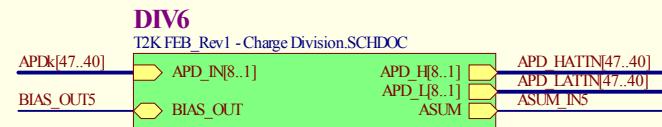
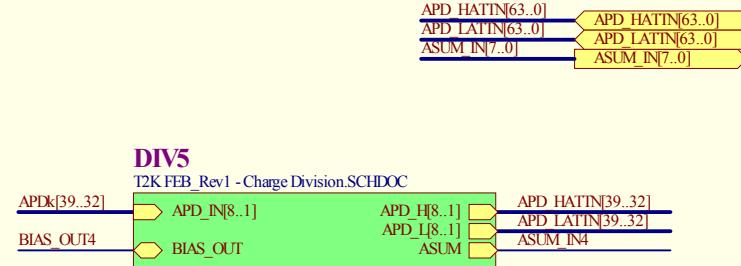
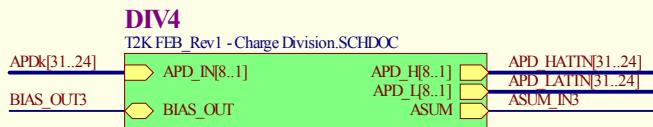
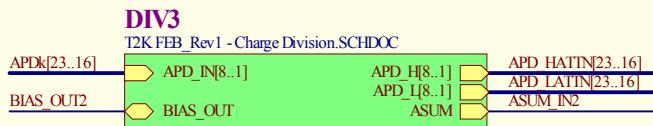
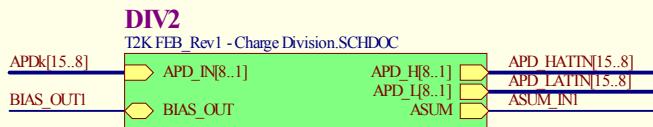
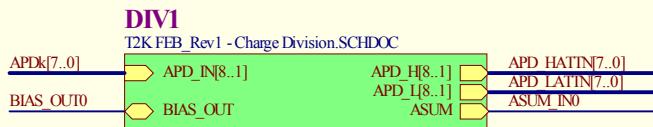


T2K FEB - Top Level

Revision	Drawing #	1
1	Sheet #:	1 of 16
	Size:	B
	Drawn by:	D.Bishop
	Date:	25/06/2008
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TRIUMF
LOGO



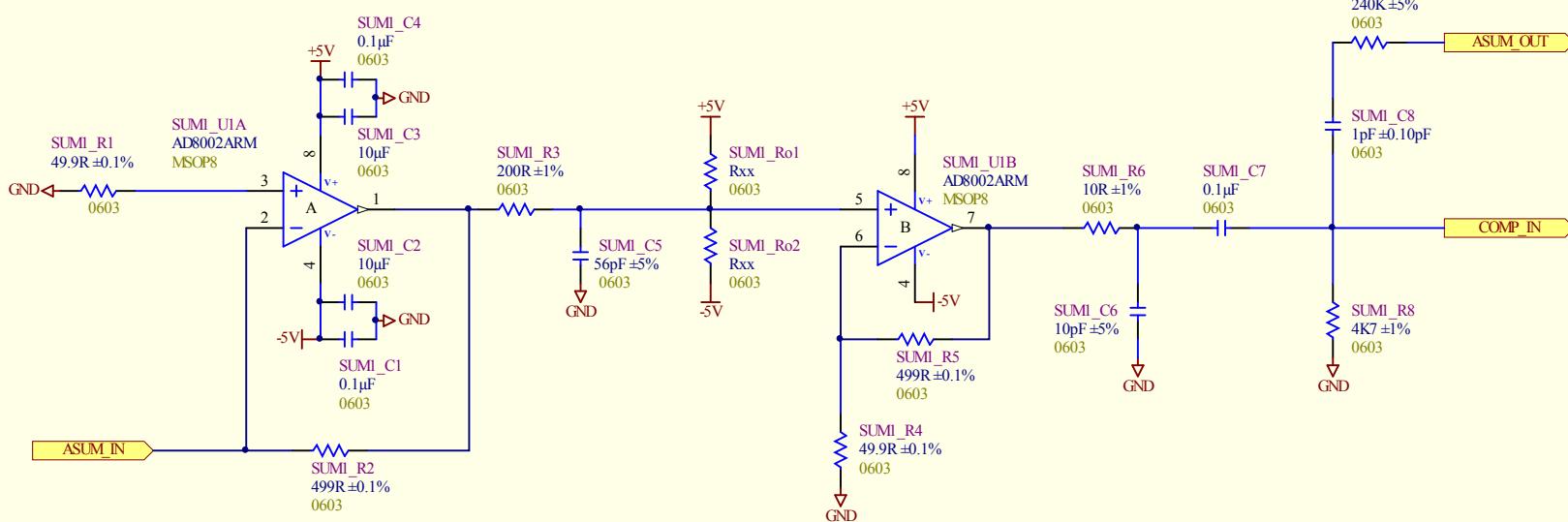
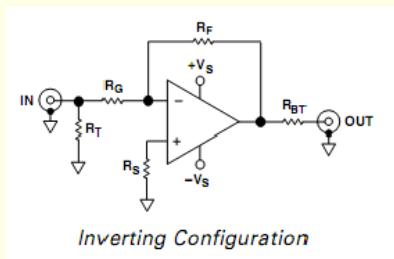


T2K FEB64 - APD Inputs

Revision 1	Drawing #:	10	TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #:	10 of 16	
	Size:	A	
	Drawn by:	D.Bishop	Date: 25/06/2008
File: G:\AHW\T2K\FEB64\Rev1\T2K FEB_Rev1 - APD Inputs.SchDoc			2:37:58 PM

Component	AD8002ARM (μ SOIC) Gain						
	-10	-2	-1	+1	+2	+10	+100
R_F (Ω)	499	499	590	1000	681	499	1000
R_G (Ω)	49.9	249	590	-	681	54.9	10
R_{BT} (Nominal) (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9
R_C (Ω)*				75	75	0	0
R_S (Ω)	49.9	49.9	49.9				
R_T (Nominal) (Ω)	-	61.9	49.9	49.9	49.9	49.9	49.9
Small Signal BW (MHz)	270	400	410	600	450	170	19
0.1 dB Flatness (MHz)	60	100	100	35	70	35	3

* R_C is recommended to reduce peaking, and minimizes input reflections at frequencies above 300 MHz. However, R_C is not required.



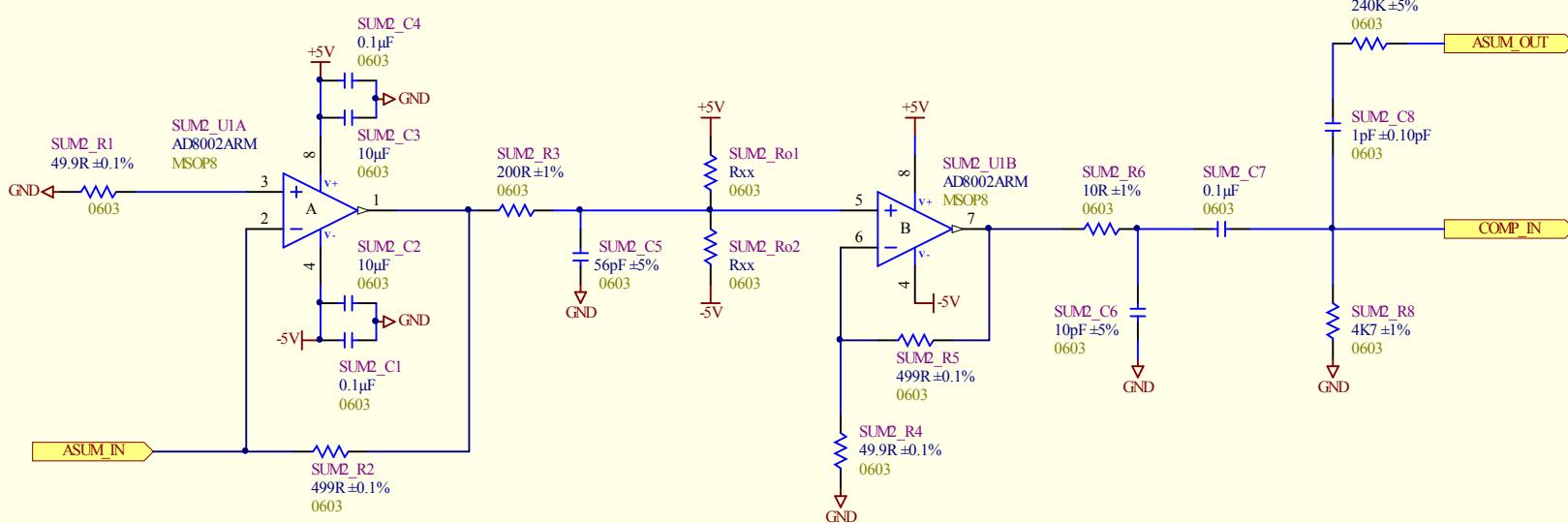
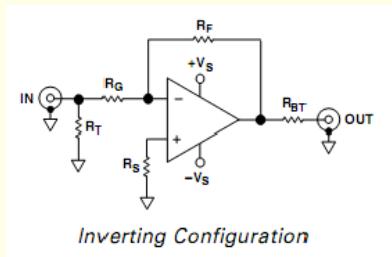
T2K FEB64 - Charge SUM Amplifier

Revision 1	Drawing #: 11	Sheet #:		Size: A	Drawn by: D. Bishop	Date: 25/06/2008	TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
		11	of 16				



Component	AD8002ARM (μ SOIC) Gain						
	-10	-2	-1	+1	+2	+10	+100
R_F (Ω)	499	499	590	1000	681	499	1000
R_G (Ω)	49.9	249	590	-	681	54.9	10
R_{BT} (Nominal) (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9
R_C (Ω)*				75	75	0	0
R_S (Ω)	49.9	49.9	49.9				
R_T (Nominal) (Ω)	-	61.9	49.9	49.9	49.9	49.9	49.9
Small Signal BW (MHz)	270	400	410	600	450	170	19
0.1 dB Flatness (MHz)	60	100	100	35	70	35	3

* R_C is recommended to reduce peaking, and minimizes input reflections at frequencies above 300 MHz. However, R_C is not required.

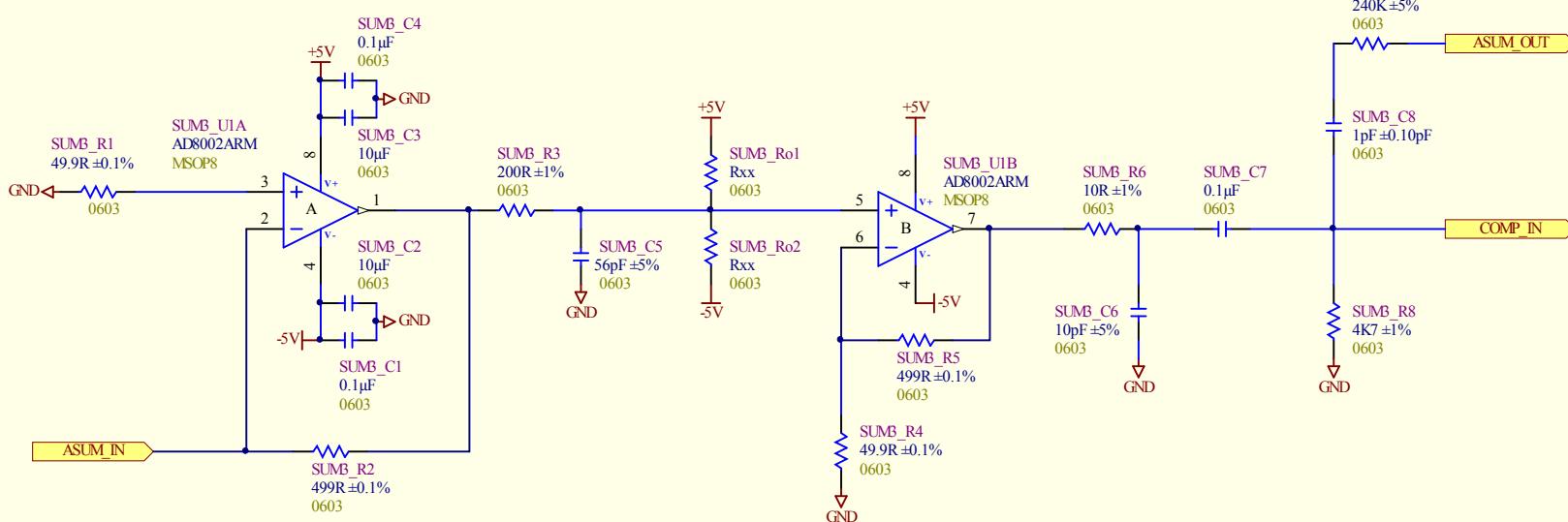
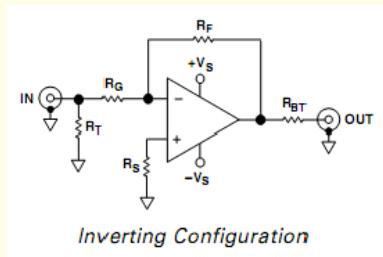


T2K FEB64 - Charge SUM Amplifier

Revision 1	Drawing #: 11	TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3	
		Sheet #: 11 of 16	Size: A
		Drawn by: D. Bishop	Date: 25/06/2008
File: G:\AHW\T2K\T2K_FEB64\Rev1\T2K FEB Rev1 - Analog SUM.SCHDOC			2:37:59 PM

Component	AD8002ARM (μ SOIC) Gain						
	-10	-2	-1	+1	+2	+10	+100
R_F (Ω)	499	499	590	1000	681	499	1000
R_G (Ω)	49.9	249	590	-	681	54.9	10
R_{BT} (Nominal) (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9
R_C (Ω)*				75	75	0	0
R_S (Ω)	49.9	49.9	49.9				
R_T (Nominal) (Ω)	-	61.9	49.9	49.9	49.9	49.9	49.9
Small Signal BW (MHz)	270	400	410	600	450	170	19
0.1 dB Flatness (MHz)	60	100	100	35	70	35	3

* R_C is recommended to reduce peaking, and minimizes input reflections at frequencies above 300 MHz. However, R_C is not required.

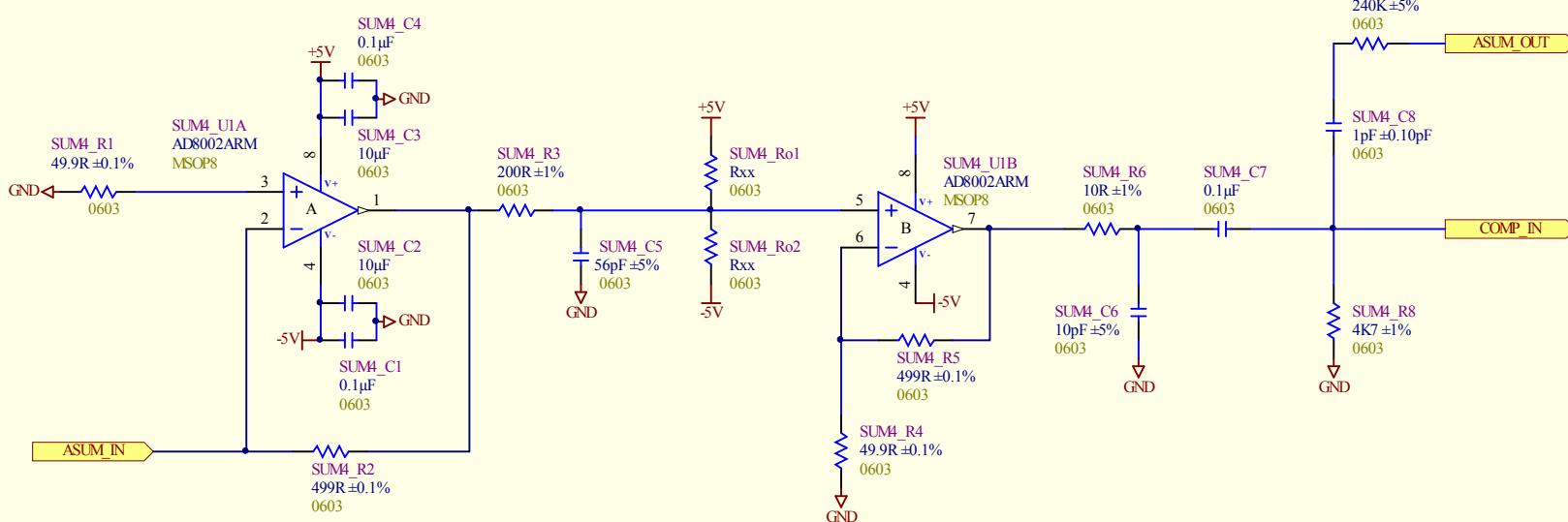
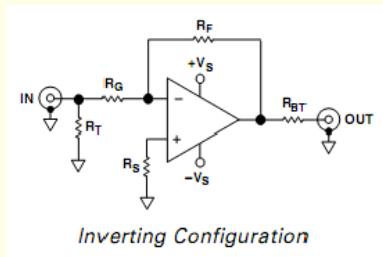


T2K FEB64 - Charge SUM Amplifier

Revision	Drawing #:	11		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3	
		Sheet #:	11 of 16		
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		File:	G:\AHW\T2K\T2K_FEB64\Rev1\T2K FEB Rev1 - Analog SUM.SCHDOC		2:37:59 PM

Component	AD8002ARM (μ SOIC) Gain						
	-10	-2	-1	+1	+2	+10	+100
R_F (Ω)	499	499	590	1000	681	499	1000
R_G (Ω)	49.9	249	590	-	681	54.9	10
R_{BT} (Nominal) (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9
R_C (Ω)*				75	75	0	0
R_S (Ω)	49.9	49.9	49.9				
R_T (Nominal) (Ω)	-	61.9	49.9	49.9	49.9	49.9	49.9
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0.1 dB Flatness (MHz)	60	100	100	35	70	35	3

* R_C is recommended to reduce peaking, and minimizes input reflections at frequencies above 300 MHz. However, R_C is not required.

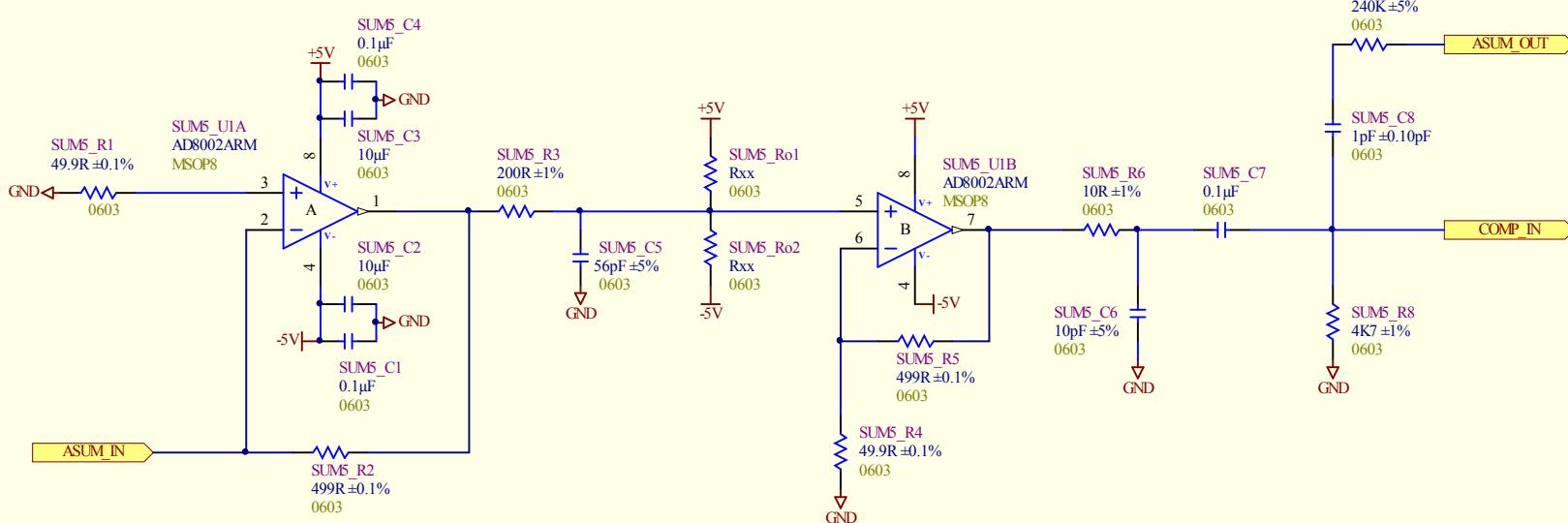
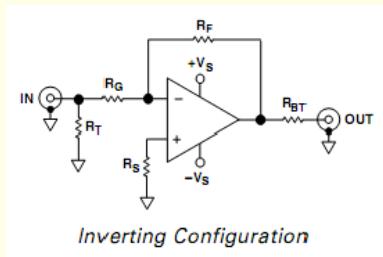


T2K FEB64 - Charge SUM Amplifier

Revision 1	Drawing #: 11	TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3	
		Sheet #: 11 of 16	Size: A
		Drawn by: D. Bishop	Date: 25/06/2008
File: G:\AHW\T2K\T2K_FEB64\Rev1\T2K FEB Rev1 - Analog SUM.SCHDOC			2:37:59 PM

Component	AD8002ARM (μ SOIC) Gain						
	-10	-2	-1	+1	+2	+10	+100
R_F (Ω)	499	499	590	1000	681	499	1000
R_G (Ω)	49.9	249	590	-	681	54.9	10
R_{BT} (Nominal) (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9
R_C (Ω)*				75	75	0	0
R_S (Ω)	49.9	49.9	49.9				
R_T (Nominal) (Ω)	-	61.9	49.9	49.9	49.9	49.9	49.9
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0.1 dB Flatness (MHz)	60	100	100	35	70	35	3

* R_C is recommended to reduce peaking, and minimizes input reflections at frequencies above 300 MHz. However, R_C is not required.

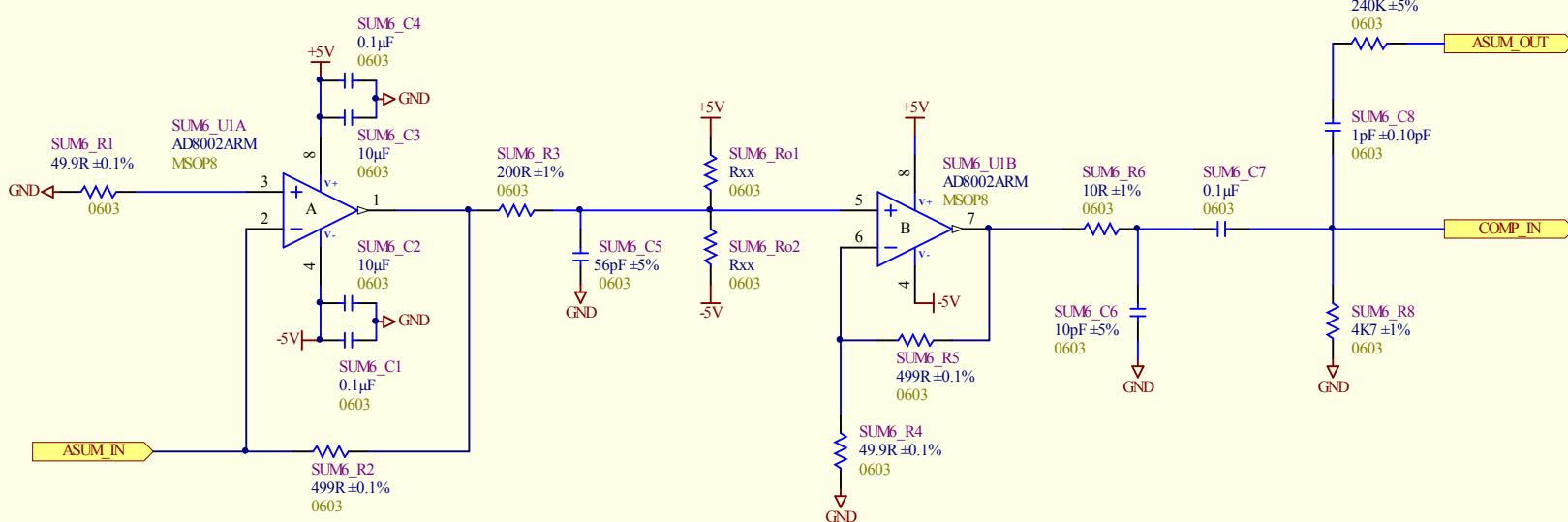
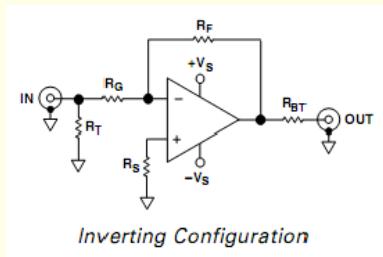


T2K FEB64 - Charge SUM Amplifier

Revision 1	Drawing #: 11	Sheet #: 11 of 16		Size: A	TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3	
		Drawn by: D. Bishop	Date: 25/06/2008			
File: G:\AHW\T2K\T2K_FEB64\Rev1\T2K FEB Rev1 - Analog SUM.SCHDOC						

Component	AD8002ARM (μ SOIC) Gain						
	-10	-2	-1	+1	+2	+10	+100
R_F (Ω)	499	499	590	1000	681	499	1000
R_G (Ω)	49.9	249	590	-	681	54.9	10
R_{BT} (Nominal) (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9
R_C (Ω)*				75	75	0	0
R_S (Ω)	49.9	49.9	49.9				
R_T (Nominal) (Ω)	-	61.9	49.9	49.9	49.9	49.9	49.9
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0.1 dB Flatness (MHz)	60	100	100	35	70	35	3

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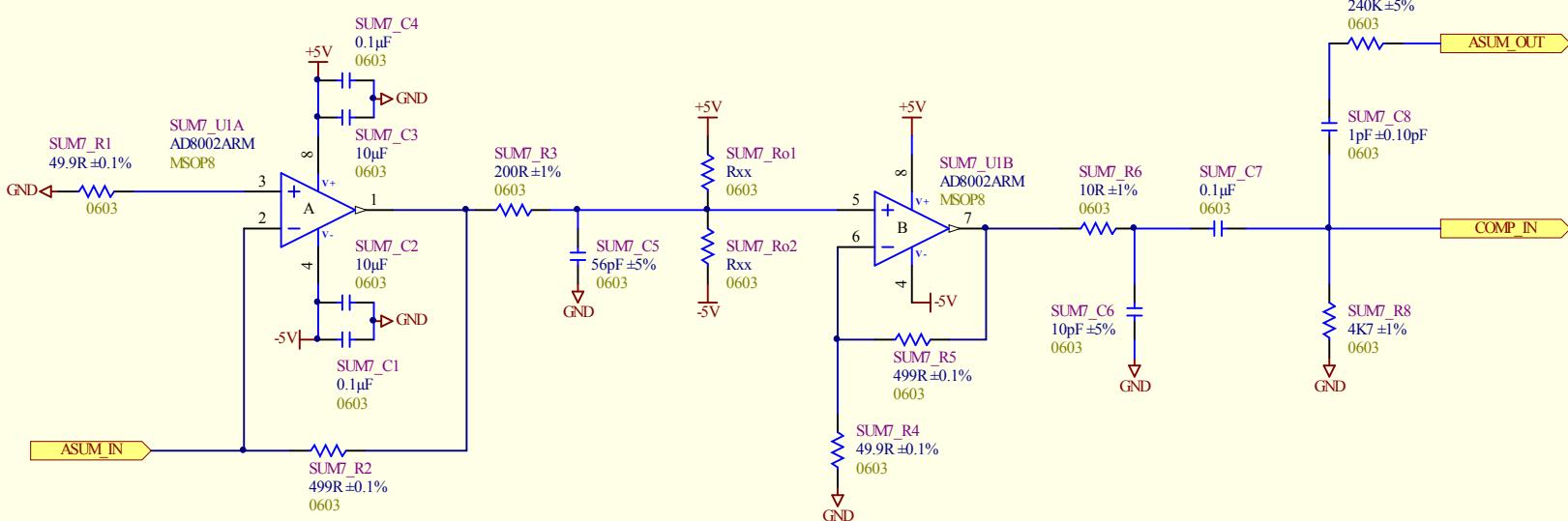
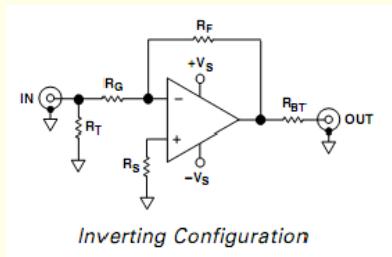
T2K FEB64 - Charge SUM Amplifier

Revision 1	Drawing #: 11	Sheet #:		Size: A	Drawn by: D. Bishop	Date: 25/06/2008	TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
		11	of 16				
File: G:\AHW\T2K\T2K_FEB64\Rev1\T2K FEB Rev1 - Analog SUM.SCHDOC							



Component	AD8002ARM (μ SOIC) Gain						
	-10	-2	-1	+1	+2	+10	+100
R_F (Ω)	499	499	590	1000	681	499	1000
R_G (Ω)	49.9	249	590	-	681	54.9	10
R_{BT} (Nominal) (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9
R_C (Ω)*				75	75	0	0
R_S (Ω)	49.9	49.9	49.9				
R_T (Nominal) (Ω)	-	61.9	49.9	49.9	49.9	49.9	49.9
Small Signal BW (MHz)	270	400	410	600	450	170	19
0.1 dB Flatness (MHz)	60	100	100	35	70	35	3

* R_C is recommended to reduce peaking, and minimizes input reflections at frequencies above 300 MHz. However, R_C is not required.



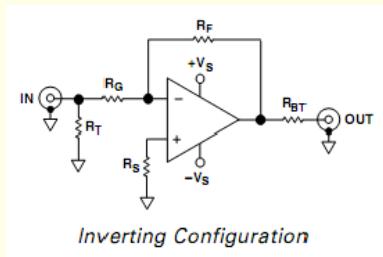
T2K FEB64 - Charge SUM Amplifier

Revision 1	Drawing #: 11	Sheet #:		Size: A	Drawn by: D. Bishop	Date: 25/06/2008	TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
		11	of 16				
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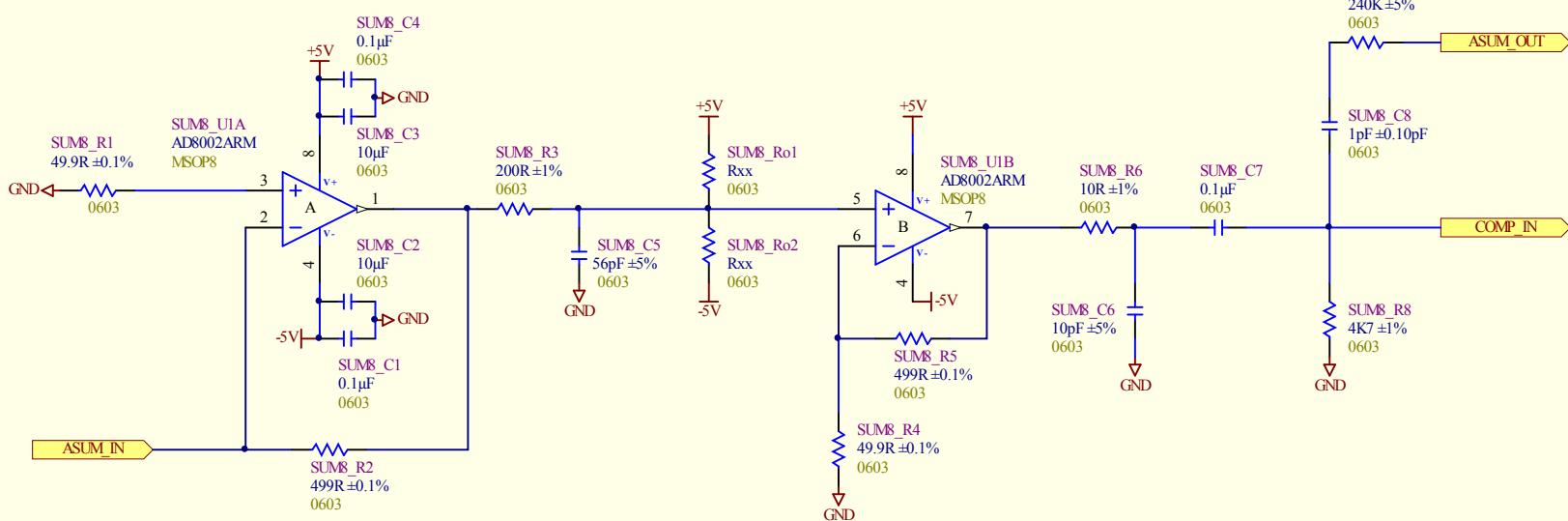


Component	AD8002ARM (μ SOIC) Gain						
	-10	-2	-1	+1	+2	+10	+100
R_F (Ω)	499	499	590	1000	681	499	1000
R_G (Ω)	49.9	249	590	-	681	54.9	10
R_{BT} (Nominal) (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9
R_C (Ω)*				75	75	0	0
R_S (Ω)	49.9	49.9	49.9				
R_T (Nominal) (Ω)	-	61.9	49.9	49.9	49.9	49.9	49.9
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0.1 dB Flatness (MHz)	60	100	100	35	70	35	3

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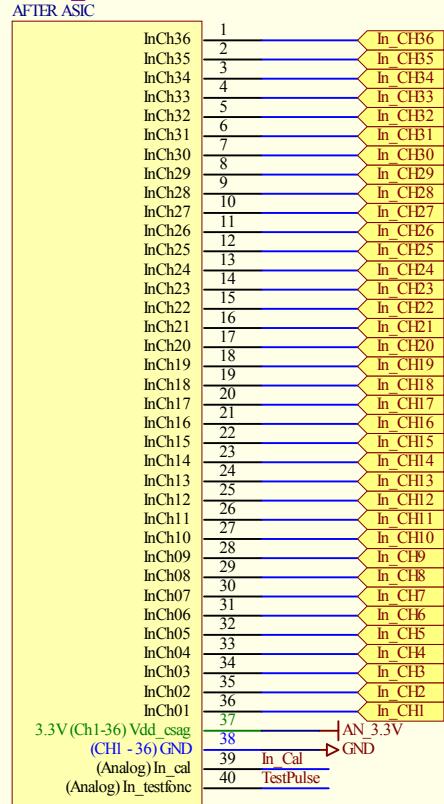
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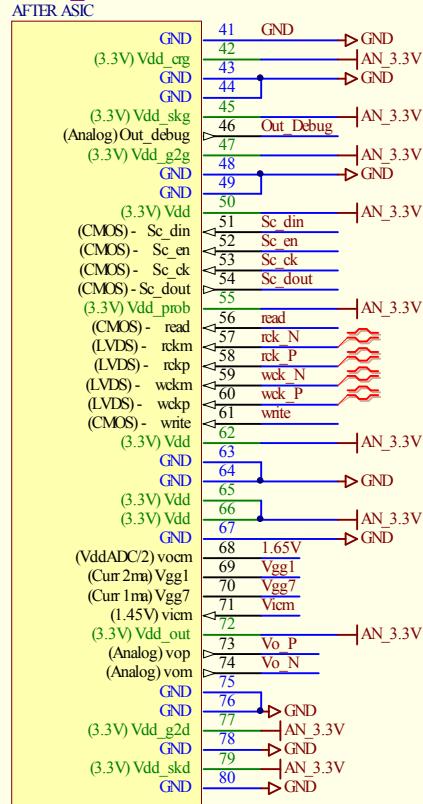
T2K FEB64 - Charge SUM Amplifier

Revision	Drawing #:	11		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3	
		Sheet #:	11 of 16		
1		Drawn by:	D. Bishop	Date: 25/06/2008	
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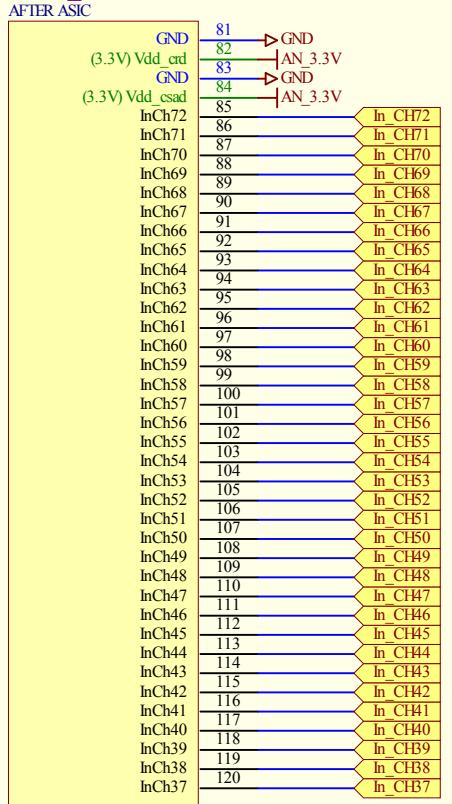
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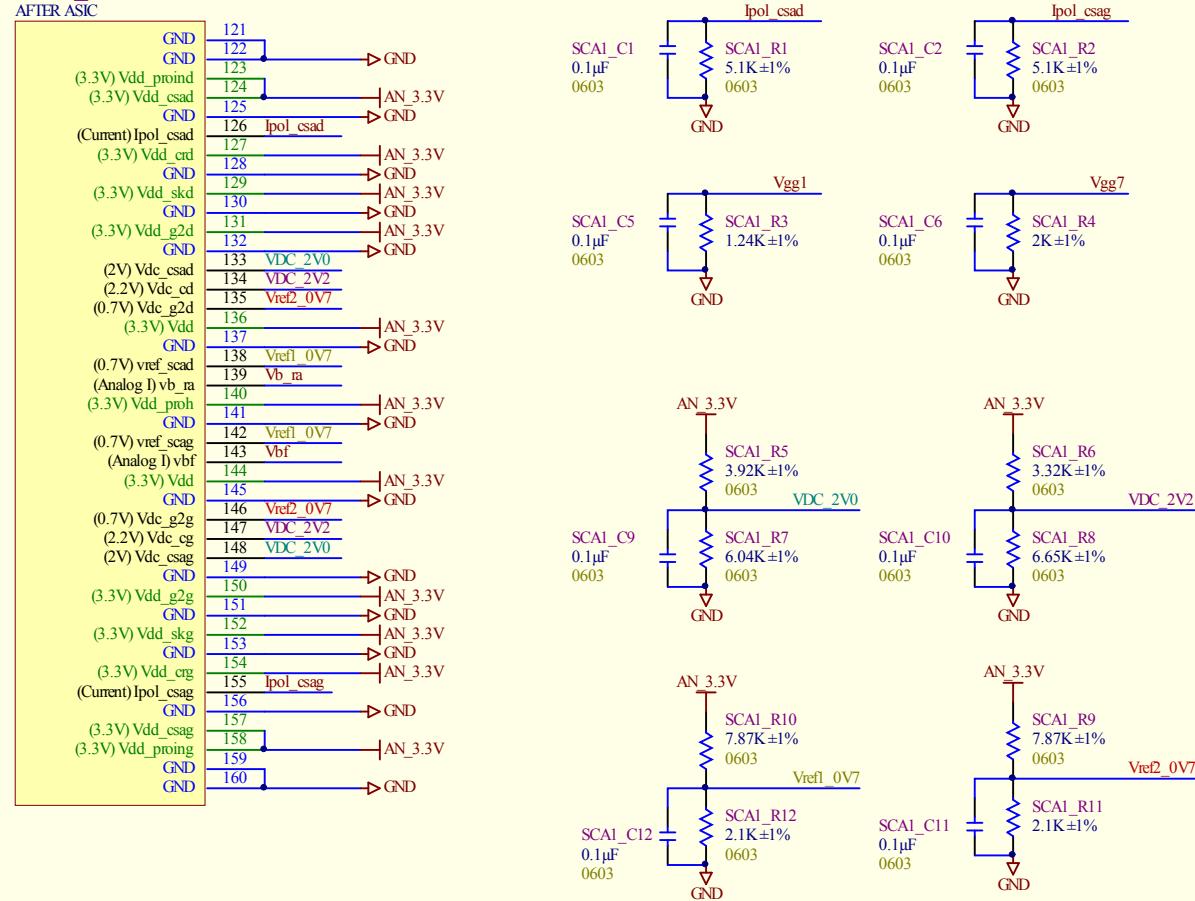
SCA1 U1B



SCA1 U1C

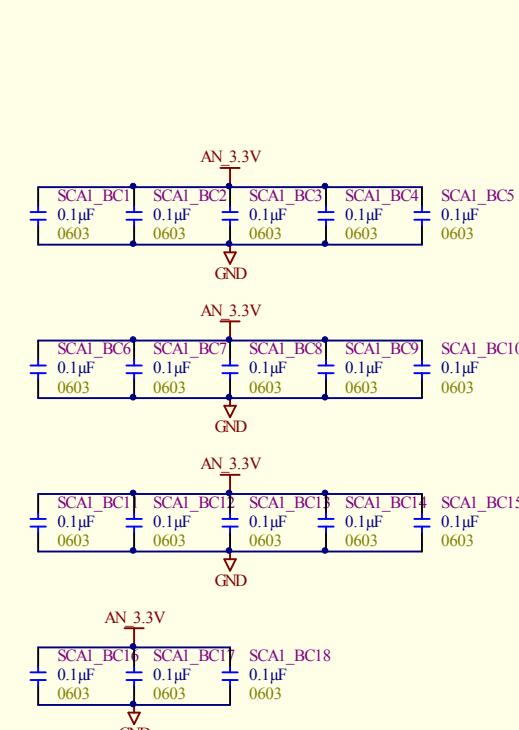


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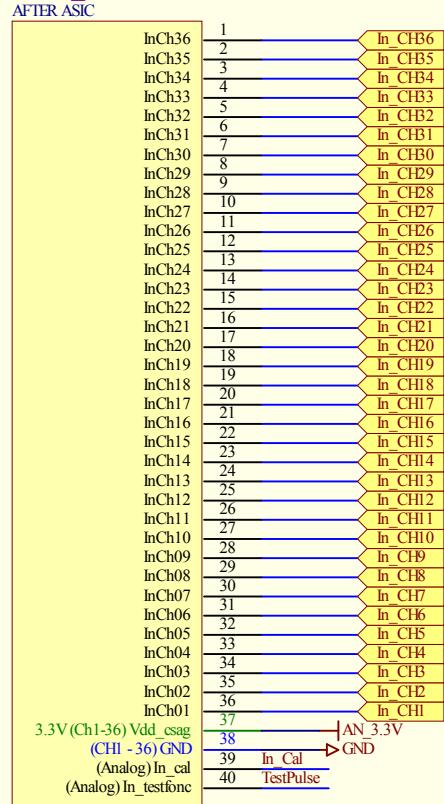


Pin 37	Vdd_c sag	9.83	CSA
Pin 157	Vdd_c sag	9.83	
Pin 84	Vdd_csd	9.83	
Pin 124	Vdd_csd	9.83	
Pin 42	Vdd_crg	3.9	CR Filter
Pin 154	Vdd_crg	3.9	
Pin 82	Vdd_crd	3.9	
Pin 127	Vdd_crd	3.9	
Pin 45	Vdd_skg	1.9	SK Filter
Pin 152	Vdd_skg	1.9	
Pin 79	Vdd_skd	1.9	
Pin 129	Vdd_skd	1.9	
Pin 47	Vdd_g2g	6.881	Gain-2
Pin 150	Vdd_g2g	6.881	
Pin 77	Vdd_g2d	6.881	
Pin 131	Vdd_g2d	6.881	
Pin 50	Vdd	3.676	
Pin 144	Vdd	3.676	
Pin 66	Vdd	6.62	
Pin 136	Vdd	6.62	
Pin 62	Vdd	0.343	
Pin 65	Vdd	0	
Pin 72	Vdd_out	16.03	
Pin 126	Ipol_csd	0.2	
Pin 155	Ipol_csg	0.2	
Pin 69	Vgg1	2	
Pin 70	Vgg7	1	

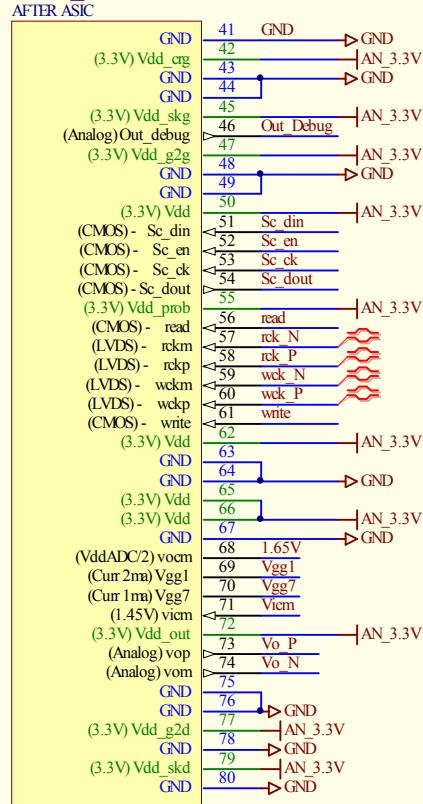
130.41 260.818



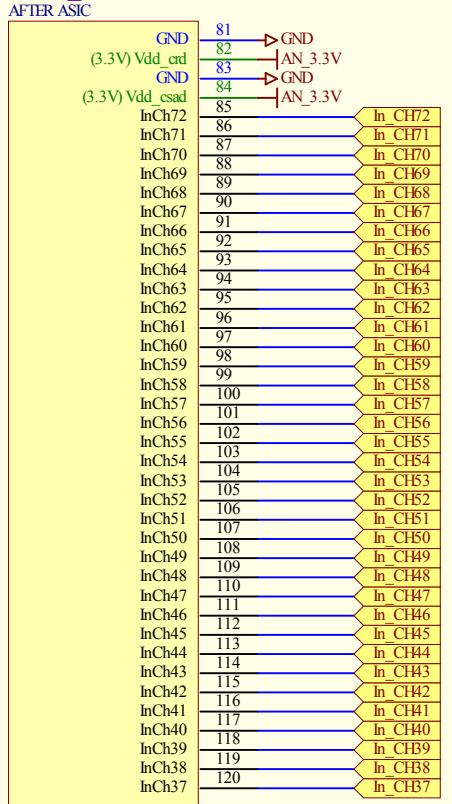
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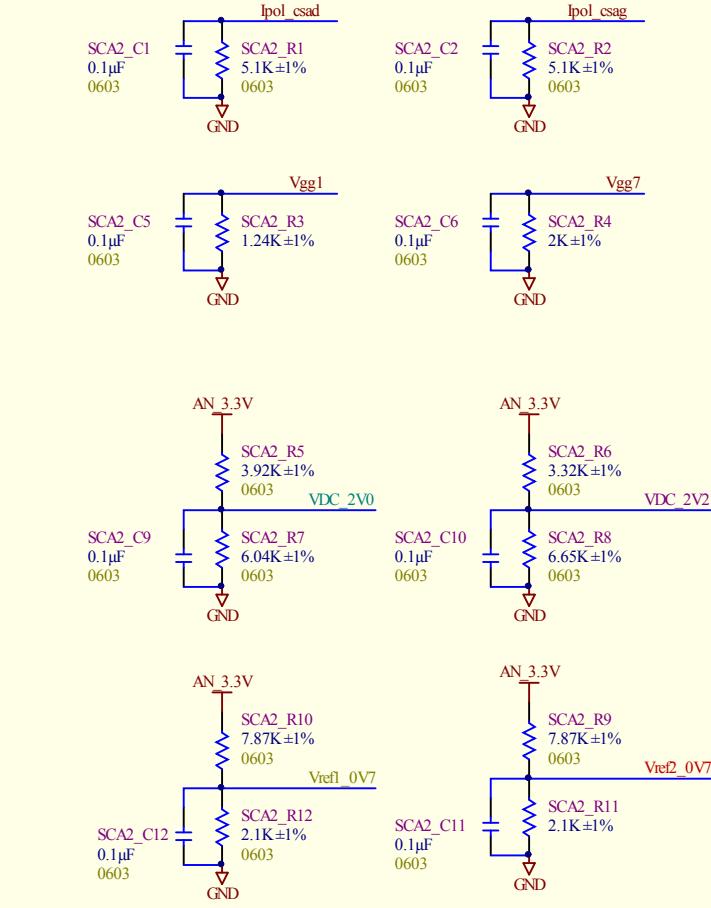
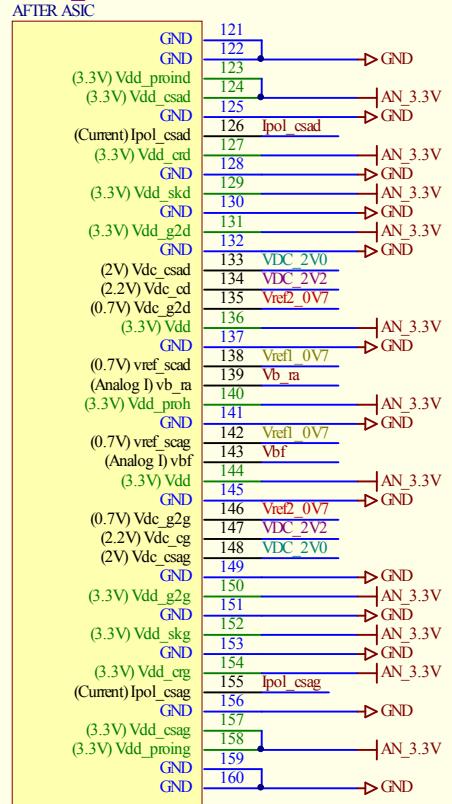
SCA2 U1B



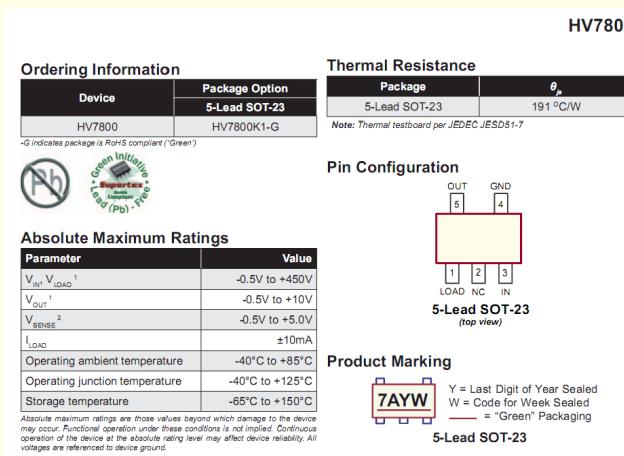
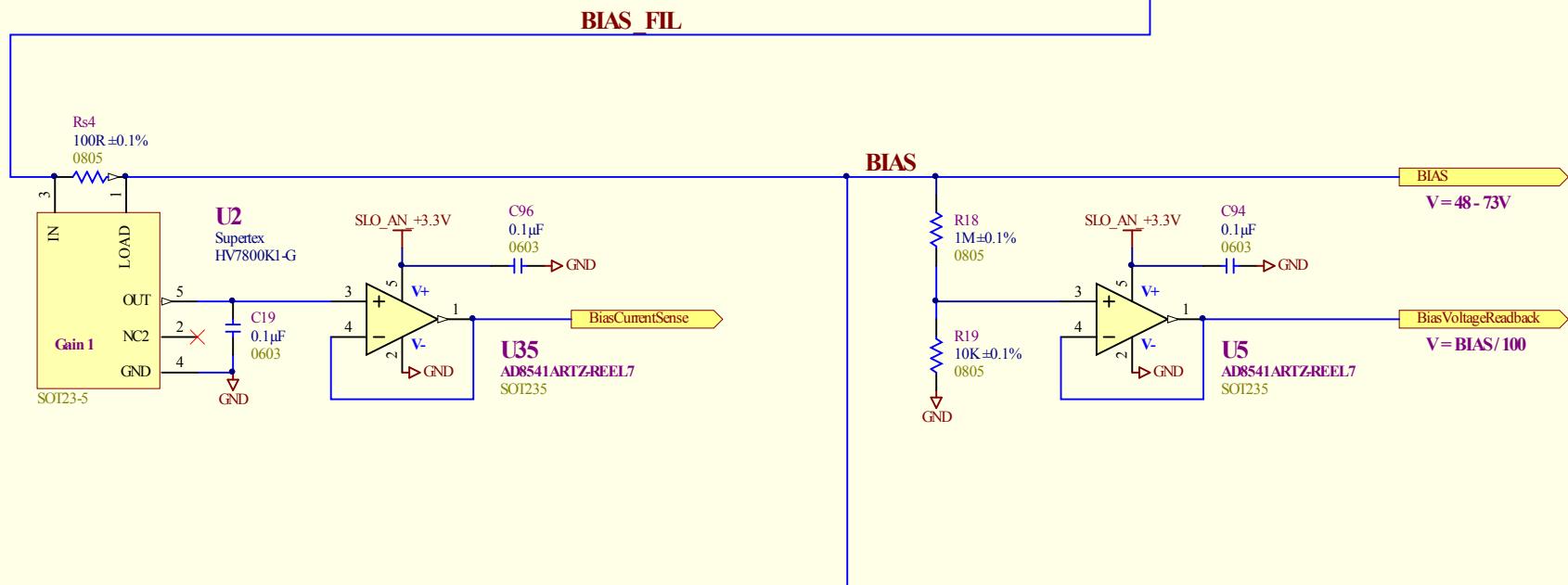
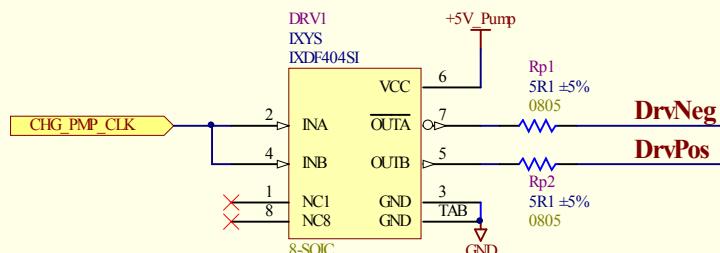
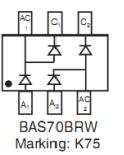
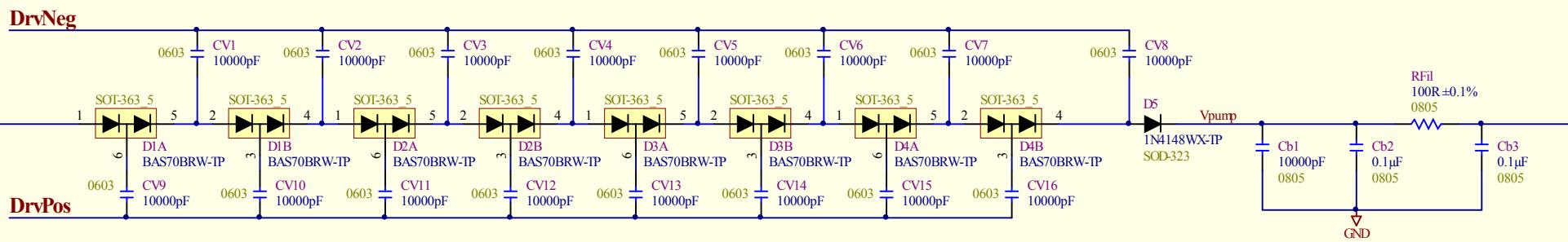
SCA2 U1C



SCA2 U1D

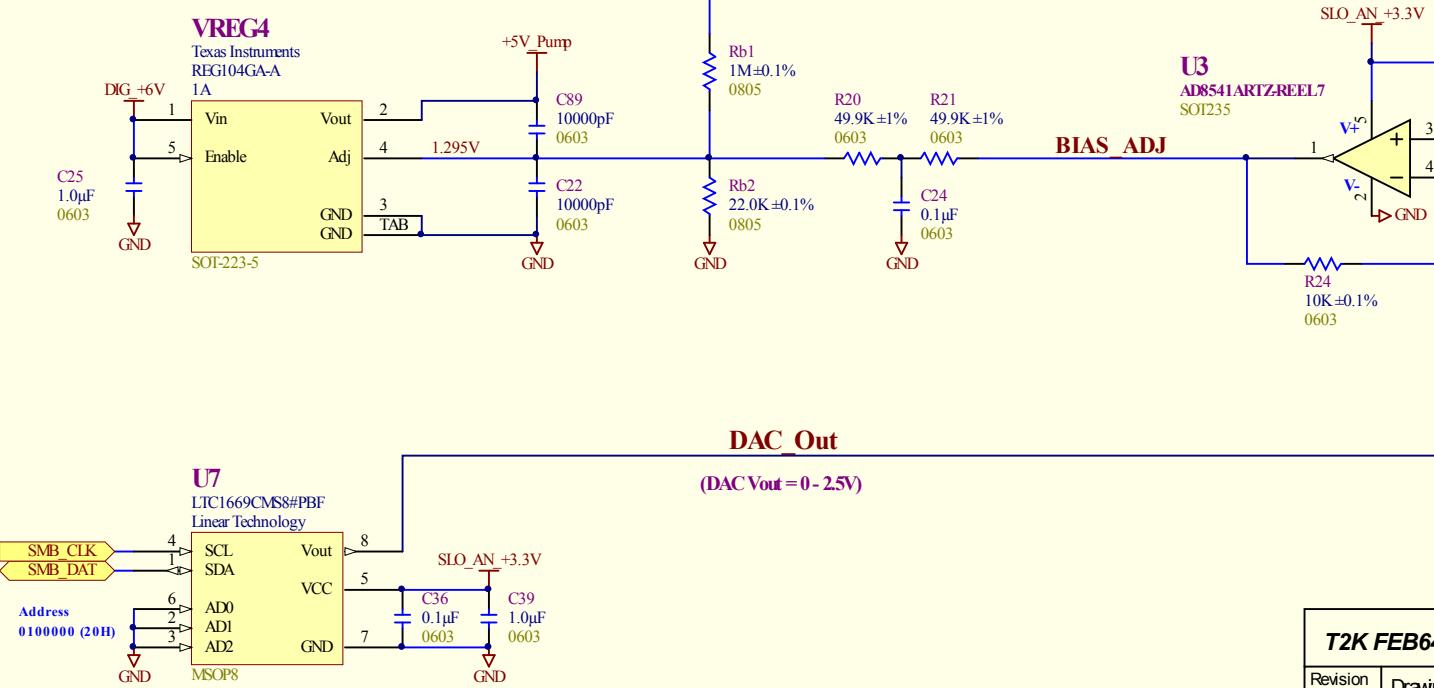


130.41 260.818



PACKAGE/ORDER INFORMATION

TOP VIEW		ORDER PART NUMBER	
SDA 1	8 V_{OUT}	LTC1669CMS8	LTC1669-8CMS8
AD1 2	7 GND	LTC1669IMS8	LTC1669-8IMS8
AD2 3	6 ADDO	MS8 PACKAGE	
SCL 4	5 V_{CC}	LTAHV	LTAHT
MS8 PACKAGE		LTAHX	LTAHU
$T_{JMAX} = 125^\circ\text{C}, \theta_{JA} = 150^\circ\text{C/W}$			



T2K FEB64: BIAS / Total Bias Current Sense

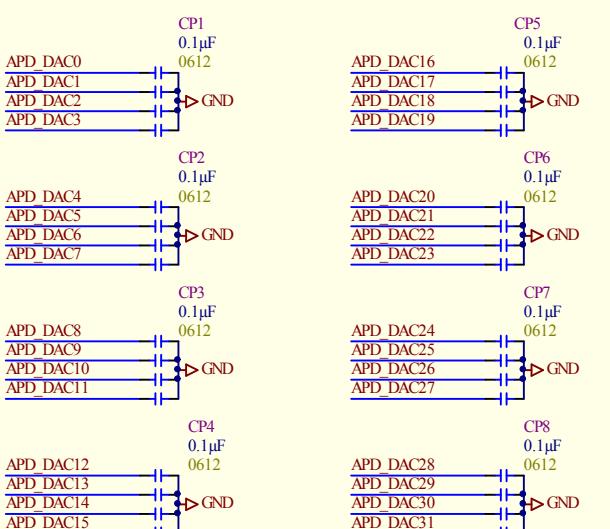
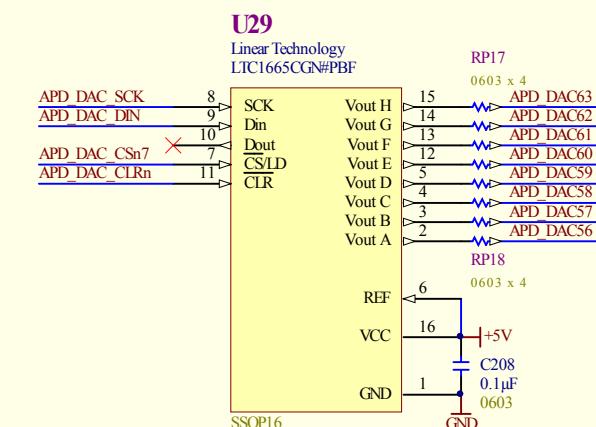
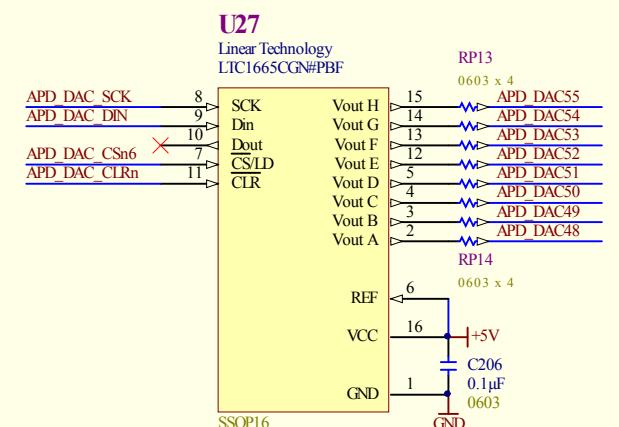
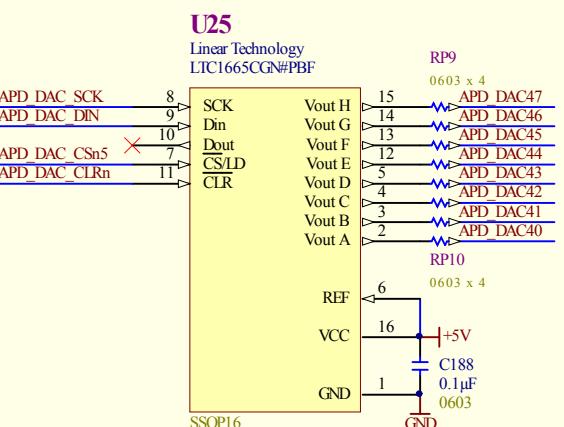
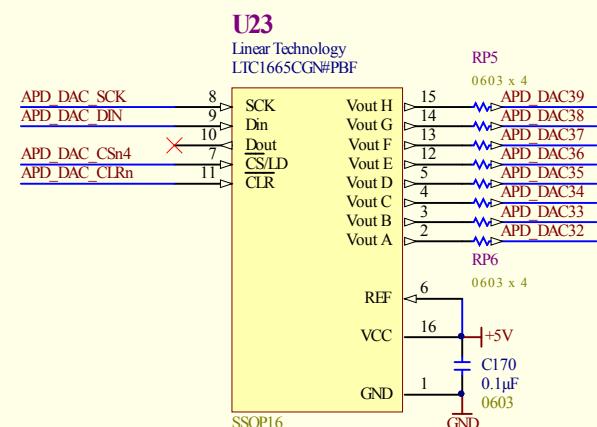
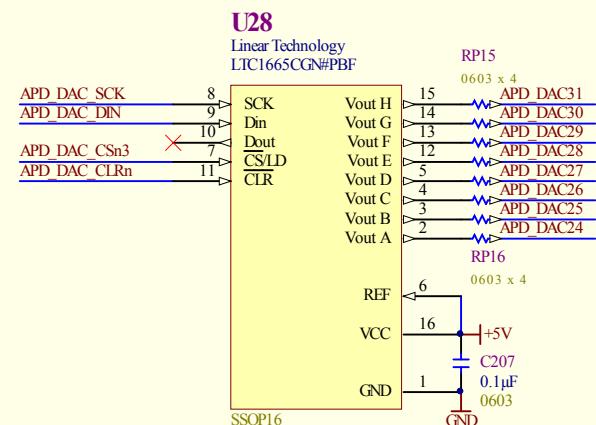
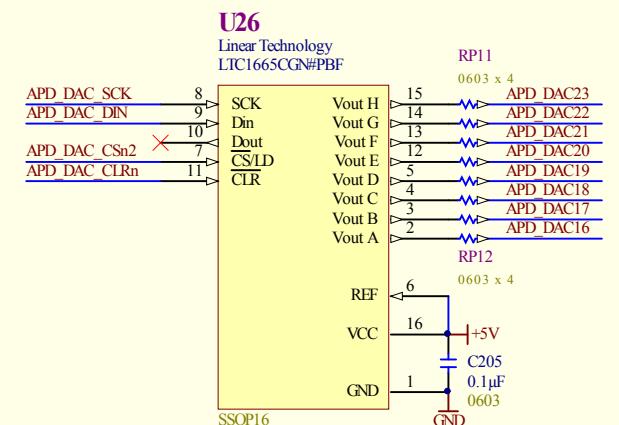
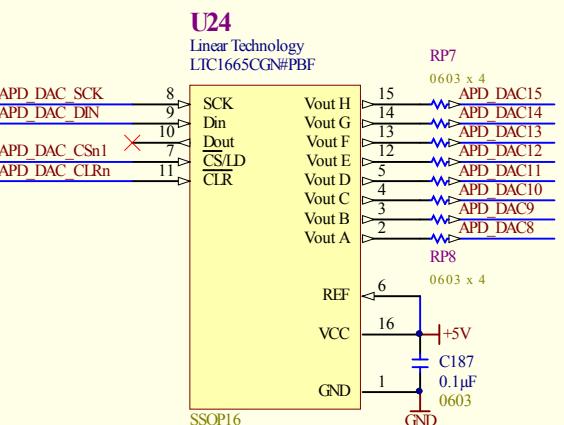
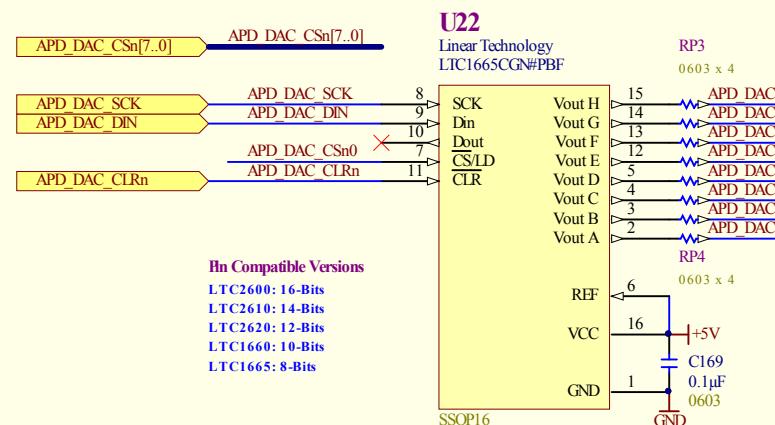
Revision	Drawing #	13	TRIUMF
1			4004 Westbrook Mall
			Vancouver, B.C.
			Canada
			V6T 2A3

Sheet #: 13 of 16 | Size: B

Drawn by: D. Bishop | Date: 25/06/2008

File: G:\AHWAT2KIT2K_FEB64\Rev1\T2K FEB_Rev1 - 80 Volt Charge Pump.SCHDOC | 2:38:00 PM

APD DAC[63..0] APD DAC[63..0]

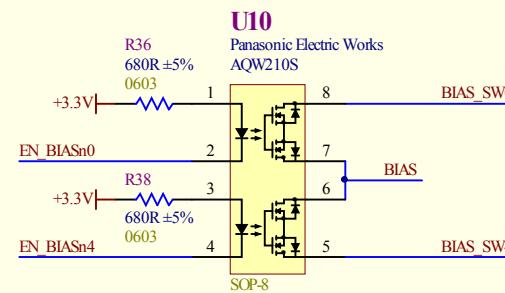
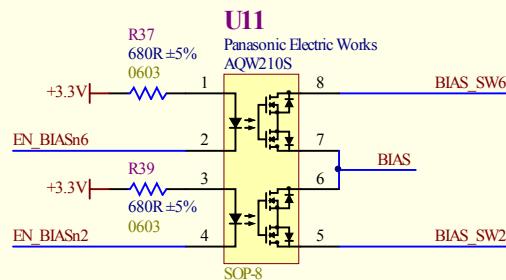
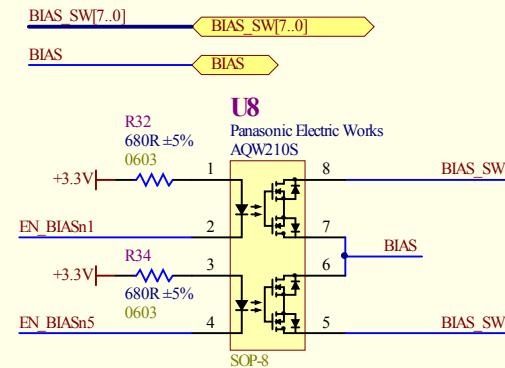
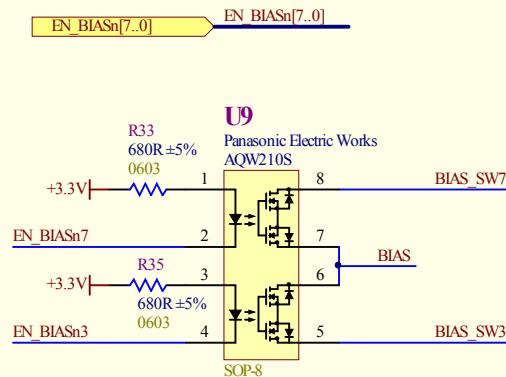


PACKAGE/ORDER INFORMATION

TOP VIEW	ORDER PART NUMBER
GND [1] VOUT A [2] VOUT B [3] VOUT C [4] VOUT D [5] REF [6] CS/LD [7] SCK [8]	LTC1665CGN LTC1665CN LTC1665IGN LTC1665IN LTC1660CGN LTC1660CN LTC1660IGN LTC1660IN
VCC [16] VOUT H [15] VOUT G [14] VOUT F [13] VOUT E [12] VOUT D [11] CLR [10] DOUT [9] DIN [8]	
GN PACKAGE 16-LEAD PLASTIC SSOP	N PACKAGE 16-LEAD PDIP
T _{JMAX} = 125°C, θ _{JA} = 150°C/W (GN) T _{JMAX} = 125°C, θ _{JA} = 100°C/W (N)	
GN PART MARKING	
1665	1660
1665I	1660I

T2K FEB64 - 64 Channel Bias Control

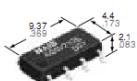
Revision	Drawing #	Sheet #:	Size:	TRIUMF
1	15	15 of 16	B	4004 Westbrook Mall Vancouver, B.C. Canada V6T 2A3
				Drawn by: D.Bishop Date: 25/06/2008
				File: G:\AHWAT2KIT\T2K_FEB64\Rev1\T2K FEB_Rev1 - 64 Channel Bias Control.SCHD
				DC:38:00 PM



Panasonic
ideas for life

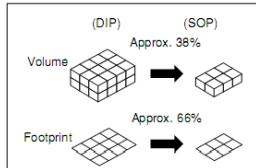
Super miniature design,
SOP (2 Form A) 8-pin type.
Controls load voltage
350V, 400V.

GU PhotoMOS (AQW210S)



mm inch

x (H) 2.1 mm (W) .173x (L) .369x (H) .083
inch —approx. 38% of the volume and
66% of the footprint size of DIP type Photo-
MOS Relays.



3. Controls low-level analog signals
PhotoMOS relays feature extremely low
closed-circuit offset voltage to enable
control of low-level analog signals without
distortion.

4. Low-level off state leakage current
In contrast to the SSR with an off state
leakage current of several milliamperes,
the PhotoMOS relay features a very small
off state leakage current of typ. 100 pA
even with the rated load voltage of 400 V
(AQW214S)

TYPICAL APPLICATIONS

- Telephones
- Measuring instruments
- Computer
- Industrial robots
- High-speed inspection machines.

FEATURES

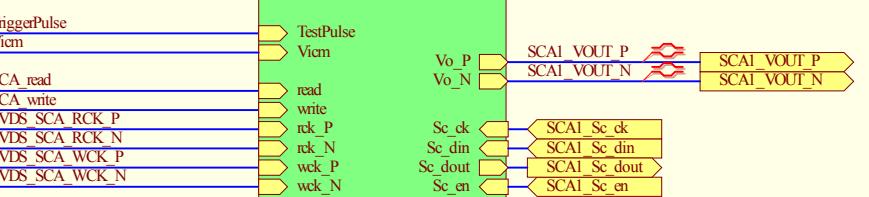
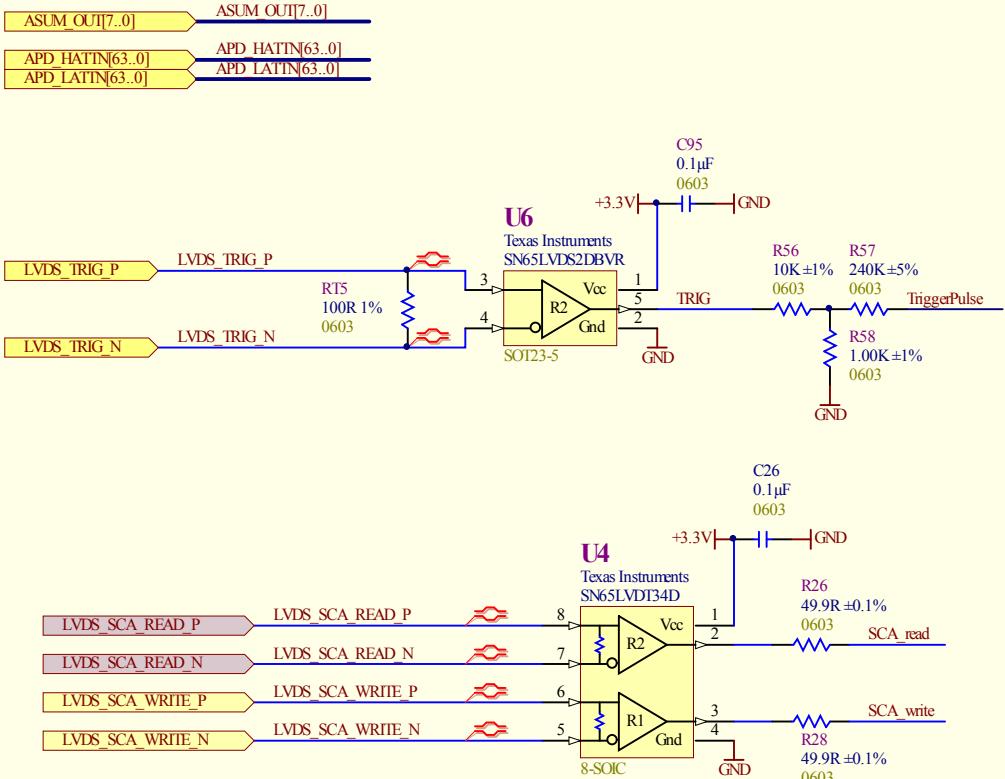
1. 2 channels in super miniature de-
sign
- The device comes standard in a tape and
reel (1,000 pcs./reel) to facilitate automati-
cic insertion machines.

The device comes in a super-miniature
SO package measuring (W) 4.4 x (L) 9.37

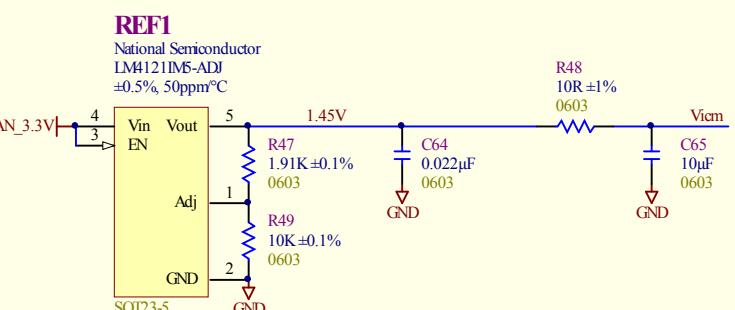
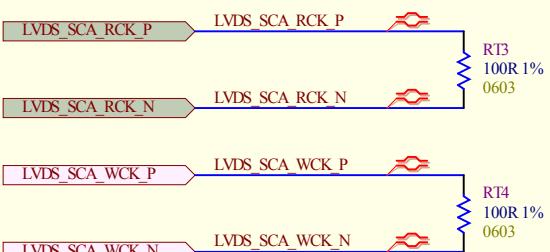
T2K FEB64 - 8 Channel Mosfet Switch

Revision	Drawing #:	16	TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
1	Sheet #:	16 of 16	Size: A
	Drawn by:	D.Bishop	Date: 25/06/2008





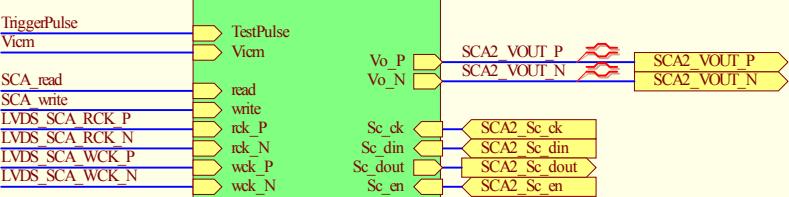
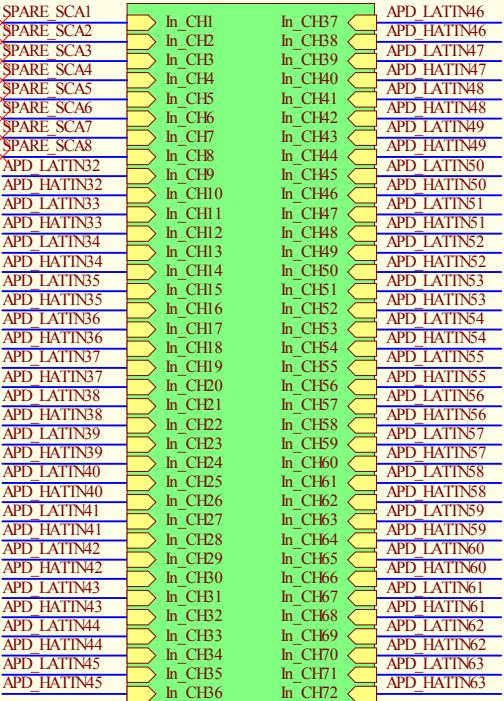
SCA - Icc approx 130mA



$$V_{out} = 1.216V(1+R47/R49)$$

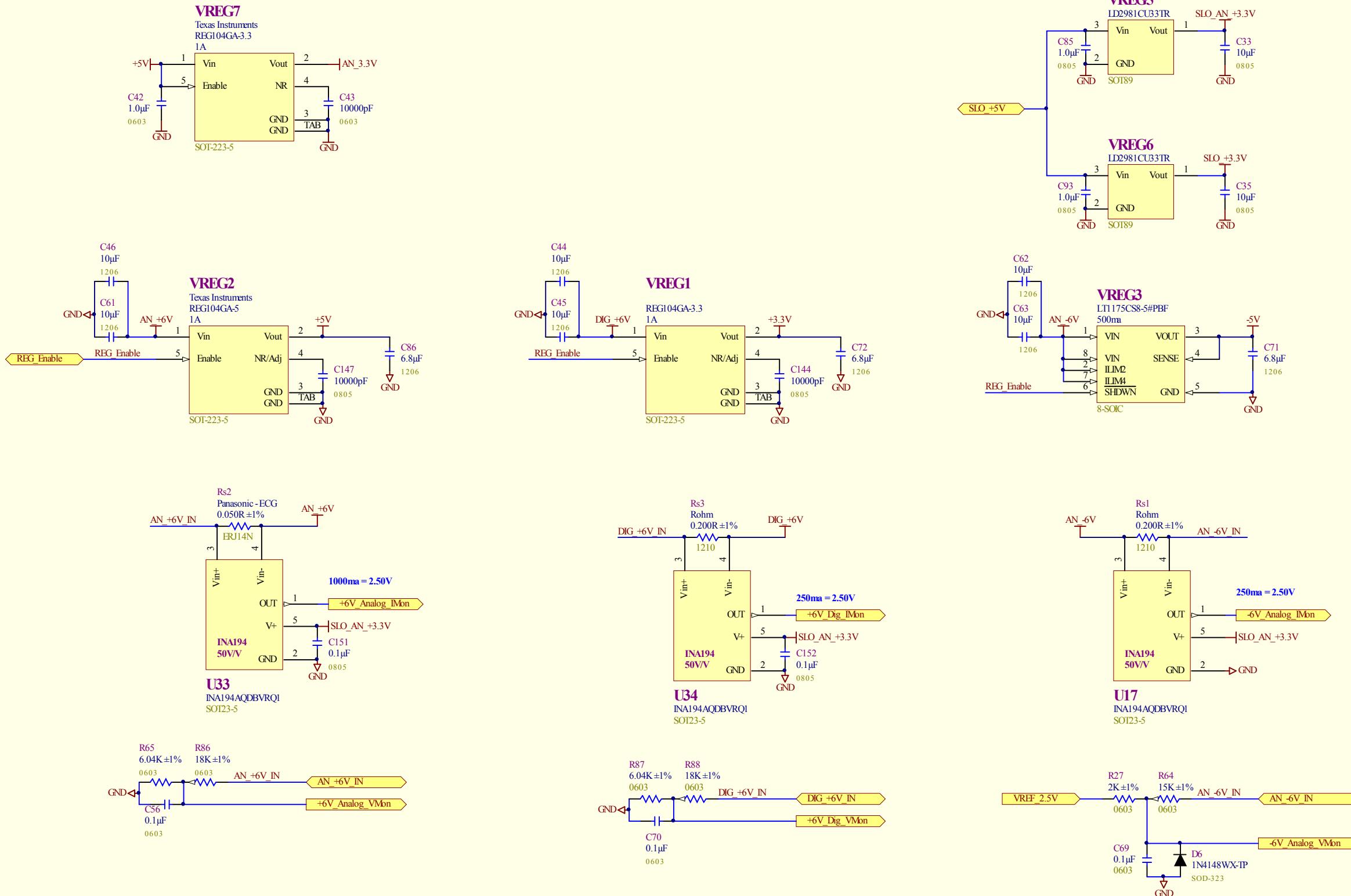
$$V_{out} = 1.216V(1.191) = 1.448 \text{ Volts}$$

Vicm= +60uA / -26uA



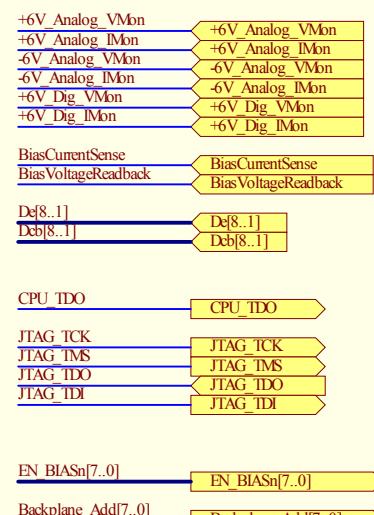
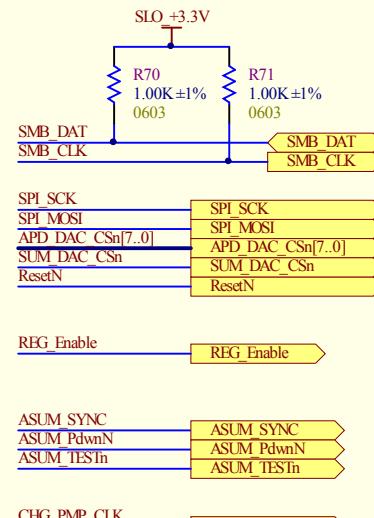
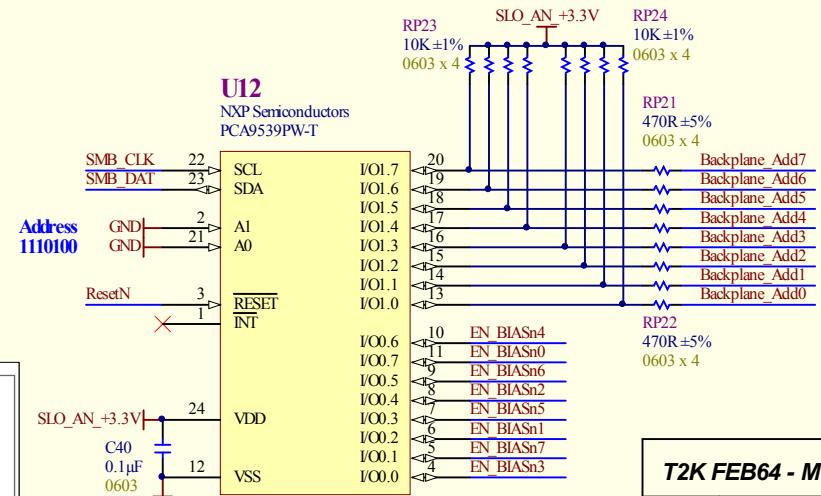
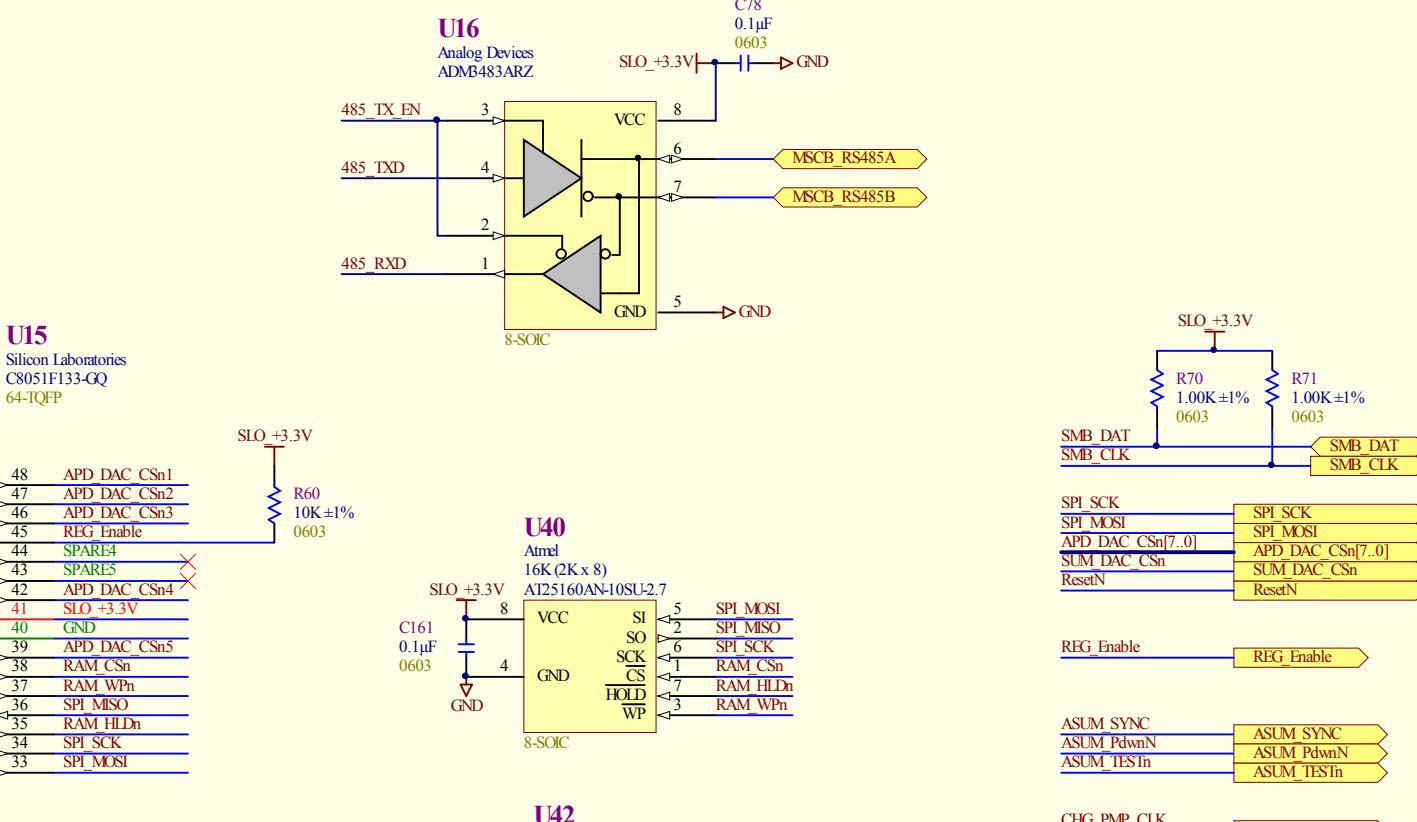
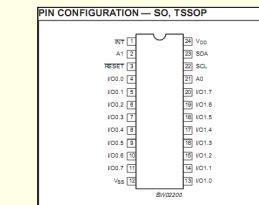
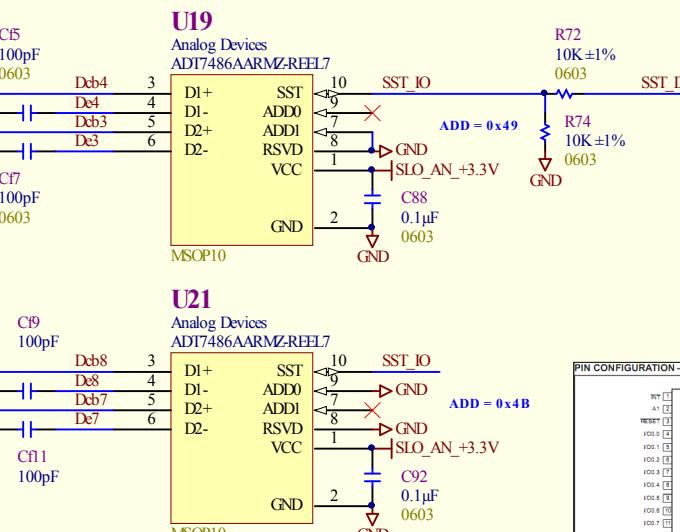
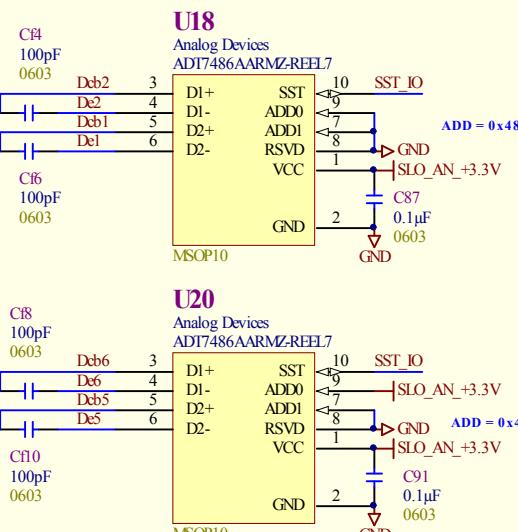
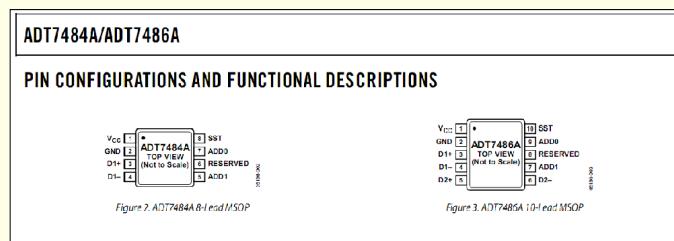
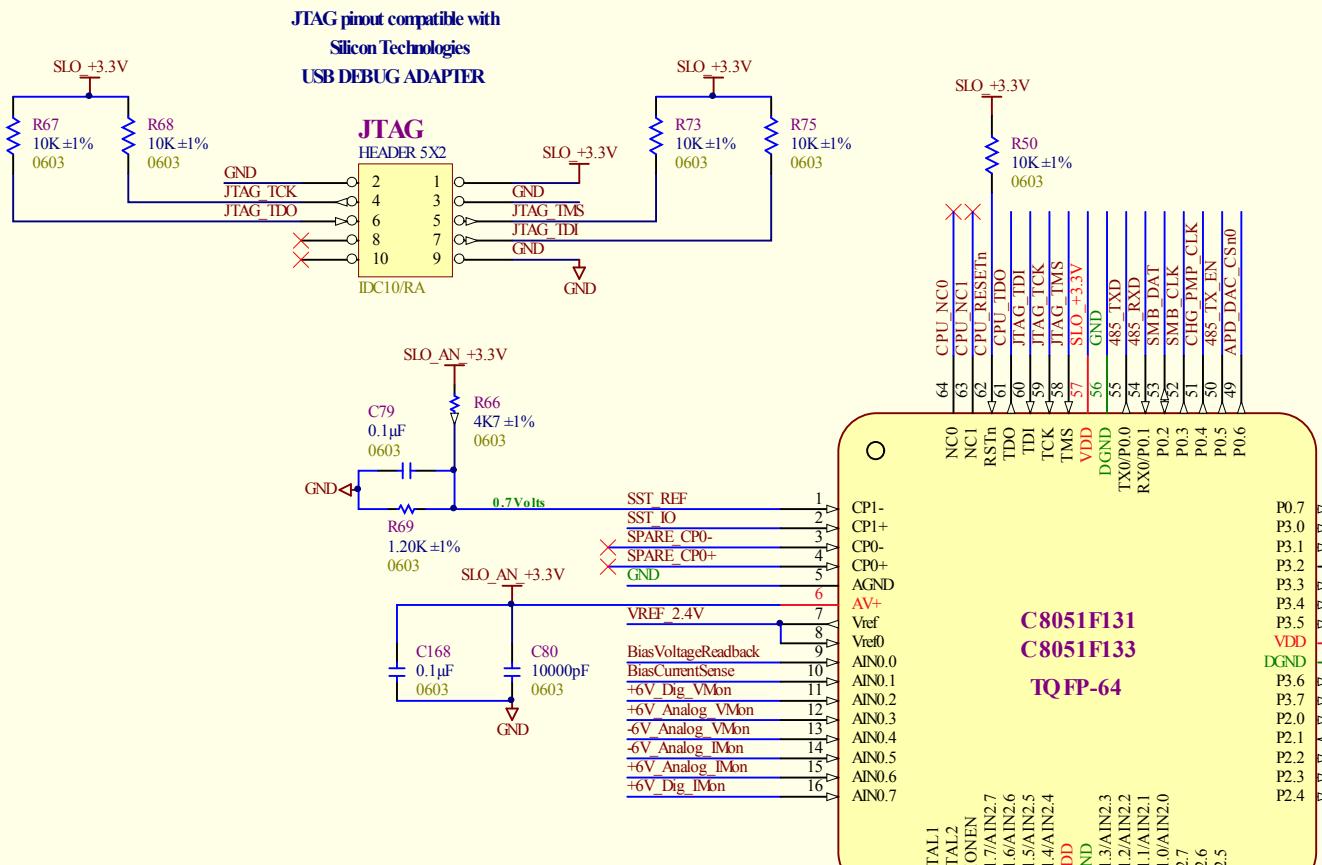
SCA - Icc approx 130mA

Revision 1	Drawing # 2	<i>TRIUMF</i> 4004 Westbrook Mall Vancouver, B.C. Canada V6T 2A3	
	Sheet #: 2 of 16 Size: B		
	Drawn by: D.Bishop	Date: 25/06/2008	
	File: G:\AHW\T2K\T2K_FEB64\Rev1\T2K FEB_Rev1 - SCA Interface.SCHDOC		2:38:00 PM



T2K FEB64 - Voltage Regulators - Volt/Curr Monitor

Revision	Drawing #	Sheet #:	Size:	TRIUMF
1	3	3 of 16	B	4004 Westbrook Mall
				Vancouver, B.C.
				Canada
				V6T 2A3
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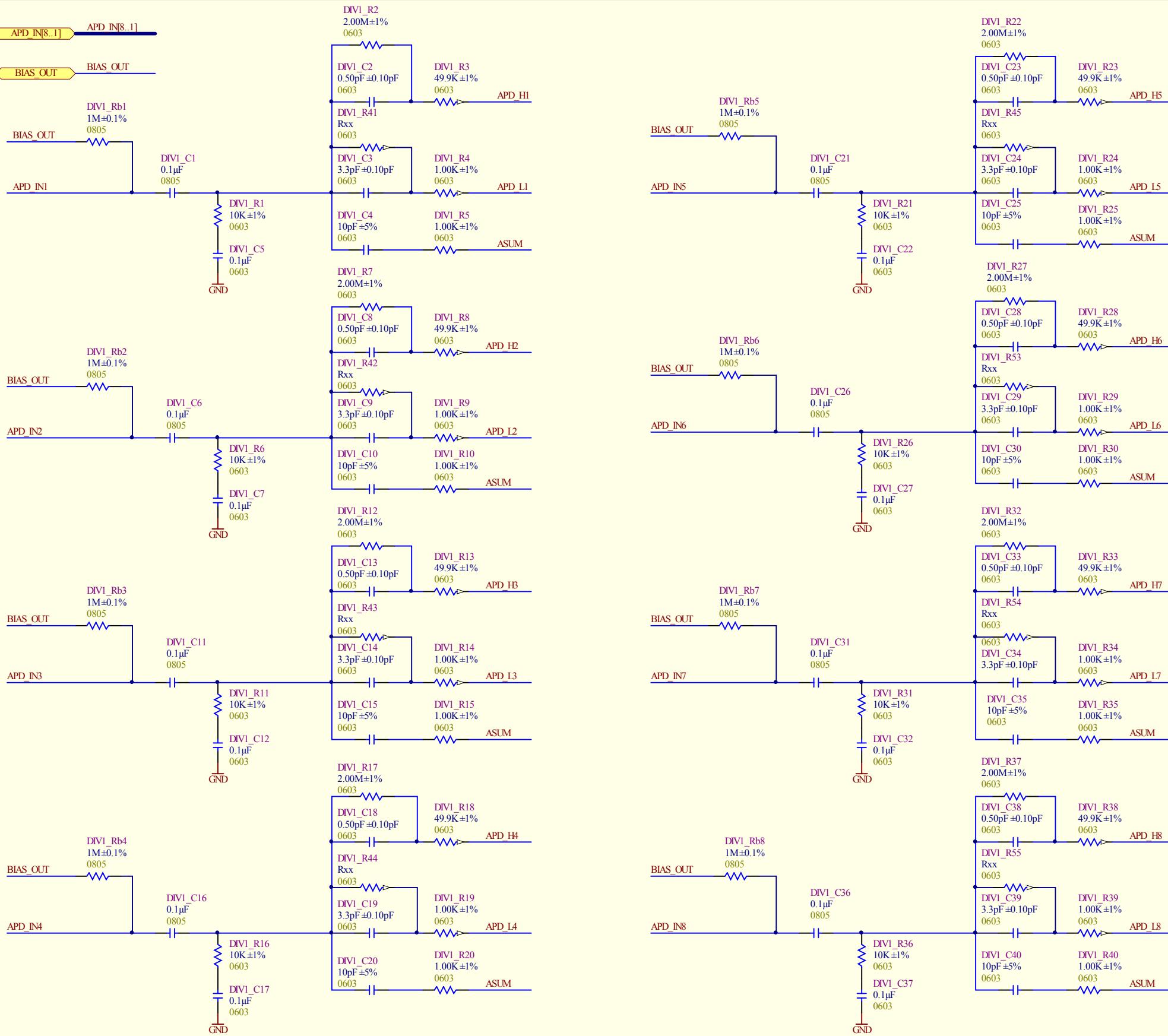


T2K FEB64 - MIDAS Slow Control

Revision	Drawing #	Sheet #:	Size:	Date:
1	4	4 of 16	B	25/06/2008
		Drawn by:	D. Bishop	
			V6T 2A3	

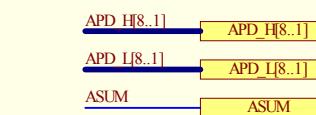
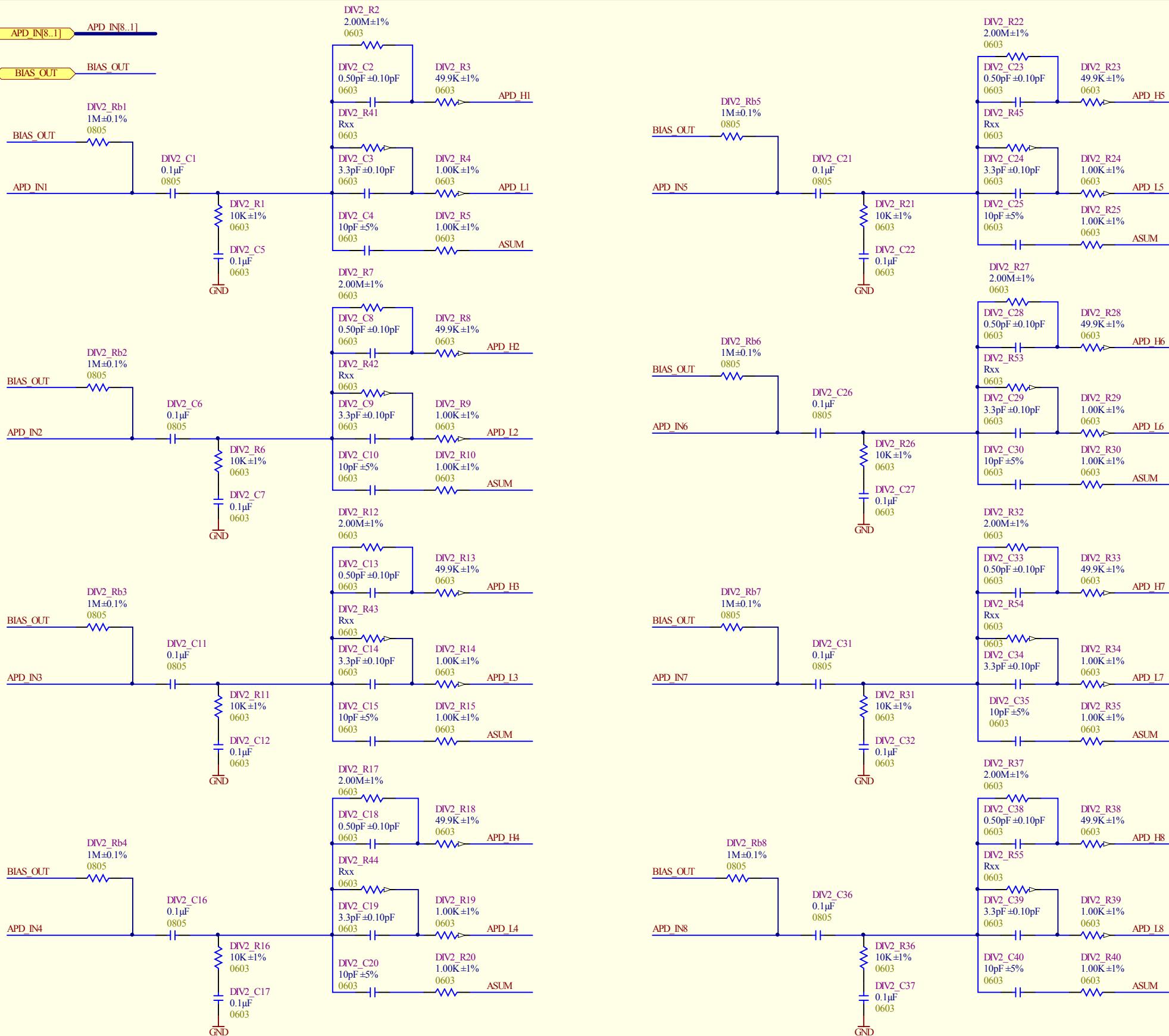


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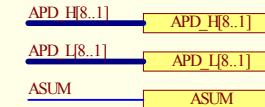
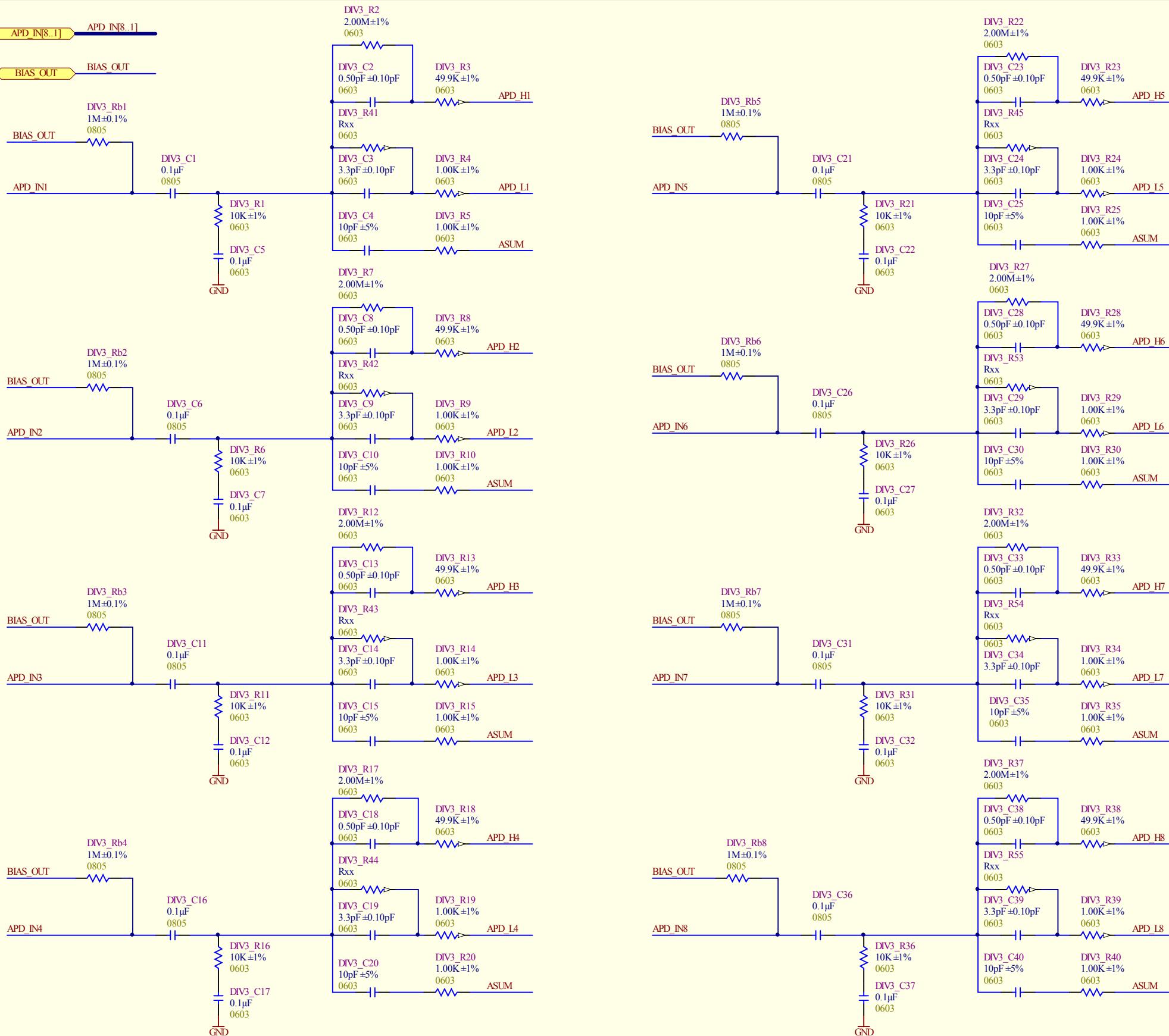
T2K FEB64 - Charge Division

Revision	Drawing #	Sheet #:	Size:	TRIUMF
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				V6T 2A3
				
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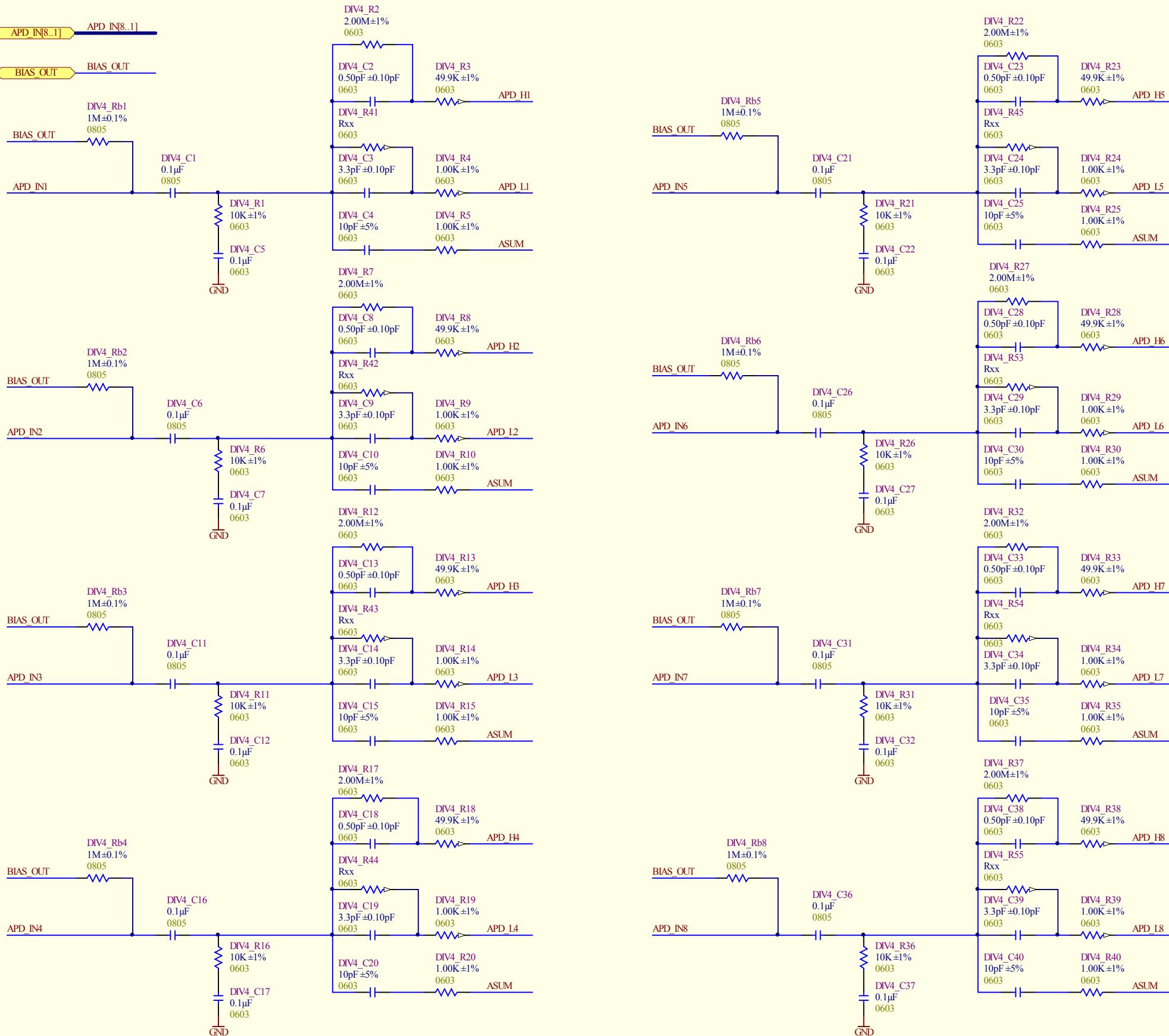
T2K FEB64 - Charge Division

Revision	Drawing #	Sheet #:	Size:	TRIUMF
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				Canada
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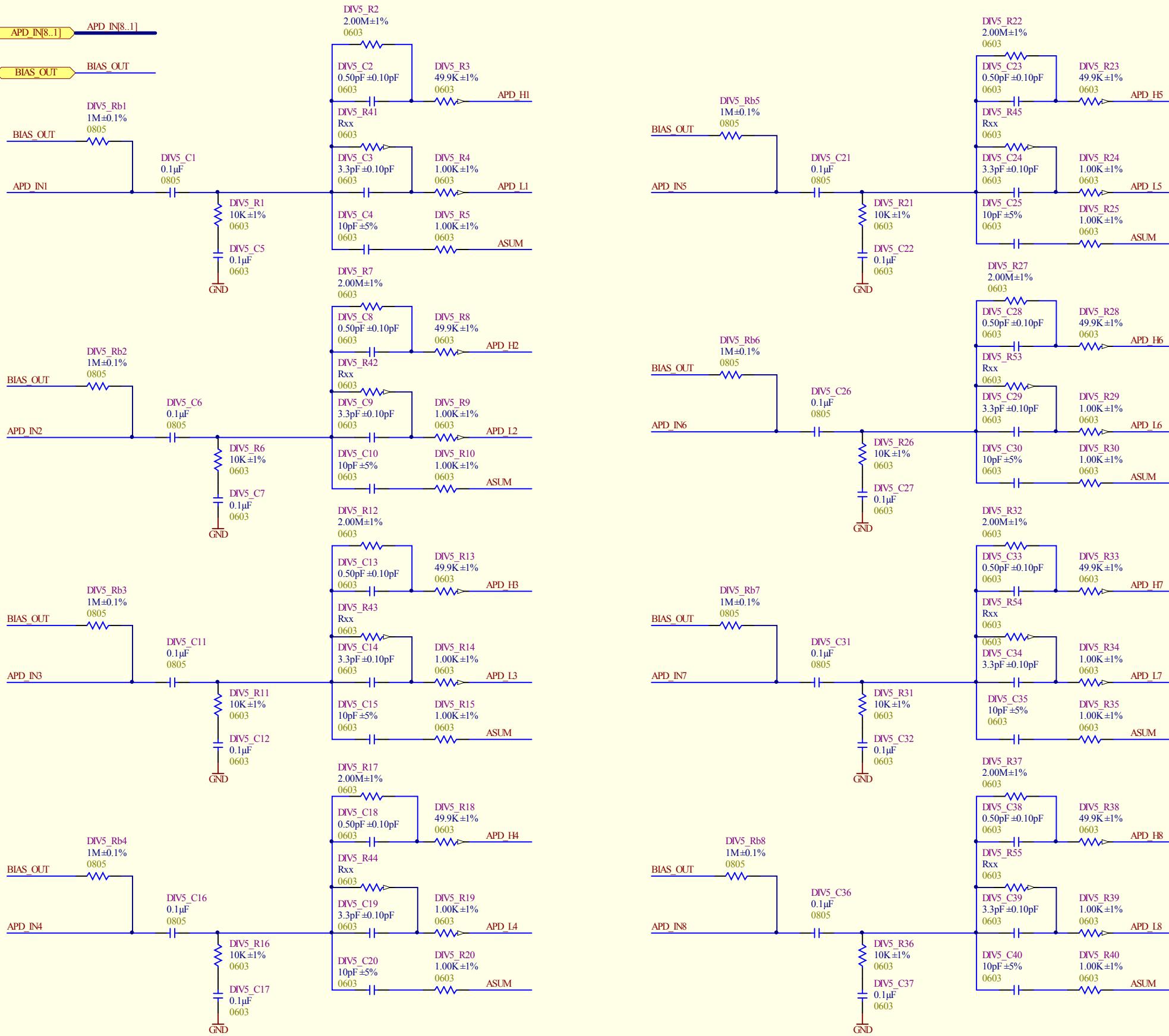
T2K FEB64 - Charge Division

Revision	Drawing #	Sheet #:	Size:	TRIUMF
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				Vancouver, B.C.
				Canada
				V6T 2A3
				
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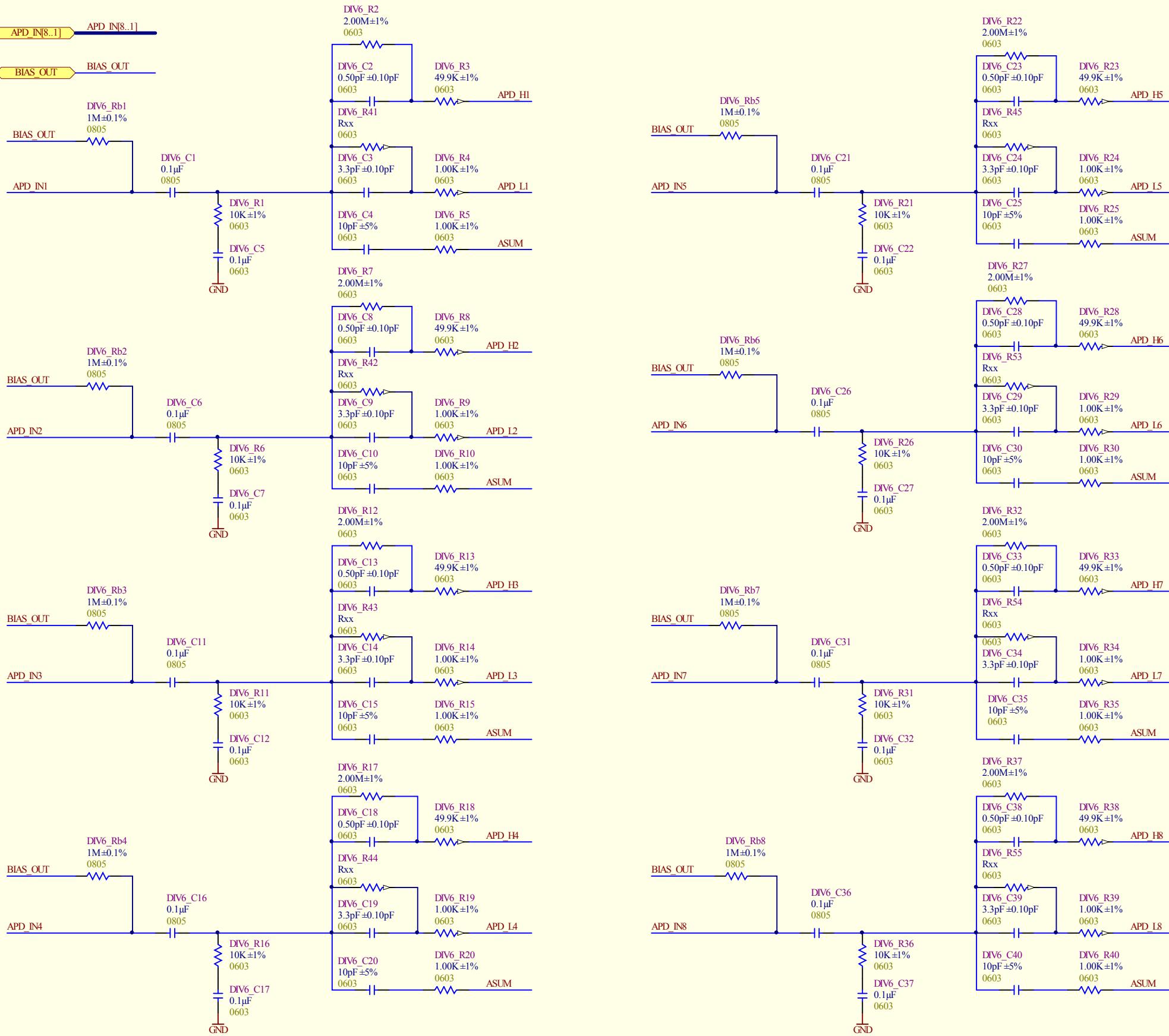
T2K FEB64 - Charge Division

Revision	Drawing #	Sheet #:	Size:	TRIUMF
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				Canada
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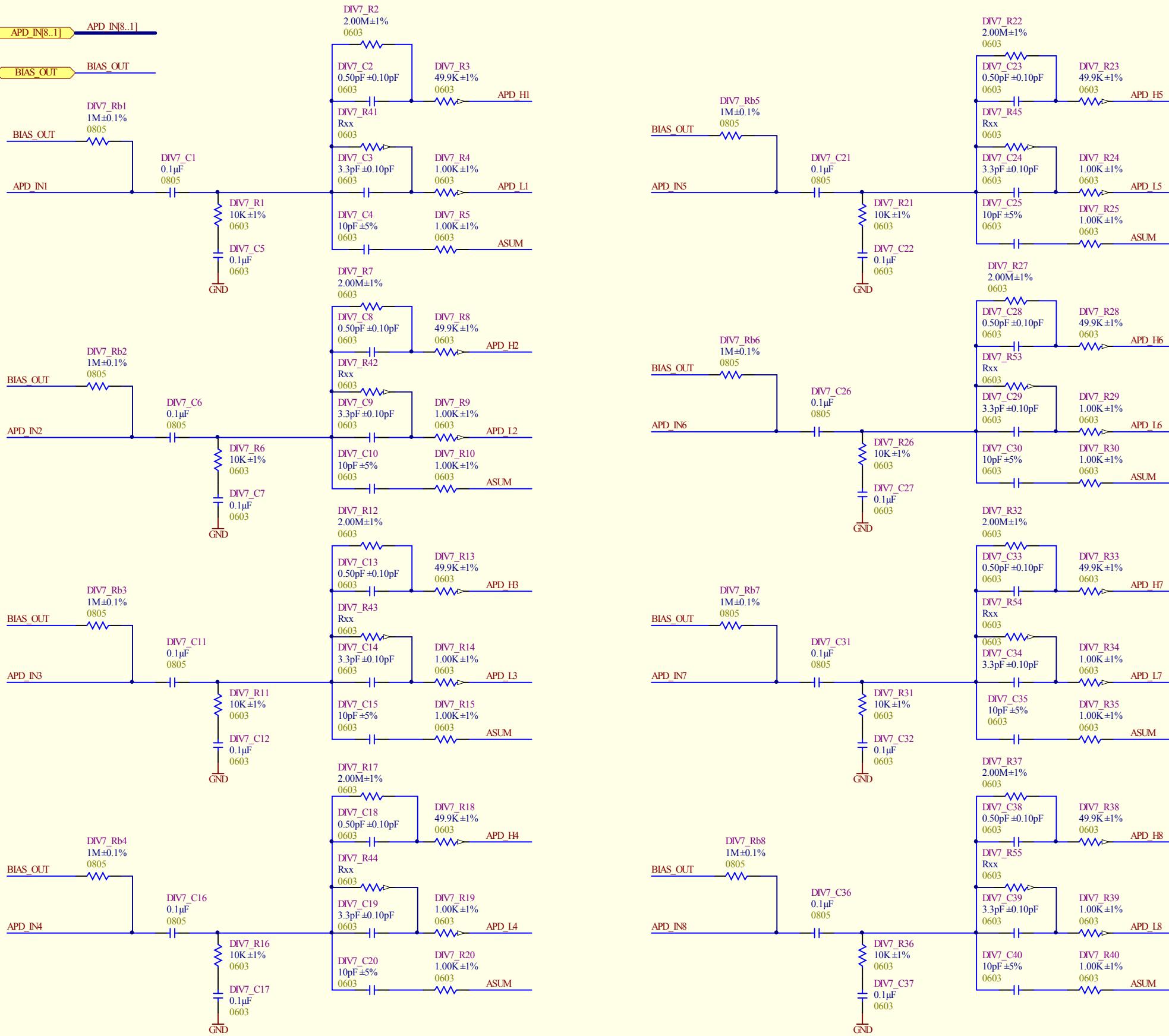
T2K FEB64 - Charge Division

Revision	Drawing #	Sheet #:	Size:	TRIUMF
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				Vancouver, B.C.
				Canada
				V6T 2A3
				
				2:38:01 PM
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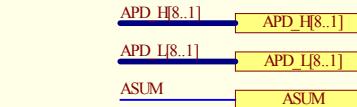
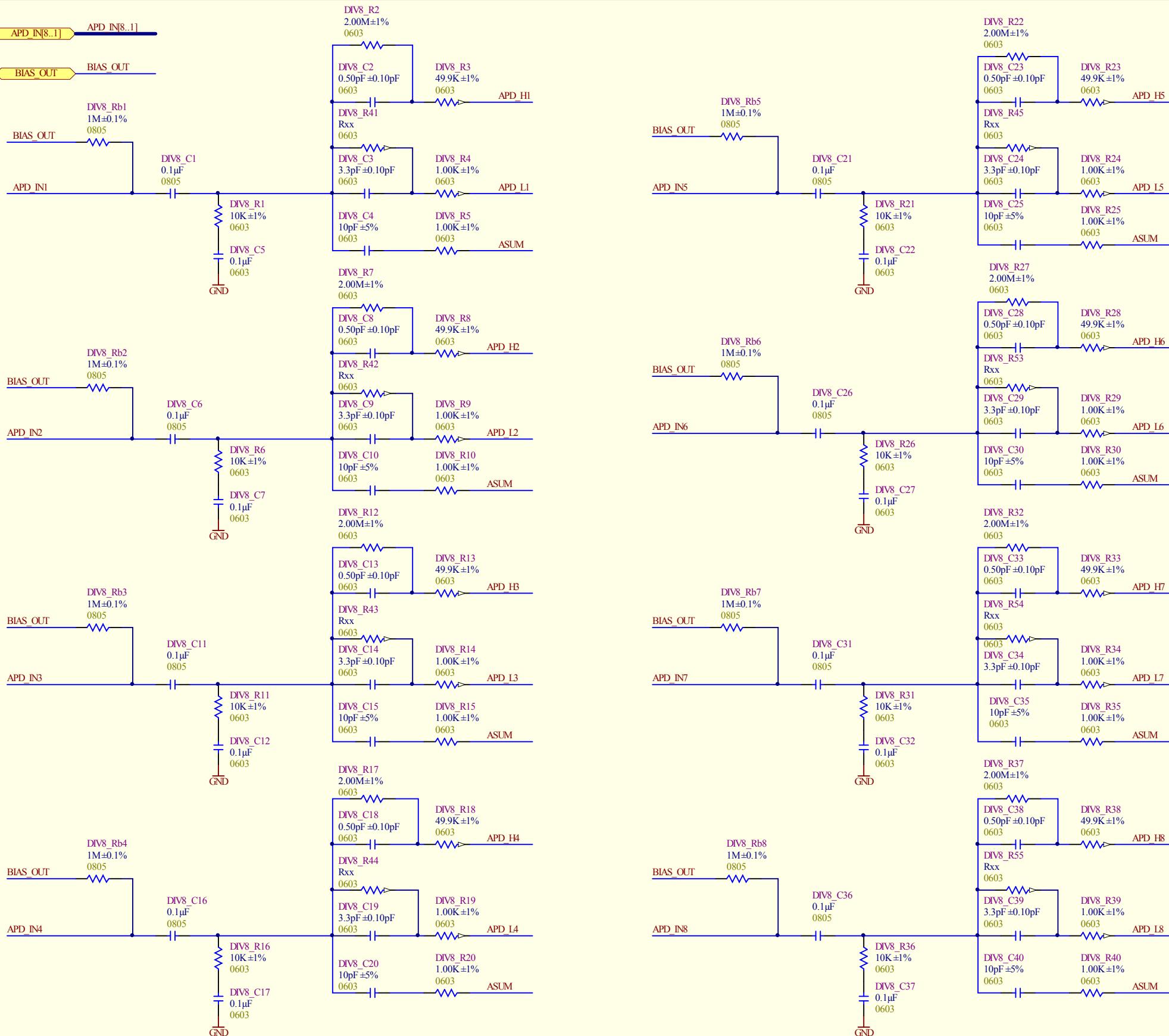
T2K FEB64 - Charge Division

Revision	Drawing #	Sheet #:	Size:	TRIUMF
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				Canada
				V6T 2A3
				
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				2:38:02 PM



T2K FEB64 - Charge Division

Revision	Drawing #	Sheet #:	Size:	TRIUMF
1	5	5 of 16	B	4004 Westbrook Mall
				Vancouver, B.C.
				Canada
				V6T 2A3
				
				File: G:\AHWAT2\KIT2K_FEB64\Rev1\T2K_FEB_Rev1-Charge Division.SCHDOC
				2:38:02 PM



T2K FEB64 - Charge Division

Revision **1**

Drawing # **5**

Sheet # **5** of **16**

Size: **B**

TRIUMF
4004 Westbrook Mall
Vancouver, B.C.
Canada
V6T 2A3



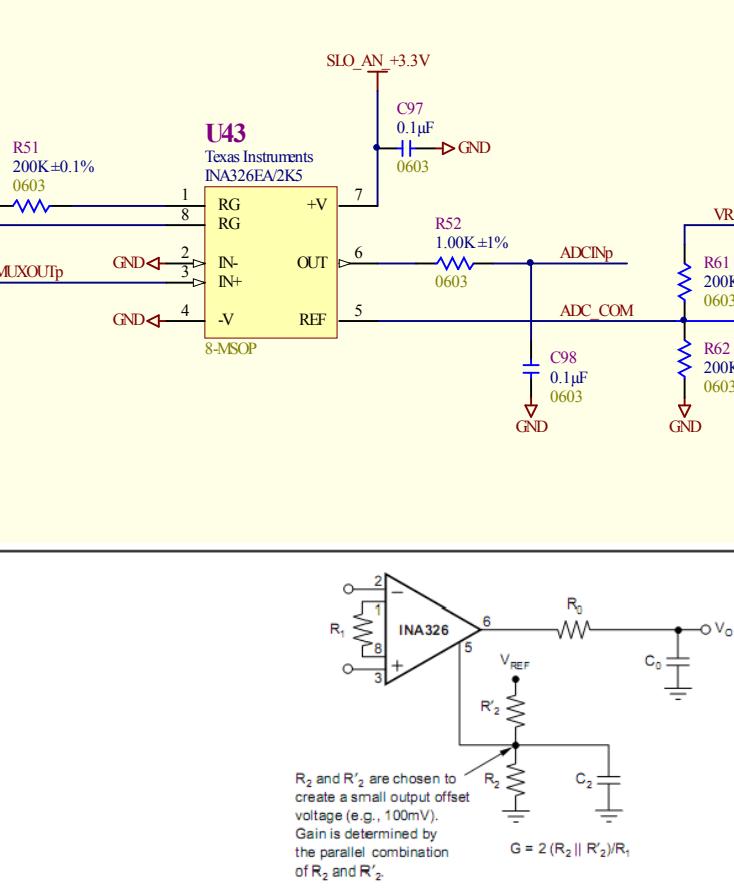
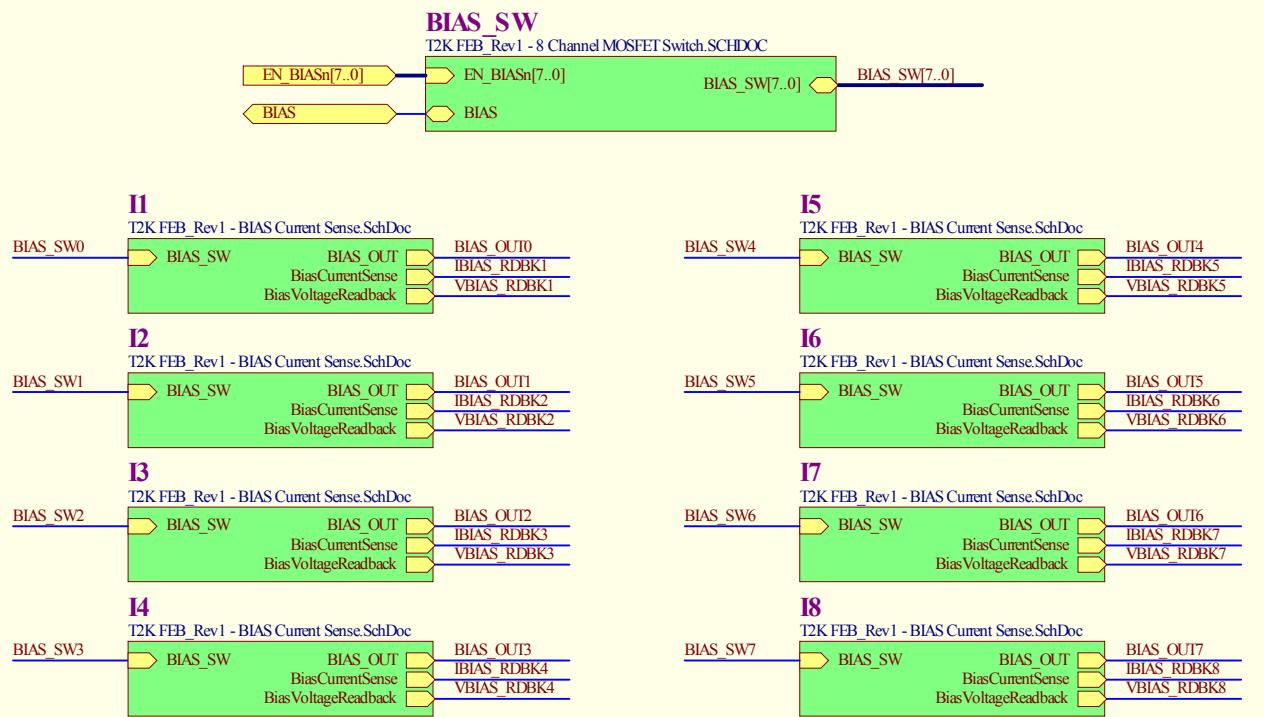
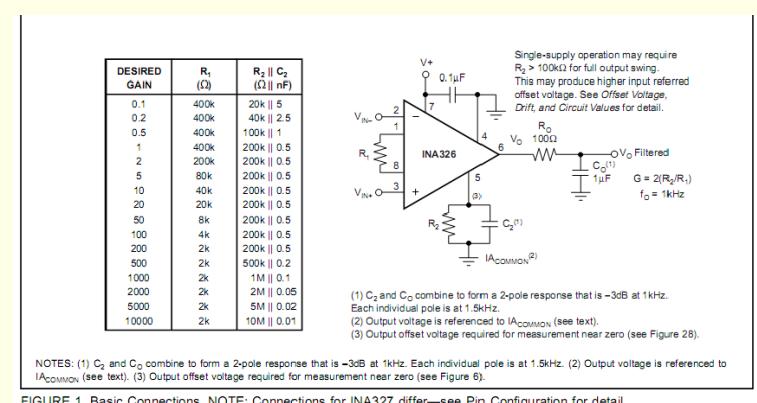


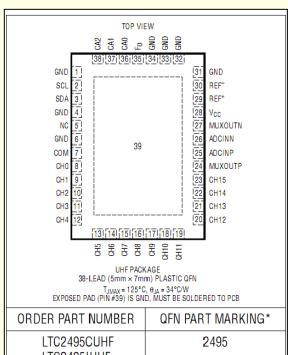
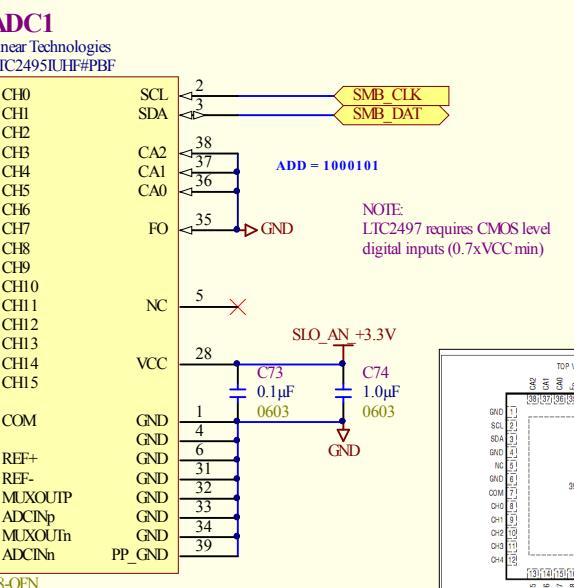
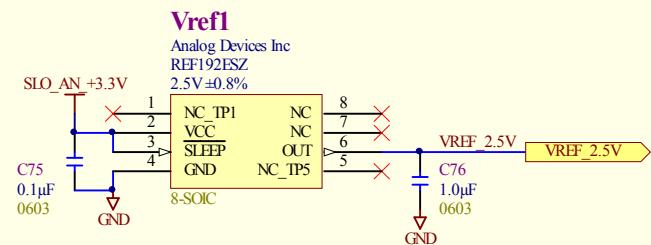
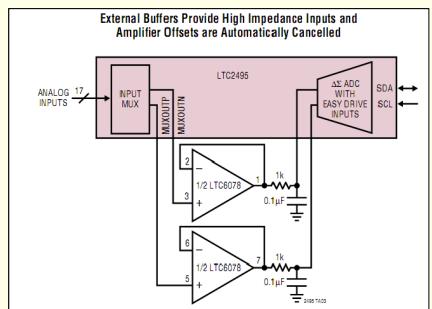
FIGURE 6. Generating Output Offset Voltage.



NOTES: (1) C₁ and C₂ combine to form a 2-pole response that is -3dB at 1kHz. Each individual pole is at 1.5kHz. (2) Output voltage is referenced to I_{A COMMON} (see text). (3) Output offset voltage required for measurement near zero (see Figure 28).

FIGURE 1. Basic Connections. NOTE: Connections for INA327 differ—see Pin Configuration for detail.

GAIN	1	4	8	16	32	64	128	256	UNIT
Input Span	±2.5	±0.625	±0.312	±0.156	±78m	±39m	±19.5m	±9.76m	V
LSB	38.1	9.54	4.77	2.38	1.19	0.596	0.298	0.149	µV
Noise Free Resolution*	65536	65536	65536	65536	65536	65536	32768	16384	Counts
Gain Error	5	5	5	5	5	5	5	8	ppm of FS
Offset Error	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	µV



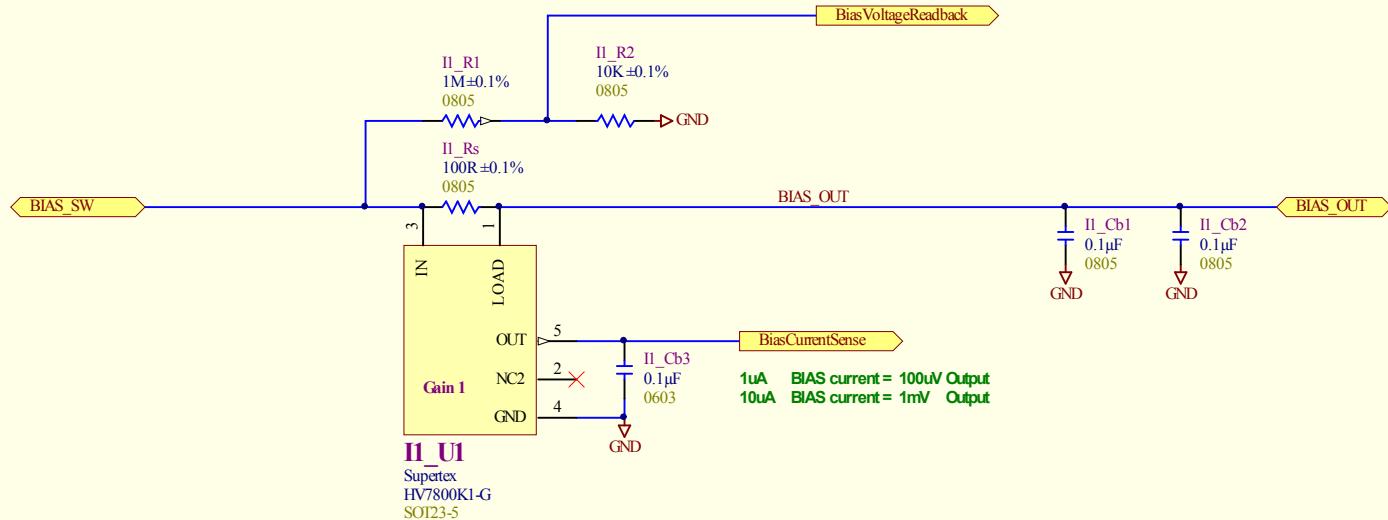
ORDER PART NUMBER QFN PART MARKING*

LTC2495CUHF LTC2495IUFH

Revision	Drawing #	6	TRIUMF
1	Sheet #:	6 of 16	4004 Westbrook Mall
	Size:	B	Vancouver, B.C.
	Drawn by:	D.Bishop	Canada
	Date:	25/06/2008	V6T 2A3

File: G:\AHWAT2KIT2K_FEB64\Rev1\T2K FEB Rev1 - BIAS Output.SchDoc

2:38:02 PM



Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
Supply						
V_{IN}	Supply voltage	8.0	-	450	V	*
I_0	Quiescent supply current	-	-	50	μA	- $V_{IN} = 8\text{V}$ to 450V , $V_{SENSE} = 0\text{mV}$
Input and Output						
R_{OUT}	OUT pin output resistance	-	3.6	-	kΩ	- ---
V_{OUT}	Output voltage	0	-	15	mV	- $V_{SENSE} = 0\text{mV}$
		79	-	121	mV	- $V_{SENSE} = 100\text{mV}$
		177	-	223	mV	- $V_{SENSE} = 200\text{mV}$
		470	-	530	mV	- $V_{SENSE} = 500\text{mV}$
Dynamic Characteristics						
t_{RISE}	Output rise time, 10% to 90%	-	0.7	-	μs	- V_{SENSE} step 5mV to 500mV
		-	-	2.0	μs	- V_{SENSE} step 0mV to 500mV
t_{FALL}	Output fall time, 90% to 10%	-	0.7	2.0	μs	- V_{SENSE} step 500mV to 0mV

Notes:

1. Referenced to GND

2. $V_{SENSE} = V_{IN} - V_{LOAD}$

Values of parameters marked with a * apply over the full temperature range

Supertex Inc. • 1235 Bordeaux Drive, Sunnyvale, CA 94089 • Tel: (408) 222-8888 • FAX: (408) 222-4895 • www.supertex.com

HV7800

Ordering Information

Device	Package Option
HV7800	5-Lead SOT-23 HV7800K1-G

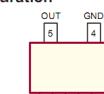
Thermal Resistance

Package	θ_θ
5-Lead SOT-23	191°C/W

Note: Thermal testboard per JEDEC JESD51-7



Pin Configuration



5-Lead SOT-23
(top view)

Product Marking

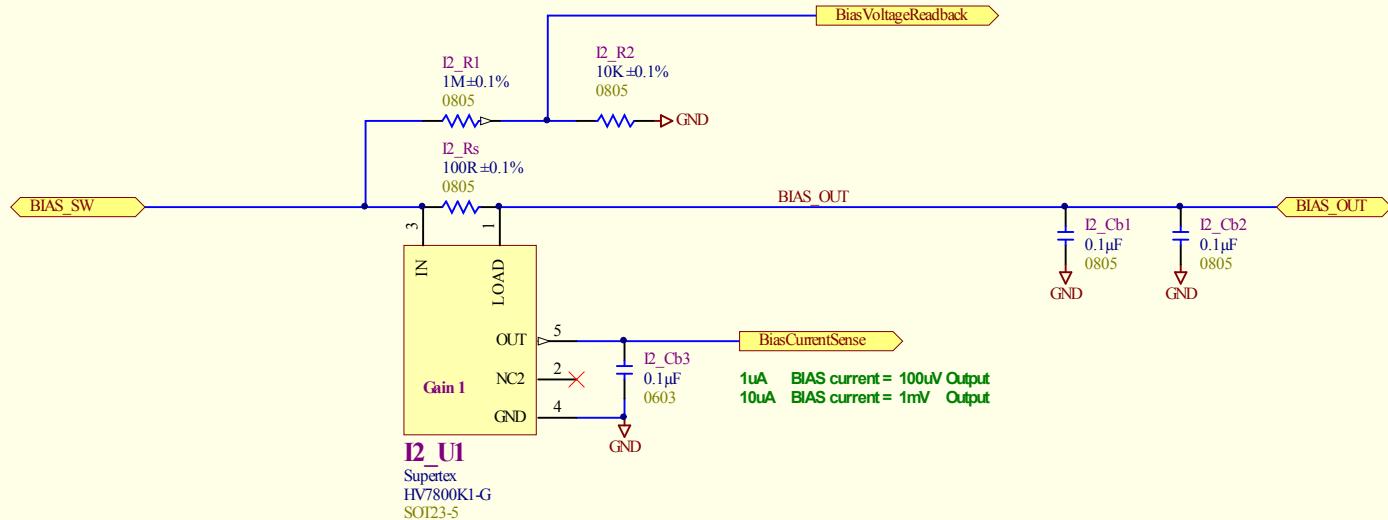


Y = Last Digit of Year Sealed
W = Code for Week Sealed
= "Green" Packaging

5-Lead SOT-23

T2K FEB64 - BIAS Current Sense

Revision	Drawing #	Sheet #:	Size:	TRIUMF	
1	7	7 of 16	A	4004 Westbrook Mall Vancouver, B.C. Canada V6T 2A3	
		Drawn by:	D.Bishop	Date: 25/06/2008	
		File: G:\AHW\T2KIT2K_FEB64\Rev1\T2K FEB Rev1 - BIAS Current Sense.SchDoc			
				2:38:02 PM	



Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
Supply						
V_{IN}	Supply voltage	8.0	-	450	V	*
I_0	Quiescent supply current	-	-	50	μA	- $V_{IN} = 8\text{V}$ to 450V , $V_{SENSE} = 0\text{mV}$
Input and Output						
R_{OUT}	OUT pin output resistance	-	3.6	-	kΩ	- ---
V_{OUT}	Output voltage	0	-	15	mV	- $V_{SENSE} = 0\text{mV}$
		79	-	121	mV	- $V_{SENSE} = 100\text{mV}$
		177	-	223	mV	- $V_{SENSE} = 200\text{mV}$
		470	-	530	mV	- $V_{SENSE} = 500\text{mV}$
Dynamic Characteristics						
t_{RISE}	Output rise time, 10% to 90%	-	0.7	-	μs	- V_{SENSE} step 5mV to 500mV
		-	-	2.0	μs	- V_{SENSE} step 0mV to 500mV
t_{FALL}	Output fall time, 90% to 10%	-	0.7	2.0	μs	- V_{SENSE} step 500mV to 0mV

Notes:

1. Referenced to GND

2. $V_{SENSE} = V_{IN} - V_{LOAD}$

Values of parameters marked with a * apply over the full temperature range

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HV7800

Ordering Information

Device	Package Option
HV7800	5-Lead SOT-23 HV7800K1-G

Thermal Resistance

Package	θ_θ
5-Lead SOT-23	191°C/W

Note: Thermal testboard per JEDEC JESD51-7

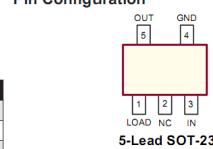


Absolute Maximum Ratings

Parameter	Value
V_{IN} , V_{LOAD} ¹	-0.5V to +450V
V_{OUT} ¹	-0.5V to +10V
V_{SENSE} ²	-0.5V to +5.0V
I_{LOAD}	±10mA
Operating ambient temperature	-40°C to +85°C
Operating junction temperature	-40°C to +125°C
Storage temperature	-65°C to +150°C

Absolute maximum ratings: those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



Product Marking

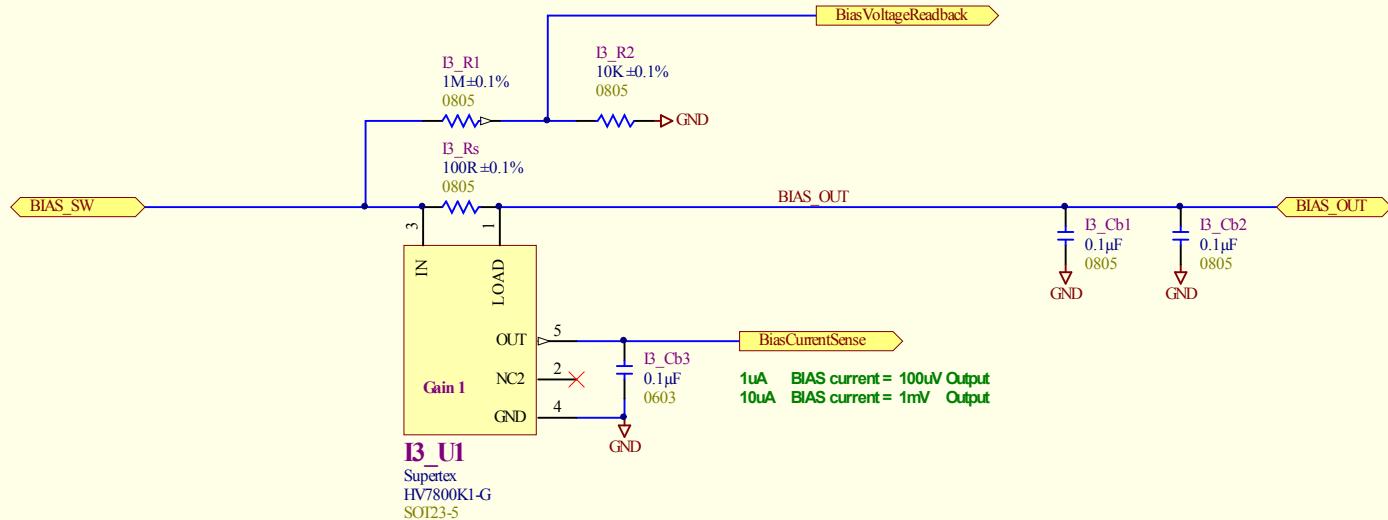


Y = Last Digit of Year Sealed
W = Code for Week Sealed
= "Green" Packaging

5-Lead SOT-23

T2K FEB64 - BIAS Current Sense

Revision	Drawing #	Sheet #	Size	TRIUMF
1	7	7 of 16	A	4004 Westbrook Mall Vancouver, B.C. Canada V6T 2A3
				Drawn by: D.Bishop Date: 25/06/2008
				File: G:\AHW\T2KIT2K_FEB64\Rev1\T2K FEB Rev1 - BIAS Current Sense.SchDoc
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Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
Supply						
V_{IN}	Supply voltage	8.0	-	450	V	*
I_Q	Quiescent supply current	-	-	50	μA	- $V_{IN} = 8\text{V}$ to 450V , $V_{SENSE} = 0\text{mV}$
Input and Output						
R_{OUT}	OUT pin output resistance	-	3.6	-	kΩ	- ---
V_{OUT}	Output voltage	0	-	15	mV	- $V_{SENSE} = 0\text{mV}$
		79	-	121	mV	- $V_{SENSE} = 100\text{mV}$
		177	-	223	mV	- $V_{SENSE} = 200\text{mV}$
		470	-	530	mV	- $V_{SENSE} = 500\text{mV}$
Dynamic Characteristics						
t_{RISE}	Output rise time, 10% to 90%	-	0.7	-	μs	- V_{SENSE} step 5mV to 500mV
		-	-	2.0	μs	- V_{SENSE} step 0mV to 500mV
t_{FALL}	Output fall time, 90% to 10%	-	0.7	2.0	μs	- V_{SENSE} step 500mV to 0mV

Notes:

1. Referenced to GND

2. $V_{SENSE} = V_{IN} - V_{LOAD}$

Values of parameters marked with a * apply over the full temperature range

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HV7800

Ordering Information

Device	Package Option
HV7800	5-Lead SOT-23 HV7800K1-G

Thermal Resistance

Package	θ_θ
5-Lead SOT-23	191°C/W

Note: Thermal testboard per JEDEC JESD51-7

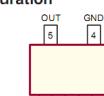


Absolute Maximum Ratings

Parameter	Value
V_{IN}, V_{LOAD} ¹	-0.5V to +450V
V_{OUT} ¹	-0.5V to +10V
V_{SENSE} ²	-0.5V to +5.0V
I_{LOAD}	±10mA
Operating ambient temperature	-40°C to +85°C
Operating junction temperature	-40°C to +125°C
Storage temperature	-65°C to +150°C

Absolute maximum ratings: those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



5-Lead SOT-23
(top view)

Product Marking

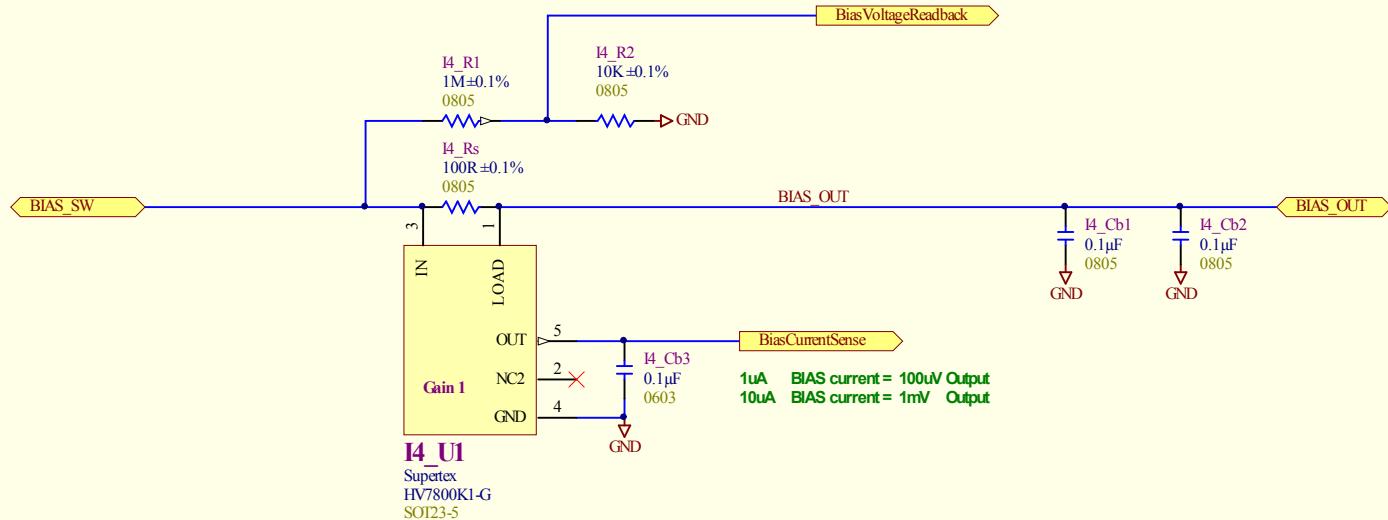


Y = Last Digit of Year Sealed
W = Code for Week Sealed
= "Green" Packaging

5-Lead SOT-23

T2K FEB64 - BIAS Current Sense

Revision	Drawing #	Sheet #	Size	TRIUMF
1	7	7 of 16	A	4004 Westbrook Mall Vancouver, B.C. Canada V6T 2A3
				Drawn by: D.Bishop Date: 25/06/2008
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Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
Supply						
V_{IN}	Supply voltage	8.0	-	450	V	*
I_Q	Quiescent supply current	-	-	50	μA	- $V_{IN} = 8\text{V}$ to 450V , $V_{SENSE} = 0\text{mV}$
Input and Output						
R_{OUT}	OUT pin output resistance	-	3.6	-	k Ω	- ---
V_{OUT}	Output voltage	0	-	15	mV	- $V_{SENSE} = 0\text{mV}$
		79	-	121		- $V_{SENSE} = 100\text{mV}$
		177	-	223		- $V_{SENSE} = 200\text{mV}$
		470	-	530		- $V_{SENSE} = 500\text{mV}$
Dynamic Characteristics						
t_{RISE}	Output rise time, 10% to 90%	-	0.7	-	μs	- V_{SENSE} step 5mV to 500mV
		-	-	2.0	- V_{SENSE} step 0mV to 500mV	
t_{FALL}	Output fall time, 90% to 10%	-	0.7	2.0	μs	- V_{SENSE} step 500mV to 0mV

Notes:

1. Referenced to GND

2. $V_{SENSE} = V_{IN} - V_{LOAD}$

Values of parameters marked with a * apply over the full temperature range

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HV7800

Ordering Information

Device	Package Option
HV7800	5-Lead SOT-23 HV7800K1-G

Thermal Resistance

Package	θ_{JA}
5-Lead SOT-23	191°C/W

Note: Thermal testboard per JEDEC JESD51-7

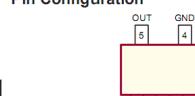


Absolute Maximum Ratings

Parameter	Value
V_{IN} , V_{LOAD} ¹	-0.5V to +450V
V_{OUT} ¹	-0.5V to +10V
V_{SENSE} ²	-0.5V to +5.0V
I_{LOAD}	$\pm 10\text{mA}$
Operating ambient temperature	-40°C to +85°C
Operating junction temperature	-40°C to +125°C
Storage temperature	-65°C to +150°C

Absolute maximum ratings: those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



5-Lead SOT-23 (top view)

Product Marking

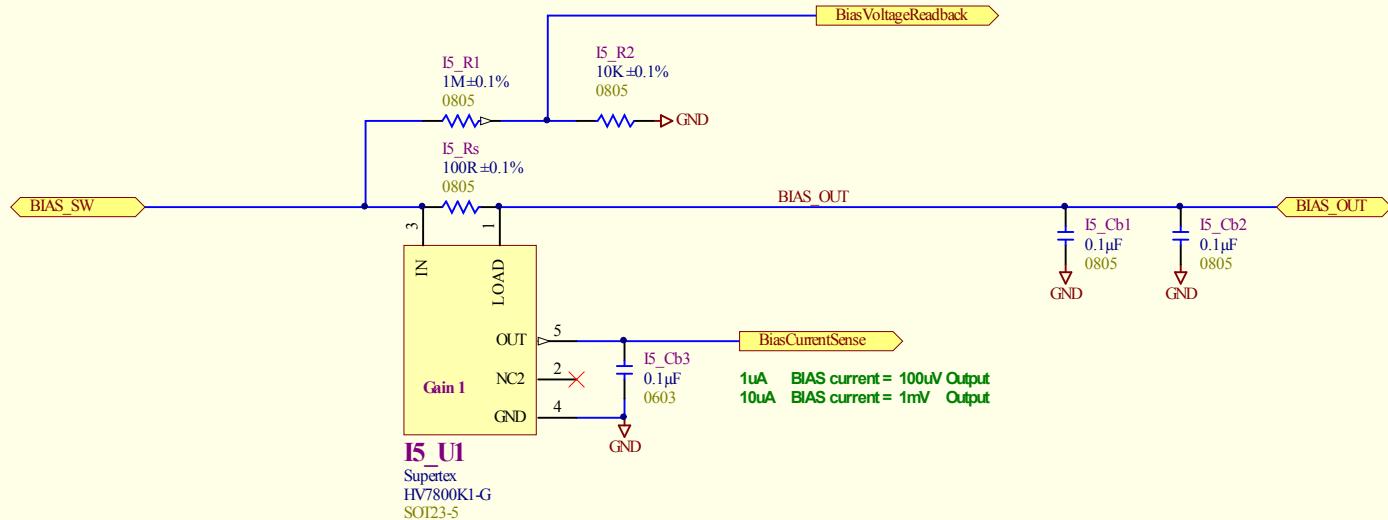


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W = Code for Week Sealed
= "Green" Packaging

5-Lead SOT-23

T2K FEB64 - BIAS Current Sense

Revision	Drawing #	Sheet #	Size	TRIUMF
1	7	7 of 16	A	4004 Westbrook Mall Vancouver, B.C. Canada V6T 2A3
				Supertex Inc.
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Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
Supply						
V_{IN}	Supply voltage	8.0	-	450	V	*
I_0	Quiescent supply current	-	-	50	μA	- $V_{IN} = 8\text{V}$ to 450V , $V_{SENSE} = 0\text{mV}$
Input and Output						
R_{OUT}	OUT pin output resistance	-	3.6	-	kΩ	- ---
V_{OUT}	Output voltage	0	-	15	mV	- $V_{SENSE} = 0\text{mV}$
		79	-	121	mV	- $V_{SENSE} = 100\text{mV}$
		177	-	223	mV	- $V_{SENSE} = 200\text{mV}$
		470	-	530	mV	- $V_{SENSE} = 500\text{mV}$
Dynamic Characteristics						
t_{RISE}	Output rise time, 10% to 90%	-	0.7	-	μs	- V_{SENSE} step 5mV to 500mV
		-	-	2.0	μs	- V_{SENSE} step 0mV to 500mV
t_{FALL}	Output fall time, 90% to 10%	-	0.7	2.0	μs	- V_{SENSE} step 500mV to 0mV

Notes:

1. Referenced to GND

2. $V_{SENSE} = V_{IN} - V_{LOAD}$

Values of parameters marked with a * apply over the full temperature range

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HV7800

Ordering Information

Device	Package Option
HV7800	5-Lead SOT-23 HV7800K1-G

Thermal Resistance

Package	θ_{JA}
5-Lead SOT-23	191°C/W

Note: Thermal testboard per JEDEC JESD51-7

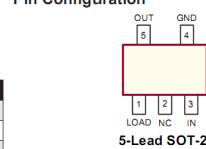


Absolute Maximum Ratings

Parameter	Value
V_{IN} , V_{LOAD} ¹	-0.5V to +450V
V_{OUT} ¹	-0.5V to +10V
V_{SENSE} ²	-0.5V to +5.0V
I_{LOAD}	±10mA
Operating ambient temperature	-40°C to +85°C
Operating junction temperature	-40°C to +125°C
Storage temperature	-65°C to +150°C

Absolute maximum ratings: those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



5-Lead SOT-23
(top view)

Product Marking

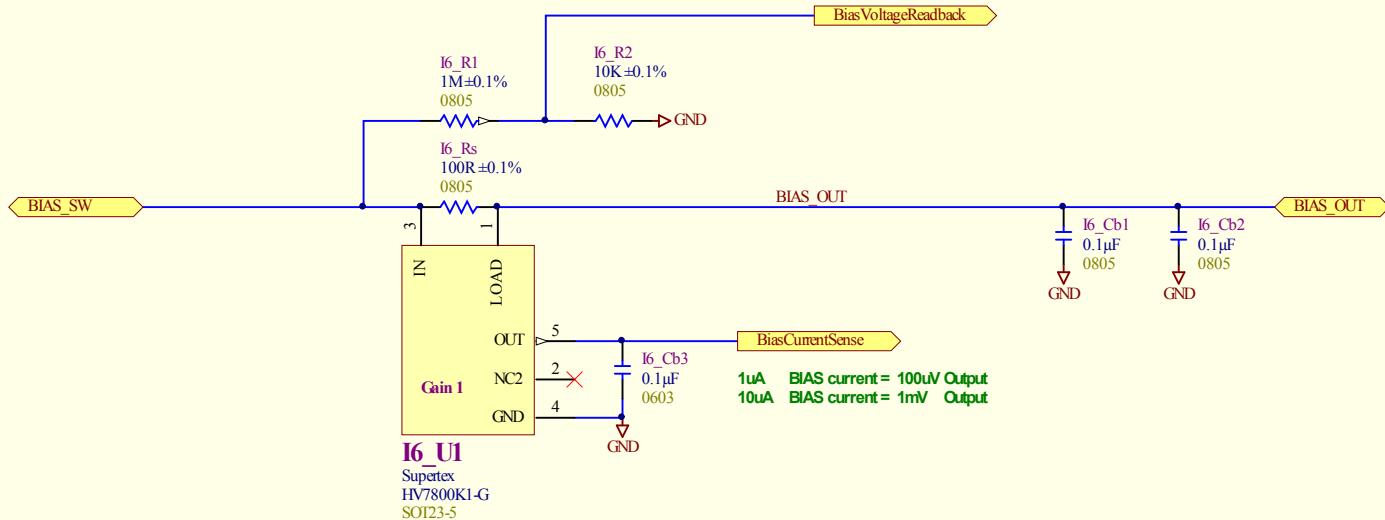


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W = Code for Week Sealed
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5-Lead SOT-23

T2K FEB64 - BIAS Current Sense

Revision	Drawing #	Sheet #	Size	TRIUMF
1	7	7 of 16	A	4004 Westbrook Mall Vancouver, B.C. Canada V6T 2A3
				Drawn by: D.Bishop Date: 25/06/2008
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Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
Supply						
V_{IN}	Supply voltage	8.0	-	450	V	*
I_q	Quiescent supply current	-	-	50	μA	- $V_{IN} = 8\text{V}$ to 450V , $V_{SENSE} = 0\text{mV}$
Input and Output						
R_{OUT}	OUT pin output resistance	-	3.6	-	k Ω	- ---
V_{OUT}	Output voltage	0	-	15	mV	- $V_{SENSE} = 0\text{mV}$
		79	-	121		- $V_{SENSE} = 100\text{mV}$
		177	-	223		- $V_{SENSE} = 200\text{mV}$
		470	-	530		- $V_{SENSE} = 500\text{mV}$
Dynamic Characteristics						
t_{RISE}	Output rise time, 10% to 90%	-	0.7	-	μs	- V_{SENSE} step 5mV to 500mV
		-	-	2.0	- V_{SENSE} step 0mV to 500mV	
t_{FALL}	Output fall time, 90% to 10%	-	0.7	2.0	μs	- V_{SENSE} step 500mV to 0mV

Notes: 1. Referenced to GND

2. $V_{SENSE} = V_{IN} - V_{LOAD}$

Values of parameters marked with a * apply over the full temperature range

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HV7800

Ordering Information

Device	Package Option
HV7800	5-Lead SOT-23 HV7800K1-G

Thermal Resistance

Package	θ_θ
5-Lead SOT-23	191°C/W

Note: Thermal testboard per JEDEC JESD51-7

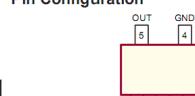


Absolute Maximum Ratings

Parameter	Value
V_{IN} V_{LOAD} ¹	-0.5V to +450V
V_{OUT} ¹	-0.5V to +10V
V_{SENSE} ²	-0.5V to +5.0V
I_{LOAD}	$\pm 10\text{mA}$
Operating ambient temperature	-40°C to +85°C
Operating junction temperature	-40°C to +125°C
Storage temperature	-65°C to +150°C

Absolute maximum ratings: those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



5-Lead SOT-23 (top view)

Product Marking

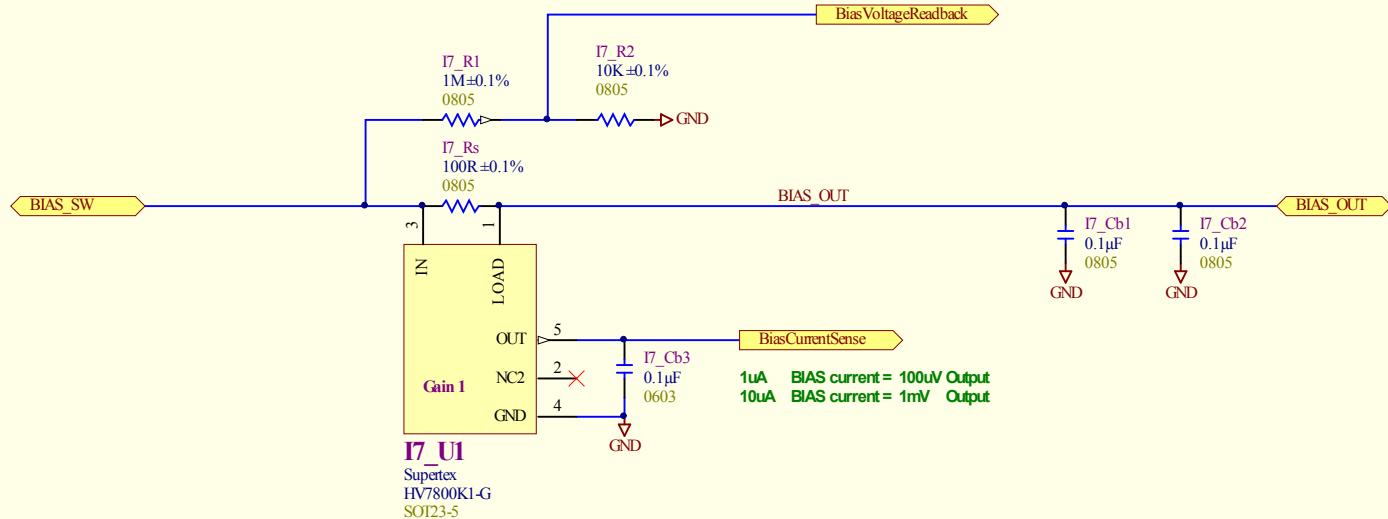


Y = Last Digit of Year Sealed
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5-Lead SOT-23

T2K FEB64 - BIAS Current Sense

Revision	Drawing #	Sheet #	Size	TRIUMF
1	7	7 of 16	A	4004 Westbrook Mall Vancouver, B.C. Canada V6T 2A3
				Drawn by: D.Bishop Date: 25/06/2008
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Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
Supply						
V_{IN}	Supply voltage	8.0	-	450	V	*
I_0	Quiescent supply current	-	-	50	μA	- $V_{IN} = 8\text{V}$ to 450V , $V_{SENSE} = 0\text{mV}$
Input and Output						
R_{OUT}	OUT pin output resistance	-	3.6	-	kΩ	- ---
V_{OUT}	Output voltage	0	-	15	mV	- $V_{SENSE} = 0\text{mV}$
		79	-	121	mV	- $V_{SENSE} = 100\text{mV}$
		177	-	223	mV	- $V_{SENSE} = 200\text{mV}$
		470	-	530	mV	- $V_{SENSE} = 500\text{mV}$
Dynamic Characteristics						
t_{RISE}	Output rise time, 10% to 90%	-	0.7	-	μs	- V_{SENSE} step 5mV to 500mV
		-	-	2.0	μs	- V_{SENSE} step 0mV to 500mV
t_{FALL}	Output fall time, 90% to 10%	-	0.7	2.0	μs	- V_{SENSE} step 500mV to 0mV

Notes:

1. Referenced to GND

2. $V_{SENSE} = V_{IN} - V_{LOAD}$

Values of parameters marked with a * apply over the full temperature range

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HV7800

Ordering Information

Device	Package Option
HV7800	5-Lead SOT-23 HV7800K1-G

Thermal Resistance

Package	θ_θ
5-Lead SOT-23	191°C/W

Note: Thermal testboard per JEDEC JESD51-7

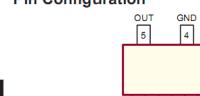


Absolute Maximum Ratings

Parameter	Value
V_{IN} , V_{LOAD} ¹	-0.5V to +450V
V_{OUT} ¹	-0.5V to +10V
V_{SENSE} ²	-0.5V to +5.0V
I_{LOAD}	±10mA
Operating ambient temperature	-40°C to +85°C
Operating junction temperature	-40°C to +125°C
Storage temperature	-65°C to +150°C

Absolute maximum ratings: those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



5-Lead SOT-23
(top view)

Product Marking

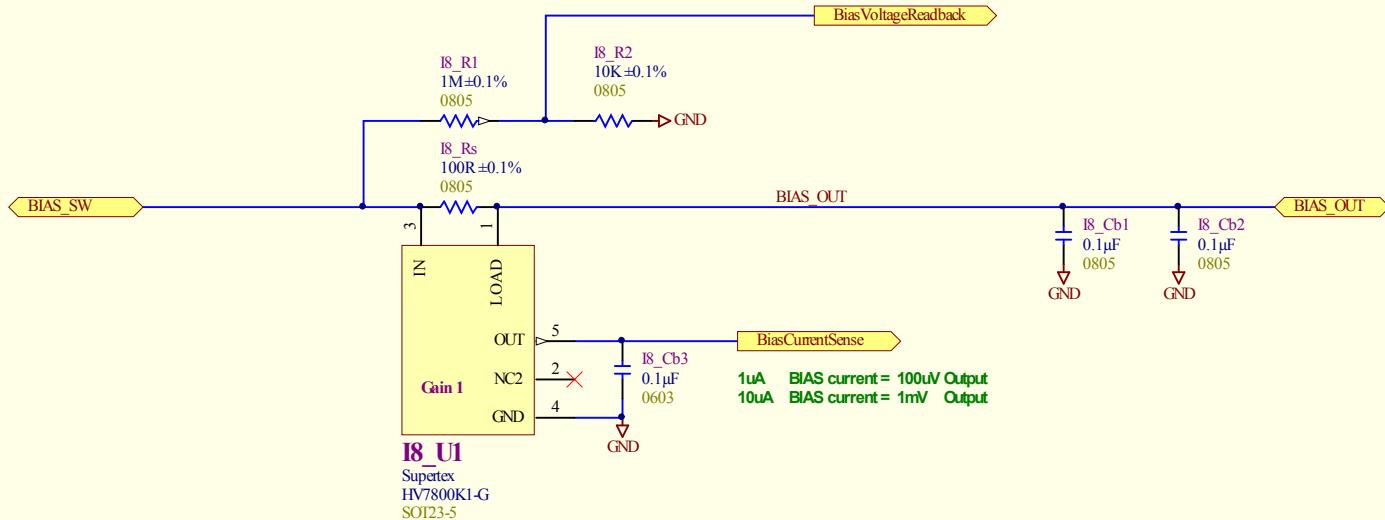


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W = Code for Week Sealed
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5-Lead SOT-23

T2K FEB64 - BIAS Current Sense

Revision	Drawing #	Sheet #	Size	TRIUMF	
1	7	7 of 16	A	4004 Westbrook Mall Vancouver, B.C. Canada V6T 2A3	
		Drawn by:	D.Bishop	Date: 25/06/2008	
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				2:38:03 PM	



Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
Supply						
V_{IN}	Supply voltage	8.0	-	450	V	*
I_0	Quiescent supply current	-	-	50	µA	- $V_{IN} = 8\text{V}$ to 450V , $V_{SENSE} = 0\text{mV}$
Input and Output						
R_{OUT}	OUT pin output resistance	-	3.6	-	kΩ	- ---
V_{OUT}	Output voltage	0	-	15	mV	- $V_{SENSE} = 0\text{mV}$
		79	-	121	mV	- $V_{SENSE} = 100\text{mV}$
		177	-	223	mV	- $V_{SENSE} = 200\text{mV}$
		470	-	530	mV	- $V_{SENSE} = 500\text{mV}$
Dynamic Characteristics						
t_{RISE}	Output rise time, 10% to 90%	-	0.7	-	µs	- V_{SENSE} step 5mV to 500mV
		-	-	2.0	µs	- V_{SENSE} step 0mV to 500mV
t_{FALL}	Output fall time, 90% to 10%	-	0.7	2.0	µs	- V_{SENSE} step 500mV to 0mV

Notes: 1. Referenced to GND

2. $V_{SENSE} = V_{IN} - V_{LOAD}$

Values of parameters marked with a * apply over the full temperature range

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HV7800

Ordering Information

Device	Package Option
HV7800	5-Lead SOT-23 HV7800K1-G

Thermal Resistance

Package	θ_θ
5-Lead SOT-23	191°C/W

Note: Thermal testboard per JEDEC JESD51-7

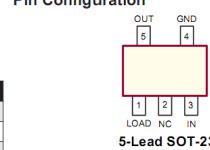


Absolute Maximum Ratings

Parameter	Value
V_{IN}, V_{LOAD} ¹	-0.5V to +450V
V_{OUT} ¹	-0.5V to +10V
V_{SENSE} ²	-0.5V to +5.0V
I_{LOAD}	±10mA
Operating ambient temperature	-40°C to +85°C
Operating junction temperature	-40°C to +125°C
Storage temperature	-65°C to +150°C

Absolute maximum ratings: those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



Product Marking



Y = Last Digit of Year Sealed
W = Code for Week Sealed
= "Green" Packaging

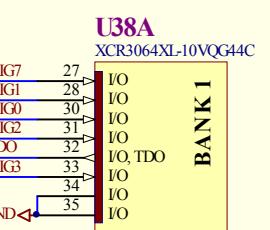
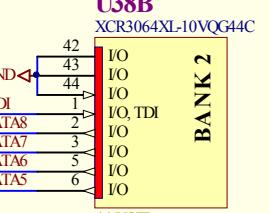
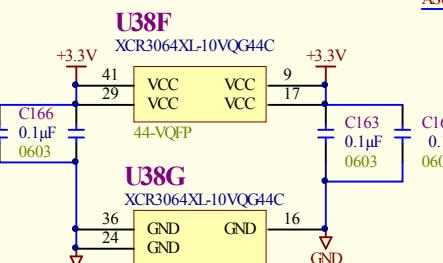
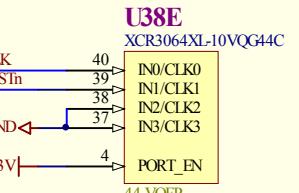
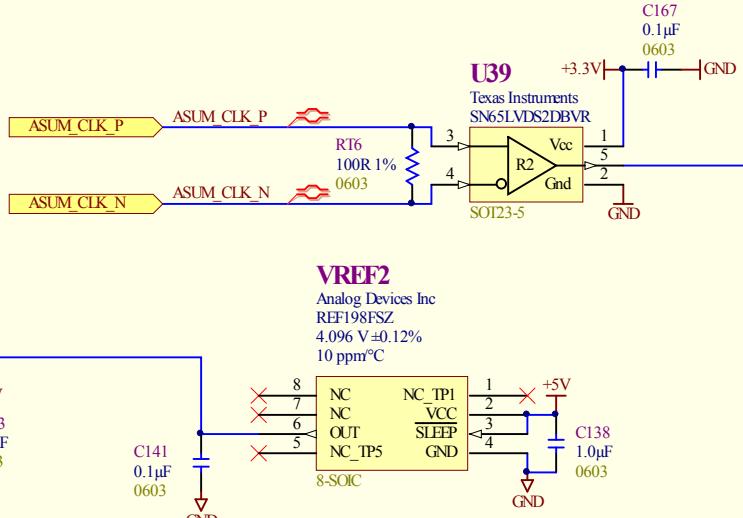
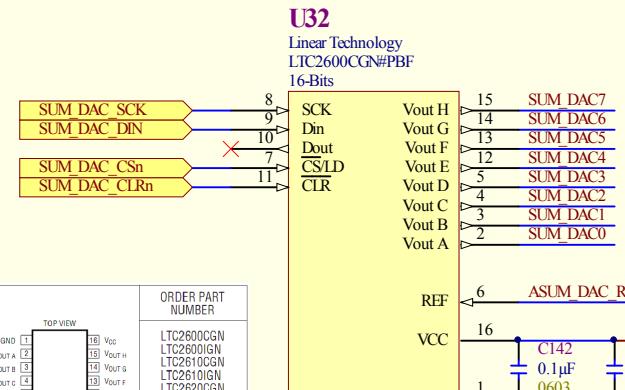
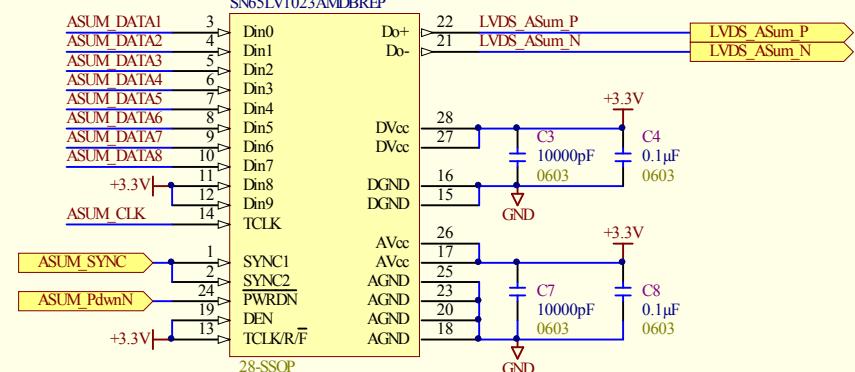
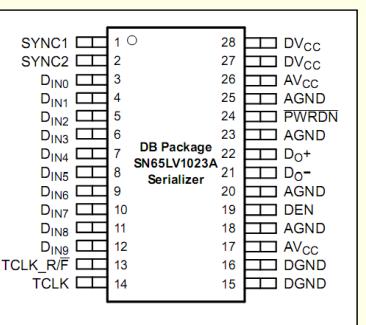
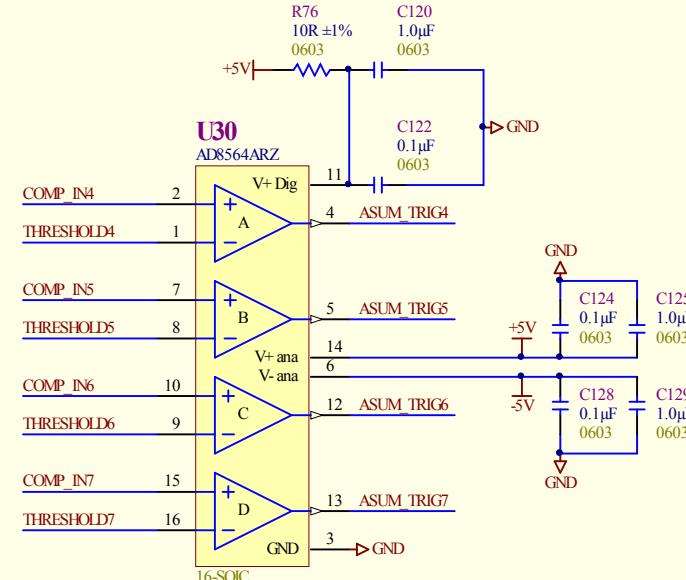
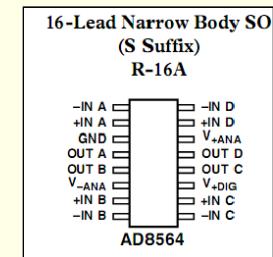
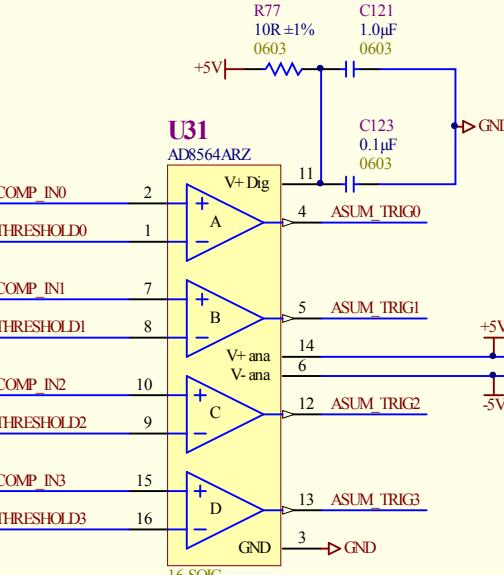
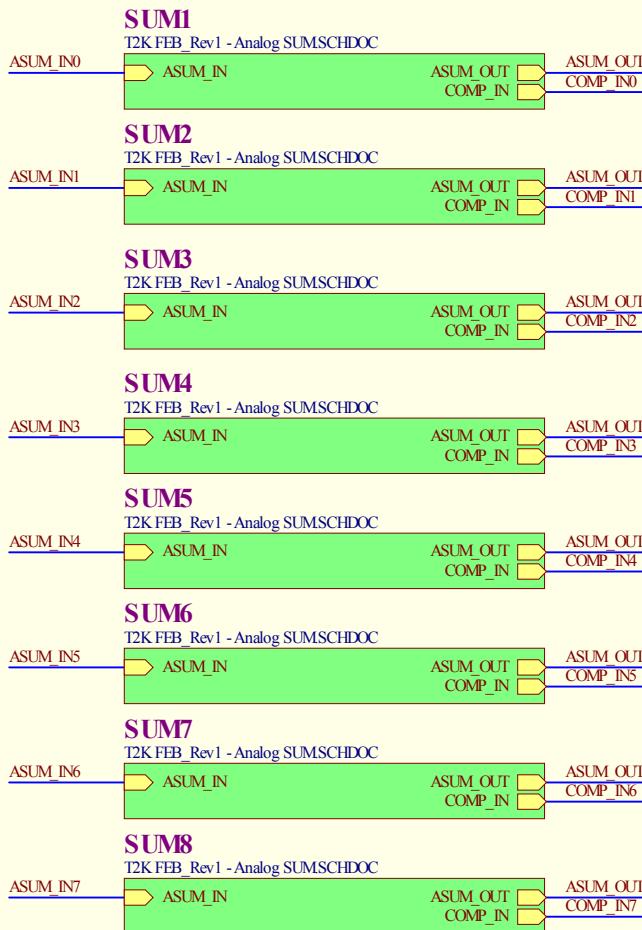
5-Lead SOT-23

T2K FEB64 - BIAS Current Sense

Revision	Drawing #	Sheet #	Size	TRIUMF
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				Drawn by: D.Bishop Date: 25/06/2008
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				2:38:03 PM

ASUM_IN[7..0]

ASUM_OUT[7..0]

**T2K FEB64 - APD SUM x 8**

Revision	Drawing #	Sheet #:	Size:	TRIUMF
1	9	9 of 16	B	4004 Westbrook Mall
				Vancouver, B.C.
				Canada
				V6T 2A3
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