CPU
T2K FEB - Slow Control.SCHDOC

MSCB_RS485A
MSCB_RS485B
SMB_CLK
SMB_DAT
EN_BIASn[8..1]
Backplane_Add[7..0]
BiasCurrentSense
BiasVoltageReadback
+6V_Analog_VMon
-6V_Analog_VMon
+6V_Dig_VMon
+6V_Analog_IMon
-6V_Analog_IMon
+6V_Dig_IMon

MSCB_RS485A
MSCB_RS485B
SMB_CLK
SMB_DAT
EN_BIASn[8..1]
Backplane_Add[7..0]
BiasCurrentSense
BiasVoltageReadback
+6V_Analog_VMon
-6V_Analog_VMon
+6V_Dig_VMon
+6V_Analog_IMon
-6V_Analog_IMon
+6V_Dig_IMon
EN_AN_+5V
EN_AN_-5V
EN_DIG_+5V

SPI_MOSI
SPI_SCK
APD_DAC_CSn[8..1]
SUM_DAC_CSn
ResetN
EN_DIG_+5V
EN_AN_+5V
EN_AN_-5V
CHG_PMP_CLK
ASUM_SYNC
ASUM_PdwnN
ASUM_TESTn
De[8..1]
Dcb[8..1]
JTAG_TCK
JTAG_TMS
CPU_TDO
JTAG_TDO
JTAG_TDI

SPI_MOSI
SPI_SCK
APD_DAC_CSn[8..1]
SUM_DAC_CSn
ResetN
EN_DIG_+5V
EN_AN_+5V
EN_AN_-5V
CHG_PMP_CLK
ASUM_SYNC
ASUM_PdwnN
ASUM_TESTn
De[8..1]
Dcb[8..1]
JTAG_TCK
JTAG_TMS
CPU_TDO
XILINX_TDO
JTAG_TDI

SCA_ADC
T2K FEB - 50MSPS ADC.SCHDOC

ADC_DTP
ADC_PDWN
SCA1_VOUT_P
SCA1_VOUT_N
SCA2_VOUT_P
SCA2_VOUT_N

ADC_DTP
ADC_PDWN
ADC_VIND_P
ADC_VIND_N
ADC_VINA_P
ADC_VINA_N

LVDS_ADC_CLK_P
LVDS_ADC_CLK_N
LVDS_ADC_DCO_P
LVDS_ADC_DCO_N
LVDS_ADC_FCO_P
LVDS_ADC_FCO_N
LVDS_ADC_DATA0_P
LVDS_ADC_DATA0_N
LVDS_ADC_DATA3_P
LVDS_ADC_DATA3_N

SCA
T2K FEB - SCA Interface.SCHDOC

SCA1_VOUT_P
SCA1_VOUT_N
SCA2_VOUT_P
SCA2_VOUT_N
LVDS_TRIG_P
LVDS_TRIG_N
APD_HATTN[64..1]
APD_LATTN[64..1]
ASUM_OUT[8..1]

SCA1_VOUT_P
SCA1_VOUT_N
SCA2_VOUT_P
SCA2_VOUT_N
LVDS_TRIG_P
LVDS_TRIG_N
APD_HATTN[64..1]
APD_LATTN[64..1]
ASUM_OUT[8..1]

SCA1_Sc_ck
SCA1_Sc_en
SCA1_Sc_din
SCA1_Sc_dout
SCA2_Sc_ck
SCA2_Sc_en
SCA2_Sc_din
SCA2_Sc_dout
LVDS_SCA_WCK_P
LVDS_SCA_WCK_N
LVDS_SCA_RCK_P
LVDS_SCA_RCK_N
LVDS_SCA_READ_P
LVDS_SCA_READ_N
LVDS_SCA_WRITE_P
LVDS_SCA_WRITE_N

APD_DAC
T2K FEB - 64 Channel Bias Control.SCHDOC

APD_DAC_CSn[8..1]
SPI_SCK
SPI_MOSI
ResetN

APD_DAC_CSn[8..1]
APD_DAC_SCK
APD_DAC_DIN
APD_DAC_CLRn

APD_DAC[64..1]

Backplane
T2K FEB - Backplane Connections.SCHDOC

LVDS_ADC_CLK_P
LVDS_ADC_CLK_N
LVDS_ADC_DCO_P
LVDS_ADC_DCO_N
LVDS_ADC_FCO_P
LVDS_ADC_FCO_N
LVDS_ADC_DATA0_P
LVDS_ADC_DATA0_N
LVDS_ADC_DATA3_P
LVDS_ADC_DATA3_N
SCA_SlowCnt_SCK0
SCA_SlowCnt_CS0
SCA_SlowCnt_MOSI0
SCA_SlowCnt_MISO0
SCA_SlowCnt_SCK1
SCA_SlowCnt_CS1
SCA_SlowCnt_MOSI1
SCA_SlowCnt_MISO1
LVDS_SCA_WCK_P
LVDS_SCA_WCK_N
LVDS_SCA_RCK_P
LVDS_SCA_RCK_N
LVDS_SCA_READ_P
LVDS_SCA_READ_N
LVDS_SCA_WRITE_P
LVDS_SCA_WRITE_N
APDk[64..1]
APDa[64..1]

LVDS_ADC_CLK_P
LVDS_ADC_CLK_N
LVDS_ADC_DCO_P
LVDS_ADC_DCO_N
LVDS_ADC_FCO_P
LVDS_ADC_FCO_N
LVDS_ADC_DATA0_P
LVDS_ADC_DATA0_N
LVDS_ADC_DATA3_P
LVDS_ADC_DATA3_N
Dcb[8..1]
De[8..1]
ASUM_CLK_P
ASUM_CLK_N
ADC_DTP
ADC_PDWN
LVDS_TRIG_P
LVDS_TRIG_N
LVDS_Asum_P
LVDS_Asum_N
MSCB_RS485A
MSCB_RS485B
BP_TCK
BP_TMS
BP_TDO
BP_TDI
AN_+6V_IN
AN_-6V_IN
DIG_+6V_IN
SLO_+5V
APDk[64..1]
Backplane_Add[7..0]
APDa[64..1]

Dcb[8..1]
De[8..1]
ASUM_CLK_P
ASUM_CLK_N
ADC_DTP
ADC_PDWN
LVDS_TRIG_P
LVDS_TRIG_N
LVDS_ASum_P
LVDS_ASum_N
MSCB_RS485A
MSCB_RS485B
JTAG_TCK
JTAG_TMS
XILINX_TDO
JTAG_TDI
AN_+6V_IN
AN_-6V_IN
DIG_+6V_IN
SLO_+5V
Backplane_Add[7..0]

REGULATORS
T2K FEB- Regulators.SCHDOC

AN_+6V_IN
AN_-6V_IN
DIG_+6V_IN
SLO_+5V
VREF_2.5V
EN_AN_+5V
EN_AN_-5V
EN_DIG_+5V

AN_+6V_IN
AN_-6V_IN
DIG_+6V_IN
SLO_+5V
VREF_2.5V
EN_AN_+5V
EN_AN_-5V
EN_DIG_+5V
+6V_Analog_VMon
-6V_Analog_VMon
+6V_Dig_VMon
+6V_Analog_IMon
-6V_Analog_IMon
+6V_Dig_IMon

+6V_Analog_VMon
-6V_Analog_VMon
+6V_Dig_VMon
+6V_Analog_IMon
-6V_Analog_IMon
+6V_Dig_IMon

BIAS_OUT
T2K FEB - BIAS Output.SchDoc

EN_BIASn[8..1]
SMB_CLK
SMB_DAT
VREF_2.5V

EN_BIASn[8..1]
SMB_CLK
SMB_DAT
VREF_2.5V
BIAS_OUT[8..1]
BIAS

BIAS_OUT[8..1]

CHRG_PUMP
T2K FEB - 80 Volt Charge Pump.SCHDOC

CHG_PMP_CLK
SMB_CLK
SMB_DAT
VREF_2.5V

CHG_PMP_CLK
SMB_CLK
SMB_DAT
VREF_2.5V
BIAS
BiasCurrentSense
BiasVoltageReadback

BIAS
BiasCurrentSense
BiasVoltageReadback

APD_INPUTS
T2K FEB - APD Inputs.SchDoc

APDa[64..1]
BIAS_OUT[8..1]

APDa[64..1]
BIAS_OUT[8..1]
APD_HATTN[64..1]
APD_LATTN[64..1]
ASUM_IN[8..1]

APD_HATTN[64..1]
APD_LATTN[64..1]
ASUM_IN[8..1]

APD_SUM
T2K FEB - APD SUM.SCHDOC

ASUM_IN[8..1]
SUM_DAC_CSn
SPI_SCK
SPI_MOSI
ResetN
ASUM_CLK_P
ASUM_CLK_N
ASUM_SYNC
ASUM_PdwnN
ASUM_TESTn

ASUM_IN[8..1]
SUM_DAC_CSn
SUM_DAC_SCK
SUM_DAC_DIN
SUM_DAC_CLRn
ASUM_CLK_P
ASUM_CLK_N
ASUM_SYNC
ASUM_PdwnN
ASUM_TESTn
ASUM_OUT[8..1]
LVDS_ASum_P
LVDS_ASum_N
JTAG_TCK
JTAG_TMS
XILINX_TDI
XILINX_TDO

ASUM_OUT[8..1]
LVDS_ASum_P
LVDS_ASum_N
JTAG_TCK
JTAG_TMS
CPU_TDO
XILINX_TDO

T2K FEB - Top Level

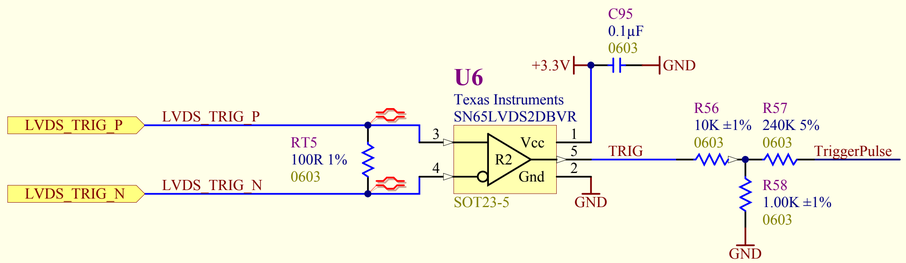
TRIUMF LOGO

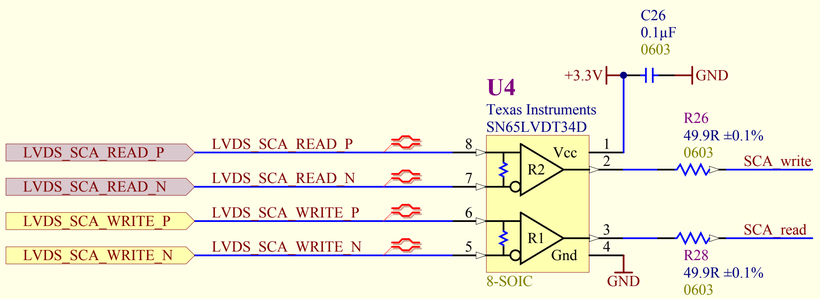
Revision **0**	Drawing #: 1		*TRIUMF* 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 1 of 16	Size: B	
	Drawn by: D.BIshop	Date: 06/02/2008	
File: C:\T2K\T2K_FEB_TRIUMF\T2K FEB - Top Level.SCHDOC			1:09:41 PM

ASUM_OUT[8..1] — ASUM_OUT[8..1]

APD_HATTN[64..1] — APD_HATTN[64..1]

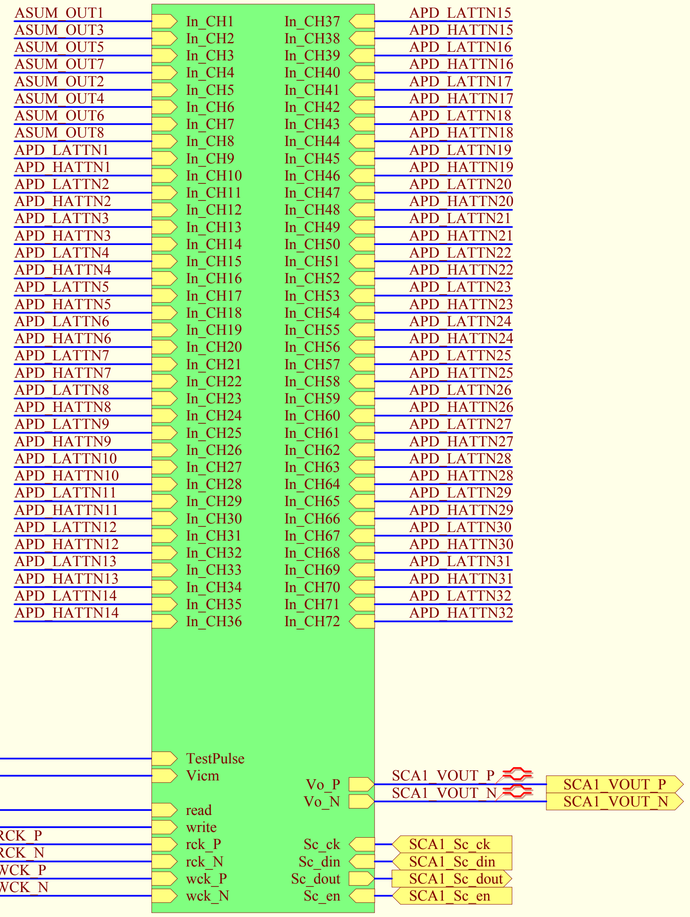
APD_LATTN[64..1] — APD_LATTN[64..1]





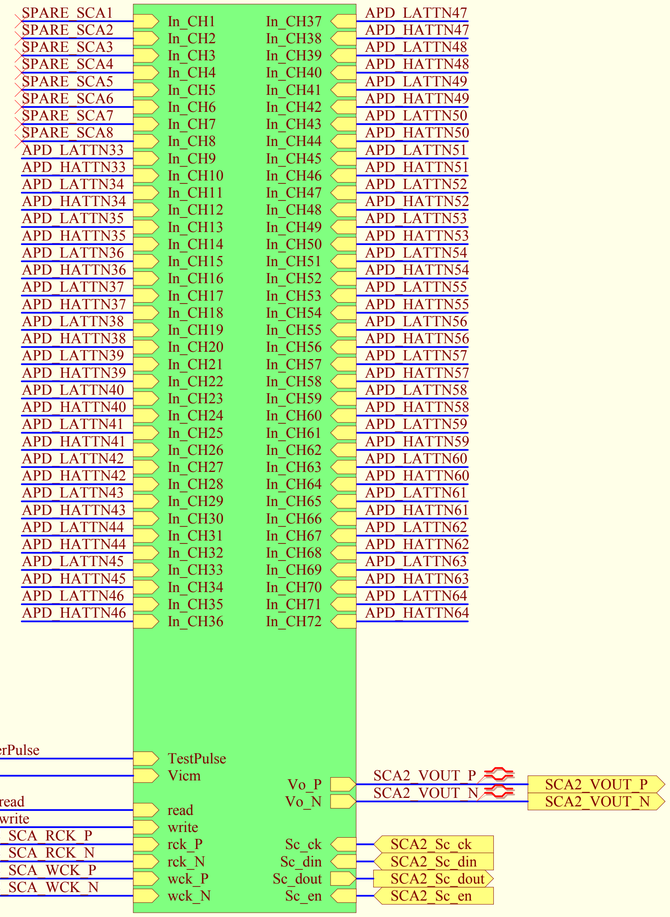
SCA1

T2K FEB - AFTER ASIC.SCHDOC



SCA2

T2K FEB - AFTER ASIC.SCHDOC

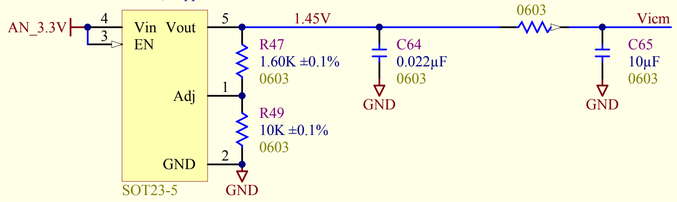


SCA - Icc approx 60ma

SCA - Icc approx 60ma

REF1

National Semiconductor
LM4121IM5-ADJ
±0.5%, 50ppm/°C



Vout = 1.25V(1+R47/R49)

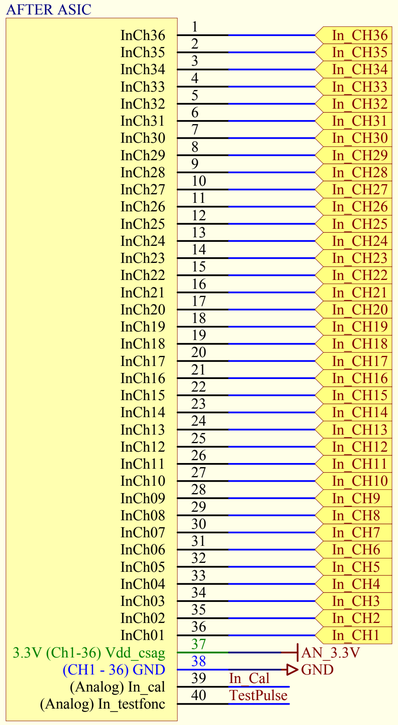
Vout = 1.25V(1.16) = 1.45 Volts

Vicm = +60uA / -26uA

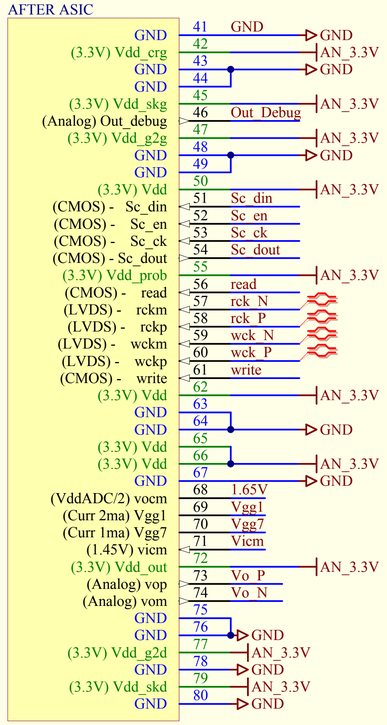
T2K FEB: SCA Interface

Revision **0**	Drawing #: 2		*TRIUMF* 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 2 of 16	Size: B	
	Drawn by: D.Bishop	Date: 06/02/2008	
File: C:\T2K\T2K_FEB_TRIUMF\T2K FEB - SCA Interface.SCHDOC			1:09:41 PM

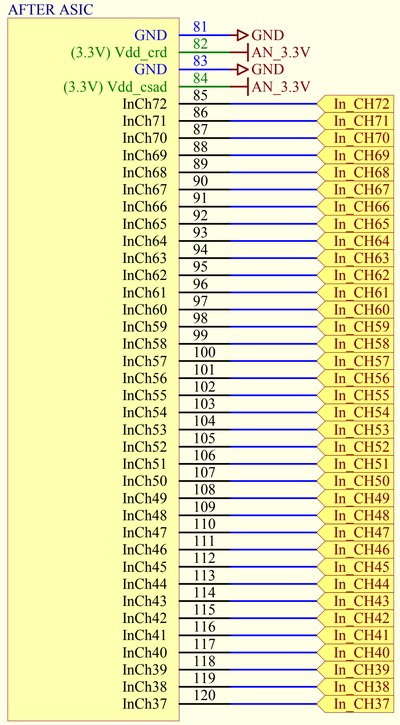
U1A
AFTER ASIC



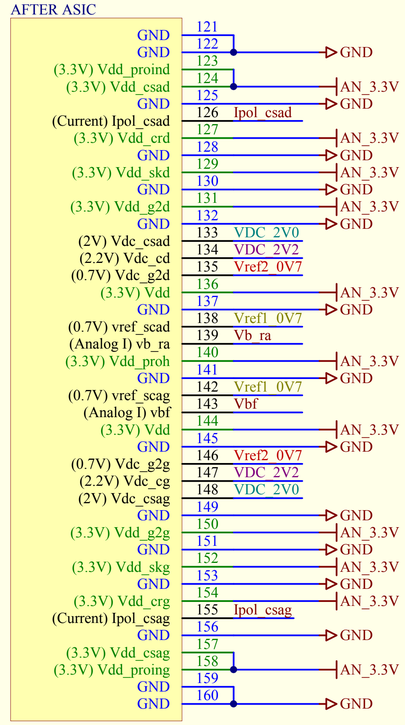
U1B
AFTER ASIC

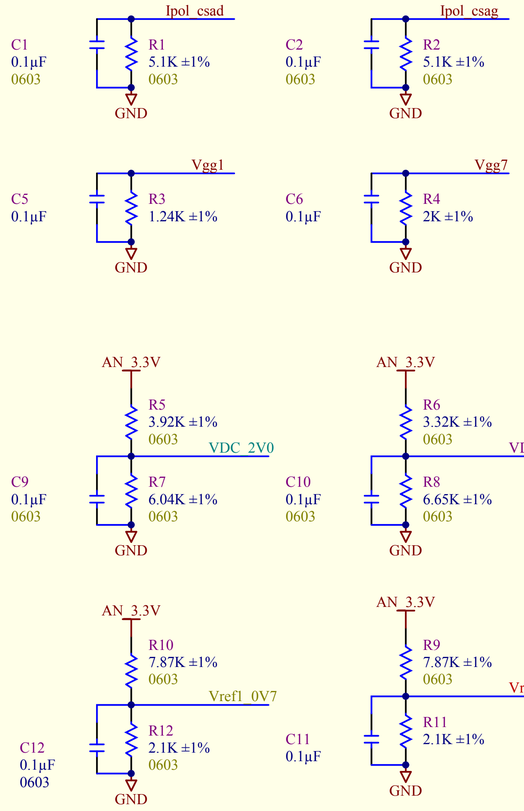


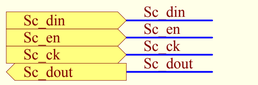
U1C
AFTER ASIC

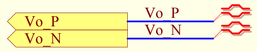


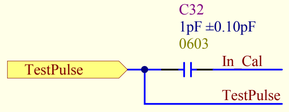
U1D
AFTER ASIC

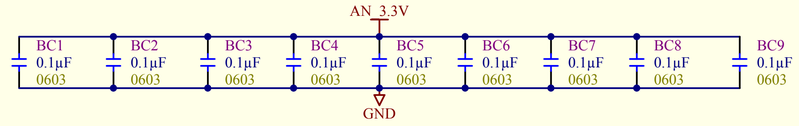


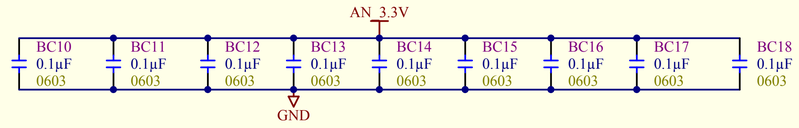


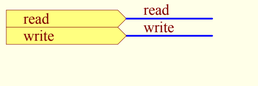


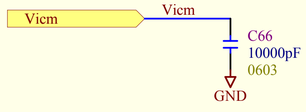


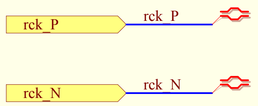


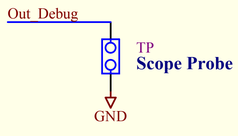












T2K FEB - AFTER ASIC

Revision 0	Drawing #: 12		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 12 of 16	Size: B	
	Drawn by: D.Bishop	Date: 06/02/2008	
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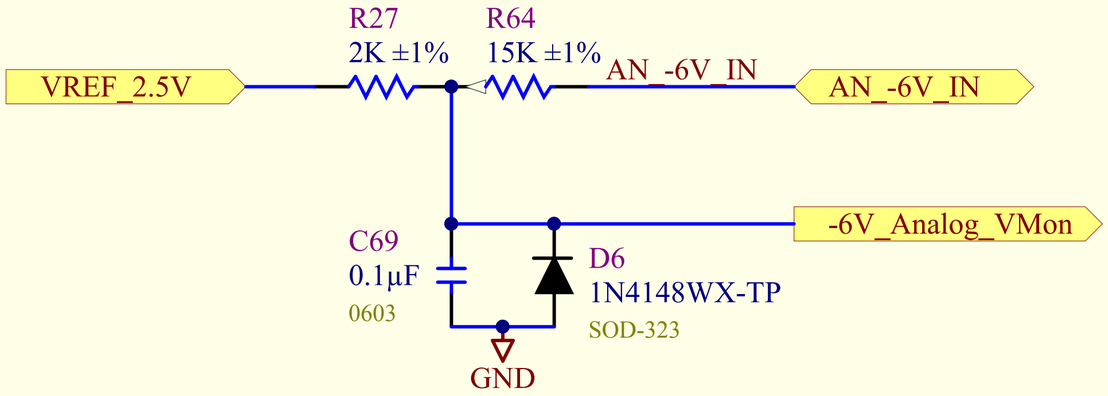

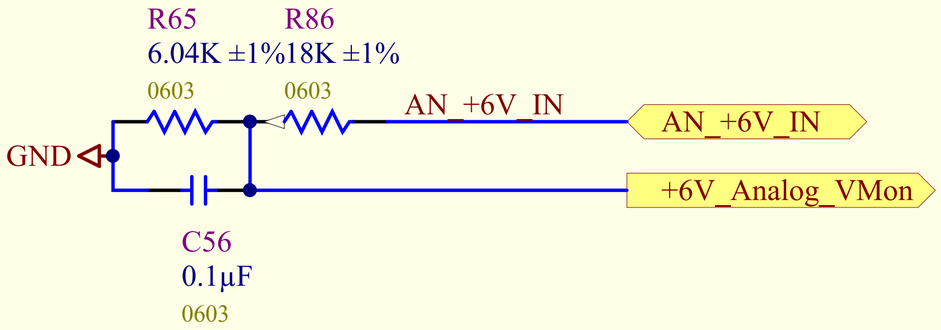

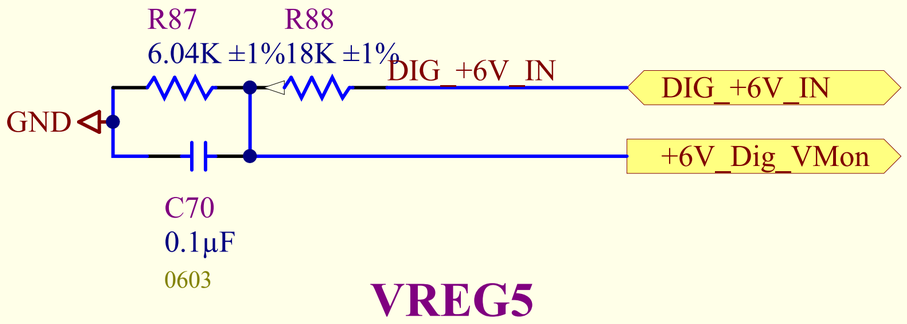

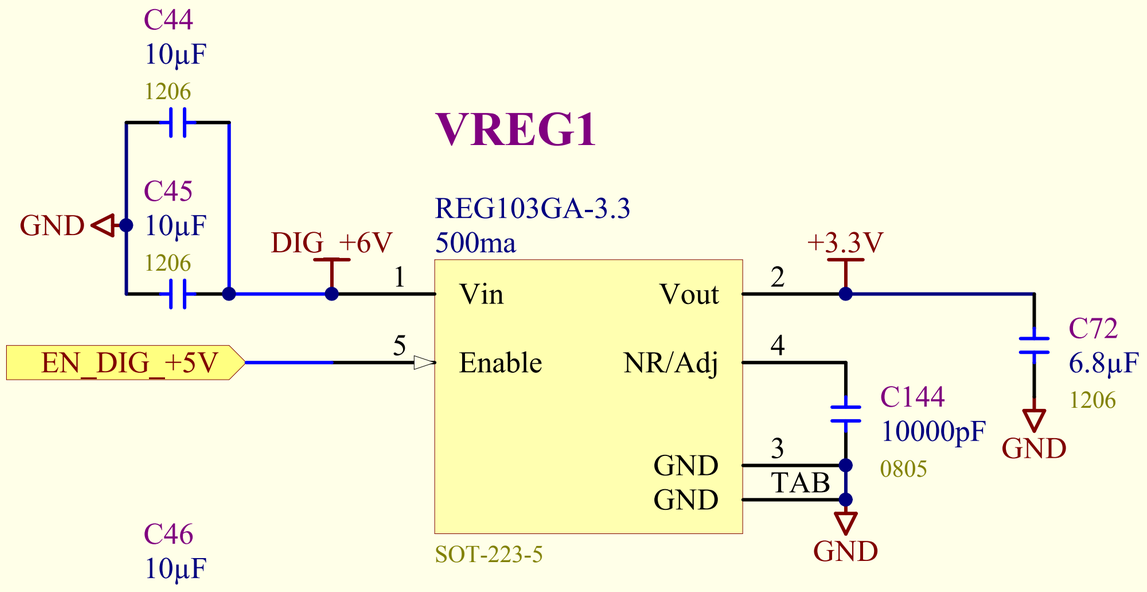

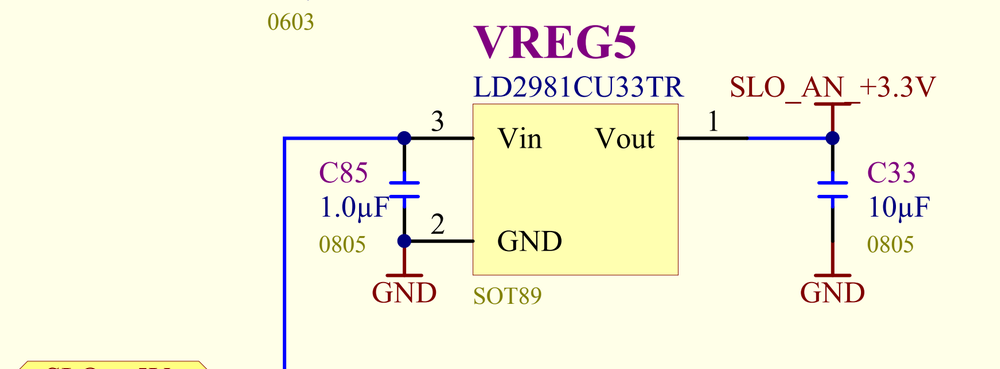

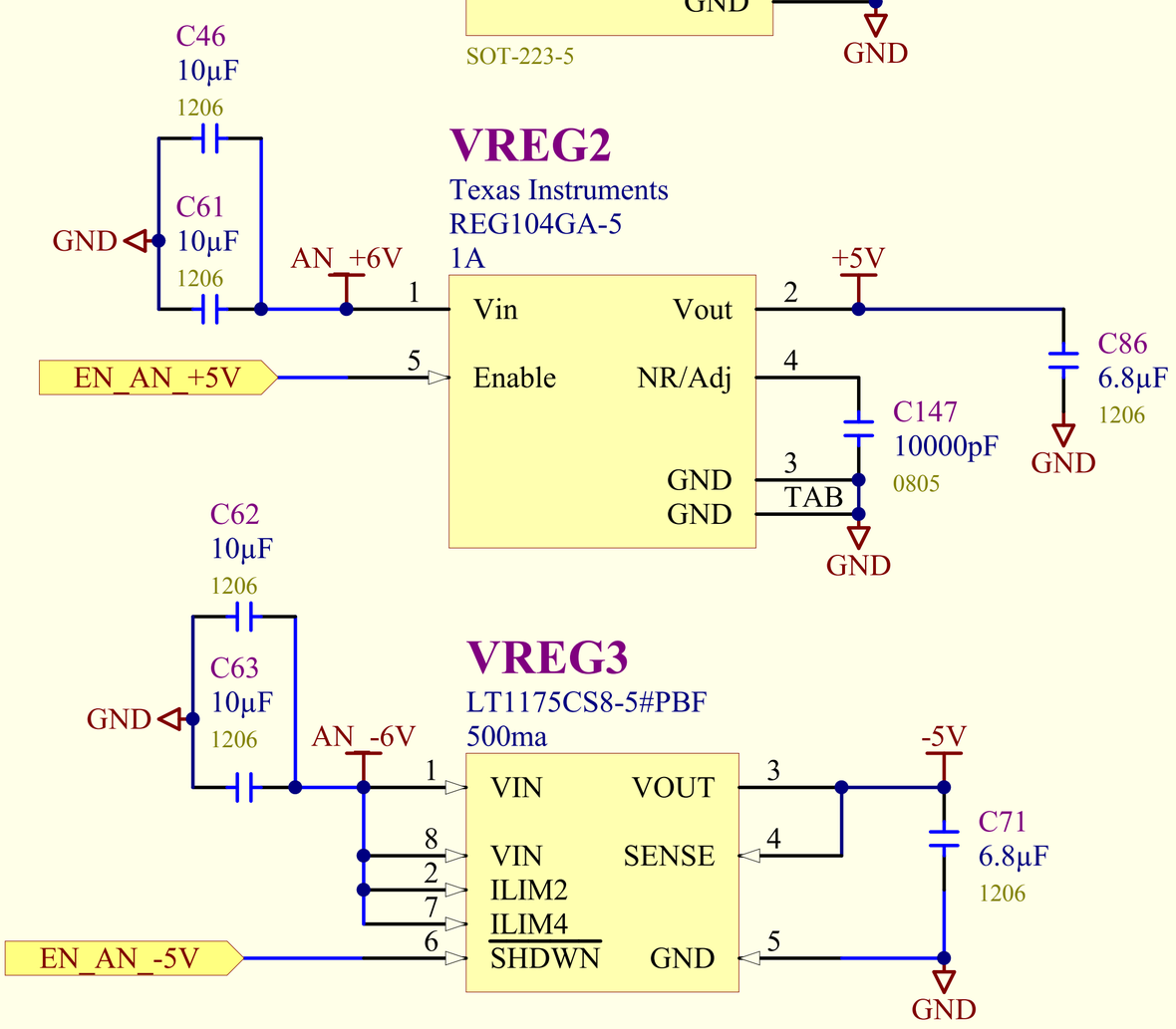

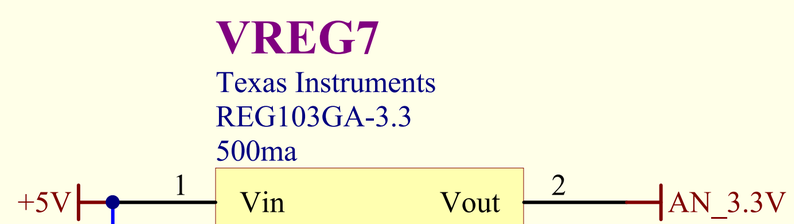

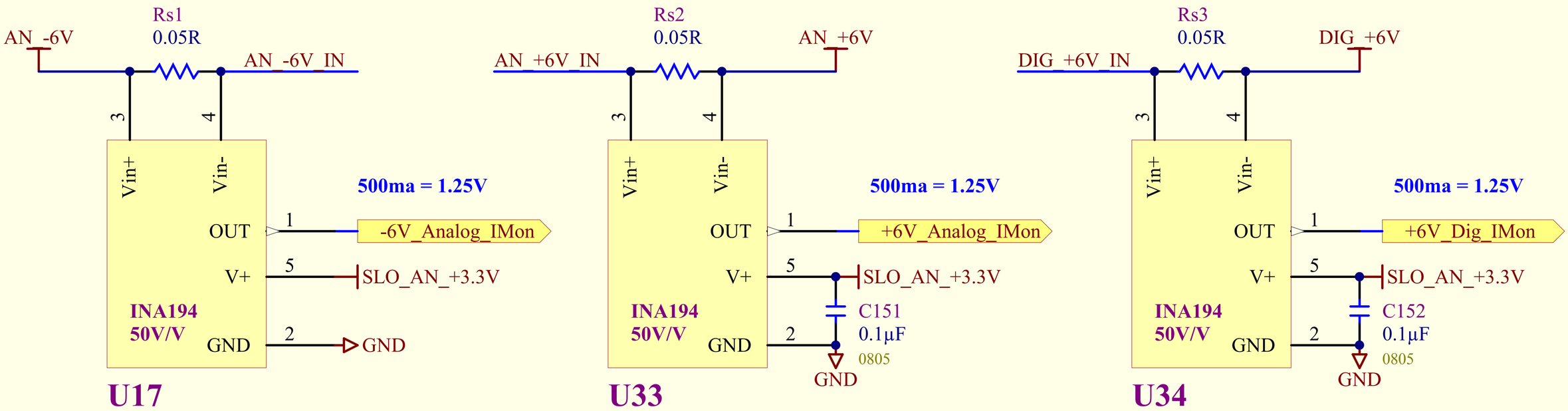

T2K FEB - Voltage Regulators - Volt/Curr Monitor

Revision 0	Drawing #: 3		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 3 of 16	Size: A	
	Drawn by: D. Bishop	Date: 06/02/2008	
File: C:\T2K\T2K_FEB_TRIUMF\T2K FEB- Regulators.SCHDOC			1:09:41 PM

U15
Silicon Laboratories
C8051F133-GQ
64-TQFP

C8051F131
C8051F133
TQFP-64

SLO_+3.3V
R50 1.00K ±1% 0603

CPU_NC0 64 | CPU_NC1 63 | CPU_RESETn 62 | CPU_TDO 61 | JTAG_TDI 60 | JTAG_TCK 59 | JTAG_TMS 58 | SLO_+3.3V 57 | GND 56 | 485_TXD 55 | 485_RXD 54 | SMB_DAT 53 | SMB_CLK 52 | CHG_PMP_CLK 51 | 485_TX_EN 50 | APD_DAC_CSn1 49

NC0 | NC1 | RSTn | TDO | TDI | TCK | TMS | VDD | DGND | TX0/P0.0 | RX0/P0.1 | P0.2 | P0.3 | P0.4 | P0.5 | P0.6

SLO_AN_+3.3V
C79 0.1µF 0603
R66 4K7 ±1% 0603
GND
R69 1.00K ±1% 0603
0.7Volts

SLO_AN_+3.3V
C168 0.1µF 0603
C80 10000pF 0603
GND

SST_REF	1	CP1-
SST_IO	2	CP1+
SPARE_CP0-	3	CP0-
SPARE_CP0+	4	CP0+
GND	5	AGND
	6	AV+
VREF_2.4V	7	Vref
	8	Vref0
BiasVoltageReadback	9	AIN0.0
BiasCurrentSense	10	AIN0.1
+6V_Dig_VMon	11	AIN0.2
+6V_Analog_VMon	12	AIN0.3
-6V_Analog_VMon	13	AIN0.4
-6V_Analog_IMon	14	AIN0.5
+6V_Analog_IMon	15	AIN0.6
+6V_Dig_IMon	16	AIN0.7

P0.7	48	APD_DAC_CSn2
P3.0	47	APD_DAC_CSn3
P3.1	46	APD_DAC_CSn4
P3.2	45	EN_AN_-5V
P3.3	44	EN_AN_+5V
P3.4	43	EN_DIG_+5V
P3.5	42	APD_DAC_CSn5
VDD	41	GND
DGND	40	SLO_+3.3V
P3.6	39	APD_DAC_CSn6
P3.7	38	RAM_CSn
P2.0	37	RAM_WPn
P2.1	36	SPI_MISO
P2.2	35	RAM_HLDn
P2.3	34	SPI_SCK
P2.4	33	SPI_MOSI

XTAL1 | XTAL2 | MONEN | P1.7/AIN2.7 | P1.6/AIN2.6 | P1.5/AIN2.5 | P1.4/AIN2.4 | VDD | GND | P1.3/AIN2.3 | P1.2/AIN2.2 | P1.1/AIN2.1 | P1.0/AIN2.0 | P2.7 | P2.6 | P2.5

17 XTAL1_IN | 18 XTAL2_OUT | 19 SLO_+3.3V | 20 ASUM_SYNC | 21 ASUM_TESTn | 22 ASUM_PdwnN | 23 SUM_DAC_CSn | 24 SLO_+3.3V | 25 GND | 26 ResetN | 27 SPARE2 | 28 SPARE3 | 29 SST_DRV | 30 SPARE1 | 31 APD_DAC_CSn8 | 32 APD_DAC_CSn7

SLO_+3.3V
C81 0.1µF 0603
C82 0.1µF 0603
C83 0.1µF 0603
GND

U40
Atmel
16K (2K x 8)
AT25160AN-10SU-2.7

SLO_+3.3V
C161 0.1µF 0603
GND

VCC	8	
GND	4	
SI	5	SPI_MOSI
SO	2	SPI_MISO
SCK	6	SPI_SCK
CS	1	RAM_CSn
HOLD	7	RAM_HLDn
WP	3	RAM_WPn

8-SOIC

U16
Analog Devices Inc
ADM3485EARZ

C78 0.1µF 0603
SLO_+3.3V
GND

485_TX_EN	3	
485_TXD	4	
485_RXD	2	
	1	
VCC	8	
	6	MSCB_RS485A
	7	MSCB_RS485B
GND	5	GND

8-SOIC

JTAG pinout compatible with
Silicon Technologies
USB DEBUG ADAPTER

SLO_+3.3V
R67 10K ±1% 0603
R68 10K ±1% 0603
GND
JTAG_TCK
JTAG_TDO

JTAG
HEADER 5X2

2	1	
4	3	GND
6	5	JTAG_TMS
8	7	JTAG_TDI
10	9	GND

IDC10/RA

SLO_+3.3V
R73 10K ±1% 0603
R75 10K ±1% 0603
GND

SLO_+3.3V
R70 1.00K ±1% 0603
R71 1.00K ±1% 0603

SMB_DAT → SMB_DAT
SMB_CLK → SMB_CLK
SPI_SCK → SPI_SCK
SPI_MOSI → SPI_MOSI
APD_DAC_CSn[8..1] → APD_DAC_CSn[8..1]
SUM_DAC_CSn → SUM_DAC_CSn
ResetN → ResetN
EN_DIG_+5V → EN_DIG_+5V
EN_AN_+5V → EN_AN_+5V
EN_AN_-5V → EN_AN_-5V
ASUM_SYNC → ASUM_SYNC
ASUM_PdwnN → ASUM_PdwnN
ASUM_TESTn → ASUM_TESTn
CHG_PMP_CLK → CHG_PMP_CLK

+6V_Analog_VMon → +6V_Analog_VMon
+6V_Analog_IMon → +6V_Analog_IMon
-6V_Analog_VMon → -6V_Analog_VMon
-6V_Analog_IMon → -6V_Analog_IMon
+6V_Dig_VMon → +6V_Dig_VMon
+6V_Dig_IMon → +6V_Dig_IMon
BiasCurrentSense → BiasCurrentSense
BiasVoltageReadback → BiasVoltageReadback
De[8..1] → De[8..1]
Dcb[8..1] → Dcb[8..1]
CPU_TDO → CPU_TDO
JTAG_TCK → JTAG_TCK
JTAG_TMS → JTAG_TMS
JTAG_TDO → JTAG_TDO
JTAG_TDI → JTAG_TDI
EN_BIASn[8..1] → EN_BIASn[8..1]
Backplane_Add[7..0] → Backplane_Add[7..0]

U18
Analog Devices
ADT7486AARMZ-REEL7

Cf4 100pF 0603
Cf6 100pF 0603

Dcb2	3	D1+	SST	10 SST_IO
De2	4	D1-	ADD0	9
Dcb1	5	D2+	ADD1	7
De1	6	D2-	RSVD	8 GND
			VCC	1 SLO_AN_+3.3V
			GND	2

ADD = 0x48
C87 0.1µF 0603
GND
MSOP10

U19
Analog Devices
ADT7486AARMZ-REEL7

Cf5 100pF 0603
Cf7 100pF 0603

Dcb4	3	D1+	SST	10 SST_IO
De4	4	D1-	ADD0	9
Dcb3	5	D2+	ADD1	7
De3	6	D2-	RSVD	8 GND
			VCC	1 SLO_AN_+3.3V
			GND	2

ADD = 0x49
R72 10K ±1% 0603 → SST_DRV
R74 10K ±1% 0603
GND
C88 0.1µF 0603
GND
MSOP10

U20
Analog Devices
ADT7486AARMZ-REEL7

Cf8 100pF 0603
Cf10 100pF 0603

Dcb6	3	D1+	SST	10 SST_IO
De6	4	D1-	ADD0	9 SLO_AN_+3.3V
Dcb5	5	D2+	ADD1	7
De5	6	D2-	RSVD	8 GND
			VCC	1 SLO_AN_+3.3V
			GND	2

ADD = 0x4A
C91 0.1µF 0603
GND
MSOP10

U21
Analog Devices
ADT7486AARMZ-REEL7

Cf9 100pF
Cf11 100pF

Dcb8	3	D1+	SST	10 SST_IO
De8	4	D1-	ADD0	9 GND
Dcb7	5	D2+	ADD1	7
De7	6	D2-	RSVD	8 GND
			VCC	1 SLO_AN_+3.3V
			GND	2

ADD = 0x4B
C92 0.1µF 0603
GND
MSOP10

U12
NXP Semiconductors
PCA9539PW-T

SLO_AN_+3.3V
RP23 10K ±1% 0603 x 4
RP24 10K ±1% 0603 x 4
RP21 470R ±5% 0603 x 4
RP22 470R ±5% 0603 x 4

SMB_CLK	22	SCL	I/O1.7	20 Backplane_Add7
SMB_DAT	23	SDA	I/O1.6	19 Backplane_Add6
			I/O1.5	18 Backplane_Add5
Address 1110100 GND	2	A1	I/O1.4	17 Backplane_Add4
GND	21	A0	I/O1.3	16 Backplane_Add3
			I/O1.2	15 Backplane_Add2
			I/O1.1	14 Backplane_Add1
ResetN	3	RESET	I/O1.0	13 Backplane_Add0
	1	INT		
			I/O0.6	10 EN_BIASn5
			I/O0.7	11 EN_BIASn1
			I/O0.5	9 EN_BIASn7
			I/O0.4	8 EN_BIASn3
SLO_AN_+3.3V	24	VDD	I/O0.3	7 EN_BIASn6
			I/O0.2	6 EN_BIASn2
			I/O0.1	5 EN_BIASn8
	12	VSS	I/O0.0	4 EN_BIASn4

C40 0.1µF 0603
GND
TSSOP-24

T2K FEB - MIDAS Slow Control

Revision 0	Drawing #: 4		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 4 of 16	Size: B	
	Drawn by: D. Bishop	Date: 06/02/2008	
File: C:\T2K\T2K_FEB_TRIUMF\T2K FEB - Slow Control.SCHDOC			1:09:42 PM

BIAS_SW
T2K FEB - 8 Channel MOSFET Switch.SCHDOC

EN_BIASn[8..1] → EN_BIASn[8..1]
BIAS → BIAS
BIAS_SW[8..1] → BIAS_SW[8..1]

I1
T2K FEB - BIAS Current Sense.SchDoc

BIAS_SW1 → BIAS_SW
BIAS_OUT → BIAS_OUT1
BiasCurrentSense → IBIAS_RDBK1
BiasVoltageReadback → VBIAS_RDBK1

I2
T2K FEB - BIAS Current Sense.SchDoc

BIAS_SW2 → BIAS_SW
BIAS_OUT → BIAS_OUT2
BiasCurrentSense → IBIAS_RDBK2
BiasVoltageReadback → VBIAS_RDBK2

I3
T2K FEB - BIAS Current Sense.SchDoc

BIAS_SW3 → BIAS_SW
BIAS_OUT → BIAS_OUT3
BiasCurrentSense → IBIAS_RDBK3
BiasVoltageReadback → VBIAS_RDBK3

I4
T2K FEB - BIAS Current Sense.SchDoc

BIAS_SW4 → BIAS_SW
BIAS_OUT → BIAS_OUT4
BiasCurrentSense → IBIAS_RDBK4
BiasVoltageReadback → VBIAS_RDBK4

I5
T2K FEB - BIAS Current Sense.SchDoc

BIAS_SW5 → BIAS_SW
BIAS_OUT → BIAS_OUT5
BiasCurrentSense → IBIAS_RDBK5
BiasVoltageReadback → VBIAS_RDBK5

I6
T2K FEB - BIAS Current Sense.SchDoc

BIAS_SW6 → BIAS_SW
BIAS_OUT → BIAS_OUT6
BiasCurrentSense → IBIAS_RDBK6
BiasVoltageReadback → VBIAS_RDBK6

I7
T2K FEB - BIAS Current Sense.SchDoc

BIAS_SW7 → BIAS_SW
BIAS_OUT → BIAS_OUT7
BiasCurrentSense → IBIAS_RDBK7
BiasVoltageReadback → VBIAS_RDBK7

I8
T2K FEB - BIAS Current Sense.SchDoc

BIAS_SW8 → BIAS_SW
BIAS_OUT → BIAS_OUT8
BiasCurrentSense → IBIAS_RDBK8
BiasVoltageReadback → VBIAS_RDBK8

BIAS_OUT[8..1] → BIAS_OUT[8..1]
VREF_2.5V → VREF_2.5V

ADC1
Linear Technologies
LTC2497CUHF#PBF

VBIAS_RDBK2	8	CH0	
VBIAS_RDBK4	9	CH1	
VBIAS_RDBK6	10	CH2	
VBIAS_RDBK8	11	CH3	
IBIAS_RDBK2	12	CH4	
IBIAS_RDBK4	13	CH5	
IBIAS_RDBK6	14	CH6	
IBIAS_RDBK8	15	CH7	
VBIAS_RDBK1	16	CH8	
VBIAS_RDBK3	17	CH9	
VBIAS_RDBK5	18	CH10	
VBIAS_RDBK7	19	CH11	
IBIAS_RDBK1	20	CH12	
IBIAS_RDBK3	21	CH13	
IBIAS_RDBK5	22	CH14	
IBIAS_RDBK7	23	CH15	
ADC_COM	7	COM	
	29	REF+	
GND	30	REF-	
	24	MUXOUTP	
	25	ADCINp	
	27	MUXOUTn	
	26	ADCINn	
	2	SCL	SMB_CLK
	3	SDA	SMB_DAT
	38	CA2	
	37	CA1	
	36	CA0	
	35	FO	GND
	5	NC	
	28	VCC	SLO_AN_+3.3V
	1	GND	
	4	GND	
	6	GND	
	31	GND	
	32	GND	
	33	GND	
	34	GND	
	39	PP_GND	

38-QFN

ADD = 1000101

NOTE:
LTC2497 requires CMOS level digital inputs (0.7xVCC min)

C73 0.1µF 0603 (SLO_AN_+3.3V)
C74 1.0µF 0603 (SLO_AN_+3.3V)

Input range:

(+/- 0.5 x VREF)

Vref1
Analog Devices Inc
REF192ESZ
2.5V ±0.8%
8-SOIC

1	NC_TP1	NC	8
2	VCC	NC	7
3	SLEEP	OUT	6
4	GND	NC_TP5	5

SLO_AN_+3.3V → VCC
C75 0.1µF 0603 → GND
VREF_2.5V → C76 0.1µF 0603 → GND

VREF_2.5V → R51 10K ±0.1% 0603 → ADC_COM
ADC_COM → R52 10K ±0.1% 0603 → GND
ADC_COM → C77 0.1µF 0603 → GND

Revision	0
Drawing #:	6
Sheet #:	6 of 16
Size:	A
Drawn by:	D.Bishop
Date:	06/02/2008

T2K FEB - BIAS Output x 64 / Voltage & Current Readback

TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3

File: C:\T2K\T2K_FEB_TRIUMF\T2K FEB - BIAS Output.SchDoc

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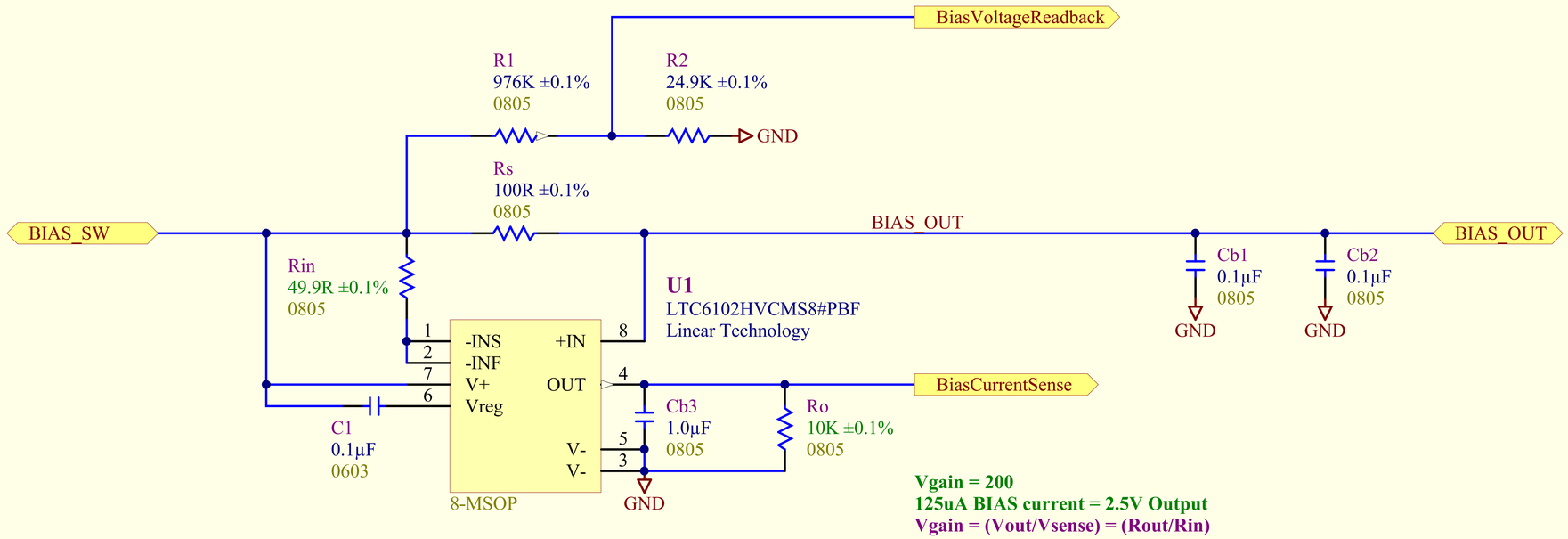

T2K FEB - BIAS Current Sense

Revision 0	Drawing #: 7		*TRIUMF* 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 7 of 16	Size: A	
	Drawn by: D.Bishop	Date: 06/02/2008	
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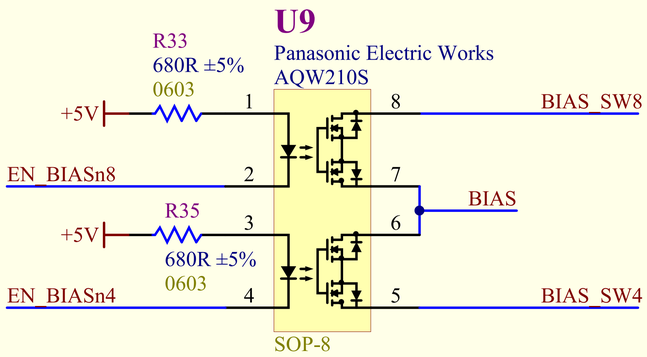
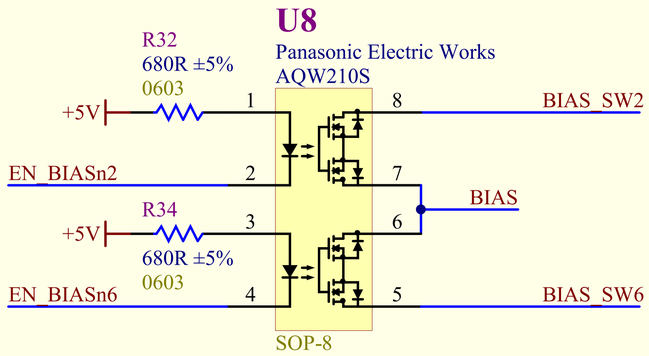
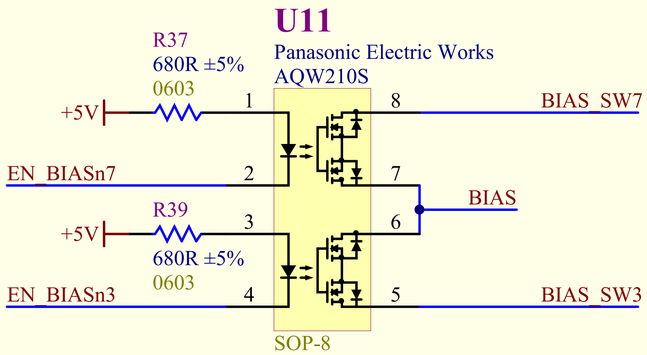
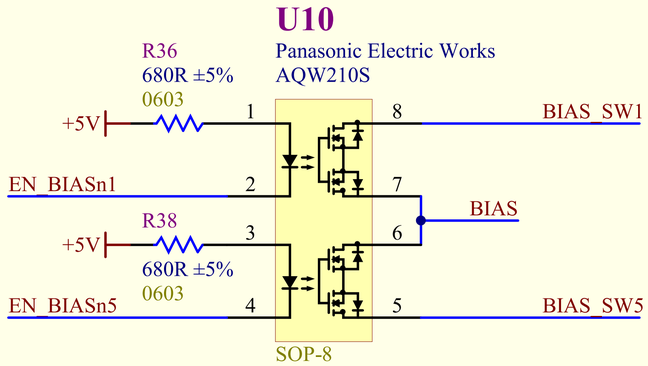








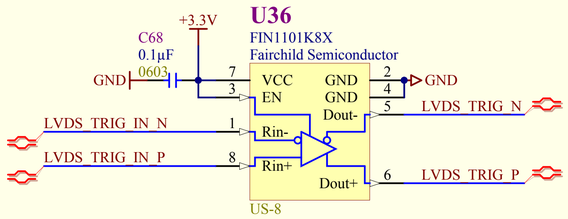
EN_BIASn[8..1] — EN_BIASn[8..1]

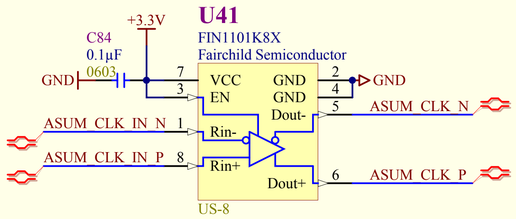
BIAS_SW[8..1] — BIAS_SW[8..1]

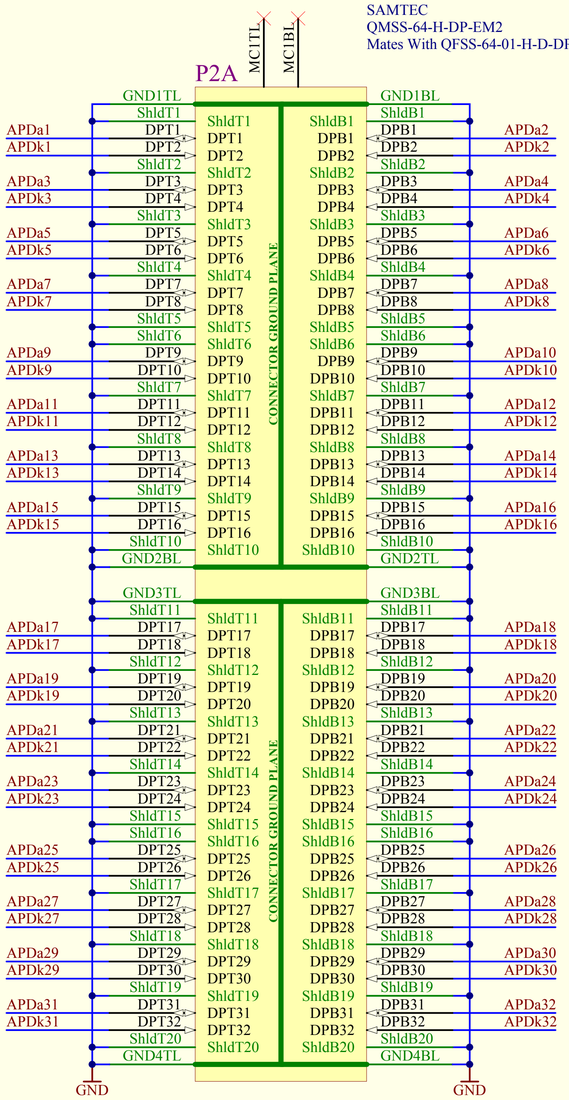
BIAS — BIAS

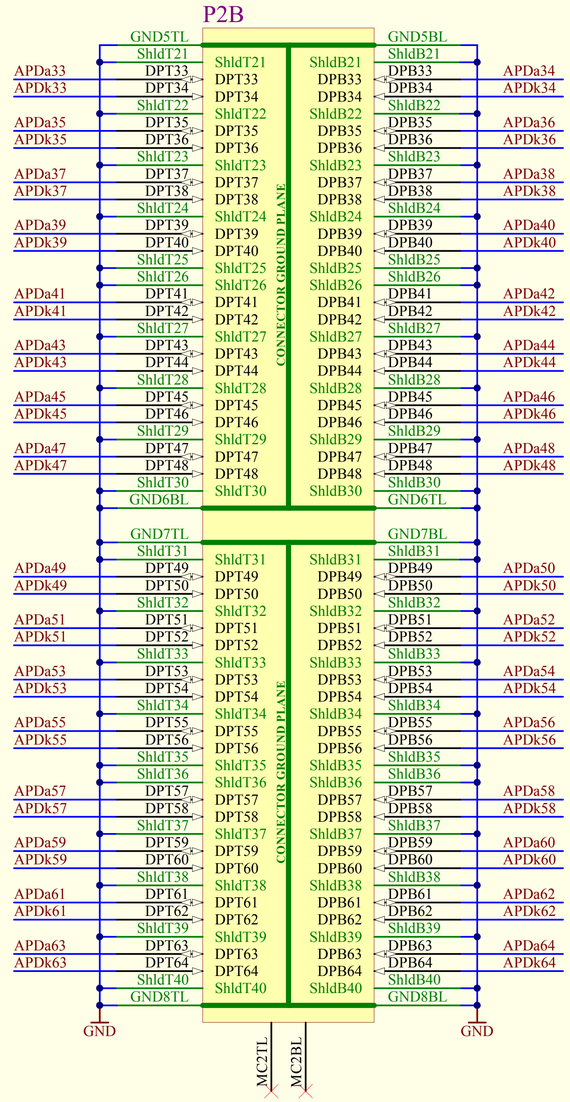
T2K FEB - 8 Channel Mosfet Switch

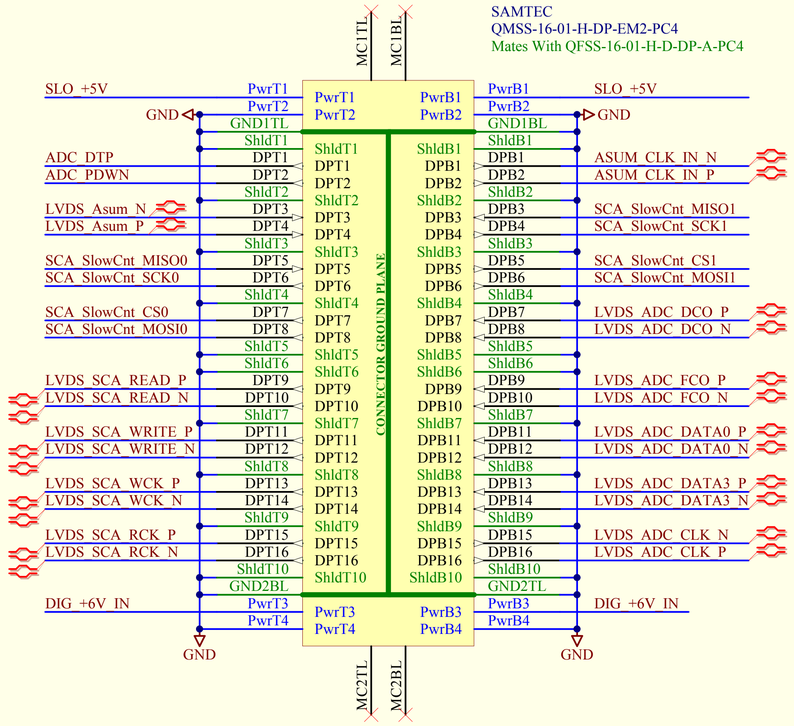
Revision 0	Drawing #: 16		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 16 of 16	Size: A	
	Drawn by: D.Bishop	Date: 06/02/2008	
File: C:\T2K\T2K_FEB_TRIUMF\T2K FEB - 8 Channel MOSFET Switch.SCHDOC			1:09:42 PM

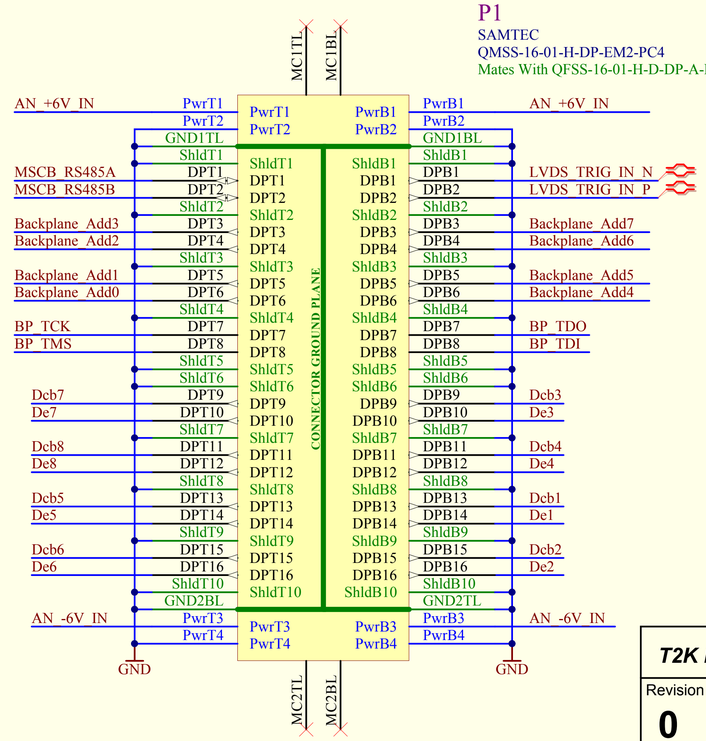


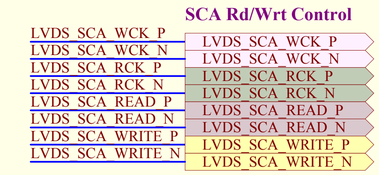


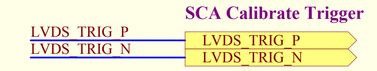


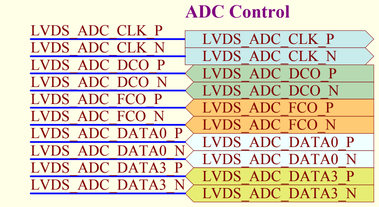


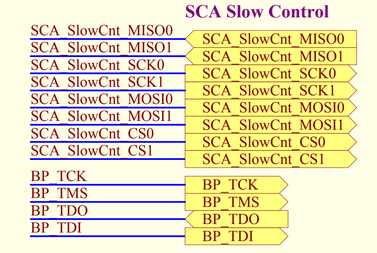


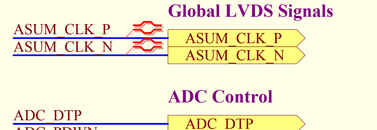


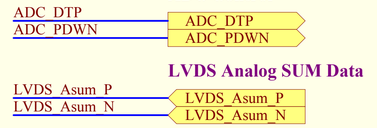


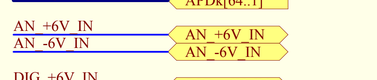


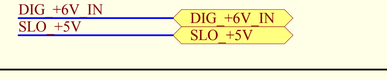












T2K FEB - Backplane Connections

Revision 0	Drawing #: 8		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 8 of 16	Size: B	
	Drawn by: Daryl Bishop	Date: 06/02/2008	

File: C:\T2K\T2K_FEB_TRIUMF\T2K FEB - Backplane Connections.SCHDOC 1:09:42 PM

ASUM_IN[8..1] — ASUM_IN[8..1]

ASUM_OUT[8..1] — ASUM_OUT[8..1]

SUM1
T2K FEB - Analog SUM.SCHDOC

ASUM_IN1 — ASUM_IN — ASUM_OUT — ASUM_OUT1
COMP_IN — COMP_IN1

SUM2
T2K FEB - Analog SUM.SCHDOC

ASUM_IN2 — ASUM_IN — ASUM_OUT — ASUM_OUT2
COMP_IN — COMP_IN2

SUM3
T2K FEB - Analog SUM.SCHDOC

ASUM_IN3 — ASUM_IN — ASUM_OUT — ASUM_OUT3
COMP_IN — COMP_IN3

SUM4
T2K FEB - Analog SUM.SCHDOC

ASUM_IN4 — ASUM_IN — ASUM_OUT — ASUM_OUT4
COMP_IN — COMP_IN4

SUM5
T2K FEB - Analog SUM.SCHDOC

ASUM_IN5 — ASUM_IN — ASUM_OUT — ASUM_OUT5
COMP_IN — COMP_IN5

SUM6
T2K FEB - Analog SUM.SCHDOC

ASUM_IN6 — ASUM_IN — ASUM_OUT — ASUM_OUT6
COMP_IN — COMP_IN6

SUM7
T2K FEB - Analog SUM.SCHDOC

ASUM_IN7 — ASUM_IN — ASUM_OUT — ASUM_OUT7
COMP_IN — COMP_IN7

SUM8
T2K FEB - Analog SUM.SCHDOC

ASUM_IN8 — ASUM_IN — ASUM_OUT — ASUM_OUT8
COMP_IN — COMP_IN8

U31
AD8564ARZ

+5V — R77 10R ±1% 0603 — C121 1.0µF 0603 — GND
C123 0.1µF 0603 — GND

COMP_IN1 2 — THRESHOLD1 1 — A — V+ Dig 11 — 4 ASUM_TRIG1
COMP_IN2 7 — THRESHOLD2 8 — B — 5 ASUM_TRIG2
V+ ana 14 — V- ana 6
COMP_IN3 10 — THRESHOLD3 9 — C — 12 ASUM_TRIG3
COMP_IN4 15 — THRESHOLD4 16 — D — GND 3 — GND — 13 ASUM_TRIG4

+5V — C126 0.1µF 0603 — C127 1.0µF 0603 — GND
-5V — C130 0.1µF 0603 — C131 1.0µF 0603 — GND

16-SOIC

RP19 470R ±5% 0603 x 4 — CP17 0.1µF 0612

SUM_DAC1 — THRESHOLD1
SUM_DAC2 — THRESHOLD2
SUM_DAC3 — THRESHOLD3 — GND
SUM_DAC4 — THRESHOLD4

SUM_DAC5 — THRESHOLD5
SUM_DAC6 — THRESHOLD6
SUM_DAC7 — THRESHOLD7 — GND
SUM_DAC8 — THRESHOLD8

RP20 470R ±5% 0603 x 4 — CP18 0.1µF 0612

U30
AD8564ARZ

+5V — R76 10R ±1% 0603 — C120 1.0µF 0603 — GND
C122 0.1µF 0603 — GND

COMP_IN5 2 — THRESHOLD5 1 — A — V+ Dig 11 — 4 ASUM_TRIG5
COMP_IN6 7 — THRESHOLD6 8 — B — 5 ASUM_TRIG6
V+ ana 14 — V- ana 6
COMP_IN7 10 — THRESHOLD7 9 — C — 12 ASUM_TRIG7
COMP_IN8 15 — THRESHOLD8 16 — D — GND 3 — GND — 13 ASUM_TRIG8

+5V — C124 0.1µF 0603 — C125 1.0µF 0603 — GND
-5V — C128 0.1µF 0603 — C129 1.0µF 0603 — GND

16-SOIC

U37
Texas Instruments
SN65LV1023AMDBREP

ASUM_DATA1 3 — Din0 — Do+ — 22 LVDS_ASum_P — LVDS_ASum_P
ASUM_DATA2 4 — Din1 — Do- — 21 LVDS_ASum_N — LVDS_ASum_N
ASUM_DATA3 5 — Din2
ASUM_DATA4 6 — Din3
ASUM_DATA5 7 — Din4
ASUM_DATA6 8 — Din5 — DVcc — 28
ASUM_DATA7 9 — Din6 — DVcc — 27
ASUM_DATA8 10 — Din7
+3.3V — 11 — Din8 — DGND — 16
12 — Din9 — DGND — 15
ASUM_CLK 14 — TCLK
AVcc — 26
ASUM_SYNC 1 — SYNC1 — AVcc — 17
2 — SYNC2 — AGND — 25
ASUM_PdwnN 24 — PWRDN — AGND — 23
19 — DEN — AGND — 20
+3.3V — 13 — TCLK/R/F — AGND — 18

+3.3V — C3 10000pF 0603 — C4 0.1µF 0603 — GND
+3.3V — C7 10000pF 0603 — C8 0.1µF 0603 — GND

28-SSOP

U32
Linear Technology
LTC2600CGN#PBF
16-Bits

SUM_DAC_SCK 8 — SCK — Vout H — 15 SUM_DAC8
SUM_DAC_DIN 9 — Din — Vout G — 14 SUM_DAC7
10 — Dout — Vout F — 13 SUM_DAC6
SUM_DAC_CSn 7 — CS/LD — Vout E — 12 SUM_DAC5
SUM_DAC_CLRn 11 — CLR — Vout D — 5 SUM_DAC4
Vout C — 4 SUM_DAC3
Vout B — 3 SUM_DAC2
Vout A — 2 SUM_DAC1
REF — 6 ASUM_DAC_REF
VCC — 16 — C142 0.1µF 0603 — C143 1.0µF 0603 — +5V
GND — 1 — GND

SSOP16

Pin Compatible Versions
LTC2610: 14Bits
LTC2620: 12Bits
LTC1660: 10Bits
LTC1665: 8-Bits

VREF2
Analog Devices Inc
REF198FSZ
4.096 V ±0.12%
10 ppm/°C

C141 0.1µF 0603 — GND
8 NC — NC_TP1 — 1 — +5V
7 NC — VCC — 2 — C138 0.1µF 0603
6 OUT — SLEEP — 3
5 NC_TP5 — GND — 4 — GND

8-SOIC

U39
Texas Instruments
SN65LVDS2DBVR

+3.3V — C167 0.1µF 0603 — GND

ASUM_CLK_P — RT6 100R 1% 0603 — 3 — Vcc — 1 — 5
ASUM_CLK_N — 4 — R2 — Gnd — 2 — GND

SOT23-5

ASUM_TESTn — ASUM_TESTn
XILINX_TDI — XILINX_TDI
XILINX_TDO — XILINX_TDO
JTAG_TMS — JTAG_TMS
JTAG_TCK — JTAG_TCK

U38E
XCR3064XL-10VQG44C

ASUM_CLK 40 — IN0/CLK0
ASUM_TESTn 39 — IN1/CLK1
38 — IN2/CLK2
37 — IN3/CLK3
4 — PORT_EN — GND

44-VQFP

U38F
XCR3064XL-10VQG44C

+3.3V — 41 VCC — VCC — 9 — +3.3V
29 VCC — VCC — 17
C165 0.1µF — C166 0.1µF — C163 0.1µF 0603 — C164 0.1µF 0603

U38G
XCR3064XL-10VQG44C

36 GND — GND — 16 — GND
24 GND

GND — 44-VQFP

U38B
XCR3064XL-10VQG44C

GND — 42 — 43 — 44 — I/O — BANK 2
XILINX_TDI 1 — I/O, TDI
ASUM_DATA8 2
ASUM_DATA7 3
ASUM_DATA6 5
ASUM_DATA5 6

44-VQFP

U38D
XCR3064XL-10VQG44C

JTAG_TMS 7 — I/O, TMS — BANK 4
ASUM_DATA4 8
ASUM_DATA3 10
ASUM_DATA2 11
ASUM_DATA1 12
13
GND — 14 — 15

44-VQFP

U38A
XCR3064XL-10VQG44C

ASUM_TRIG8 27 — I/O — BANK 1
ASUM_TRIG2 28
ASUM_TRIG1 30
ASUM_TRIG3 31
XILINX_TDO 32 — I/O, TDO
ASUM_TRIG4 33
34
GND — 35

44-VQFP

U38C
XCR3064XL-10VQG44C

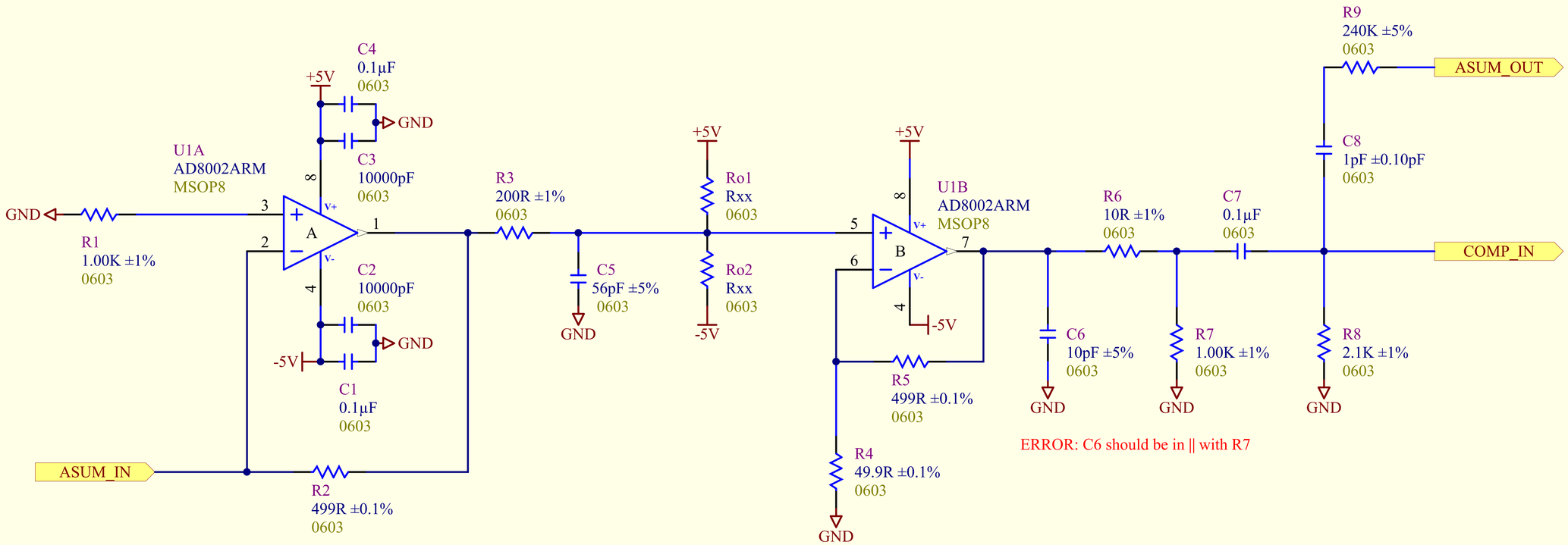
GND — 18 — 19 — 20 — 21 — I/O — BANK 3
ASUM_TRIG5 22
ASUM_TRIG6 23
ASUM_TRIG7 25
JTAG_TCK 26 — I/O, TCK

44-VQFP

T2K FEB - APD SUM x 8

Revision	Drawing #: 9		TRIUMF
0	Sheet #: 9 of 16	Size: B	4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Drawn by: D.Bishop	Date: 06/02/2008	

File: C:\T2K\T2K_FEB_TRIUMF\T2K FEB - APD SUM.SCHDOC — 1:09:42 PM



T2K 8 Channel Bias - OP Amps

Revision **0**	Drawing #: 11		*TRIUMF* 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 11 of 16	Size: A	
	Drawn by: D. Bishop	Date: 06/02/2008	
File: C:\T2K\T2K_FEB_TRIUMF\T2K FEB - Analog SUM.SCHDOC			1:09:42 PM

APDa[64..1] → APDa[64..1]

BIAS_OUT[8..1] → BIAS_OUT[8..1]

APD_HATTN[64..1] → APD_HATTN[64..1]

APD_LATTN[64..1] → APD_LATTN[64..1]

ASUM_IN[8..1] → ASUM_IN[8..1]

DIV1

T2K FEB - Charge Division.SCHDOC

APDa[8..1] → APD_IN[8..1]

BIAS_OUT1 → BIAS_OUT

APD_H[8..1] → APD_HATTN[8..1]

APD_L[8..1] → APD_LATTN[8..1]

ASUM → ASUM_IN1

DIV2

T2K FEB - Charge Division.SCHDOC

APDa[16..9] → APD_IN[8..1]

BIAS_OUT2 → BIAS_OUT

APD_H[8..1] → APD_HATTN[16..9]

APD_L[8..1] → APD_LATTN[16..9]

ASUM → ASUM_IN2

DIV3

T2K FEB - Charge Division.SCHDOC

APDa[24..17] → APD_IN[8..1]

BIAS_OUT3 → BIAS_OUT

APD_H[8..1] → APD_HATTN[24..17]

APD_L[8..1] → APD_LATTN[24..17]

ASUM → ASUM_IN3

DIV4

T2K FEB - Charge Division.SCHDOC

APDa[32..25] → APD_IN[8..1]

BIAS_OUT4 → BIAS_OUT

APD_H[8..1] → APD_HATTN[32..25]

APD_L[8..1] → APD_LATTN[32..25]

ASUM → ASUM_IN4

DIV5

T2K FEB - Charge Division.SCHDOC

APDa[40..33] → APD_IN[8..1]

BIAS_OUT5 → BIAS_OUT

APD_H[8..1] → APD_HATTN[40..33]

APD_L[8..1] → APD_LATTN[40..33]

ASUM → ASUM_IN5

DIV6

T2K FEB - Charge Division.SCHDOC

APDa[48..41] → APD_IN[8..1]

BIAS_OUT6 → BIAS_OUT

APD_H[8..1] → APD_HATTN[48..41]

APD_L[8..1] → APD_LATTN[48..41]

ASUM → ASUM_IN6

DIV7

T2K FEB - Charge Division.SCHDOC

APDa[56..49] → APD_IN[8..1]

BIAS_OUT7 → BIAS_OUT

APD_H[8..1] → APD_HATTN[56..49]

APD_L[8..1] → APD_LATTN[56..49]

ASUM → ASUM_IN7

DIV8

T2K FEB - Charge Division.SCHDOC

APDa[64..57] → APD_IN[8..1]

BIAS_OUT8 → BIAS_OUT

APD_H[8..1] → APD_HATTN[64..57]

APD_L[8..1] → APD_LATTN[64..57]

ASUM → ASUM_IN8

T2K FEB - APD Inputs

Revision **0**	Drawing #: 10		*TRIUMF* 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 10 of 16	Size: A	
	Drawn by: D.Bishop	Date: 06/02/2008	
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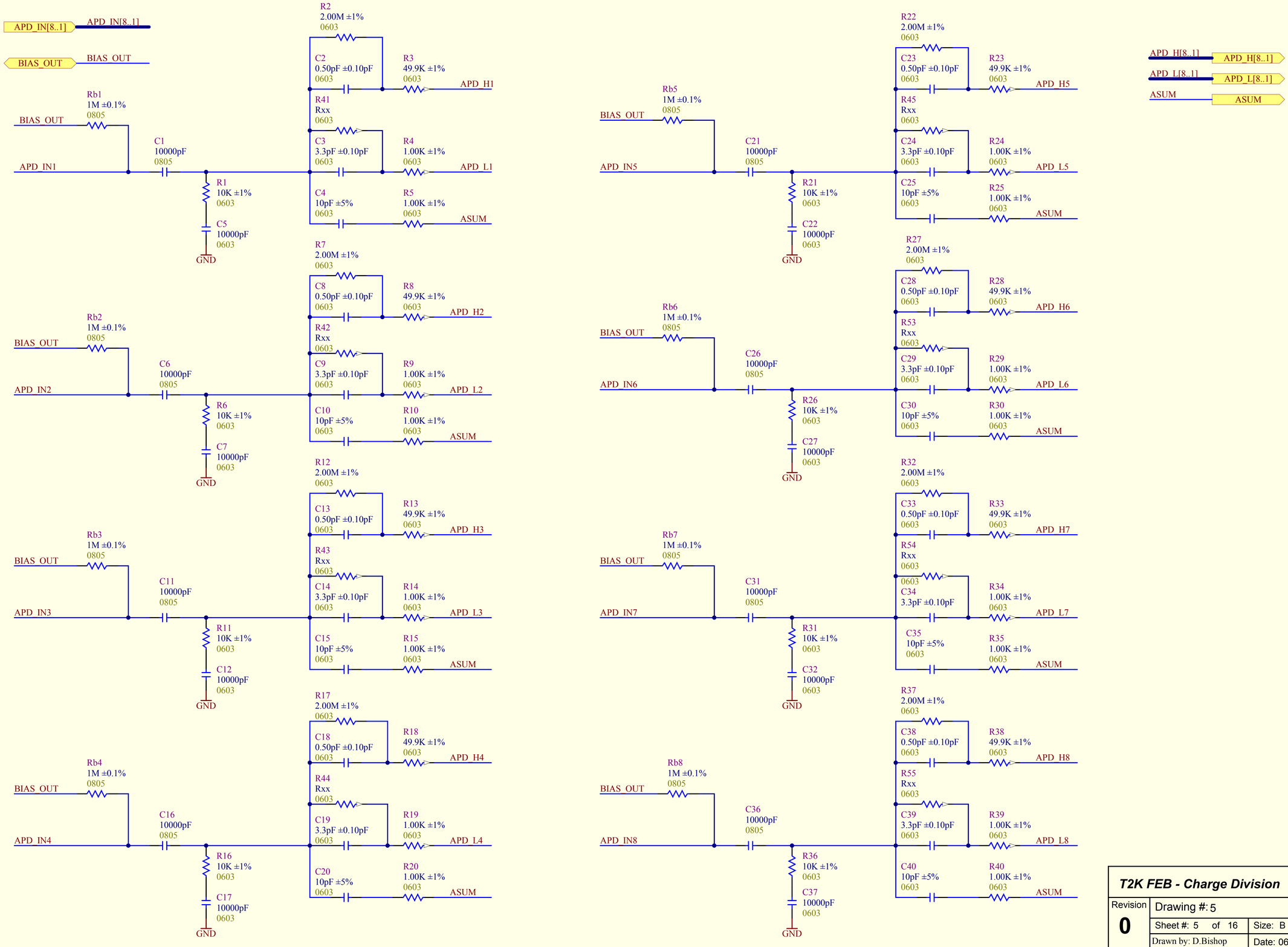

T2K FEB - Charge Division

Revision 0	Drawing #: 5		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 5 of 16	Size: B	
	Drawn by: D.Bishop	Date: 06/02/2008	
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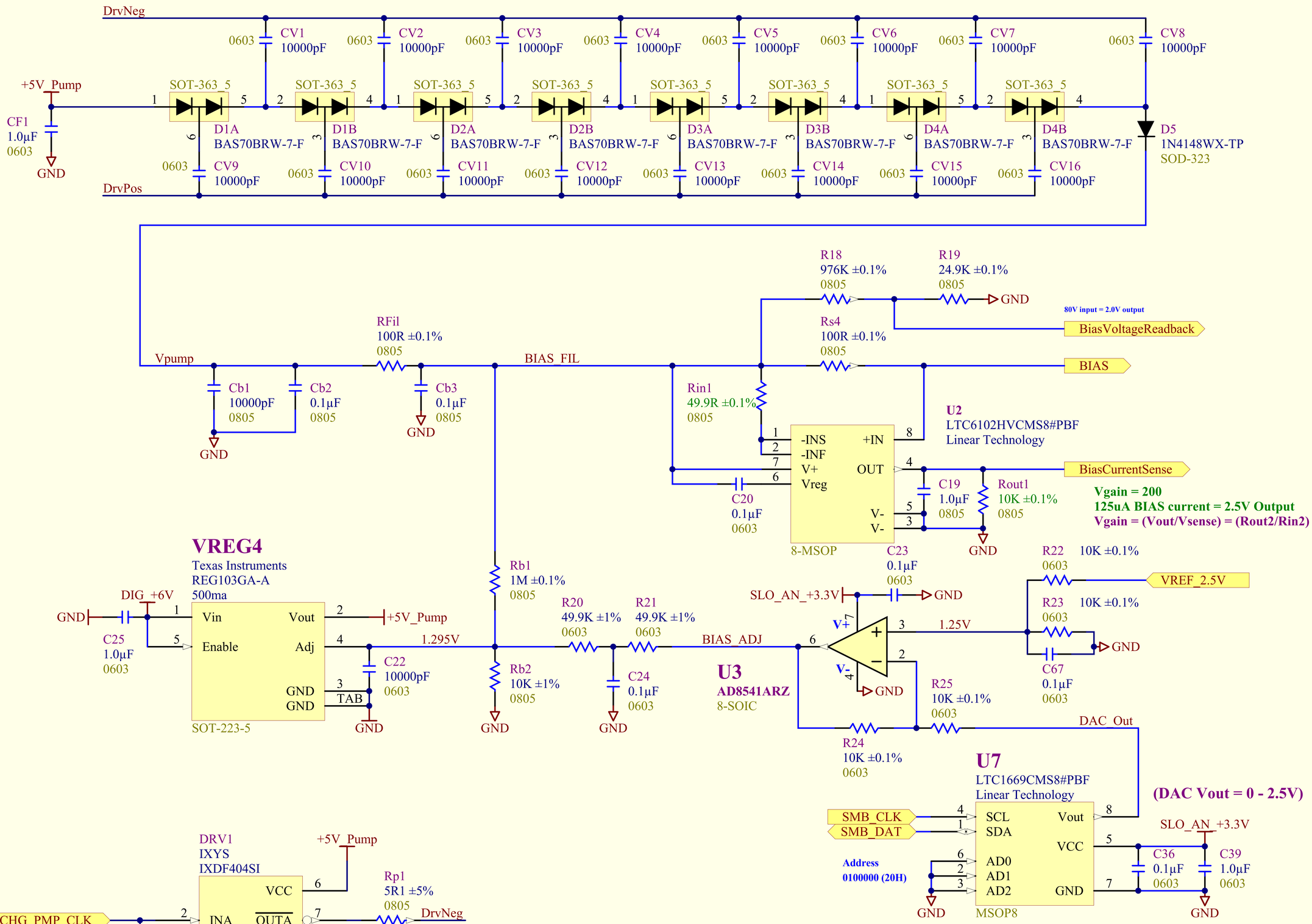
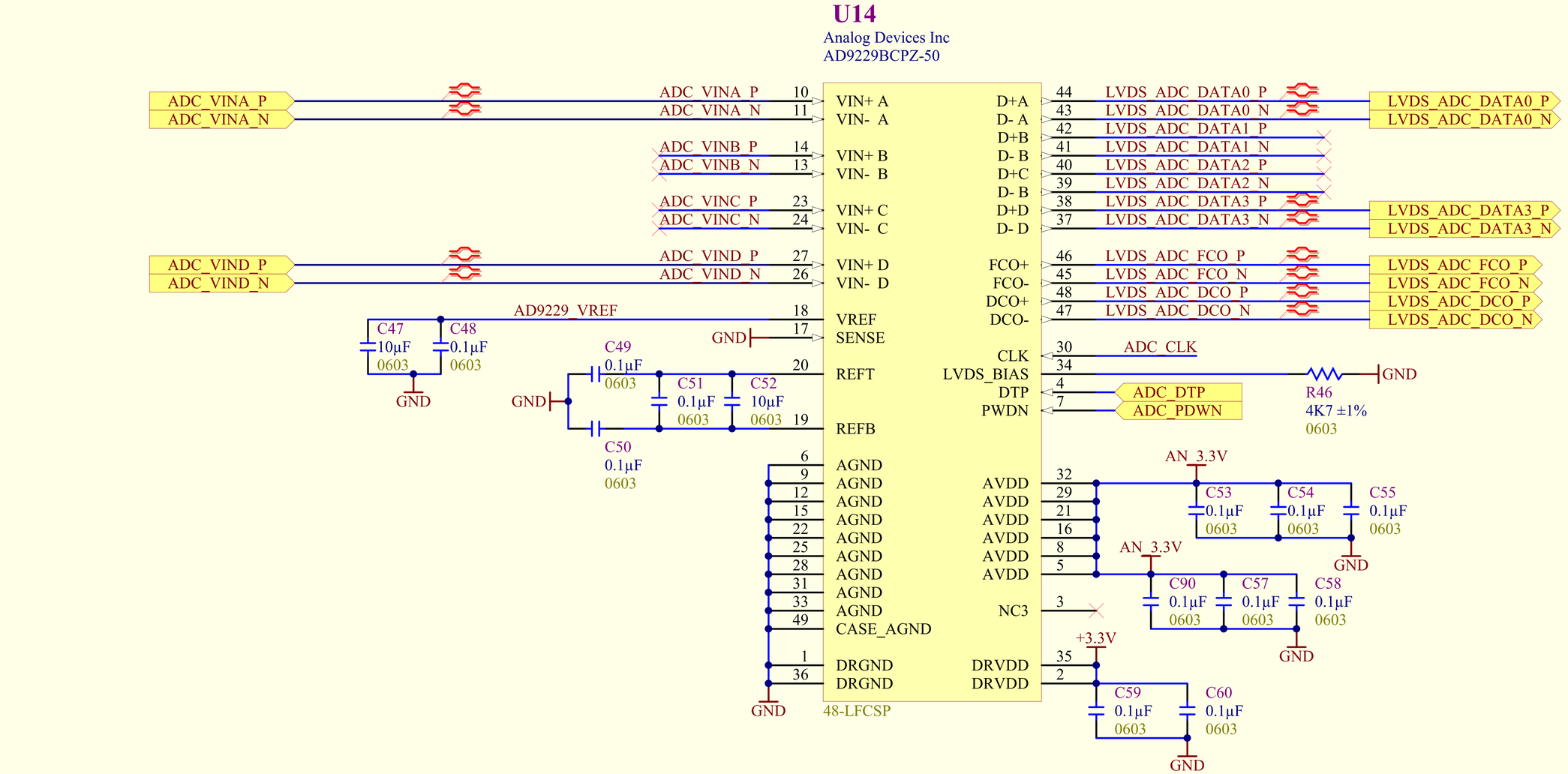


T2K FEB: BIAS / Total Bias Current Sense

Revision 0	Drawing #: 13		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 13 of 16	Size: A	
	Drawn by: D. Bishop	Date: 06/02/2008	
File: C:\T2K\T2K_FEB_TRIUMF\T2K FEB - 80 Volt Charge Pump.SCHDOC			1:09:43 PM



T2K FEB - 65MSPS ADC			
Revision **0**	Drawing #: 14		*TRIUMF* 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 14 of 16	Size: A	
	Drawn by: D.Bishop	Date: 06/02/2008	
File: C:\T2K\T2K_FEB_TRIUMF\T2K FEB - 50MSPS ADC.SCHDOC			1:09:43 PM

APD_DAC[64..1]

APD_DAC_CSn[8..1]

APD_DAC_SCK
APD_DAC_DIN
APD_DAC_CLRn

Pin Compatible Versions
LTC2600: 16-Bits
LTC2610: 14-Bits
LTC2620: 12-Bits
LTC1660: 10-Bits
LTC1665: 8-Bits

U22
Linear Technology
LTC1665CGN#PBF
SSOP16

RP3 0603 x 4: APD_DAC8, APD_DAC7, APD_DAC6, APD_DAC5
RP4 0603 x 4: APD_DAC4, APD_DAC3, APD_DAC2, APD_DAC1

APD_DAC_CSn1

C169 0.1µF 0603

U24
Linear Technology
LTC1665CGN#PBF
SSOP16

RP7 0603 x 4: APD_DAC16, APD_DAC15, APD_DAC14, APD_DAC13
RP8 0603 x 4: APD_DAC12, APD_DAC11, APD_DAC10, APD_DAC9

APD_DAC_CSn2

C187 0.1µF 0603

U26
Linear Technology
LTC1665CGN#PBF
SSOP16

RP11 0603 x 4: APD_DAC24, APD_DAC23, APD_DAC22, APD_DAC21
RP12 0603 x 4: APD_DAC20, APD_DAC19, APD_DAC18, APD_DAC17

APD_DAC_CSn3

C205 0.1µF 0603

U28
Linear Technology
LTC1665CGN#PBF
SSOP16

RP15 0603 x 4: APD_DAC32, APD_DAC31, APD_DAC30, APD_DAC29
RP16 0603 x 4: APD_DAC28, APD_DAC27, APD_DAC26, APD_DAC25

APD_DAC_CSn4

C207 0.1µF 0603

U23
Linear Technology
LTC1665CGN#PBF
SSOP16

RP5 0603 x 4: APD_DAC40, APD_DAC39, APD_DAC38, APD_DAC37
RP6 0603 x 4: APD_DAC36, APD_DAC35, APD_DAC34, APD_DAC33

APD_DAC_CSn5

C170 0.1µF 0603

U25
Linear Technology
LTC1665CGN#PBF
SSOP16

RP9 0603 x 4: APD_DAC48, APD_DAC47, APD_DAC46, APD_DAC45
RP10 0603 x 4: APD_DAC44, APD_DAC43, APD_DAC42, APD_DAC41

APD_DAC_CSn6

C188 0.1µF 0603

U27
Linear Technology
LTC1665CGN#PBF
SSOP16

RP13 0603 x 4: APD_DAC56, APD_DAC55, APD_DAC54, APD_DAC53
RP14 0603 x 4: APD_DAC52, APD_DAC51, APD_DAC50, APD_DAC49

APD_DAC_CSn7

C206 0.1µF 0603

U29
Linear Technology
LTC1665CGN#PBF
SSOP16

RP17 0603 x 4: APD_DAC64, APD_DAC63, APD_DAC62, APD_DAC61
RP18 0603 x 4: APD_DAC60, APD_DAC59, APD_DAC58, APD_DAC57

APD_DAC_CSn8

C208 0.1µF 0603

CP1 0.1µF 0612: APD_DAC1, APD_DAC2, APD_DAC3, APD_DAC4
CP2 0.1µF 0612: APD_DAC5, APD_DAC6, APD_DAC7, APD_DAC8
CP3 0.1µF 0612: APD_DAC9, APD_DAC10, APD_DAC11, APD_DAC12
CP4 0.1µF 0612: APD_DAC13, APD_DAC14, APD_DAC15, APD_DAC16
CP5 0.1µF 0612: APD_DAC17, APD_DAC18, APD_DAC19, APD_DAC20
CP6 0.1µF 0612: APD_DAC21, APD_DAC22, APD_DAC23, APD_DAC24
CP7 0.1µF 0612: APD_DAC25, APD_DAC26, APD_DAC27, APD_DAC28
CP8 0.1µF 0612: APD_DAC29, APD_DAC30, APD_DAC31, APD_DAC32
CP9 0.1µF 0612: APD_DAC33, APD_DAC34, APD_DAC35, APD_DAC36
CP10 0.1µF 0612: APD_DAC37, APD_DAC38, APD_DAC39, APD_DAC40
CP11 0.1µF 0612: APD_DAC41, APD_DAC42, APD_DAC43, APD_DAC44
CP12 0.1µF 0612: APD_DAC45, APD_DAC46, APD_DAC47, APD_DAC48
CP13 0.1µF 0612: APD_DAC49, APD_DAC50, APD_DAC51, APD_DAC52
CP14 0.1µF 0612: APD_DAC53, APD_DAC54, APD_DAC55, APD_DAC56
CP15 0.1µF 0612: APD_DAC57, APD_DAC58, APD_DAC59, APD_DAC60
CP16 0.1µF 0612: APD_DAC61, APD_DAC62, APD_DAC63, APD_DAC64

T2K FEB - 64 Channel Bias Control (LTC1665 x 8)

Revision	Drawing #: 15		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
0	Sheet #: 15 of 16	Size: B	
	Drawn by: D.Bishop	Date: 06/02/2008	
File: C:\T2K\T2K_FEB_TRIUMF\T2K FEB - 64 Channel Bias Control.SCHDOC			1:09:43 PM