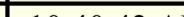
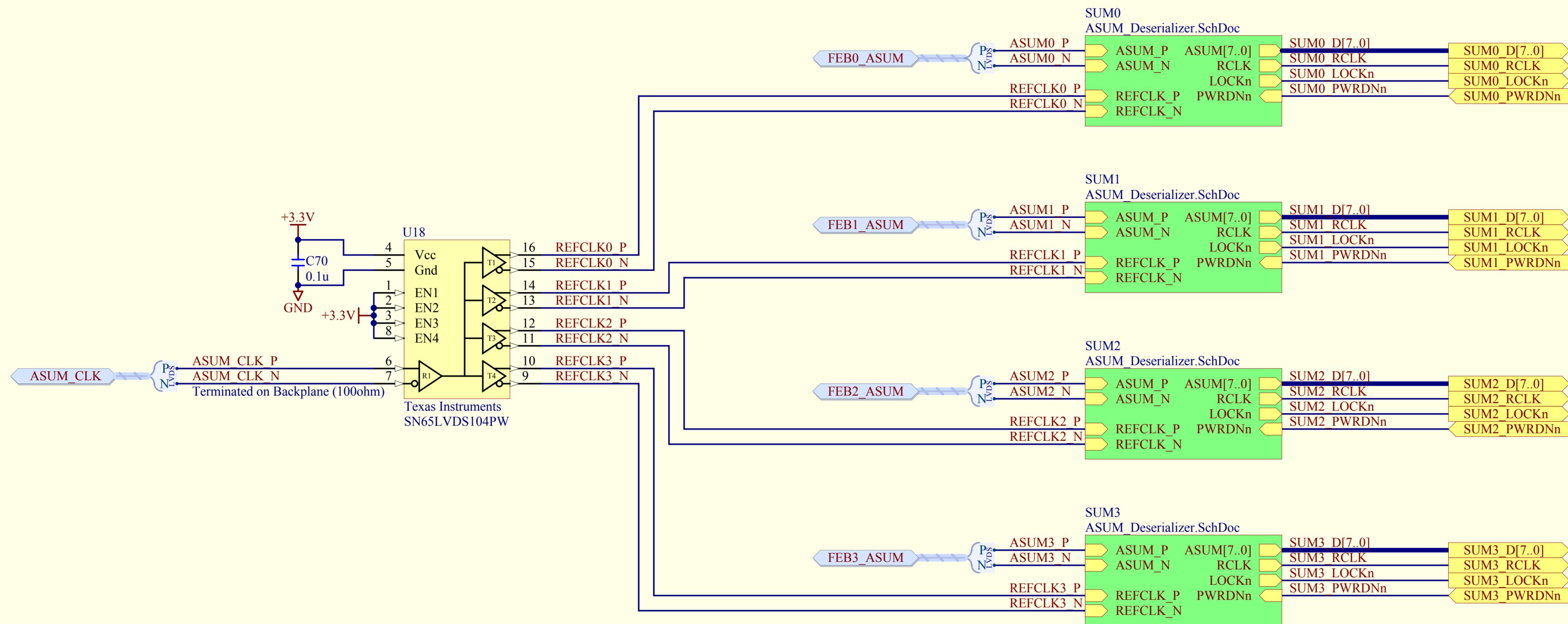


*T2K CMB - Crate Master Board*

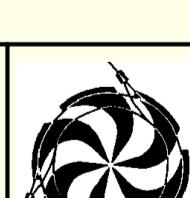
Revision	Drawing #: 1	TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3	
A	Sheet #: 1 of 14	Size: B	
	Drawn by: C. Ohlmann	Date: 06/03/2008	
File: M:\edevel\Altium\Projects\T2K_CMB\TopLevel.SchDoc			10:40:42 AM



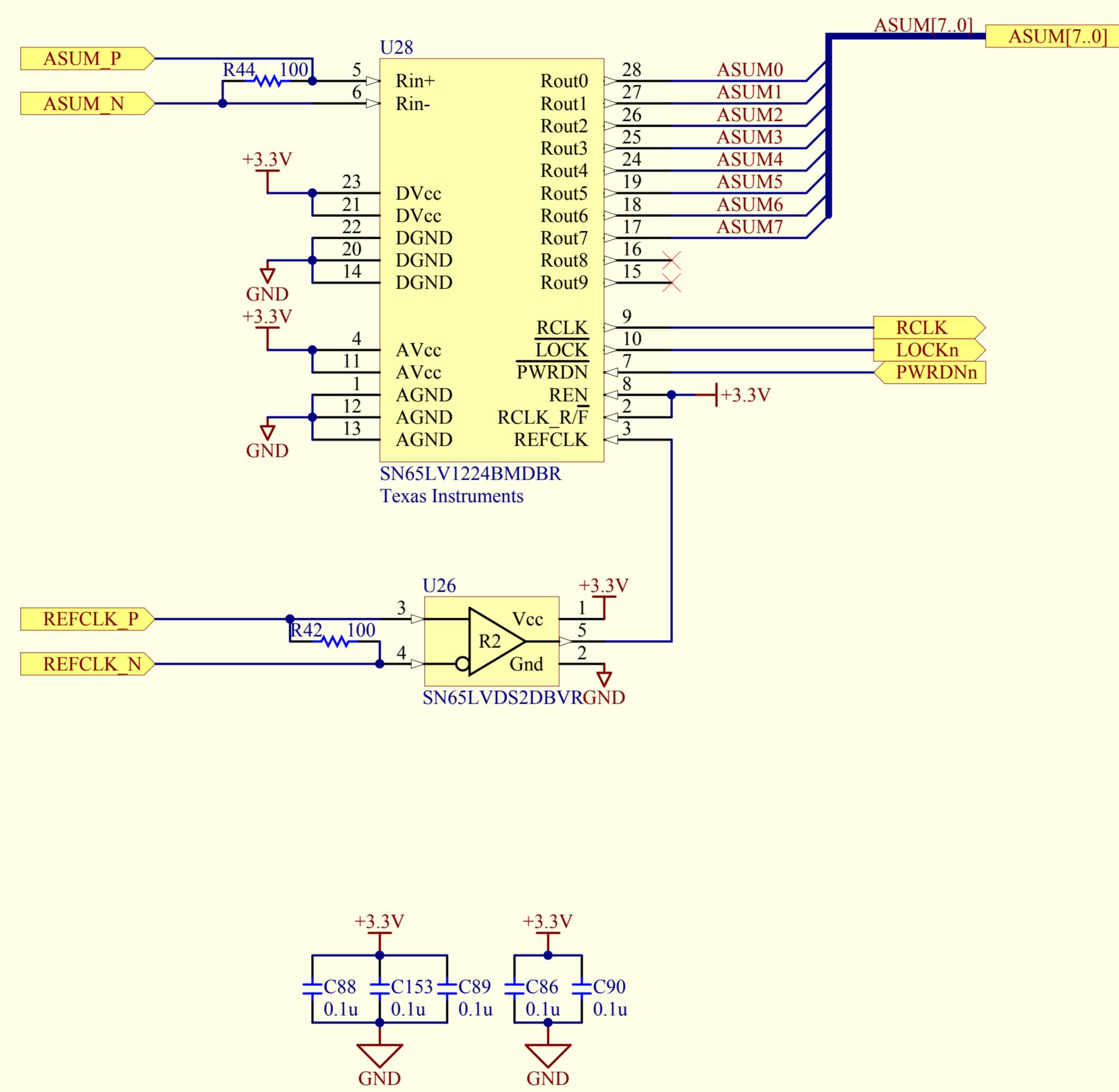
**T2K\_CMB - Crate Master Board (ASUM)**

Revision	Drawing #: 2	TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
A	Sheet #: 2 of 14   Size: B	
	Drawn by: C. Ohlmann   Date: 06/03/2008	

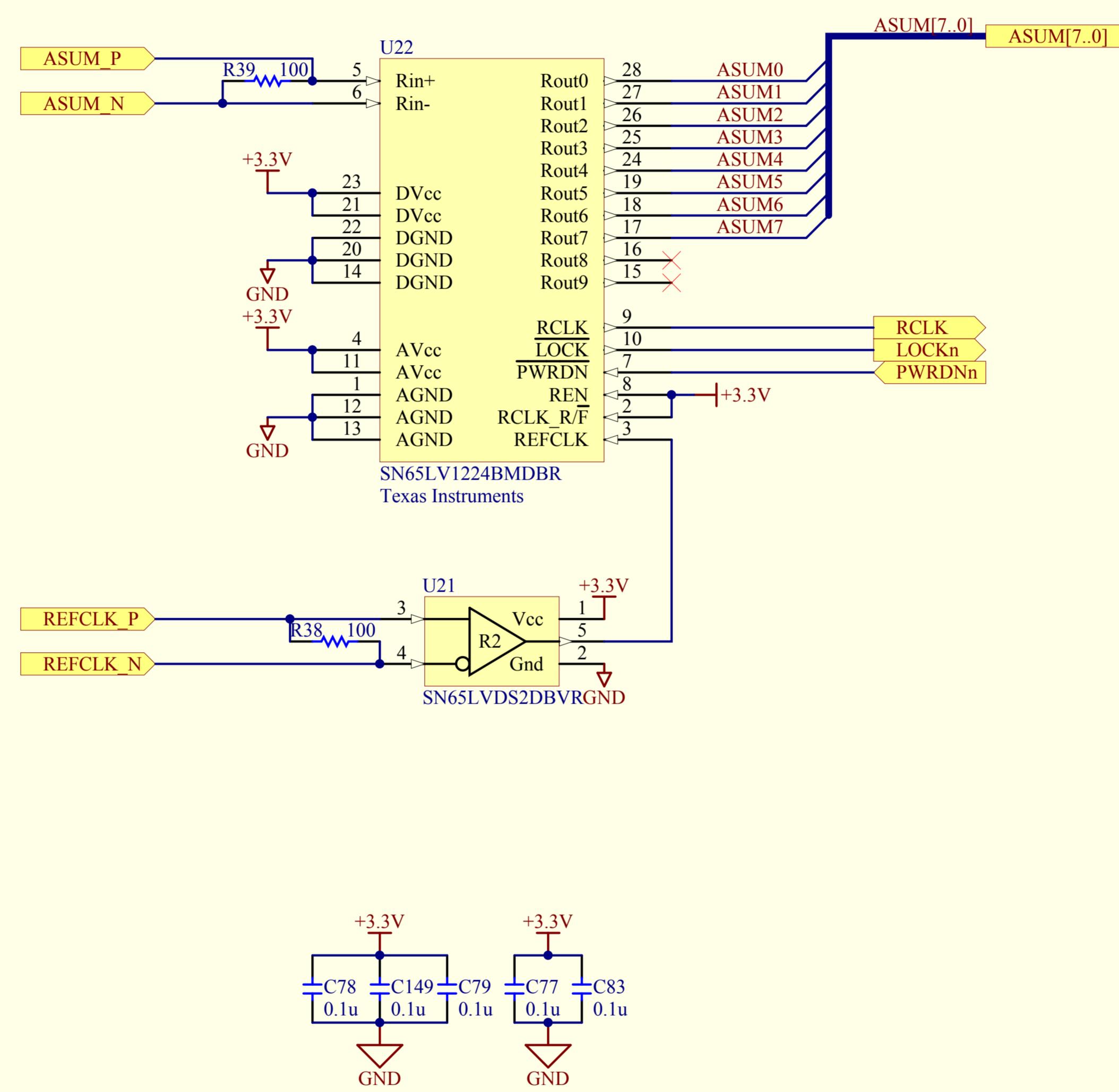
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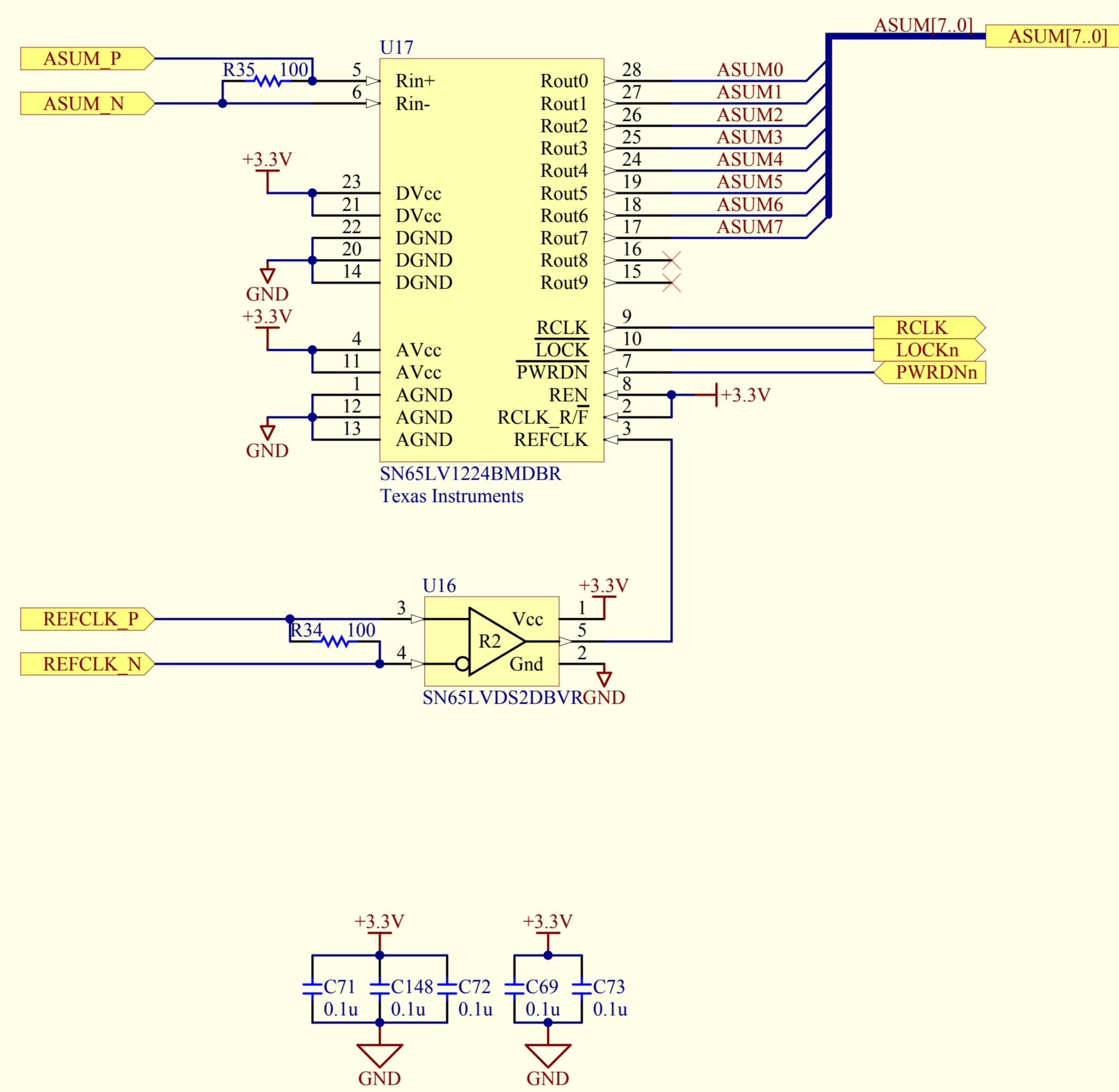
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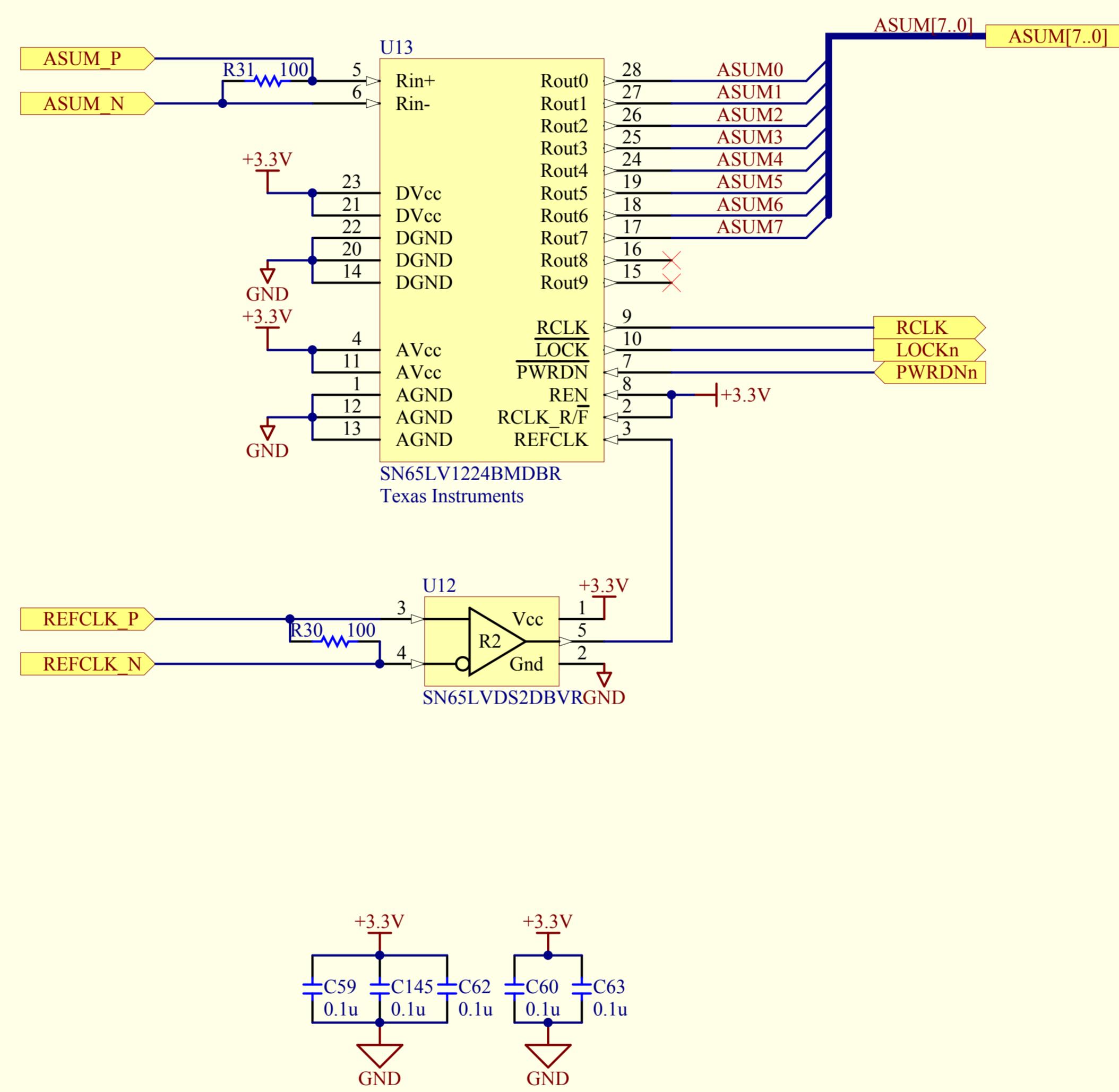
T2K_CMB - Crate Master Board (ASUM Deserializer)			
Revision	Drawing #: 3		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
A	Sheet #: 3	of 14	Size: B
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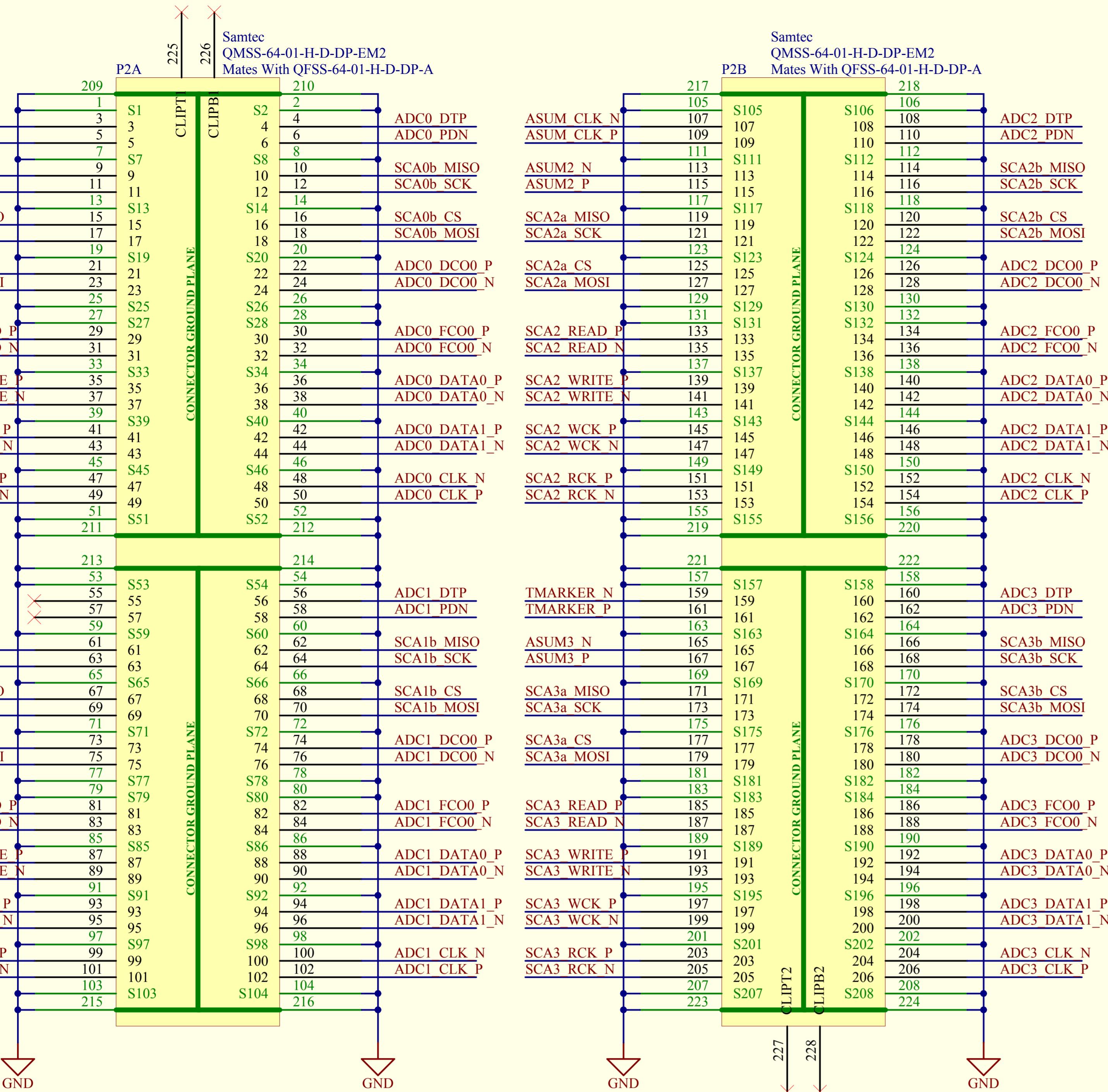
T2K_CMB - Crate Master Board (ASUM Deserializer)			
Revision	Drawing #: 3		TRIUMF
<b>A</b>	Sheet #: 3	of 14	4004 Wesbrook Mall
			Vancouver, B.C.
			Canada
			V6T 2A3
	Drawn by: C. Ohlmann	Date: 06/03/2008	
			10:40:43 AM
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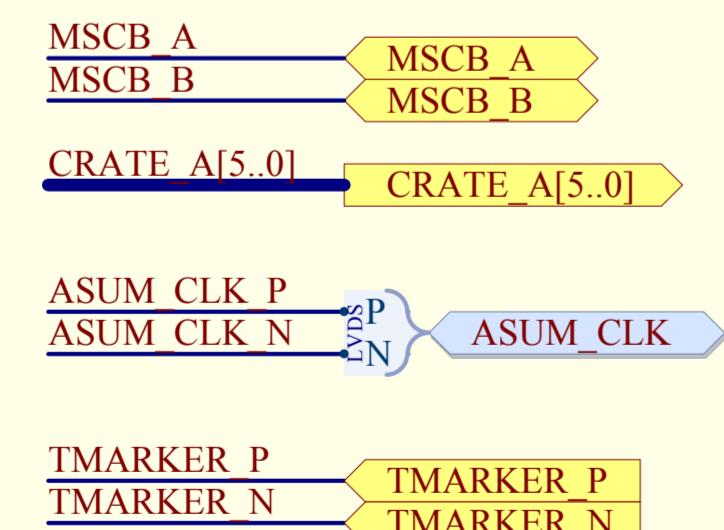
T2K_CMB - Crate Master Board (ASUM Deserializer)			
Revision	Drawing #: 3		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
A	Sheet #: 3	of 14	Size: B
	Drawn by: C. Ohlmann	Date: 06/03/2008	
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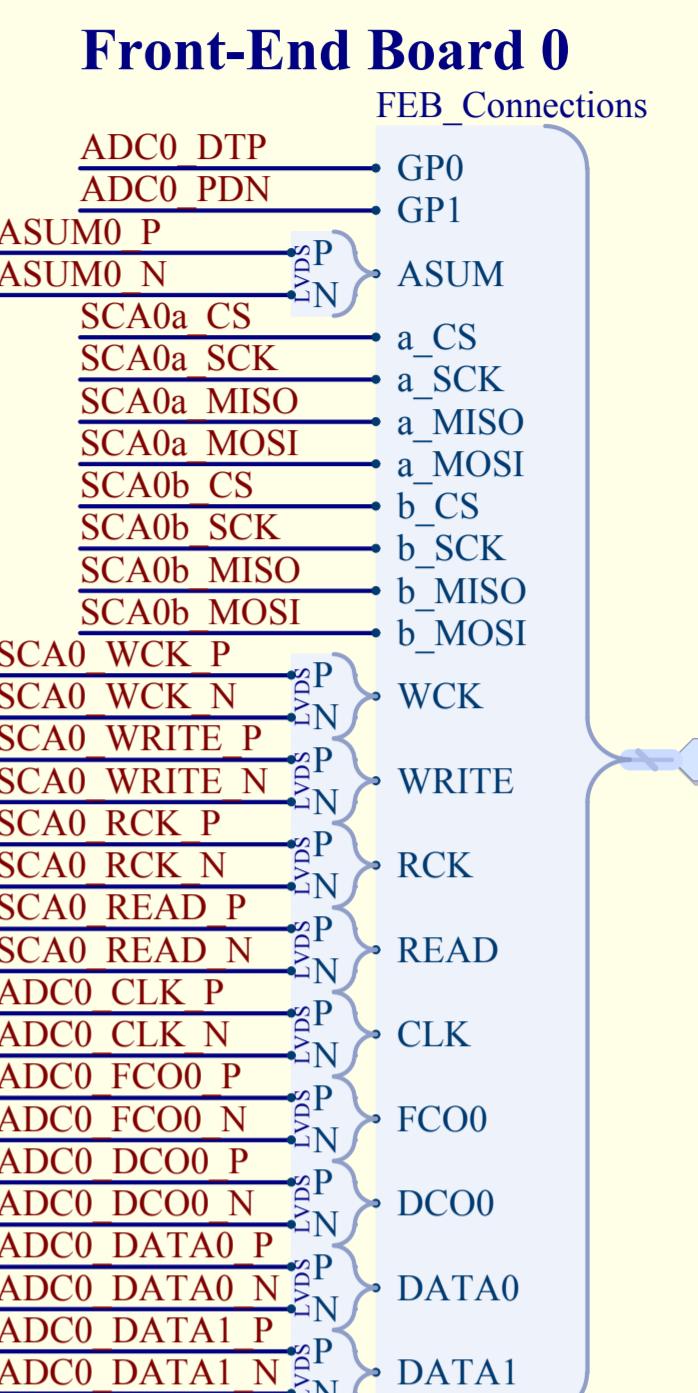
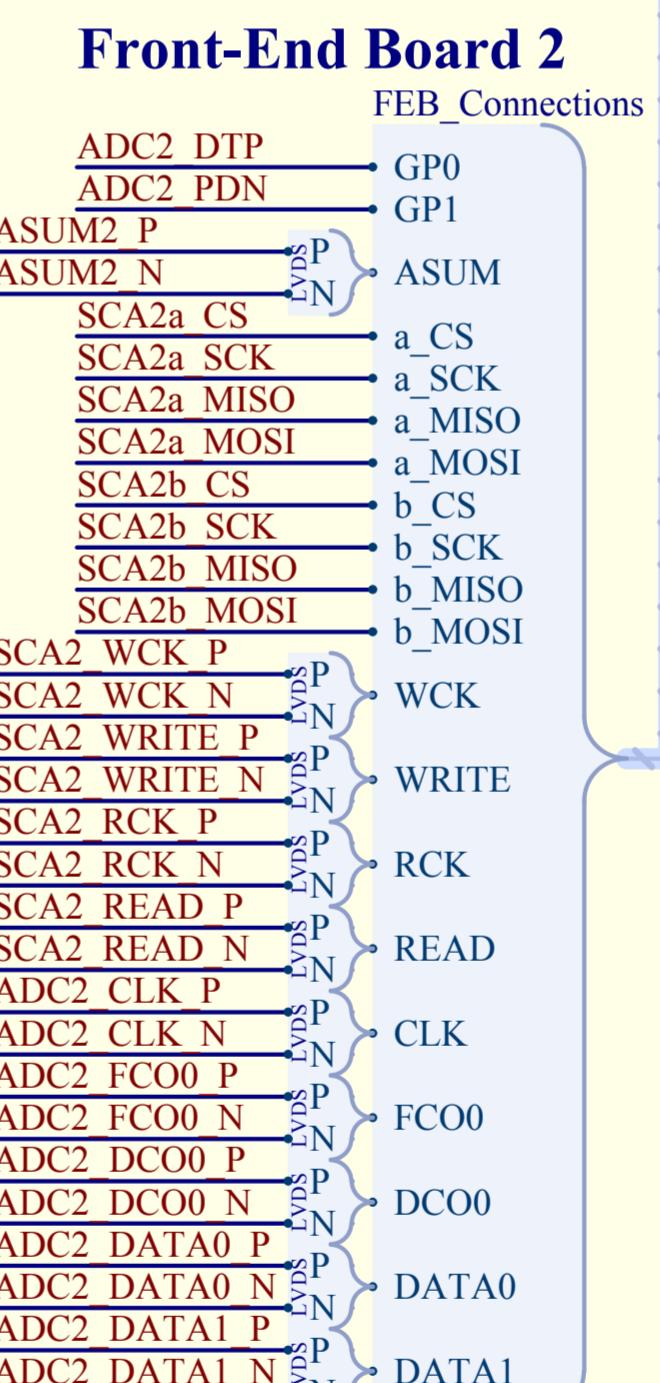
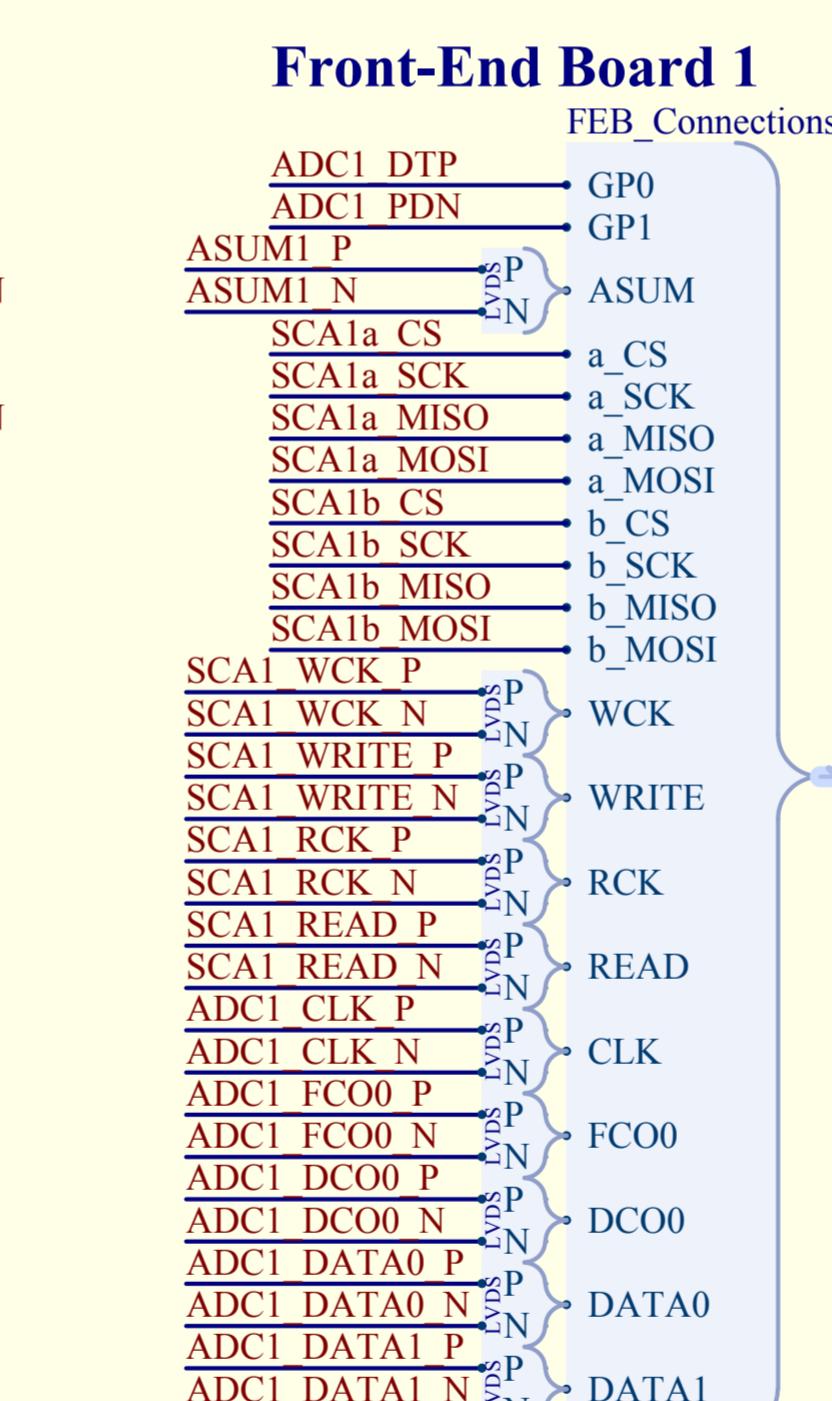
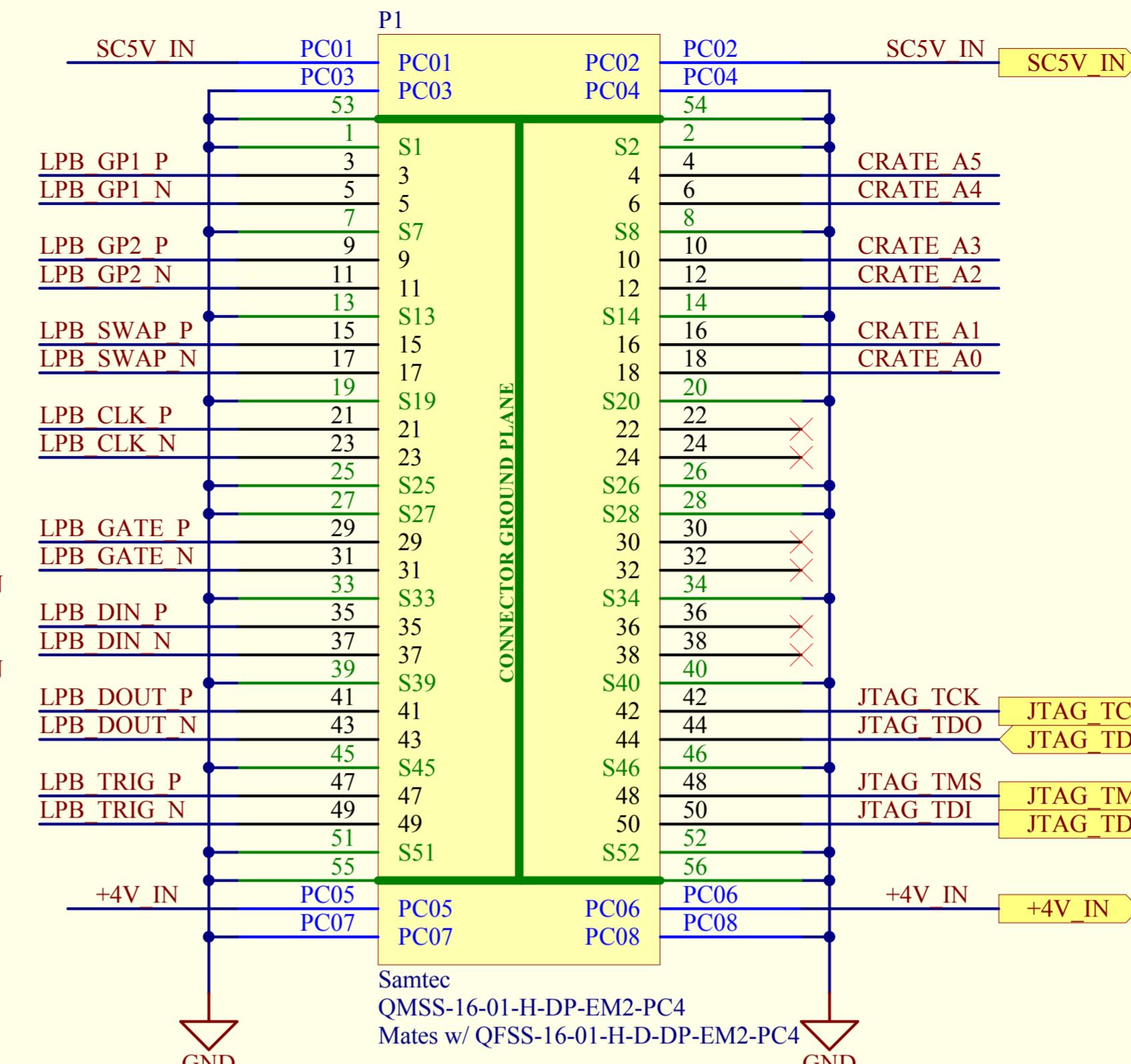
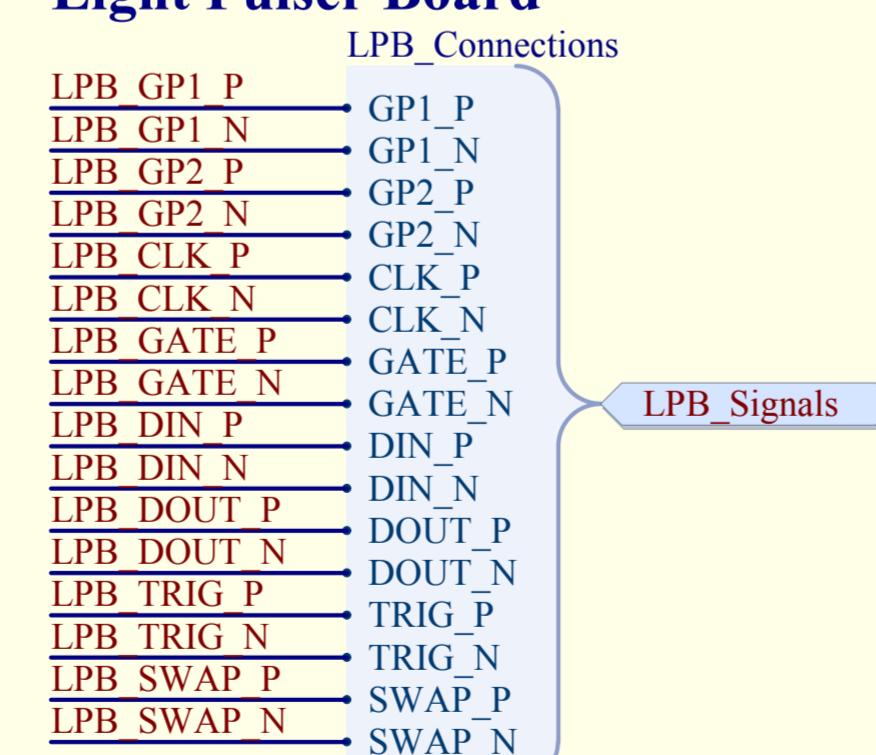
T2K_CMB - Crate Master Board (ASUM Deserializer)			
Revision	Drawing #: 3		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
A	Sheet #: 3	of 14	Size: B
	Drawn by: C. Ohlmann	Date: 06/03/2008	
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### MSCB and Global Signals



### Light Pulser Board

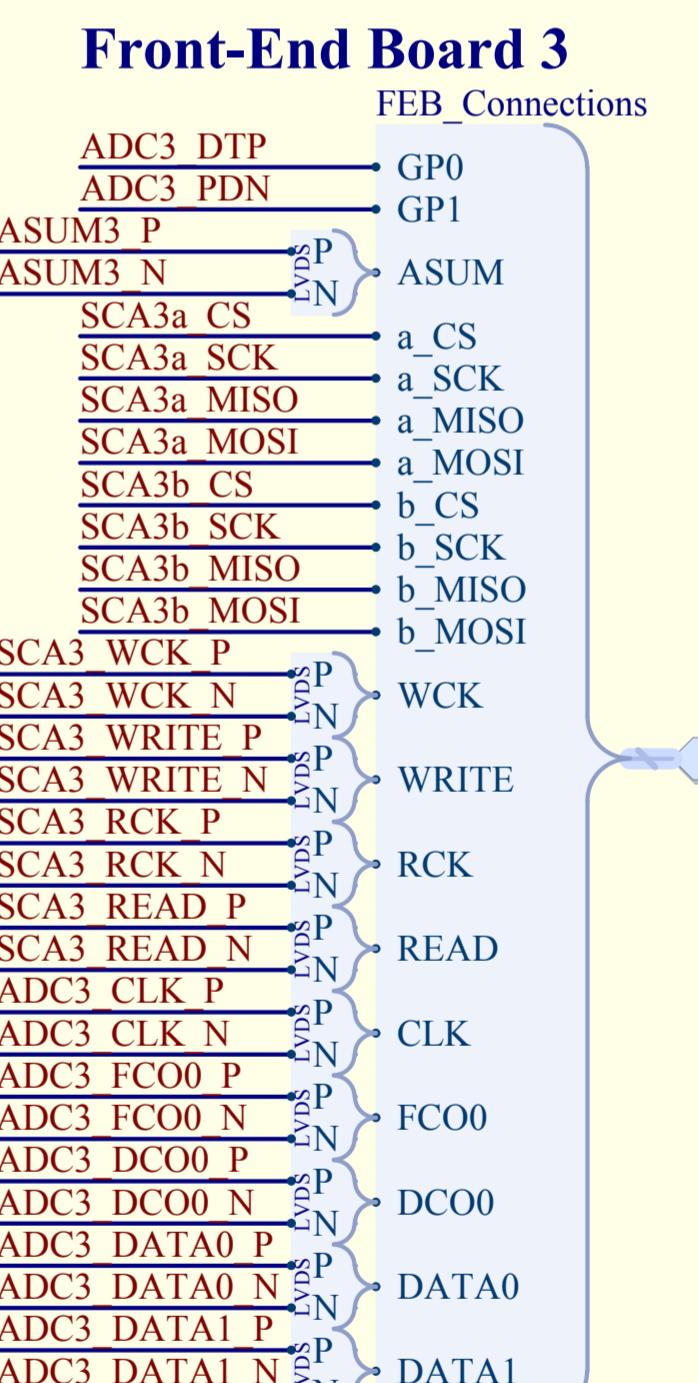


FEB0\_Signals

FEB1\_Signals

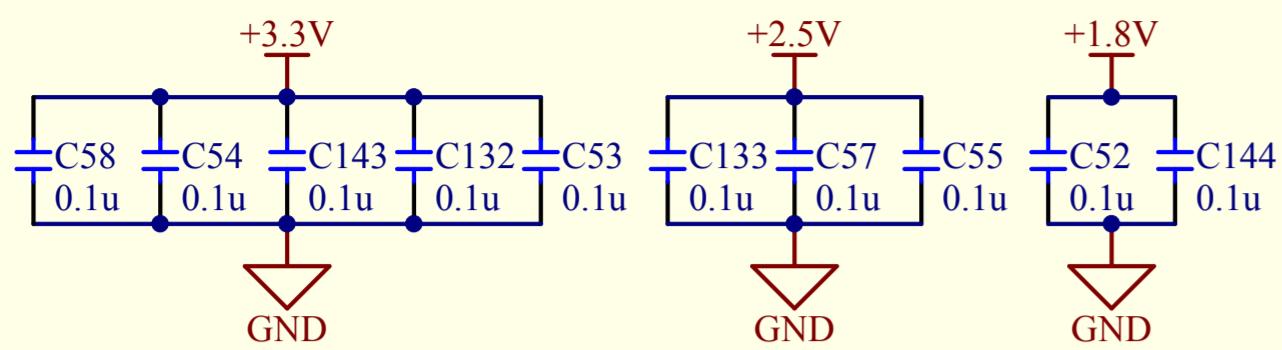
FEB2\_Signals

FEB3\_Signals

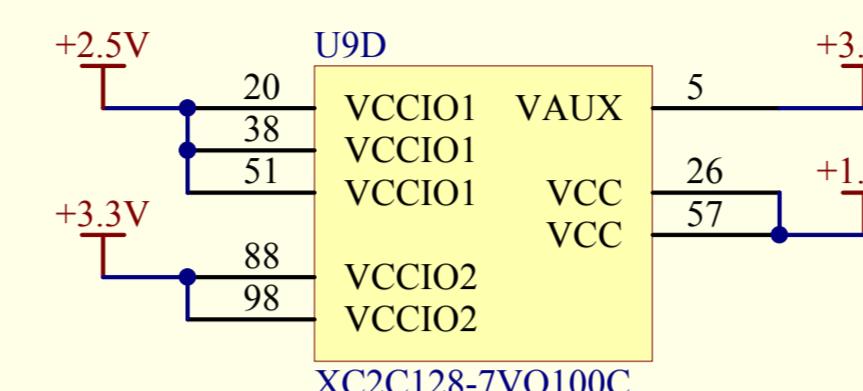


### T2K\_CMB - Crate Master Board (Backplane Connections)

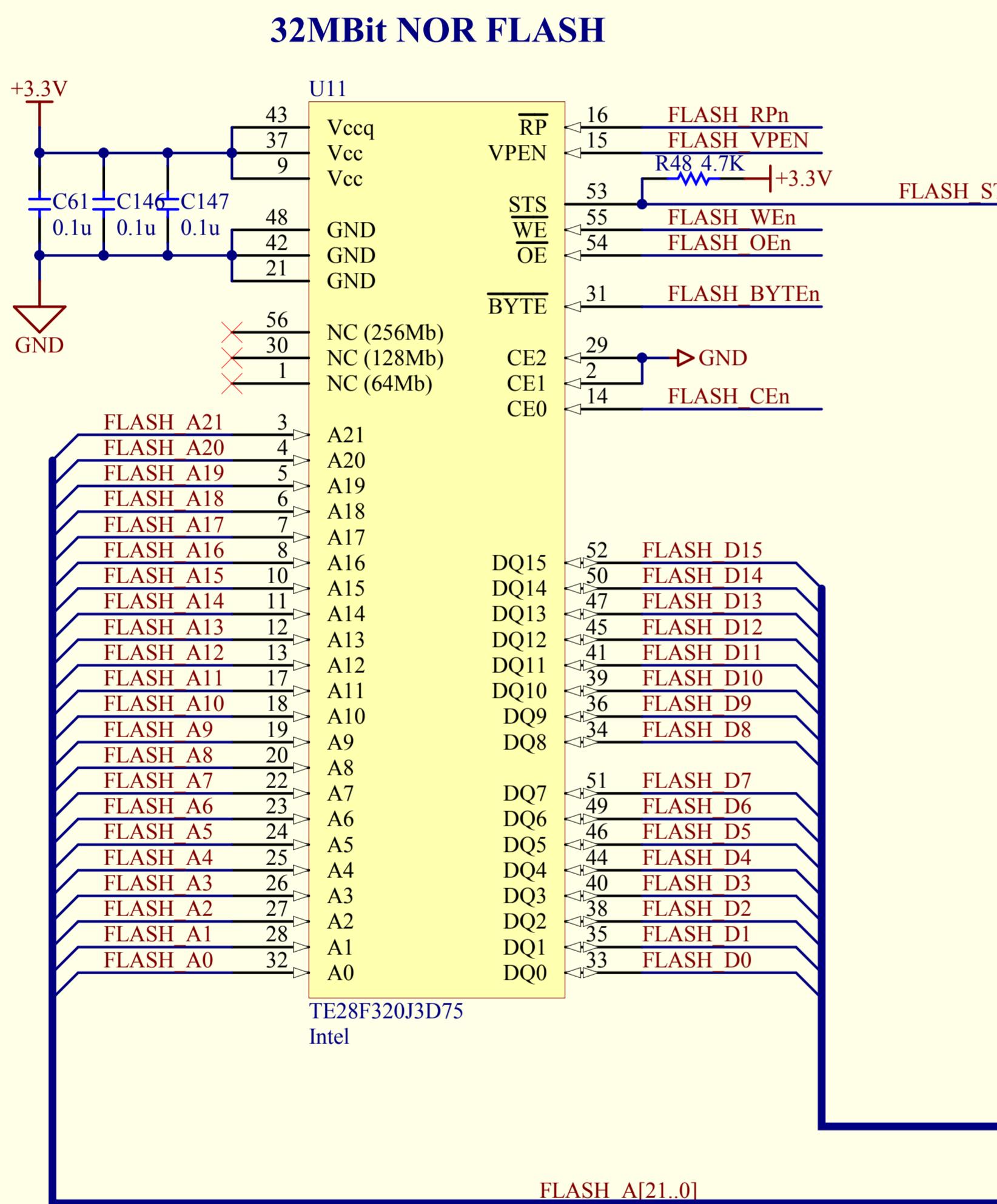
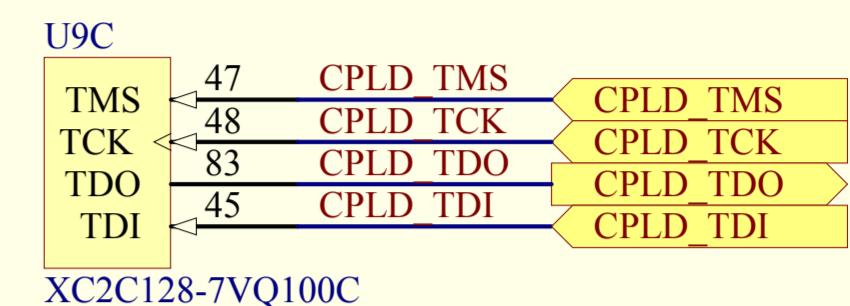
Revision	Drawing #:	4	TRIUMF
A	Sheet #:	4 of 14	4004 Wesbrook Mall
	Size:	B	Vancouver, B.C.
	Drawn by:	C. Ohlmann	Canada
	Date:	06/03/2008	V6T 2A3
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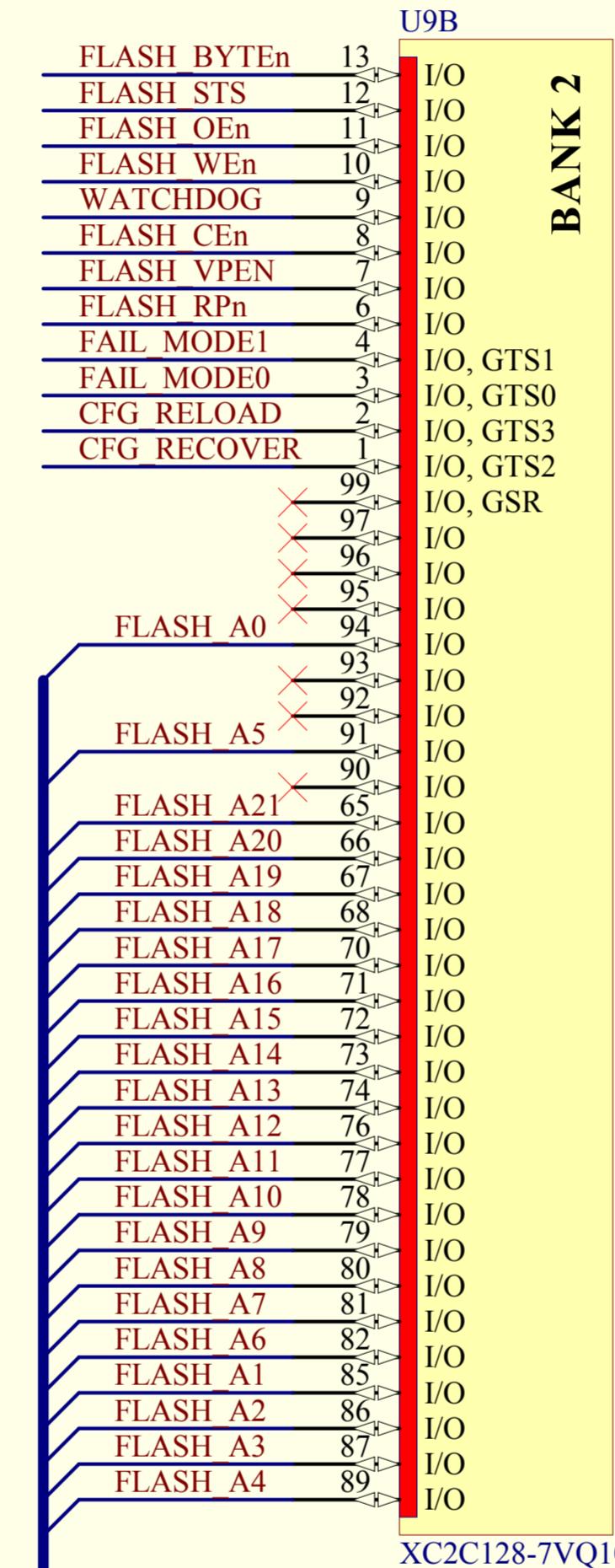
### CPLD POWER/GND



### CPLD JTAG Interface

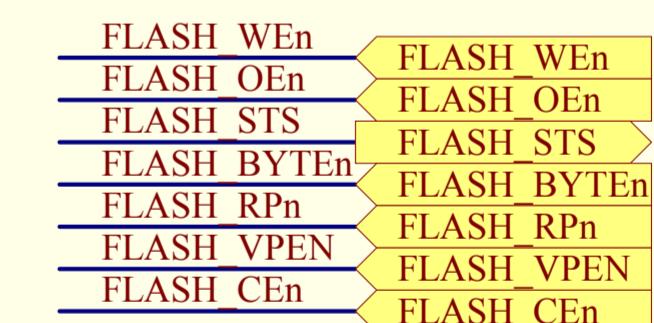
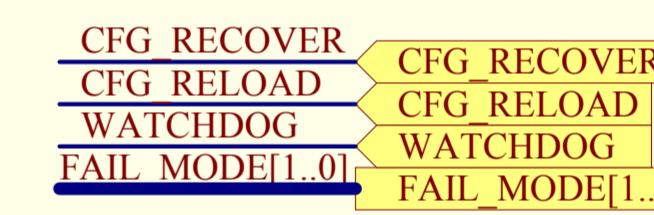
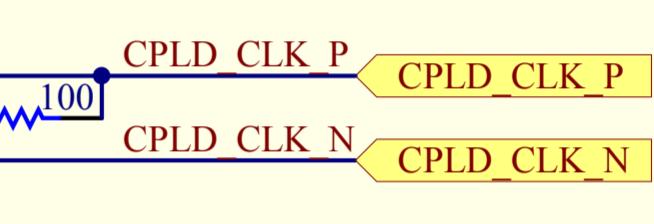
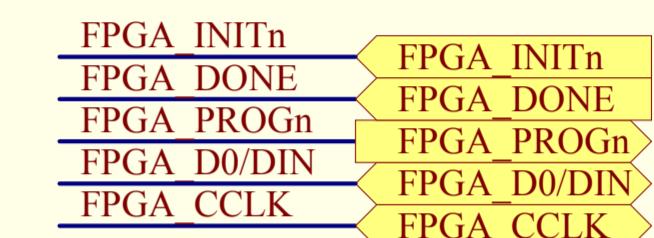
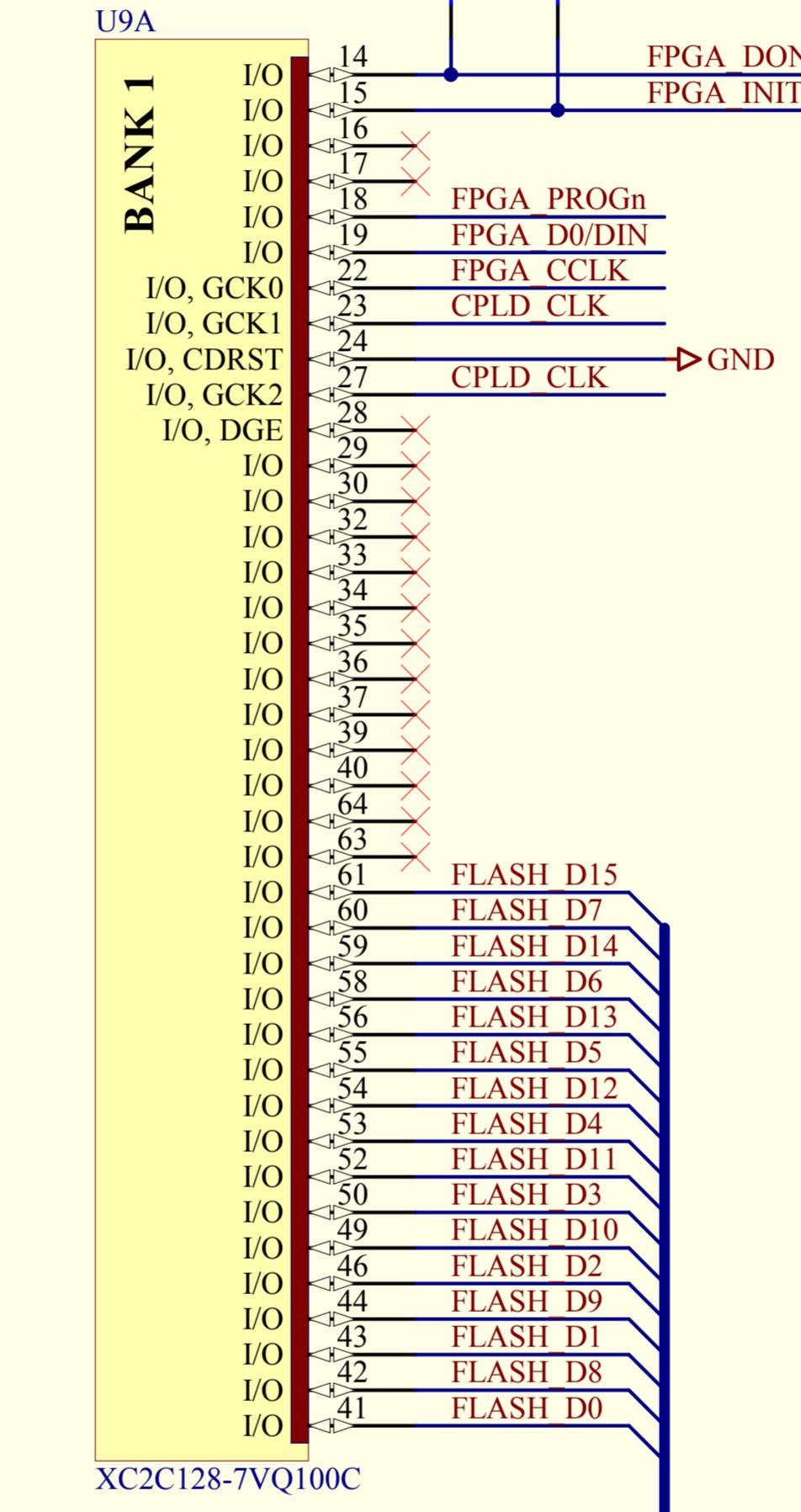


### 32MBit NOR FLASH



### 3.3V IO

### 2.5V IO



### T2K\_CMB - Crate Master Board (Configuration)

Revision	Drawing #: 5	TRIUMF
A	Sheet #: 5 of 14   Size: B	4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Drawn by: C. Ohlmann	Date: 06/03/2008
	File: M:\edev\Altium\Projects\T2K_CMB\CPLDandFlashMemory.SchDoc	10:40:43 AM

### Bank Voltage = +3.3V

U8A	
BANK 0	B24 FLASH STS
IO_L01N_0/VRP_0	A24 FLASH BYTEn
IO_L01P_0/VRN_0	D21 FLASH D8
IO_L02N_0	C21 FLASH OEn
IO_L02P_0	E20 FLASH D0
IO_L03N_0	D20 FLASH D1
IO_L03P_0/VREF_0	F19 FLASH D10
IO_L05_0/No_Pair	E19 FLASH D9
IO_L06N_0	E18 FLASH D4
IO_L06P_0	D19 FLASH D11
IO_L07N_0	C19 FLASH D2
IO_L07P_0	B19 FLASH WEn
IO_L08N_0	A19 WATCHDOG
IO_L08P_0	D18 FLASH D3
IO_L09N_0	G18 FLASH A12
IO_L09P_0/VREF_0	F18 FLASH D12
IO_L37N_0	D17 FLASH CEn
IO_L37P_0	G17 FLASH A10
IO_L38N_0	H16 FLASH A10
IO_L38P_0	F17 FLASH D13
IO_L39N_0	F16 FLASH D14
IO_L39P_0	E17 FLASH A11
IO_L43N_0	D17 FLASH D5
IO_L43P_0	G16 FLASH D6
IO_L44N_0	E16 FLASH VPEN
IO_L45N_0	D15 FLASH A21
IO_L67N_0	IO_L67P_0
IO_L68N_0	D15 FLASH D7
IO_L68P_0	C15 FLASH RPn
IO_L69N_0	H15 FLASH A9
IO_L69P_0/VREF_0	H14 FLASH A8
IO_L73N_0	G14
IO_L73P_0	E14
IO_L74N_0/GCLK7P	D14
IO_L74P_0/GCLK6S	C14
IO_L75N_0/GCLK5P	B14
IO_L75P_0/GCLK4S	

### Bank Voltage = +3.3V

U8B	
BANK 1	I0_L75N_1/GCLK3P B13
IO_L75P_1/GCLK2S	C13
IO_L02N_0	D13
IO_L74N_1/GCLK1P	E13
IO_L74P_1/GCLK0S	F13
IO_L73N_1	G13
IO_L73P_1	H13 FLASH A7
IO_L69N_1/VREF_1	I12 FLASH A6
IO_L69P_1	C12 FAIL MODE1
IO_L68N_1	D12 FLASH A18
IO_L68P_1	E12 FLASH A19
IO_L67N_1	F12 FLASH A20
IO_L45N_1/VREF_1	D11 FAIL MODE0
IO_L45P_1	E11 FLASH A17
IO_L44N_1	G12
IO_L44P_1	G11
IO_L43N_1	D10 FLASH A15
IO_L43P_1	E10 FLASH A16
IO_L39N_1	F11 FLASH A2
IO_L39P_1	F10 FLASH A3
IO_L38N_1	H11 FLASH A1
IO_L38P_1	G10 CFG RELOAD
IO_L37N_1	C9
IO_L37P_1	D9 FLASH A4
IO_L09N_1/VREF_1	F9
IO_L09P_1	G9
IO_L08N_1	A8 LOS
IO_L08P_1	B8 RateSelect
IO_L07N_1	C8 FLASH A0
IO_L07P_1	D8 FLASH A13
IO_L06N_1	E9 FLASH A14
IO_L06P_1	F8 FLASH A5
IO_L05_1/No_Pair	D7 ModDef0
IO_L03N_1/VREF_1	E7
IO_L03P_1	C6 TX_Disable
IO_L02N_1	D6 TX_Fault
IO_L02P_1	A3 ModDef1
IO_L01N_1/VRP_1	B3 ModDef2
IO_L01P_1/VRN_1	

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### Bank Voltage = +2.5V

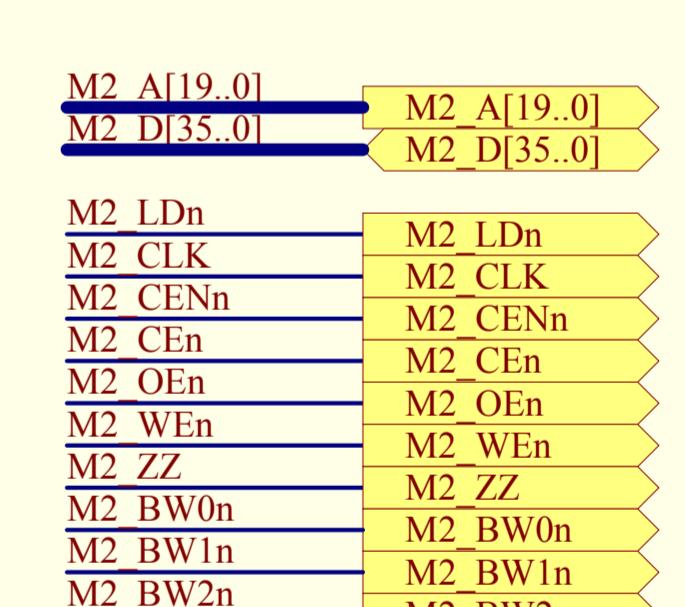
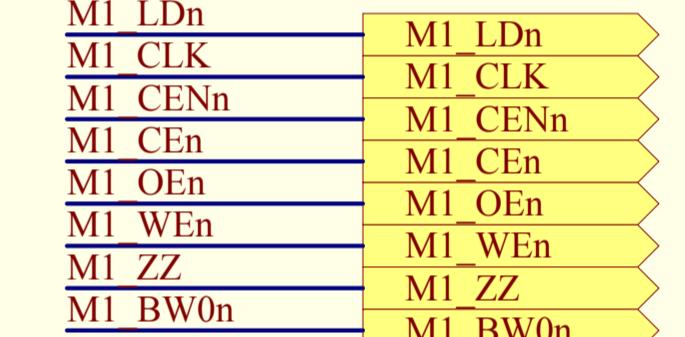
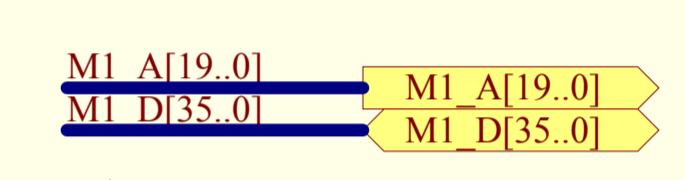
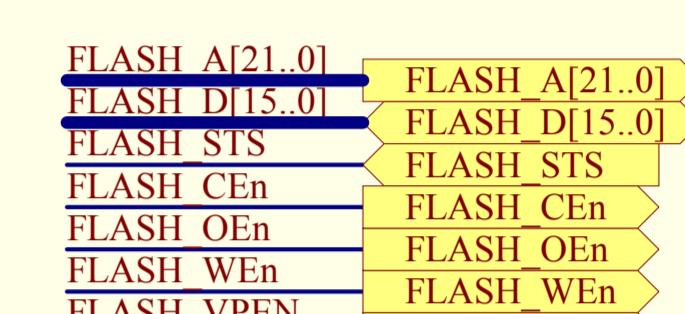
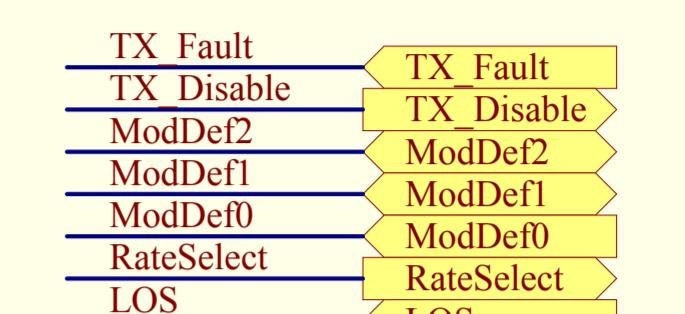
U8C	
BANK 2	I0_L01N_2/VRP_2 C4 M1 CLK
IO_L01P_2/VRN_2	D3 M1 CEEn
IO_L02N_2	A2 M1 D17
IO_L02P_2	B1 M1 D16
IO_L03N_2	C2 M1 D15
IO_L03P_2	E1 M1 D14
IO_L04N_2/VREF_2	D2 M1 D13
IO_L04P_2	D1 M1 D12
IO_L05N_2	E4 M1 A16
IO_L05P_2	E3 M1 A17
IO_L06N_2	E2 M1 D11
IO_L06P_2	E1 M1 D10
IO_L43N_2	G6 M1 D18
IO_L43P_2	G5 M1 D19
IO_L44N_2	G4 M1 D20
IO_L44P_2	G3 M1 D9
IO_L45N_2	F1 M1 ZZ
IO_L45P_2	G1 M1 D8
IO_L46N_2/VREF_2	H6 M1 A3
IO_L46P_2	H5 M1 A2
IO_L47N_2	H4 M1 A15
IO_L47P_2	H3 M1 D22
IO_L48N_2	H2 M1 D7
IO_L48P_2	H1 M1 D6
IO_L49N_2	J7 M1 A13
IO_L49P_2	J6 M1 A14
IO_L50N_2	J5 M1 D21
IO_L50P_2	J4 M1 D23
IO_L51N_2	J3 M1 A4
IO_L51P_2	J2 M1 D5
IO_L52N_2	K6 M1 A18
IO_L52P_2	K5 M1 LDn
IO_L53N_2	K4 M1 A5
IO_L53P_2	K3 M1 A1
IO_L54N_2	J1 M1 D4
IO_L54P_2	K1 M1 D3
IO_L55N_2	K7 M1 D24
IO_L55P_2	L8 M1 D25
IO_L56N_2	L7 M1 CEEn
IO_L56P_2	M7 M1 WEn
IO_L57N_2	L6 M1 A19
IO_L57P_2	L5 M1 A0
IO_L58N_2	L4 M1 OEn
IO_L58P_2	L3 M1 D26
IO_L59N_2	L2 M1 D2
IO_L59P_2	L1 M1 D1
IO_L60N_2	M8 M1 D29
IO_L60P_2	N8 M1 D30
IO_L85N_2	M6 M1 D28
IO_L85P_2	M5 M1 D27
IO_L86N_2	M4 M1 A7
IO_L86P_2	M3 M1 A6
IO_L87N_2	M2 M1 D0
IO_L87P_2	M1 M1 A12
IO_L88N_2/VREF_2	N7 M1 BW1n
IO_L88P_2	N6 M1 BW0n
IO_L89N_2	N5 M1 A10
IO_L89P_2	N4 M1 A9
IO_L90N_2	N3 M1 A8
IO_L90P_2	N2 M1 A11

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### Bank Voltage = +2.5V

U8D	
BANK 3	I0_L90N_3 P2 M2 A18
IO_L90P_3	P3 M2 CEEn
IO_L89N_3	P4 M2 WEn
IO_L89P_3	P5 M2 CLK
IO_L88N_3	P6 M1 BW3n
IO_L88P_3	P7 M1 BW2n
IO_L87N_3/VREF_3	R1 M2 A15
IO_L87P_3	R2 M2 A14
IO_L86N_3	R3 M2 OEn
IO_L86P_3	R4 M2 LDn
IO_L85N_3	R5 M1 D34
IO_L85P_3	R6 M1 D33
P8	M1 D31
R8	M1 D32
T1	M2 A13
T2	M2 D17
T3	M1 D35
T4	M2 A4
T5	M2 BW1n
T6	M2 BW0n
R7	M2 A2
T7	M2 A3
T8	M2 D18
U7	M2 D19
U1	M2 D16
V1	M2 D15
U3	M2 BW2n
U4	M2 BW3n
U5	M2 A5
U6	M2 A1
V2	M2 D14
V3	M2 CEEn
IO_L51P_3	V4 M2 D20
IO_L50N_3	V5 M2 D22
IO_L50P_3	V6 M2 A19
IO_L49N_3	V7 M2 A6
IO_L49P_3	W1 M2 D13
IO_L48N_3	W2 M2 D12
IO_L48P_3	W3 M2 D21
IO_L47N_3	W4 M2 A0
IO_L47P_3	W5 M2 A17
W6	M2 A16
IO_L46P_3	Y1 M2 D11
IO_L45P_3	Y2 M2 D9
IO_L44N_3	Y3 M2 D23
IO_L44P_3	Y4 M2 D24
Y5	M2 D25
AB3	M2 ZZ
AB4	M2 D26
AC1	M2 D8
AC2	M2 D7
AD1	M2 D6
AD2	M2 D5
AE1	M2 D4
AF2	M2 D3
AC3	M2 D28
AD4	M2 D0
AE3	M2 D2
AF3	M2 D1
IO_L03N_3/VREF_3	IO_L03P_3
IO_L02N_3	IO_L02P_3
IO_L01N_3/VRP_3	IO_L01P_3/VRN_3

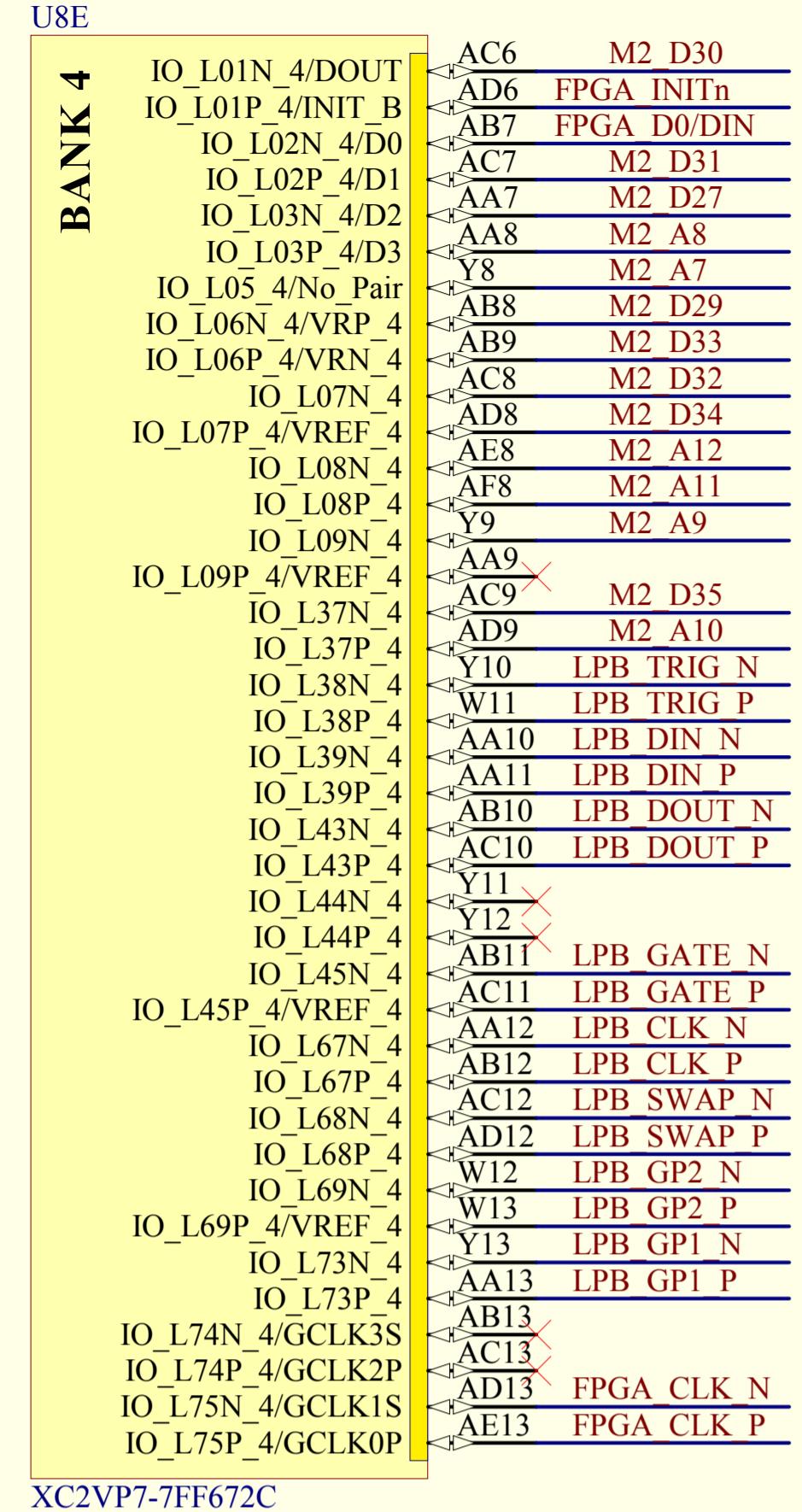
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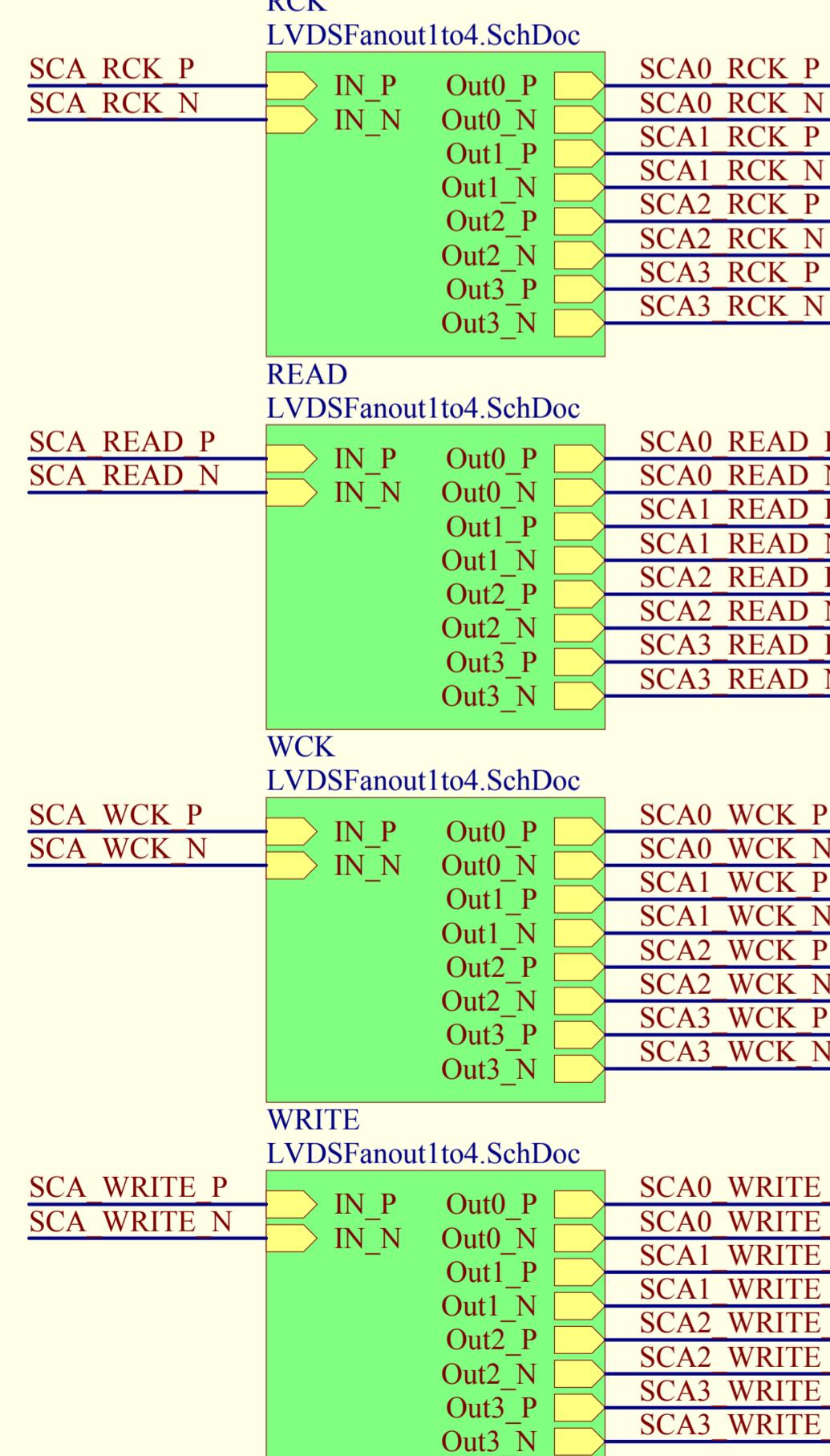
T2K\_CMB - Crate Master Board (FPGA - IO Bank 0-3)

Revision	Drawing #:		6	TRIUMF
A	Sheet #:	6	of 14	4004 Wesbrook Mall
	Size:	B		Vancouver, B.C.
	Drawn by:	C. Ohlmann	Date:	Canada 06/03/2008
	File:</			

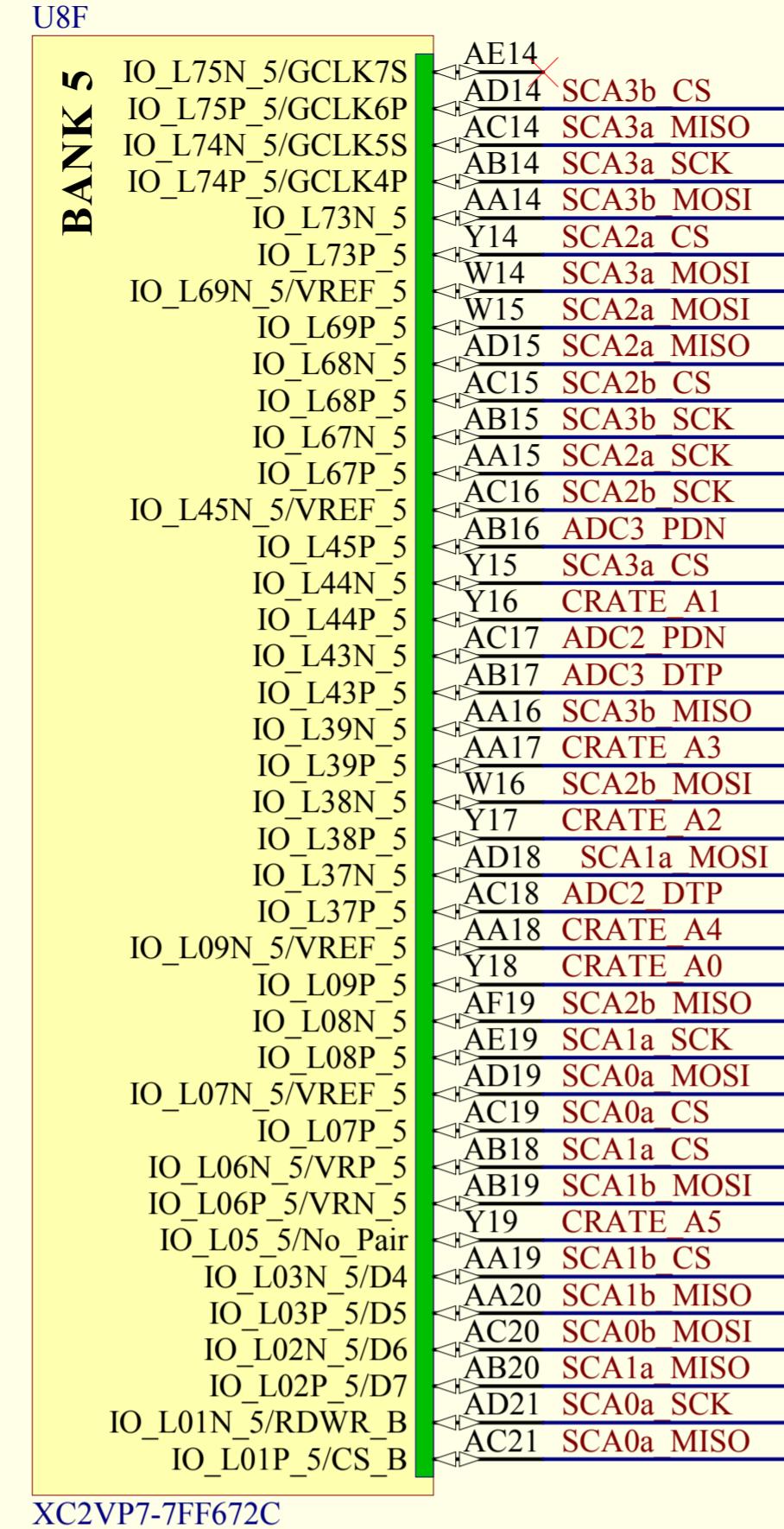
## Bank Voltage = +2.5V



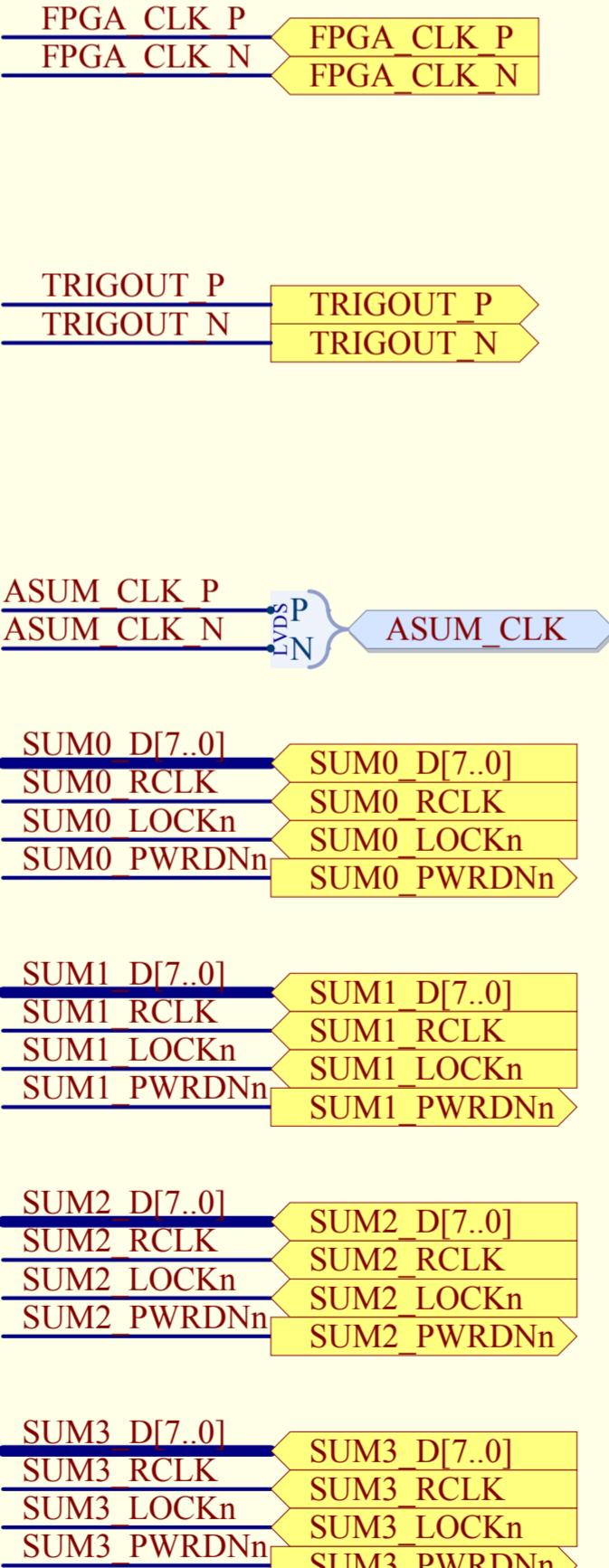
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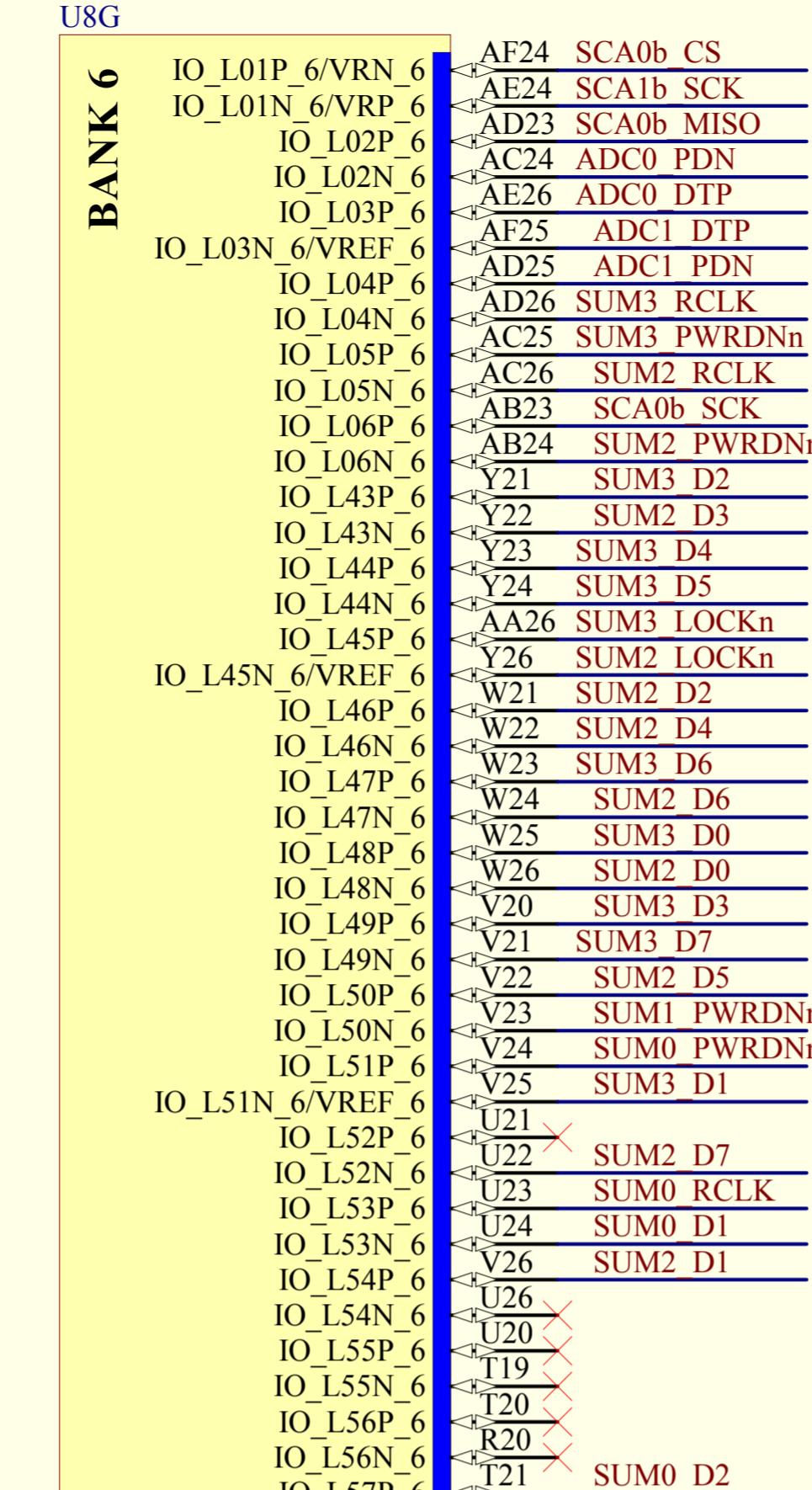
## Bank Voltage = +3.3V

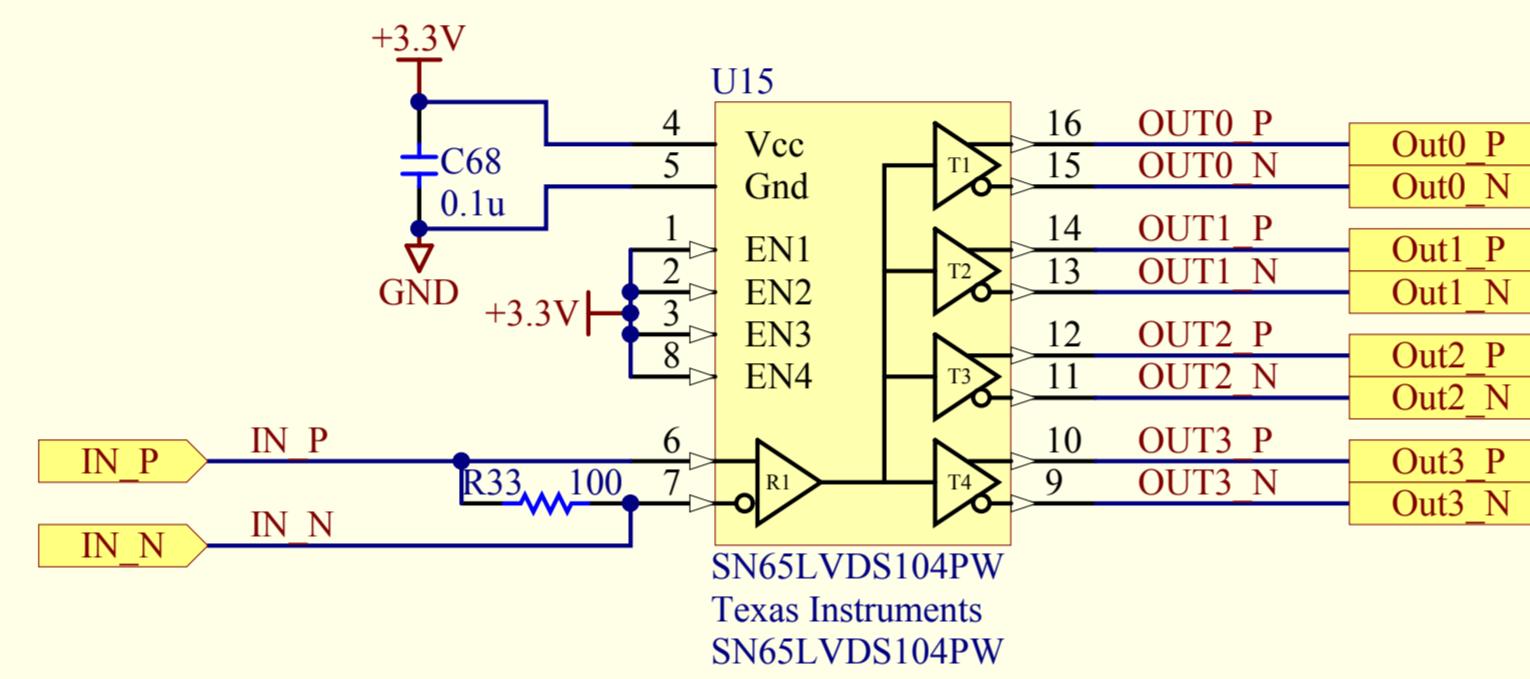


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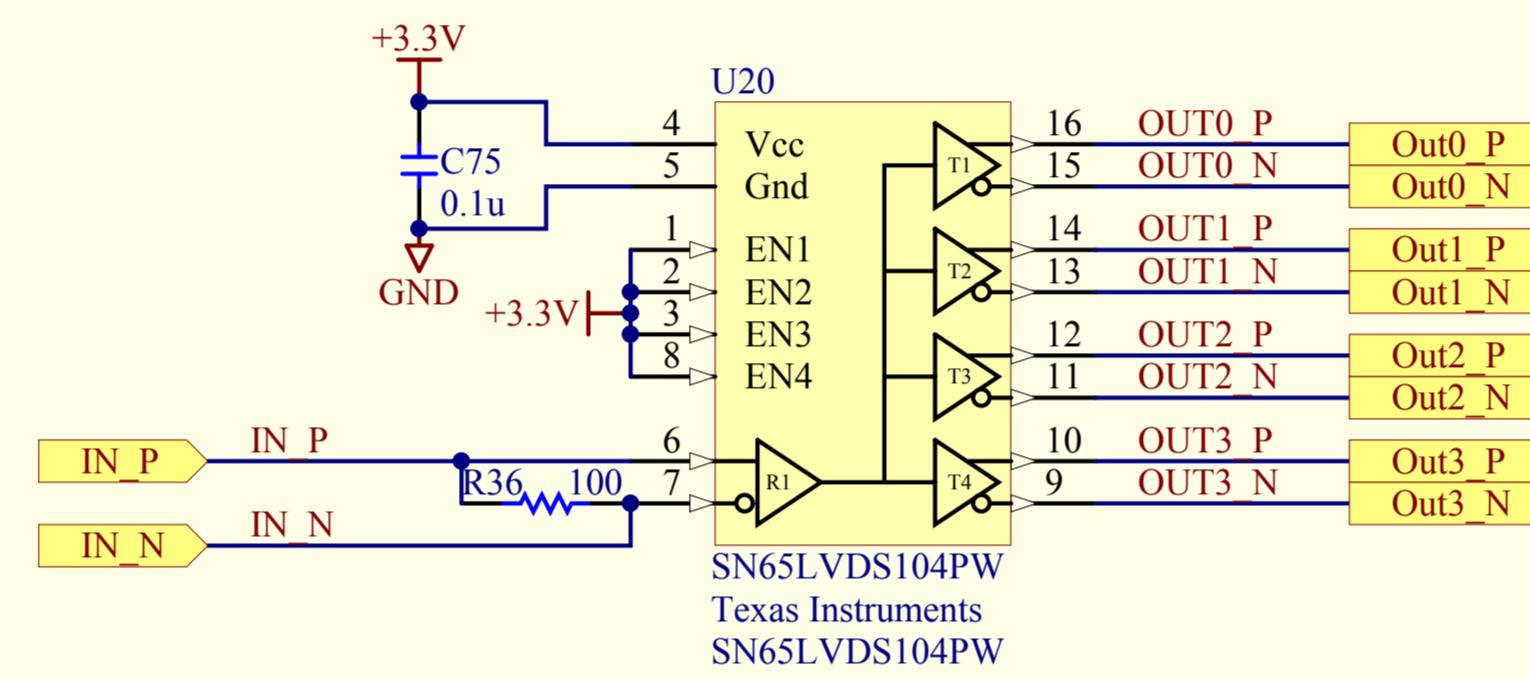
## Bank Voltage = +3.3V





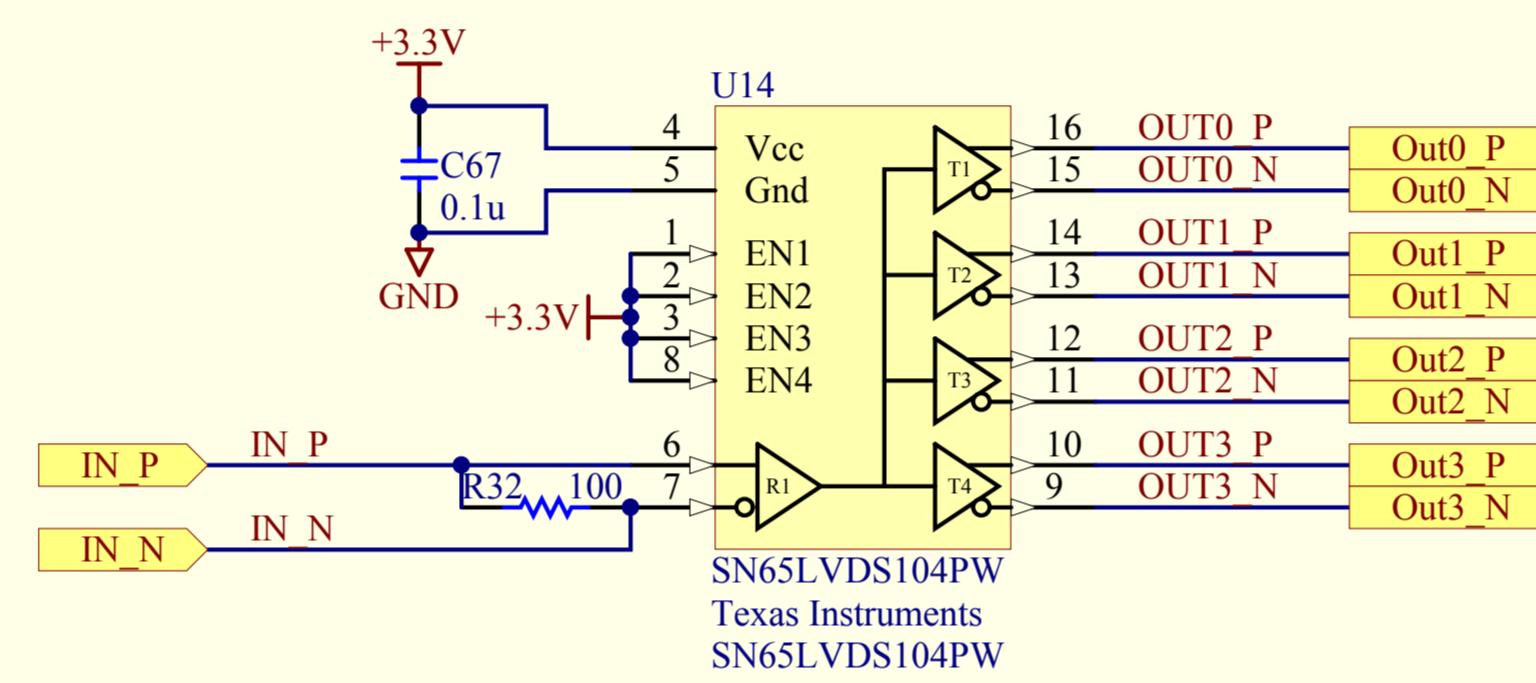
**T2K\_CMB - Crate Master Board (1:4 LVDS Fanout)**

Revision <b>A</b>	Drawing #: 8	TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 8 of 14	Size: B
	Drawn by: C. Ohlmann	Date: 06/03/2008
File: M:\edev\Altium\Projects\T2K_CMB\LVDSFanout1to4.SchDoc		10:40:44 AM



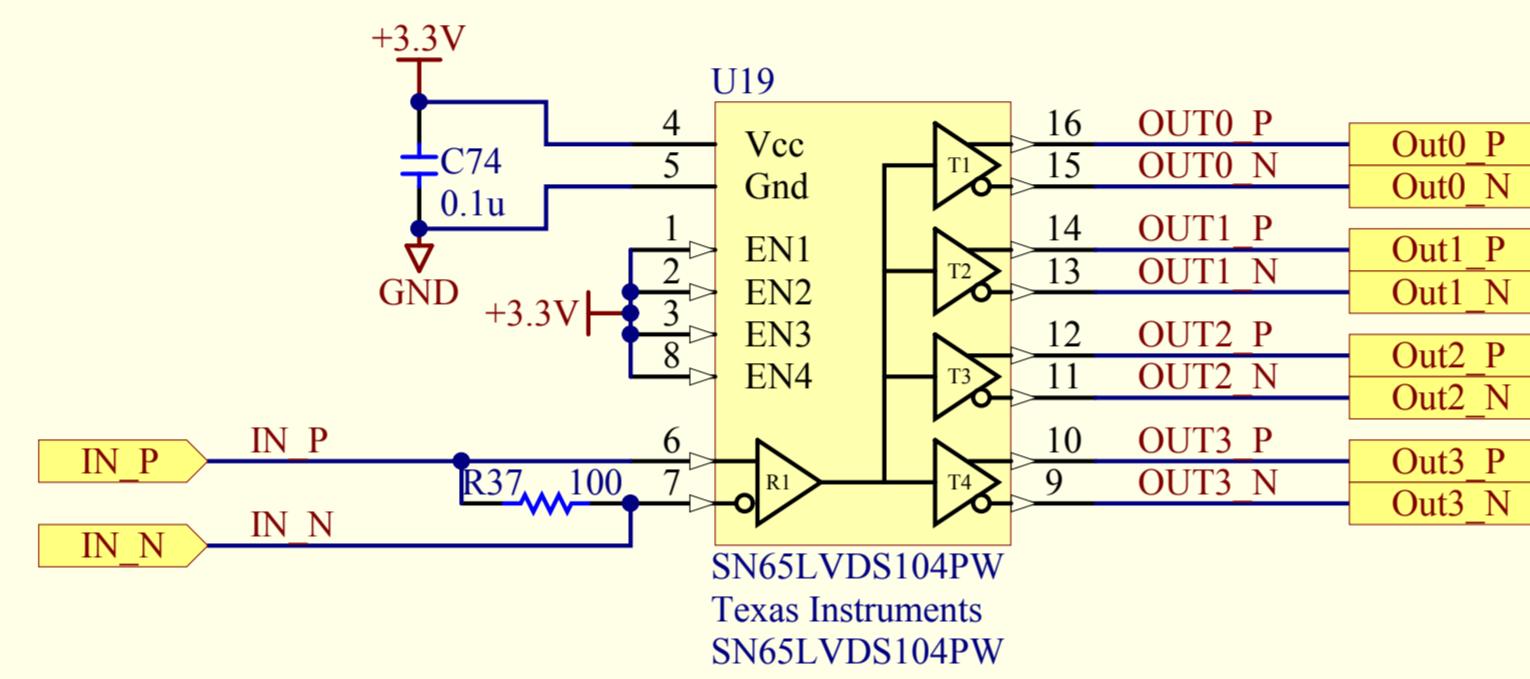
**T2K\_CMB - Crate Master Board (1:4 LVDS Fanout)**

Revision <b>A</b>	Drawing #: 8	TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 8 of 14	Size: B
	Drawn by: C. Ohlmann	Date: 06/03/2008
File: M:\edev\Altium\Projects\T2K_CMB\LVDSFanout1to4.SchDoc		10:40:44 AM



**T2K\_CMB - Crate Master Board (1:4 LVDS Fanout)**

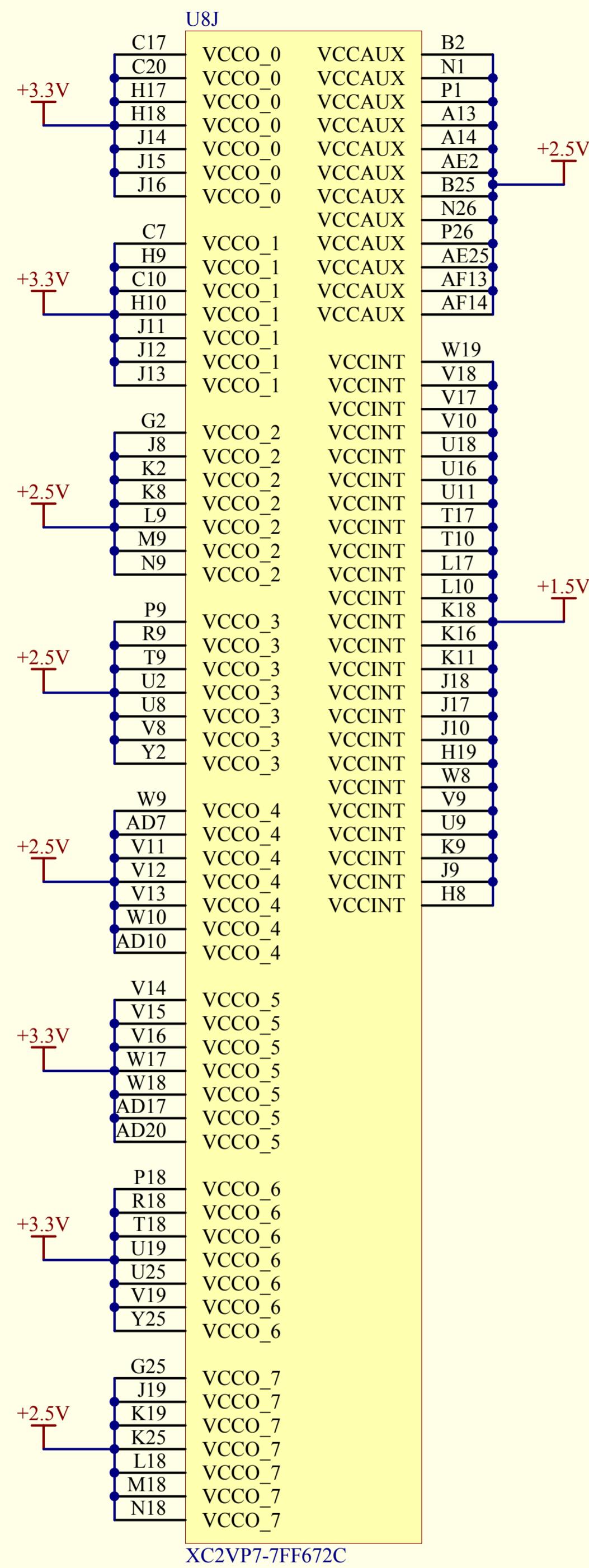
Revision <b>A</b>	Drawing #: 8	TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 8 of 14	Size: B
	Drawn by: C. Ohlmann	Date: 06/03/2008
File: M:\edev\Altium\Projects\T2K_CMB\LVDSFanout1to4.SchDoc		10:40:44 AM

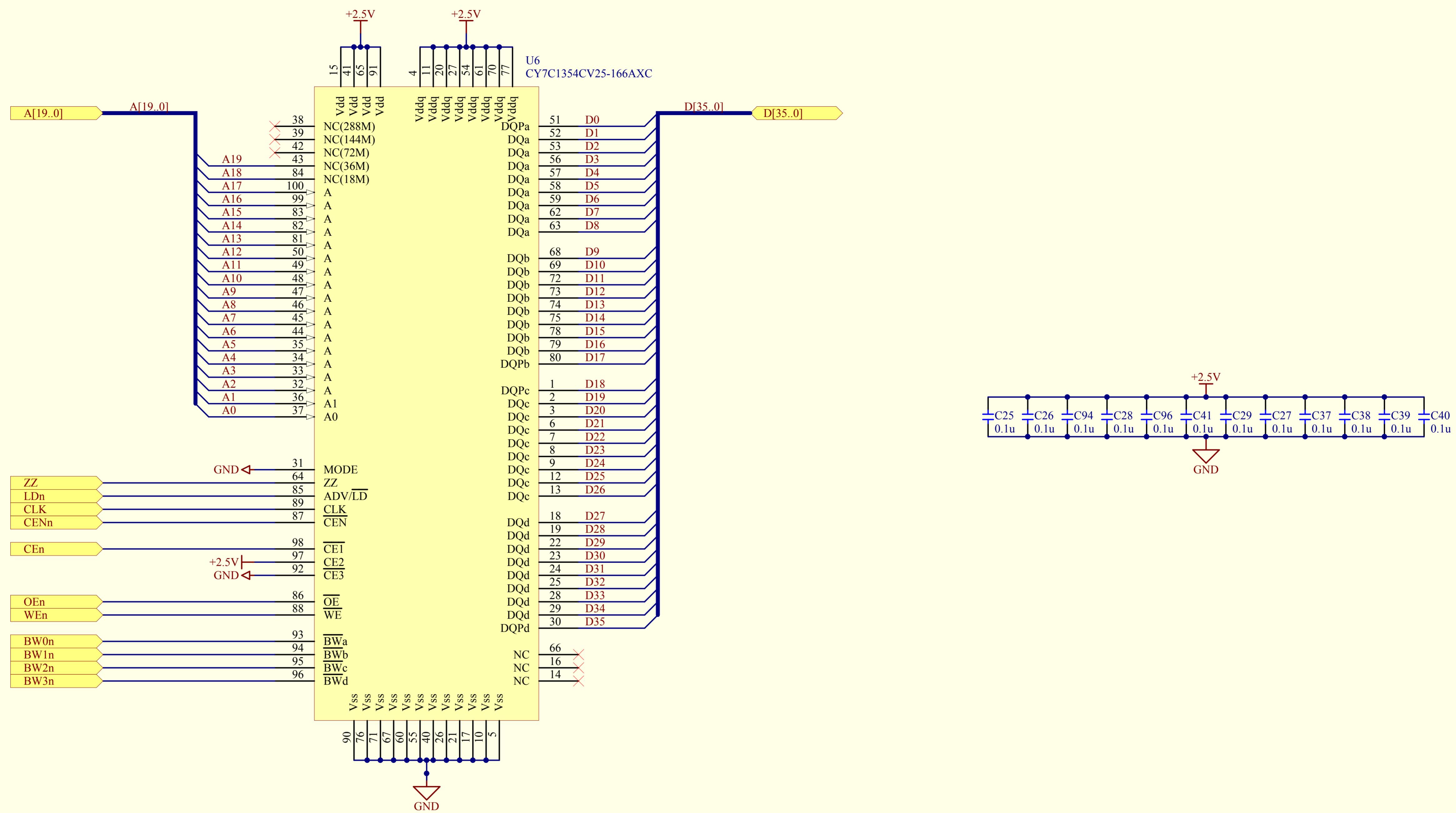


**T2K\_CMB - Crate Master Board (1:4 LVDS Fanout)**

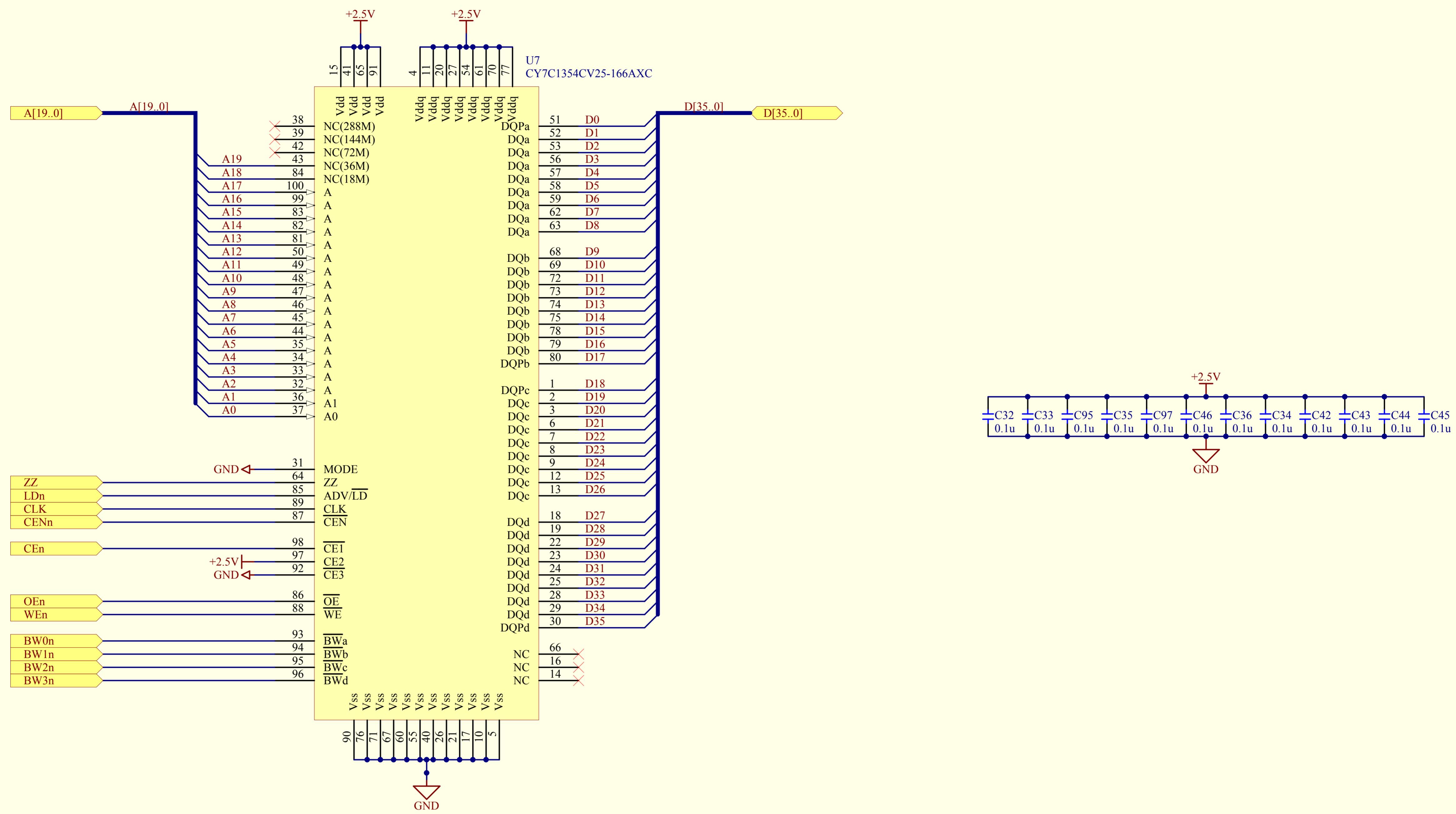
Revision <b>A</b>	Drawing #: 8	TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 8 of 14	Size: B
	Drawn by: C. Ohlmann	Date: 06/03/2008
File: M:\edev\Altium\Projects\T2K_CMB\LVDSFanout1to4.SchDoc		10:40:44 AM

### FPGA POWER PINS



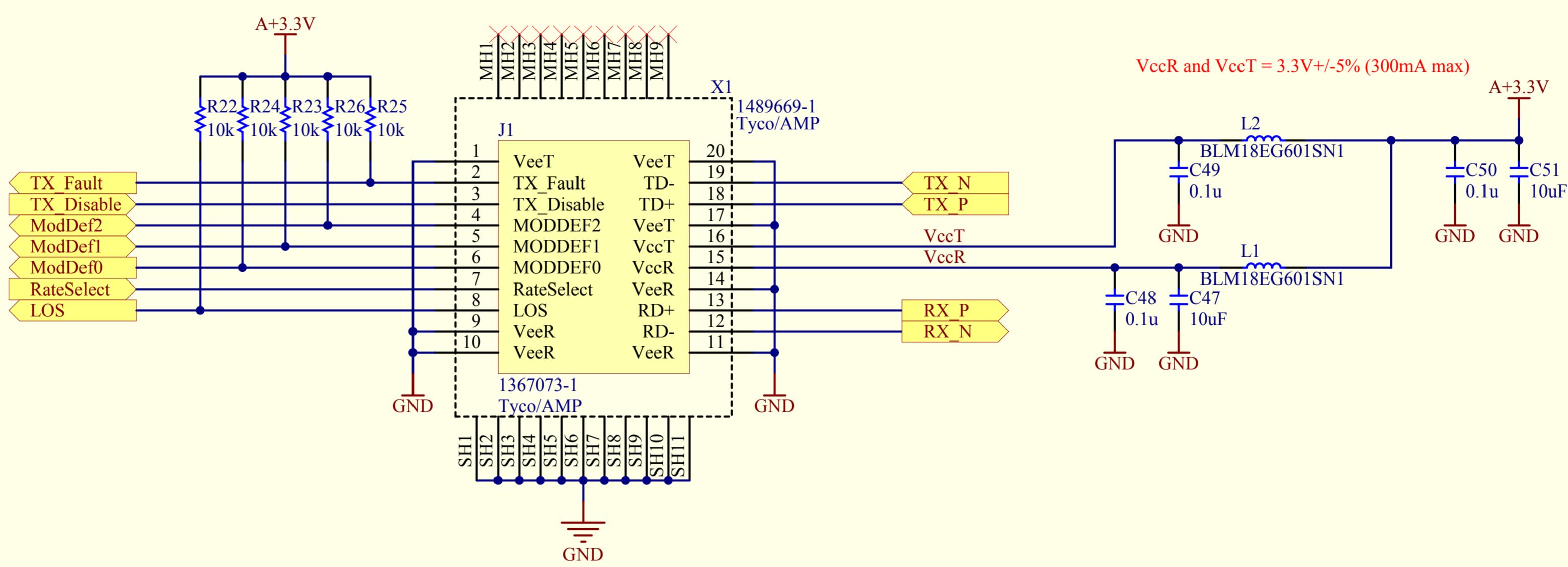


<b><i>T2K_CMB - Crate Master Board (SRAM)</i></b>				
<b>A</b>	Drawing #: 10			
	Sheet #: 10 of 14	Size: B		
	Drawn by: C. Ohlmann	Date: 06/03/2008		
File: M:\edudev\Altium\Projects\T2K_CMB\MemorySRAM.SchDoc				10:40:44 AM



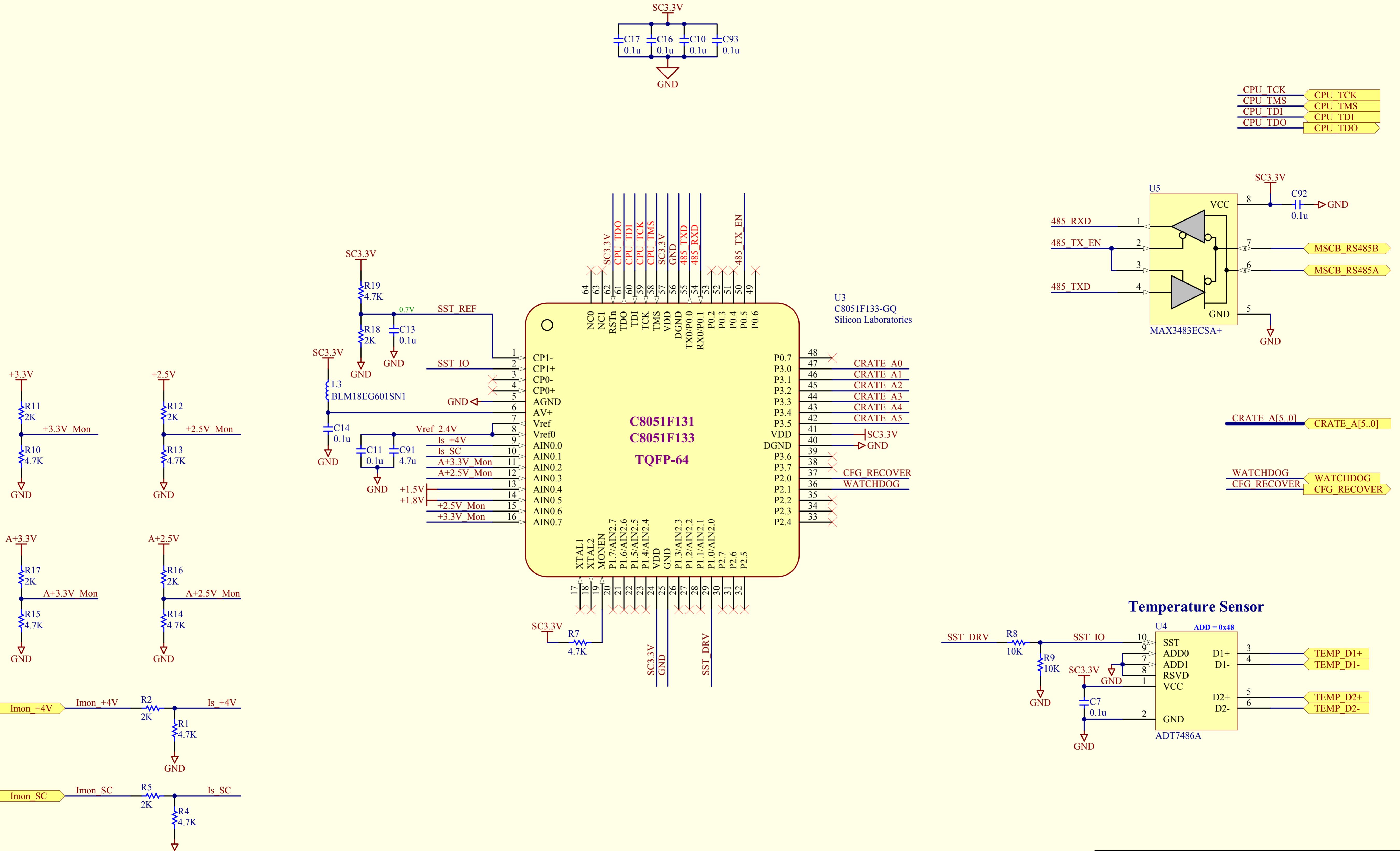
T2K\_CMB - Crate Master Board (SRAM)

Revision	Drawing #: 10	TRIUMF
A	Sheet #: 10 of 14	4004 Wesbrook Mall
		Vancouver, B.C.
	Drawn by: C. Ohlmann	Canada
	Date: 06/03/2008	V6T 2A3
File: M:\edev\Altium\Projects\T2K_CMB\MemorySRAM.SchDoc		
10:40:44 AM		



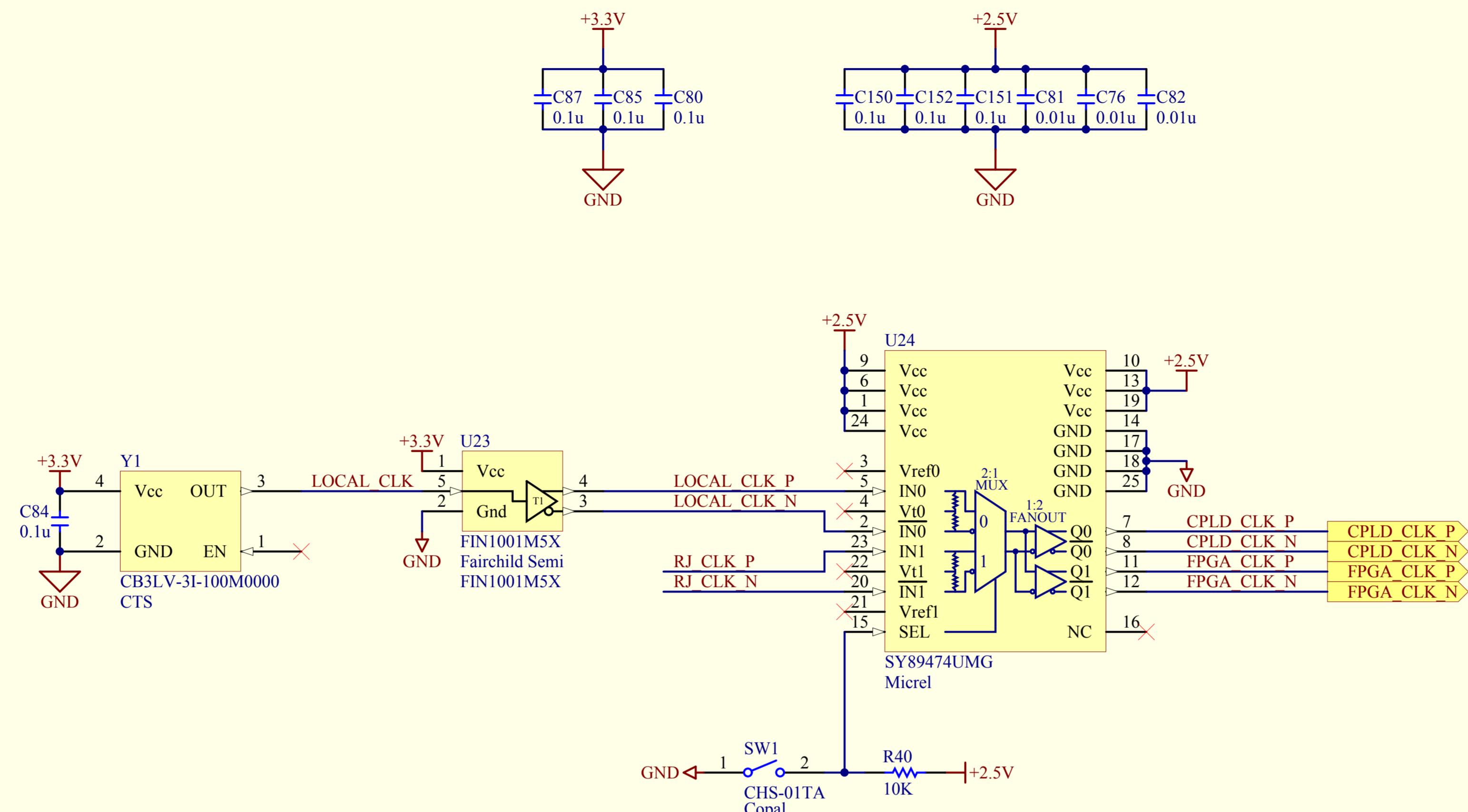
T2K\_CMB - Crate Master Board (Optical Link)

Revision	Drawing #: 11	TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
A	Sheet #: 11 of 14	Size: B
	Drawn by: C. Ohlmann	Date: 06/03/2008
File: M:\edev\Altium\Projects\T2K_CMB\OpticalLink.SchDoc		10:40:45 AM

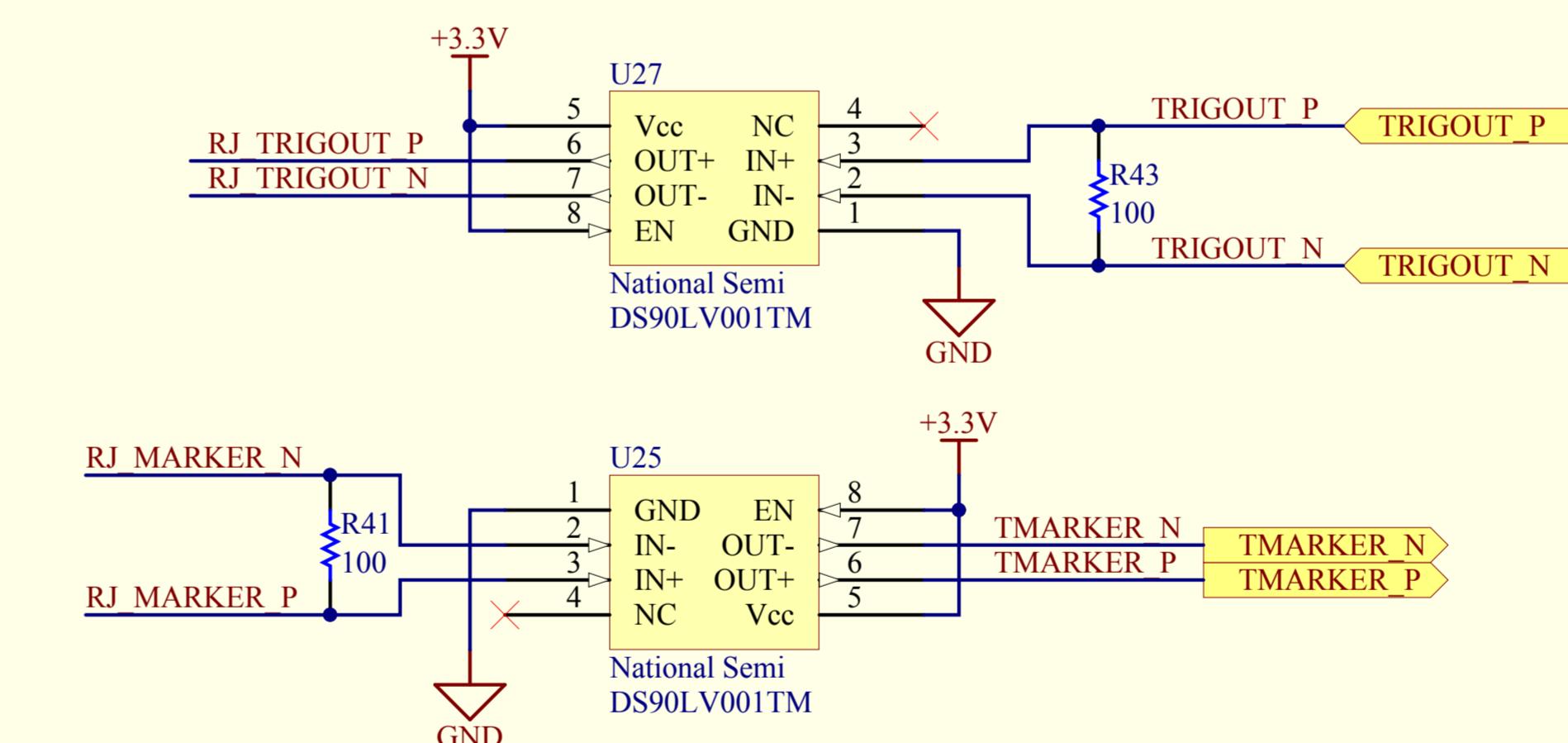
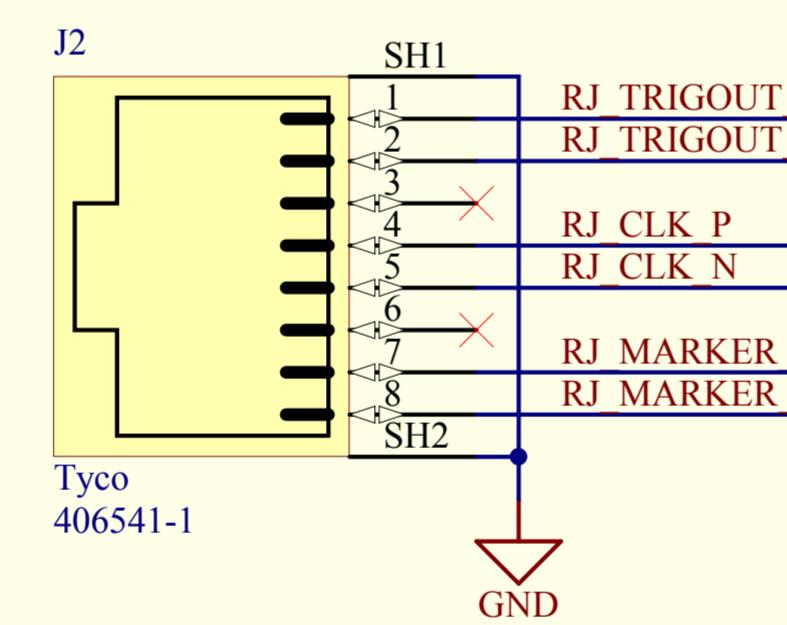


T2K\_CMB - Crate Master Board (Slow Control)

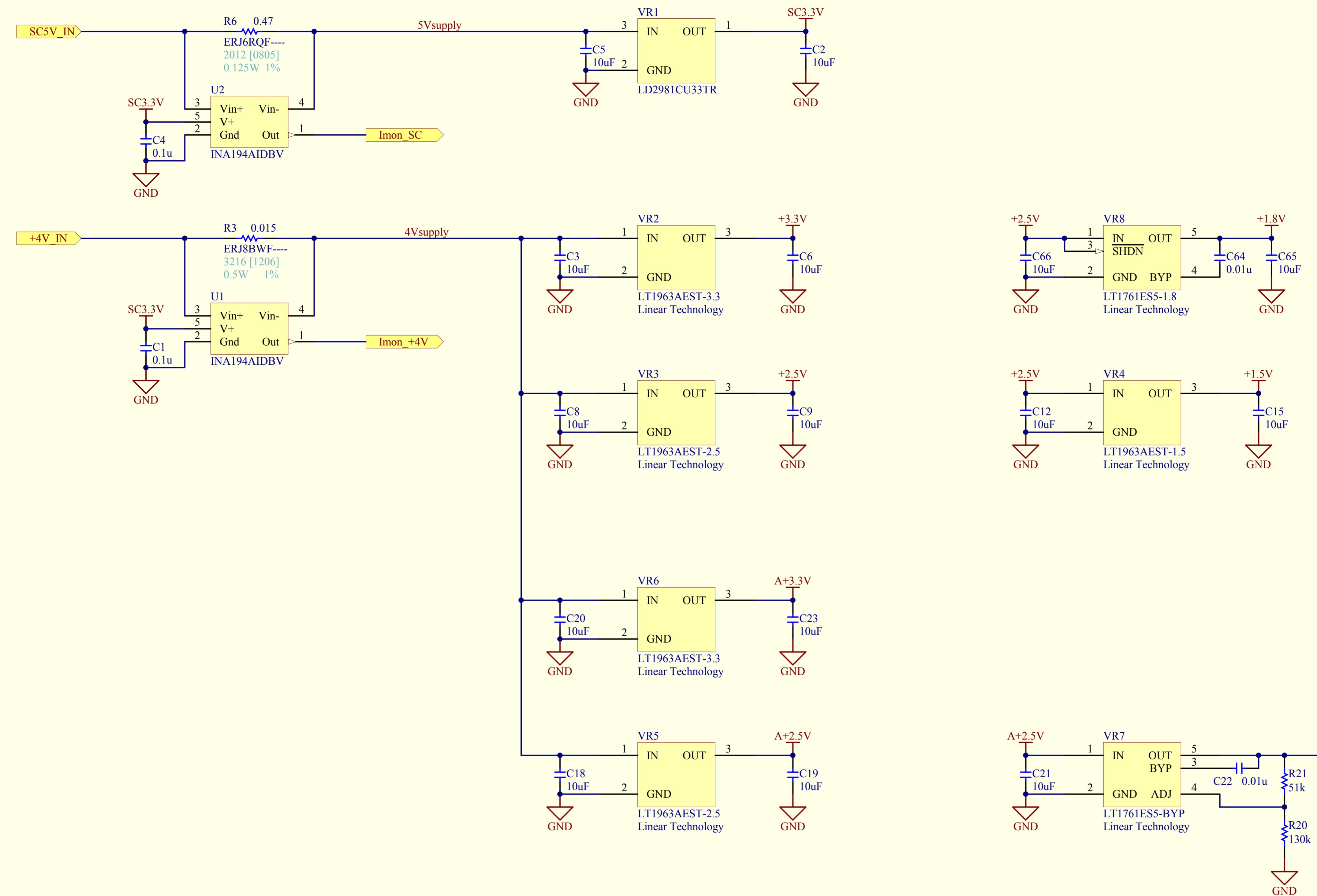
Revision <b>A</b>	Drawing #: 12 Sheet #: 12 of 14 Size: B Drawn by: C. Ohlmann Date: 06/03/2008	TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
File: M:\edev\Altium\Projects\T2K_CMB\SlowControl.SchDoc 10:40:45 AM		



Cable Termination (Standard)	
WHITE/orange	
ORANGE/white	
WHITE/green	
BLUE/white	
WHITE/blue	
GREEN/white	
WHITE/brown	
BROWN/white	



T2K_CMB - Crate Master Board (Clock / Trigger)			
Revision	Drawing #: 13	TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3	
A	Sheet #: 13 of 14	Size: B	
	Drawn by: C. Ohlmann	Date: 06/03/2008	
File: M:\edev\Altium\Projects\T2K_CMB\TimingMarkerAndTrigger.SchDoc			10:40:45 AM



T2K_CMB - Crate Master Board (Voltage Regulators)			
Revision	Drawing #: 14	TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3	
<b>A</b>	Sheet #: 14 of 14	Size: B	
	Drawn by: C. Ohlmann	Date: 06/03/2008	
File: M:\edev\Altium\Projects\T2K_CMB\VoltageRegulators.SchDoc			10:40:45 AM

