# Gurmeet Singh

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## Summary

*I have over 25 years of leading edge technical experience both as a leader and an individual contributor with a record of highly effective, flawless and prolific execution. I can quickly deploy the highly potent mix of EDA tools, programming and circuits expertise. My strengths include excellent communication and analytical skills, breadth of knowledge and ingenuity.*

## Experience

### [18-20]  Machine Learning SOC Startup, Methodology and Global Clocking Engineer

- Design of global clock distribution network, model the reconvergent network, simulate with spice and implement using ICC2. Setup custom compiler schematic and netlisting environment with extracted views. Characterize PVT sensitivity of library cells and level shifters with spice simulations.
- Defined physical design methodology for a very large 7nm Machine Learning SoC for process corners and timing margins. Place and route on a million gate low voltage design.  Set up Redhawk-Seascape flow for EM/IR.

### [15-17] Consultant

- Physical design methodology and netlist-to-gds flow development in tcl using Cadence toolset.  Also Assura physical verification and logical equivalence (lec) flows.
- Hierarchical implementation of an instance array design including floorplanning, power grid, pin placement, place and route, logical equivalence and physical verification. Silicon success.
- Abstract generation of analog macros and hierarchical instances to allow for through the block routing.
- Mixed-signal custom CAD support including SKILL programming
- Set up Virtuoso QRC extraction flow for full chip STA, set up and run full chip STA with Tempus, set up and run full chip LEC with Conformal. Silicon success.

### [13-14] Qualcomm Technologies, Senior Staff Engineer

- Top level floorplan, power grid with multiple power domains, using CPF/UPF for a mixed signal design, automated floorplan generation with Tcl. Wrote power intent CPF from scratch. Full chip formal (LEC) and low power (CLP) verification using Cadence tools. Apache Redhawk EM/IR analysis, debug and fixes. My leadership enabled a rare ahead of schedule tapeout. Silicon success.

### [08-13] Consultant

- Developed a 40 nm automated and optimized, tapeout ready, Cadence based implementation flow.
- Wrote Tcl scripts for a correct by construction, tunable flow used for all blocks.
- Developed automated, tapeout ready, STA setup using Primetime-SI using Tcl/Perl scripts.
- Implemented several large blocks at tapeout quality using the above flow ; the resulting GDSII were timing, LEC, LVS/DRC clean. Silicon success.
- Setup 40nm Cadence based, automated, tapeout ready, block level implementation flow.
- Hierarchical physical implementation flow in 65nm technology using Cadence.
- Telecom ASIC: Implementation of two large blocks using Magma. Silicon Success.
- 65nm WiFi ASIC: Implementation of large block using Magma. Silicon Success.
- 65nm WiFi ASIC: Full chip EM/IR signoff using Apache-Redhawk. Silicon Success.

### [06-08] Teranetics, Principal Engineer

- 130nm/65nm 10GBASE-T PHY ASIC: Implement many large blocks, some using x-route. Automate implementation, static timing analysis, logical equivalence and physical verification flows. Power estimation; power reduction using special cells. Silicon Success.

**[04-06] Airgo Networks, Physical Design Manager**
· Multiple WiFi ASICs: Implement many blocks using Magma. Automate PTSI STA, formal, Calibre
  PV flows. Full chip EM/IR signoff using Apache-Redhawk. Tapeout signoff/jobview. ECOs, I/O
  Spice sims, IP integration, Methodology, project management. Silicon success.

**[01-04] Transmeta, senior Member, Technical Staff**
· 1.2/1.8GHz Efficeon CPUs: Implement Hypertransport PnR blocks; Register File design. ECOs.
  Setup latch compatible STA flow. Array and noise methodologies. Silicon Success (#1,#2).

**[99-01] Sun Microsystems, Member, Technical Staff**
· UltraSparc V CPU: CAM Register File, Custom logic circuit design
· 1.2GHz UltraSparc III CPU: Port a dozen 130nm dynamic circuit blocks, including adders up to
  64-bits, from 180nm to 130nm. Silicon success.

**[97-99] Intel Corporation, Design Engineer**
· 833MHz Pentium III Xeon CPU: High speed dynamic circuit design for L2$ ECC, L2$ STA/EM/IR
  verification. Silicon success.
· 600 MHz Pentium III CPU : GTL I/O circuit design. Silicon success.

**[94-97] ST Microelectronics, Design Engineer**
· Circuit Design of 32kx8, 128kx8 SRAMs. Silicon success. CAD setup.
· Reverse engineer a register file and re-implement, verify functionality using verilog switch level
  simulation. Silicon success.

## Education

**[1989-93] M.Engg., Electrical Comm, Indian Institute of Science.**
First class with distinction. Alumni medal, Best Student, 1990-93
**[1986-89] B.Sc., Physics, Delhi University.**
First class with distinction, Gold medal, Best Student: 1987/88/89.