Gurmeet Singh

(650) 793-1051 gurmeet.postbox@gmail.com Sunnyvale CA 94086

Summary

I have extensive and broad experience in Physical Design and a long history of successful, productized tapeouts, sometimes using flows that I set up. [U.S.Citizen.]

www.linkedin.com/in/gurmeet
https://swiftgurmeet.github.io/st/resume_gurmeet_singh.pdf
github.com

Experience

[2022-2024] Intel Foundry Services, Physical Design Methodology Engineer

- Set up and use an implementation (rtl2gds) flow for Intel 18A node using Cadence Flowtool that supports numerous flow, technology, power/performance/area optimization options. This enabled batch jobs with up to thousands of parallel runs with different options, IPs, libraries and metal stacks for regressions or analysis. Started the git repo for the flow and made over 150 commits.
- Worked with Cadence to productize an Intel18A PPA oriented reference flow usable by customers to jump start their own implementation flows.
- Set up infrastructure for analyzing a large number of Intel18A synthesis/place&route runs on industry standard IPs with Cadence based Genus/Innovus based flow, collect PPA and other QOR metrics and continually document/present them visually using Python-Matplotlib and R-ggplot2.
- Continually use the above infrastructure to benchmark and optimize the PPA metrics of industry standard IPs and publish results with different versions of Intel18A libraries and PDKs.
- Worked with Cadence to produce a performance optimized implementation and the associated hierarchical RTL2GDS flow for a high performance ARM core (Cortex-X925 "Blackhawk") on the Intel18A process.

[2020-2022] Samsung Austin Research Center, Physical Design Consultant

- Physical implementation (rtl2gds) of 3 large GPU blocks to tapeout [Silicon Success] on a 4nm technology using Cadence Innovus, including floorplanning in SNPS, meeting all area/power/timing requirements. Over 75 timing/DRC/other ECOs. Provide guidance to the CAD team on methodology.
- PnR flow development in SNPS fusion compiler for 3nm (Samsung 3GAP) technology

[18-20] Esperanto Technologies, Methodology and Global Clocking Engineer

- Defined physical design methodology for 7nm process corners including very low voltage operation and timing margins
- Design of global clock distribution network for a very large 7nm SoC, model the reconvergent network, simulate with spice, implement using ICC2 and resimulate with extracted spice netlist. Publish chip level clock specification document.
- Block level place and route implementation of a million gate low voltage design.
- Set up a custom compiler schematic and netlisting environment with extracted views. Characterize PVT sensitivity of library cells, esp. level shifters and a ring oscillator with spice simulations and publish results.
- Set up and define methodology for an EM/IR flow using Ansys Redhawk/Seascape
- Support and manage PLL, DLL, DDR, PCIE vendors through weekly meetings.

[15-17] Consultant, zGlue Inc

- Physical design methodology and netlist-to-gds flow development in tcl using Cadence toolset. Also developed Assura physical verification and logical equivalence (lec) flows.
- Hierarchical implementation of an instance array design including floorplanning, power grid, pin placement, place and route, logical equivalence and physical verification. Silicon success.
- Abstract (LEF) generation of analog macros and hierarchical instances to allow for through the block routing.
- Mixed-signal custom CAD support including SKILL programming
- Set up Virtuoso QRC extraction flow for full chip STA, set up and run full chip STA with Tempus, set up and run full chip LEC with Conformal. Silicon success.

[13-14] Qualcomm Technologies, Senior Staff Engineer

- Top level floorplan, power grid with multiple power domains, using CPF/UPF for a mixed signal design, automated floorplan generation with Tcl. Wrote power intent CPF from scratch. Full chip formal (LEC) and low power (CLP) verification using Cadence tools. Apache Redhawk EM/IR analysis, debug and fixes. My leadership enabled a rare ahead of schedule tapeout. Silicon success.

[12-13] Cadence Design Systems, Staff Applications Engineer

- Developed complete, automated rtl2gds flow (14nm/finFET); optimized for PPA and validated on A9 ARM core with Neon coprocessor (TT Nominal @ 2.5 GHz).

[08-12] Consultant/PD Engineer

- Developed and deployed a 40 nm automated and optimized, tapeout ready, Cadence based implementation flow.
- Wrote Tcl scripts for a correct by construction, tunable flow used to implement all blocks.
- Developed automated, tapeout ready, STA setup using Primetime-SI using Tcl/Perl scripts.
- Implemented many large blocks at tapeout quality using the above flow ; the resulting GDSII were timing, LEC, LVS/DRC clean. Silicon success.
- Set up 40nm Cadence based, automated, tapeout ready, block level implementation flow.
- Developed hierarchical physical implementation flow in 65nm technology using Cadence.
- Telecom ASIC: Tapeout implementation of two large blocks using Magma. Silicon Success.
- 65nm WiFi ASIC: Tapeout implementation of large block using Magma. Silicon Success.
- 65nm WiFi ASIC: Full chip EM/IR signoff using Apache-Redhawk. Silicon Success.

[06-08] Teranetics, Principal Engineer

- 130nm/65nm 10GBASE-T PHY ASIC: Implement many large blocks, some using x-route, for a rare project using diagonal signal routing. Automate implementation, static timing analysis, logical equivalence and physical verification flows. Power estimation; power reduction using special cells. Silicon Success.

[04-06] Airgo Networks, Physical Design Manager

- Multiple WiFi ASICs: Implement many blocks using Magma. Automate PTSI STA, formal, Calibre PV flows. Automated Apache-Redhawk flow and used it for full chip EM/IR signoff. Did tapeout processes/signoff/jobview/ftp to foundry. Silicon success.
- ECOs, I/O Spice sims, IP integration, Methodology, project management.

[01-04] Transmeta, senior Member, Technical Staff

- 1.2/1.8GHz Efficeon CPUs: Implement Hypertransport PnR blocks; Register File design. ECOs. Setup latch compatible STA flow. Array and noise methodologies. Silicon Success (#1,#2).

[99-01] Sun Microsystems, Member, Technical Staff

- UltraSparc V CPU: CAM Register File, Custom logic circuit design
- 1.2GHz UltraSparc III CPU: Port a dozen 130nm dynamic circuit blocks, including adders up to 64-bits, from 180nm to 130nm. Silicon success.

[97-99] Intel Corporation, Design Engineer

- 833MHz Pentium III Xeon CPU: High speed dynamic circuit design for L2$ ECC, L2$ STA/EM/IR verification. Silicon success.
- 600 MHz Pentium III CPU : GTL I/O circuit design. Silicon success.

[94-97] ST Microelectronics, Design Engineer

- Circuit Design of 32kx8, 128kx8 SRAMs. Silicon success. CAD setup.
- Reverse engineer a register file and re-implement, verify functionality using verilog switch level simulation. Silicon success.

Education

[2015-2018] Coursera: 26 Certifications

Completed a total of 26 courses with certificates, mostly with over 90% grade with specializations in Machine Learning, Statistical Inference and Big Data.

[1989-93] M.Engg., ECE, Indian Institute of Science

First class with distinction. Alumni medal, Best Student, 1990-93

Thesis on "Symbolic Compaction of Analog Integrated Circuits"

[1986-89] B.Sc., Physics, Delhi University.

First class with distinction, Gold Medals, Best Student, 1987/88/89.

Physical Design, Implementation, Flow, Methodology, Tapeout, Synthesis, Place, Route, PnR, P&R, Placement, Partitioning, Assembly, Clock Tree, CTS, Placement, Routing, STA, Signoff, Physical Verification, Power Grid, Spice, Simulation, Logical Equivalence, Parasitics Extraction, LPE, Optimization, Automation, CAD, EDA, Programming, Scripting, Python, Tcl, R, Perl, Shell,Cadence, Innovus, Synopsys, Primetime, Ansys, Apache, Redhawk