Gurmeet Singh

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https://swiftgurmeet.github.io/resume/

Summary

I have over 25 years of leading edge technical experience both as a leader and an individual contributor with a record of highly effective, flawless and prolific execution. I've contributed significantly to the design of many successful products including the original Pentium III, Ultrasparc III, Power Efficient X86, pioneering silicons like MIMO WiFi, 10GB Ethernet, PCIE SSD controller, Audio Codec (think Alexa) and a 2.5D interposer. My strengths include good communication and analytical skills, breadth of knowledge and ingenuity. Lately, I've been learning about Data Science and Machine Learning.

I'm unable to travel outside the San Francisco Bay Area.

Experience

[16-17] CONSULTANT, ZGLUE INC.

- Physical design methodology and netlist-to-gds flow development in tcl using Cadence toolset. Also Assura physical verification and logical equivalence (lec) flows.
- Hierarchical implementation of an instance array design including floorplanning, power grid, pin placement, place and route, logical equivalence and physical verification.
- Abstract generation of analog macros and hierarchical instance to allow for through the block routing.
- Mixed-signal custom CAD support including SKILL programming
- Setup Virtuoso QRC extraction flow for full chip STA, set up and run full chip STA with Tempus, set up and run full chip LEC with Conformal. Silicon success.

[15-16] STUDENT

- Data Science/Machine Learning/Programming Student - See courses below
- Kaggle Participant
- Swift programmer

[13-14] QUALCOMM TECHNOLOGIES, SENIOR STAFF ENGINEER

Top level floorplan, power grid with multiple power domains, using CPF/UPF for a mixed signal design, automated floorplan generation with Tcl. Wrote power intent CPF from scratch. Full chip formal (LEC) and low power (CLP) verification using Cadence tools. Apache Redhawk EM/IR debug and fixes. My leadership enabled a rare ahead of schedule tapeout. Silicon success (WCD9335).

[12-13] CADENCE DESIGN SYSTEMS, STAFF APPLICATION ENGINEER

Developed complete, automated rtl2gds flow (14nm/finFET) using Cadence tools. Using the same, implemented an ARM A9 design @ 2.4GHz. Implemented a 28nm DDR-PHY IP for tapeout.

[11-12] SANDFORCE INC., PRINCIPAL ENGINEER

- Developed a 40 nm automated and optimized, tapeout ready, Cadence based implementation flow.
- Wrote Tcl scripts for a correct by construction, tunable flow used for all blocks.
- Developed automated, tapeout ready, STA setup using Primetime-SI using Tcl/Perl scripts.
- Implemented several large blocks at tapeout quality using the above flow ; the resulting GDSII were timing, LEC, LVS/DRC clean. Silicon success.
- Helped grow the size and capability of the physical design team and lead technical direction.

[08-11] CONTRACTOR @(QUALCOMM, SANDISK)

- Setup 40nm Cadence based, automated, tapeout ready, block level implementation flow.
- Hierarchical physical implementation flow in 65nm technology using Cadence.
- 65nm WiFi ASIC: Implementation of large block using Magma. Silicon Success.
- 65nm WiFi ASIC: Full chip EM/IR signoff using Apache-Redhawk. Silicon Success.

[06-08] TERANETICS, PRINCIPAL ENGINEER

130nm/65nm 10GBASE-T PHY ASIC: Implement many large blocks, some using x-route. Automate implementation, static timing analysis, logical equivalence and physical verification flows. Power estimation; power reduction using special cells. Silicon Success.

[04-06] AIRGO NETWORKS, PHYSICAL DESIGN MANAGER

Multiple WiFi ASICs: Implement many blocks using Magma. Automate PTSI STA, formal, Calibre PV flows. Full chip EM/IR signoff using Apache-Redhawk. Tapeout signoff/jobview. ECOs, I/O Spice sims, IP integration, Methodology, project management. Silicon success.

[01-04] TRANSMETA, SMTS

1.2/1.8GHz Efficeon CPUs: Implement Hypertransport PnR blocks; Register File design. ECOs. Setup latch compatible STA flow. Array and noise methodologies. Silicon Success.

[99-01] SUN MICROSYSTEMS, MTS

- UltraSparc V CPU: CAM Register File, Custom logic circuit design
- 1.2GHz UltraSparc III CPU: Port a dozen 130nm dynamic circuit blocks, including adders up to 64-bits, from 180nm to 130nm. Silicon success.

[97-99] INTEL CORPORATION, DESIGN ENGINEER

- 833MHz Pentium III Xeon CPU: High speed dynamic circuit design for L2$ ECC, L2$ STA/EM/IR verification. Silicon success.
- 600 MHz Pentium III CPU : GTL I/O circuit design. Silicon success.

[94-97] ST MICROELECTRONICS, DESIGN ENGINEER

Circuit Design of 32kx8, 128kx8 SRAMs. Silicon success. CAD setup. Reverse engineer a register file and re-implement, verify functionality using verilog switch level simulation. Silicon success.

Education

I was the best student in my class for all seven years of college level education, including four at India's best engineering institution.

[2015-2016]: ONLINE COURSERA COURSES

- Machine Learning
- Machine Learning With Big Data
- Practical Machine Learning
- R Programming
- Statistical Inference
- Reproducible Research
- Regression Models
- Functional Programming Principles in Scala
- Object Oriented Programming in Java
- Financial Markets
- Graph Analytics for Big Data
- Hadoop Platform and Application Framework
- The Data Scientist's Toolbox
- Getting and Cleaning Data
- Exploratory Data Analysis
- Developing Data Products
- Introduction to Big Data
- Introduction to Big Data Analytics
- HTML, CSS and Javascript for Web Developers

[12/2006] U.C. BERKELEY EVENING COURSE

Introduction to Digital Signal Processing Course, UC Berkeley, A Grade

[1989-93] M.ENGG., ELECTRICAL COMM, INDIAN INSTITUTE OF SCIENCE.

First class with distinction. Alumni medal, Best Student, 1990-93

[1986-89] B.SC., PHYSICS, DELHI UNIVERSITY.

First class with distinction, Gold medal, Best Student: 1987/88/89.

References

Available on request, including my recent supervisors.