



## Gurmeet Singh

(650) 793-1051

gurmeet.postbox@gmail.com

1055 Manet Dr. #80, Sunnyvale CA 94087

### Summary

I have over 25 years of experience in ASIC physical design/flow/methodology and circuit design. My strengths include good communication and analytical skills, breadth of knowledge and ingenuity.

### Experience

#### **[2016-17] CONSULTANT, ZGLUE INC. (2 SILICON SUCCESSES)**

- Physical design methodology, netlist-to-gds, DRC/LVS, QRC, STA and LEC flows.
- Hierarchical arrayed floorplanning, power grid, place and route, abstract generation.

#### **[2014-15] QUALCOMM TECHNOLOGIES, SENIOR STAFF ENGINEER (SILICON SUCCESS)**

Top level floorplanning (flat 2.5M instances), power grid with multiple power domains, wrote CPF. Full chip LEC/CLP. Apache-Redhawk EM/IR debug and fixes. Beat the schedule. Received two Qualstars.

#### **[2012-13] CADENCE DESIGN SYSTEMS, STAFF APPLICATION ENGINEER**

Developed complete, automated rtl2gds flow (14nm/finFET); validated on A9/Neon ARM core.

#### **[2011-12] SANDFORCE INC., PRINCIPAL ENGINEER (SILICON SUCCESS)**

- Developed and rolled out 40 nm Cadence PnR and PTSI STA flows; used for several large blocks.

#### **[2008-11] CONTRACTOR/ENGINEER @(MULTIPLE) (3 SILICON SUCCESSES)**

- Setup 40nm hierarchical and block level flows.
- Telecom ASIC: Magma implementation of two large blocks.
- WiFi ASICs: Magma implementation of a large block, Full chip EM/IR signoff.

#### **[2006-08] TERANETICS, PRINCIPAL ENGINEER (SILICON SUCCESS)**

130nm 10GBASE-T PHY: Implement large blocks, some with x-route. Implementation, static timing analysis, logical equivalence and physical verification flows. Power estimation.

#### **[2004-06] AIRGO NETWORKS, PHYSICAL DESIGN MANAGER (SILICON SUCCESS)**

Multiple WiFi ASICs: Blocks' implementation with Magma. Automate PTSI STA, LEC, Calibre PV flows. Full chip EM/IR signoff using Apache-Redhawk. Tapeout, IP integration, Methodology, project management.

#### **[2001-04] TRANSMETA, SENIOR MEMBER OF TECHNICAL STAFF (2 SILICON SUCCESSES)**

1.2/1.8GHz Efficeon CPUs: Implement Hypertransport PnR blocks; Register File design. Setup latch compatible STA flow. Array and noise methodologies. Silicon Success.

#### **[1999-2001] SUN MICROSYSTEMS, MEMBER, TECHNICAL STAFF (SILICON SUCCESS)**

- UltraSparc III/V CPUs: Dynamic adders, CAM Register File, Custom logic circuit design

#### **[1997-99] INTEL CORPORATION, DESIGN ENGINEER (2 SILICON SUCCESSES)**

- 600 MHz Pentium III/833MHz Xeon CPUs: High speed dynamic circuit design for L2\$ ECC

#### **[1994-97] ST MICROELECTRONICS, DESIGN ENGINEER (2 SILICON SUCCESSES)**

Circuit Design of 32kx8, 128kx8 SRAMs, Real Time Clock. Switch level verification.

### Education

**[1989-93] M.ENG., ELECTRICAL COMM., INDIAN INSTITUTE OF SCIENCE (ALUMNI MEDAL)**

**[1986-89] B.SC., PHYSICS, DELHI UNIVERSITY (GOLD MEDAL)**