SYMBOLIC COMPACTION OF ANALOG INTEGRATED CIRCUITS

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Abstract

CAD tools for analog layout design have lagged behind their digital counterparts. A compaction system for analog layouts must additionally handle symmetry constraints. An attempt has been made in this project to solve the analog compaction problem entirely in the graph domain. By eliminating the use of Linear Programming for solving the symmetry constraints, as done in most of the previous approaches, the algorithm can run fast enough to be of use. Various types of user defined constraints have been modeled as either mixed or symmetry constraints, to be suitably included in graph based approach to compaction. One such technique has been implemented and tested.