



# Gurmeet Singh

(650) 793-1051      gurmeet.postbox@gmail.com      1055 Manet Dr. #80, Sunnyvale CA 94087  
<https://swiftgurmeet.github.io/resume/>

## Summary

I've recently invested significant effort to learn about machine learning and data science. I have worked as a VLSI design engineer for many years. My strengths include good communication and analytical skills, quick learning and ingenuity.

## Experience

### [2015-2018] MACHINE LEARNING PROFESSIONAL

- Python, R, bit of Scala, Swift
- Tensorflow, Keras, NumPy
- CNN, RNN, GBM
- Expert Linux User

Coursera courses:

- Neural Networks and Deep Learning
- Structuring Machine Learning Projects
- Improving Deep Neural Networks: Hyper-parameter tuning, Regularization and Optimization
- Convolution Neural Networks
- Sequence Models
- Machine Learning
- Machine Learning With Big Data
- Practical Machine Learning
- R Programming
- Statistical Inference
- Reproducible Research
- Regression Models
- Functional Programming Principles in Scala
- Object Oriented Programming in Java
- Graph Analytics for Big Data
- Hadoop Platform and Application Framework
- The Data Scientist's Toolbox
- Getting and Cleaning Data
- Exploratory Data Analysis
- Developing Data Products
- Introduction to Big Data
- Introduction to Big Data Analytics
- HTML, CSS and Javascript for Web Developers

**[2016-2017] CONSULTANT, ZGLUE INC. (2 SILICONS SUCCESSES)**

- IOT silicon: Physical design, methodology.

**[2014-2015] QUALCOMM TECHNOLOGIES, SENIOR STAFF ENGINEER (SILICON SUCCESS)**

Audio Codec physical design. Beat the schedule. Received two Qualstars.

**[2012-2013] CADENCE DESIGN SYSTEMS, STAFF APPLICATION ENGINEER**

Developed rtl2gds flow (14nm/finFET); proven on A9/Neon ARM core.

**[2011-2012] SANDFORCE INC., PRINCIPAL ENGINEER (SILICON SUCCESS)**

Physical design implementation, methodology and flow development.

**[2008-2011] CONTRACTOR/ENGINEER @(MULTIPLE) (3 SILICON SUCCESSES)**

- Physical design methodology and flow development; WiFi ASIC design.

**[2006-2008] TERANETICS, PRINCIPAL ENGINEER (SILICON SUCCESS)**

130nm 10GBASE-T PHY ASIC design.

**[2004-2006] AIRGO NETWORKS, PHYSICAL DESIGN MANAGER (SILICON SUCCESS)**

Multiple WiFi ASIC design, project management.

**[2001-2004] TRANSMETA, SENIOR MEMBER OF TECHNICAL STAFF**

Efficeon CPU circuit and physical design

**[1999-2001] SUN MICROSYSTEMS, MEMBER, TECHNICAL STAFF (SILICON SUCCESS)**

UltraSparc III/V CPU circuit design.

## Education

**M.ENG., ELECTRICAL COMM., INDIAN INSTITUTE OF SCIENCE (ALUMNI MEDAL)**

**B.SC., PHYSICS, DELHI UNIVERSITY (GOLD MEDAL)**