# Summary

I have over 25 years of experience in ASIC physical design/flow/methodology and circuit design. My strengths include good communication and analytical skills, breadth of knowledge and ingenuity.

U.S. citizen.

# Experience

[2016-17] Consultant, ZGlue Inc. (2 Silicon successes)

* Physical design methodology, netlist-to-gds, DRC/LVS, QRC, STA and LEC flows.
* Hierarchical arrayed floorplanning, power grid, place and route, abstract generation.

[2014-15] Qualcomm Technologies, Senior Staff Engineer (silicon success)

Top level floorplanning (flat 2.5M instances), power grid with multiple power domains, wrote CPF. Full chip LEC/CLP. Apache-Redhawk EM/IR debug and fixes. Beat the schedule. Received two Qualstars.

[2012-13] Cadence Design Systems, Staff Application Engineer

Developed complete, automated rtl2gds flow (14nm/finFET); validated on A9/Neon ARM core.

[2011-12] Sandforce Inc., Principal Engineer (silicon success)

* Developed and rolled out 40 nm Cadence PnR and PTSI STA flows; used for several large blocks.

[2008-11] Contractor/Engineer @(multiple) (3 silicon succeses)

* Setup 40nm hierarchical and block level flows.
* Telecom ASIC: Magma implementation of two large blocks.
* WiFi ASICs: Magma implementation of a large block, Full chip EM/IR signoff.

[2006-08] Teranetics, Principal Engineer (silicon success)

# Gurmeet Singh

(650) 793-1051 gurmeet.postbox@gmail.com 1055 Manet Dr. #80, Sunnyvale CA 94087

130nm 10GBASE-T PHY: Implement large blocks, some with x-route. Implementation, static timing analysis, logical equivalence and physical verification flows. Power estimation.

[2004-06] Airgo Networks, Physical Design Manager (silicon success)

Multiple WiFi ASICs: Blocks’ implementation with Magma. Automate PTSI STA, LEC, Calibre PV flows. Full chip EM/IR signoff using Apache-Redhawk. Tapeout, IP integration, Methodology, project management.

[2001-04] Transmeta, senior Member OF Technical Staff (2 silicon successes)

1.2/1.8GHz Efficeon CPUs: Implement Hypertransport PnR blocks; Register File design. Setup latch compatible STA flow. Array and noise methodologies. Silicon Success.

[1999-2001] Sun Microsystems, Member, Technical Staff (silicon success)

* UltraSparc III/V CPUs: Dynamic adders, CAM Register File, Custom logic circuit design

[1997-99] Intel Corporation, Design Engineer (2 silicon successes)

* 600 MHz Pentium III/833MHz Xeon CPUs: High speed dynamic circuit design for L2$ ECC

[1994-97] ST Microelectronics, Design Engineer (2 silicon successes)

Circuit Design of 32kx8, 128kx8 SRAMs, Real Time Clock. Switch level verification.

# Education

[1989-93] M.Engg., Electrical Comm., Indian Institute of Science (alumni medal)

[1986-89] B.Sc., Physics, Delhi University (gold medal)