Georgia Institute of Technology

School of Computer Science

CS3220: Fall, 2014

Project 2: Single Cycle Processor

Version 1.0

Due: Sunday, October 12th, 2014 at 11:55pm

Project description:

In this project, you will design a single-cycle processor and synthesize it on your FPGA board. The processor should be able to support the entire set of instructions described in the project-isa.pdf on the course webpage (http://www.cc.gatech.edu/~hadi/teaching/cs3220/01-2014fa/doc/project/project-isa.pdf).

We provide two assembly code files, Test2.a32 and Sorter2.a32, and a sample object file, Sample.mif. The object file shows how you can generate object files from assembly code. You should implement your own assembler that reads the assembly code and generate the object files.

Note that there is no performance requirement (the logic optimization is not needed) and the only criterion for this project is the functionality.

Do not procrastinate. To get you started, we have provided you with a Project2.zip file with settings, timing requirements, and some of the Verilog codes for the design. It is highly recommended to begin work on the assembler and on the processor design immediately. You can manually create an object file to test your design until your assembler works. Once your assembler works, if your design still has problems, you could use the assembler to create test programs that can help you expose the problems in the design.

What to hand in via T-Square:

There are two things you have to submit.

(1) A brief 1-page report (PDF). You should write this report by yourself (your partner will write his/her own report and submit it). The report should describe the approach taken, which problems were encountered and how they were fixed, and what the student's own contribution (i.e. which member of the group did what) to the project was. Note that it is fine if the two members of the group worked together (as in, sat together and got something working), and it is OK to say so in the report. If your report is missing, you will lose 50% of the points that you would otherwise earn. You should follow the following specific naming format:

SCProc[Student's Full Name].pdf (e.g. SCProcJongsePark.pdf).

(2) Quartus Project that includes Verilog files, assembler, and assembled files (ZIP file)

You should also submit zip file containing the entire Quartus project directory that includes your Verilog codes, assembler, and assembled .mif files. Your design should include a separate module for the controller of the single-cycle processor. You should name this file SCProcController.v. The project directory name and the zip file name should comply with the following naming formats:

Directory: SCProc[Student's Full Name] (e.g. SCProcJongsePark)
Zip file: SCProc[Student's Full Name].zip (e.g. SCProcJongsePark.zip)

Finally, you should submit your files through t-square.

Rules:

This project is a team project so you should work together with your teammate. The project file you submit should be the same as the one submitted by your teammate but you should write your own report by yourself (your partner will write his/her own report and submit it).