ARTUN DALYAN

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Summary: I am an enthusiastic new graduate hardware design engineer with experience in Analog and Digital Design projects and researches and working knowledge in machine learning. With my experience and knowledge, I am hoping to be part of the next major leap in technology industry.

EDUCATION

Electrical Engineering & Computer Sciences (EECS) Student at University of California, Berkeley (Class of 2020)

CourseWork

- Data Structures (CS61B), Designing Information Devices and Systems I (EE16A), Designing Information Devices and Systems II (EE16B), Machine Structures (CS61 C), The Structure and Interpretation of Computer Programs (CS61A), Microelectronic Devices and Circuits (EE105), Signals and Systems (EE120) Introduction to Robotics(EECS C106A), Introduction to Digital Design and Integrated Circuits (EECS 151) Robotic Manipulation and Interaction(EECS C106B), Introduction to Machine Learning(CS 189), Analog Integrated Circuits (EE 140)
- 3.32/4 GPA

PROJECTS

Analog Design for a Microprocessor

- Designing all analog components including 8 bit successive-approximation analog to digital converter (ADC), programmable gain switched capacitor pre-amplifier (PGA), bandgap voltage reference and Temperature sensor (BGT), Analog multiplexer (MUX) and Analog and digital voltage regulators (AREG, DREG) with a team of three using Cadence Design software. ADC and part of BGT are designed by myself. ADC is able to perform 100k samples/second with 4mV LSB.

EMG Based Control for Hand Prostheses

- Develop a pre-processing procedure to better actuate a prosthetic arm using muscle signals from the forearm of a patient with the use of Surface Electromyography (sEMG) sensors. Website: https://minabeshay.github.io/sEMG-ProjectWebsite/ As a result open-close hand motions classified with 85% accuracy.

CPU Design on FPGA

- Designing a 3-stage pipelined RISC-V CPU with a UART for tethering on Xilinx Pynq platform. On top of this CPU, audio synthesizer is implemented with PWM Controller, FIFO and a simple polyphonic subtractive synthesizer with amplitude (ADSR) envelopes.
- CPU performs 97 MHz with 1.1 CPI.

C.H.A.D. Robot

- Design and control of a Baxter robot using ROS to play Beer Pong. Website: https://chad-bot.github.io/Beer-Pong/
- Computer Vision for detecting cups, Path Planning to aim at cups and a custom end effector design helped us achieving robot functions.

Multistage Amplifier Design

- Common Source-Common Gate-Common Drain stages are connected 97.5V/V midband gain with a 3V peak-to-peak output swing and 80Hz - 350kHz bandwidth are established. BS170 NMOS transistor and BS250 PMOS transistor are used.

SIXTEEN Robot Car

- Built bottom-up a voice-controlled car using the Arduino IDE and a Texas Instruments Launchpad.
- Assembled a mic-board, built the whole circuit system, created a closed-loop feedback controlled algorithm, and used least squares to optimize the performance of the motors.
- Voice-detection and word-classification for the voice control feature are done using PCA and SVD methods.

BearMaps

- Developed the back-end of a mapping application of Berkeley using Java, Apache Maven, and images downloaded from OpenStreetMap. Created a quad tree to filter through thousands of images and raster the appropriate ones into the front end. It can handle features such as moving the screen by dragging, zooming in/out, and double clicking two points to find the shortest path. Employed A* (A star) algorithm using a priority queue to find the shortest path between two given points.

WORK AND EXPERIENCE

EECS Undergraduate Research (May 2020 - Present) Berkeley, California

- Designing a Time-to-Digital Converter Architecture for an ion analyzer with picosecond resolution using a 0.18um technology
- Ongoing project to achieve picosecond resolution for a time-of-flight chip to be used in a satellite.

T-Mobile Alternative Coverage Solutions Internship(May 2019 - August 2019) Concord, California

- Learn about 5G architecture: New antenna systems (Massive MiMo) and 5G signal processing.
- Evaluated potential venues and identify requirements for system design, including RF data collection.
- Assisted engineers with RF modeling & analyze indoor propagation and capacity.
- Applied link budget analysis, macro design, design standards, traffic analysis to help develop tools.

- Assisted engineers with troubleshooting of DAS and Small Cell systems
- Designed a RF model to improve cell coverage for an indoor venue.

IST Network Engineering Student Assistant (Starting November 2018 - Present)**Berkeley, California**

- Designing Network systems for University of California, Berkeley
- Setting up the infrastructure for network systems and configuration for network subnet and VLans.

PERSONAL

Languages

- Turkish, English - Native ; French-Professional Working Proficiency; Latin - Limited Working Proficiency

Skills

- Vivado, Cadence, Office Programs (Word, Excel, PowerPoint, Access), PID Control, ROS, Op-Amp Design Unix, Java, Python, SQL, Scheme, C, DVE, RISC-V, SPICE, Verilog, FPGA, Signal Analysis(Digital and Analog), Computer Vision, Network System Configuration, Power BI, DAX, IBwave, Machine Learning