Circuits Lab 8: Current-Mirror Differential Amplifier

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April 2025

Experiment 1: Voltage Transfer Characteristics

The objective of this experiment is to analyze the voltage transfer characteristics (VTC) of a current-mirror differential amplifier, constructed with an nMOS differential pair, two simple pMOS current mirrors, and a simple nMOS current mirror

To setup the experiment, we set up an nMOS differential pair and nMOS current mirror using ALD1106 quad nMOS transistor arrays, and our two pMOS current mirrors using an ALD1107 quad pMOS transistor array. Using a voltage divider, we set the base voltage to $V_b = 1.2$ volts, giving us a moderate to strong inversion with a base current measured to be $I_b \approx 165$ microamps.

To create our Voltage Transfer Characteristic, we used a voltage divider to hold V_2 (the inverting input) constant while sweeping V_1 (the non-inverting input) from 0 to 5 volts. We repeated this experiment three times, for three different values of V_2: $V_2 = 2.5$, 3.5, and 4.5 volts. While controlling our inputs, we measured the output voltage, V_{out}. Our results can be seen in **Figure 1**.

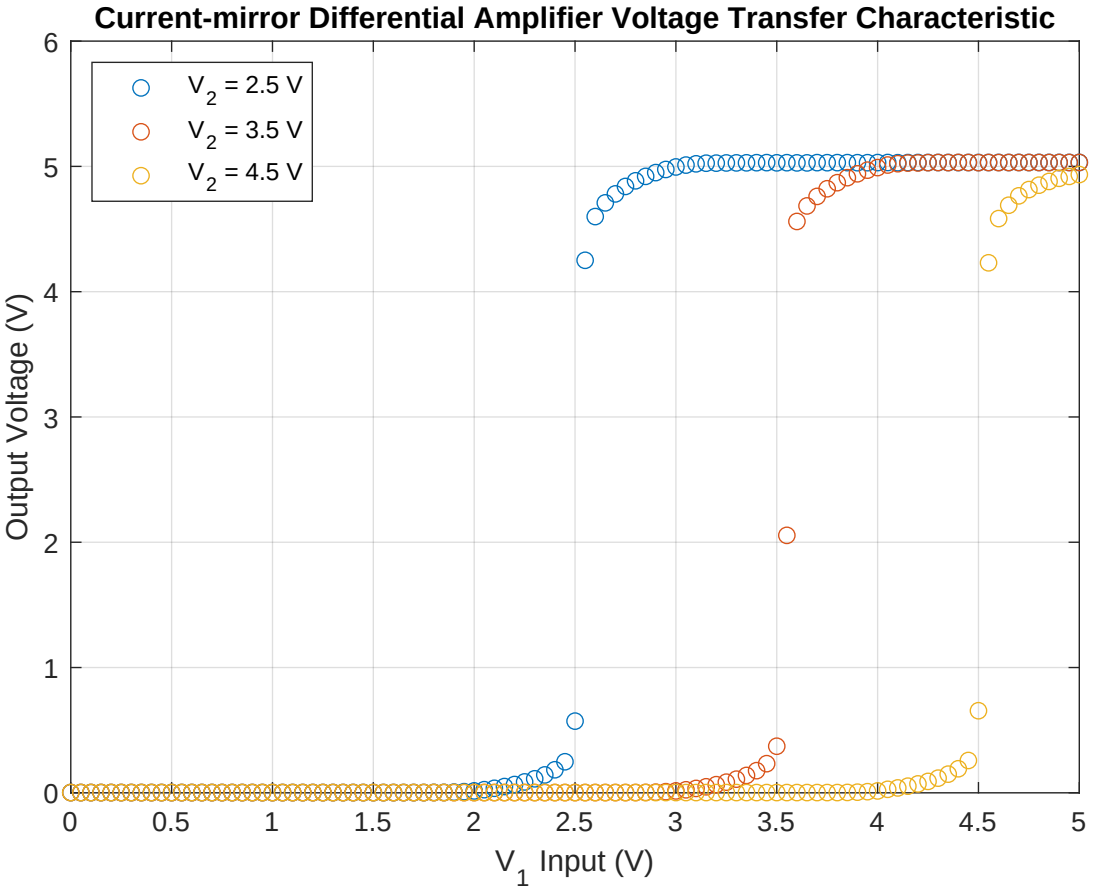

Figure 1: A plot of the input and output voltage of the nMOS current-mirror differential amplifier, also known as a Voltage Transfer Characteristic. The input voltage is swept over V_1 while V_2 is held constant at three different values.

To further analyze our data, we can compare the VTC of our nMOS current-mirror differential amplifier to the VTC of our nMOS differential amplifier from Lab 7.

In Lab 7, the output voltage of the nMOS differential amplifier remained at 0V until $V_1 = V_{in}$ was around 0.6 volts, the turn-on voltage. Then, it began to increase linearly until $V_1 > V_2$, at which point it would jump and saturate at the top rail. However, in **Figure 1**, we can see that the output voltage remains at 0V, until $V_1 > V_2$, at which point it also jumps and saturates at the top rail.

These differences can be explained by the two additional current mirrors, which allow us to pull down V_{out} to ground with the nMOS current-mirror differential amplifier, whereas V_{out} in Lab 7 was not tied to ground.

Experiment 2: Transconductance, Resistance, and Gain

In Experiment 2, our goal is to calculate the incremental output resistance, incremental transconductance gain, and differential-mode voltage gain of our current-mirror differential amplifier.

Note: for Experiment 2, we kept the bias voltage at 1.2 volts, meaning we are operating above

threshold with a moderate to strong inversion for each of the different parts of Experiment 2.

For the first part of part of Experiment 2, we aimed to determine the differential-mode voltage gain directly from our nMOS current-mirror differential amplifier. To do this, we held V_2 at 3.5 volts using a voltage divider and swept around $V_{dm} = V_1 - V_2$ while measuring V_{out}. Our results are shown in **Figure 2.**

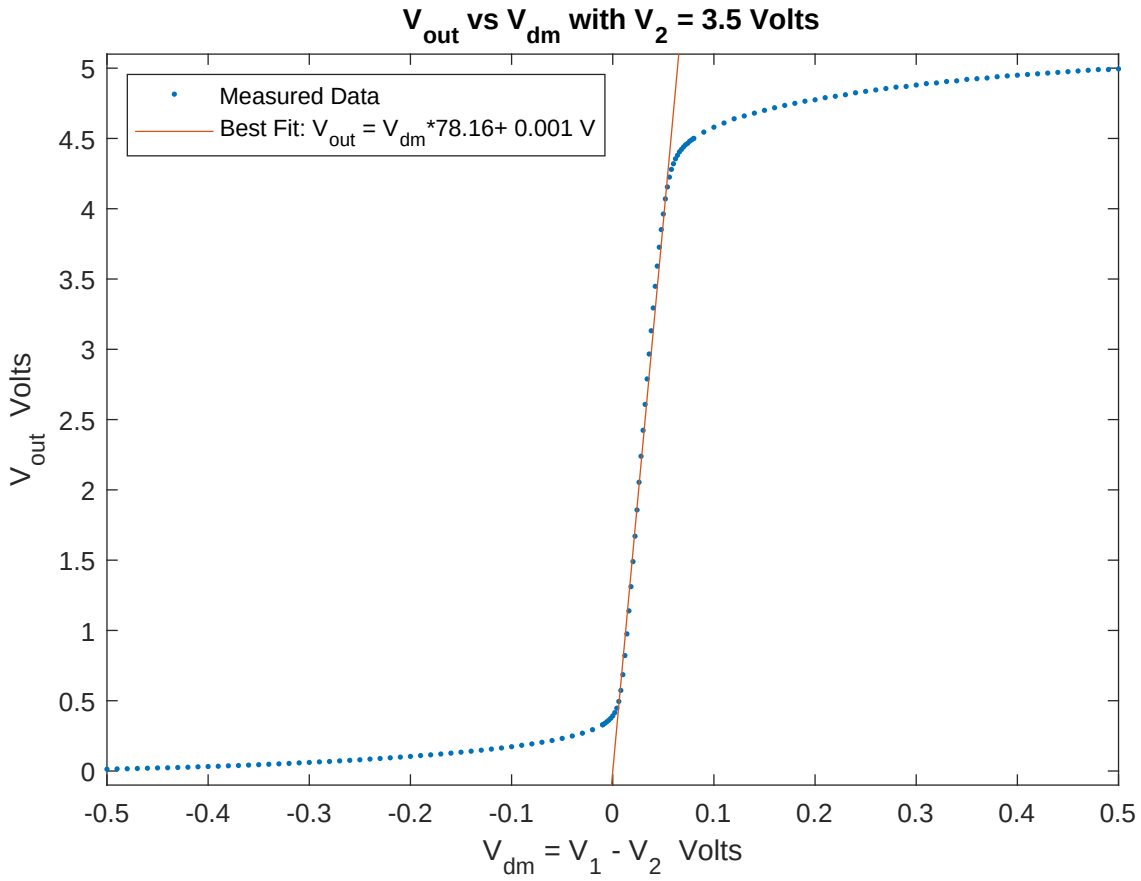

Figure 2: Plot of V_{dm} vs V_{out} with $V_2 = 3.5$ volts for our nMOS current-mirror differential amplifier. The line of best fit is around the steepest slope, $V_{dm} = 0$, which corresponds to the highest differential-mode voltage gain.

As we can see from **Figure 3**, differential-mode voltage gain when $V_{dm} \approx 0$ is ≈ 78. This is the steepest slope, which corresponds to the highest gain.

Next, we want to calculate the incremental output resistance. To do so, we set V_{dm} to zero volts and swept over V_{out} while measuring I_{out}. Since $V_{dm} = 0$, we know the voltage gain will be high and I_{out} will be zero as long as M2 and M4 are saturated. The slope of this graph will allow us to calculate the incremental output resistance, $R_{out} = \frac{\delta V_{out}}{\delta I_{out}}$. Our results for this experiment are shown in **Figure 3**.

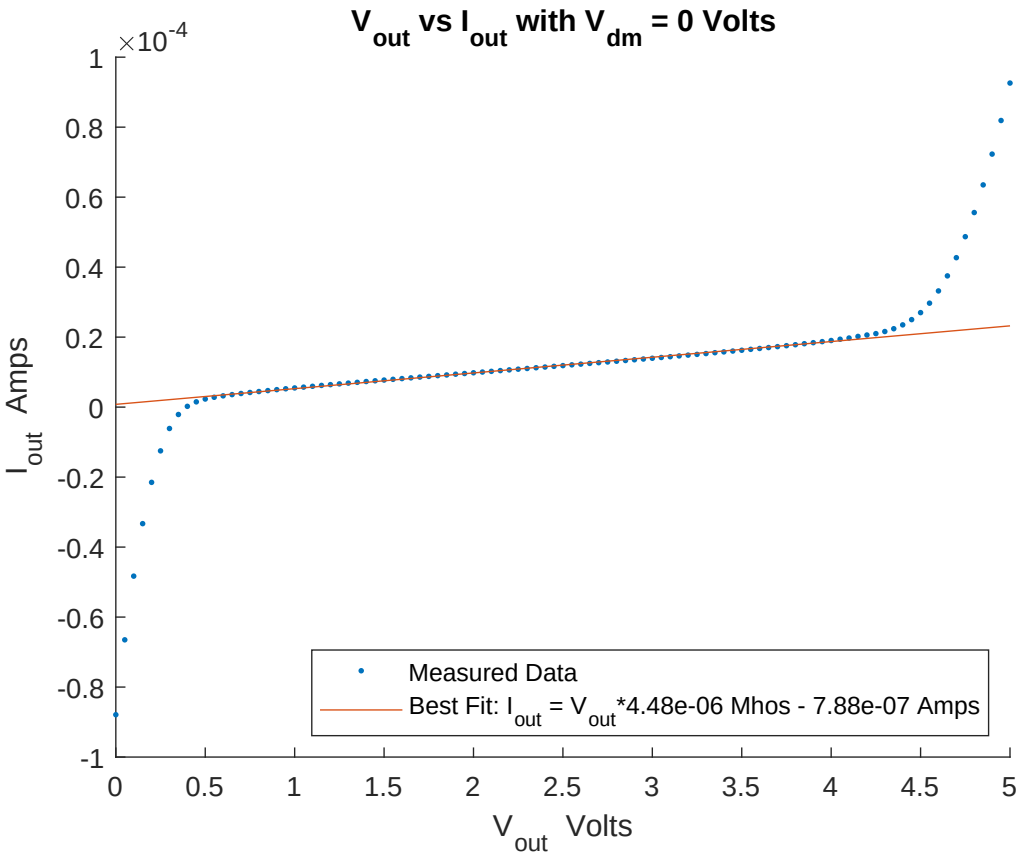

Figure 3: Plot of V_{out} vs I_{out} with V_{dm} held at zero volts for our nMOS current-mirror differential amplifier. Our line of best fit is fit to the "shallow" part of the curve, where $I_{out} \approx 0$ and M2 and M4 are saturated.

As we can see in the graph, $I_{out} \approx 0$ between $V_{out} = 0.6$ volts and $V_{out} = 4.3$ volts. This is the range of voltages (of V_{out}) where the gain of the circuit is large (as long as $V_{dm} = 0$).

From the slope of our best fit line, we can also determine our incremental output resistance, R_{out}

$$\text{Given: } \frac{\delta I_{out}}{\delta V_{out}} = 4.48e-6 \text{ Mhos} \rightarrow R_{out} = \frac{\delta V_{out}}{\delta I_{out}} = \frac{1}{4.48e-6} = 223.2\text{k}\Omega$$

to be 223.2kΩ.

For the next part of Experiment 2, we want to calculate the incremental transconductance gain. To do this, we fixed V_{out} at 2.5 volts, where we know the gain is high from referencing **Figure 3**. Then, we measured I_{out} as we swept V_{dm}. We can then extract G_{dm} from the slope of the line, as $G_{dm} = \frac{\delta I_{out}}{\delta V_{dm}}$. Our results are shown in **Figure 4**.

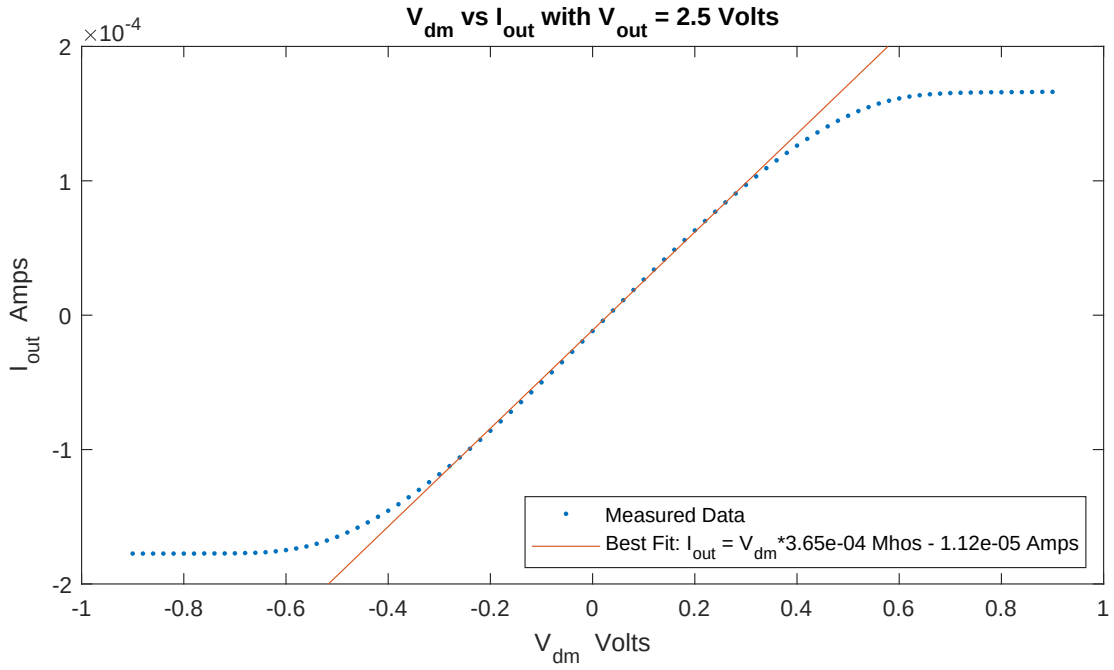

Figure 4: Plot of I_{out} over V_{dm} with V_{out} held at 2.5 volts for our nMOS current-mirror differential amplifier. Our line of best fit is fit around $V_{dm} = 0$, the flattest part of our curve.

From **Figure 4** can directly extract our incremental transconductance gain from the slope of our line of best fit as:

$$G_{dm} = \frac{\delta I_{out}}{\delta V_{dm}} = 3.65e-4 \text{ Mhos}$$

Additionally, we can see that I_{out} saturates when $V_{dm} < -0.6$ V or $V_{dm} > 0.6$ V. When it saturates, it saturates at approximately the bias current, $I_b \approx 165$ microamps. The lower limit for I_{out} is $I_{out} \approx -175$ microamps, while the upper limit is $I_{out} \approx 166$ microamps.

Lastly, using our measured incremental output resistance, R_{out}, and measured incremental transconductance gain, G_{dm}, we can calculate our differential-mode voltage gain when $V_{dm} = 0$ (where the gain is highest). We can use the formula:

$$A_{dm} = \frac{\delta V_{out}}{\delta V_{dm}} = \frac{\delta V_{out}}{\delta I_{out}} \cdot \frac{\delta I_{out}}{\delta V_{dm}} = R_{out} \cdot G_{dm} = 223.2 \text{ k}\Omega \cdot 3.65e-4 \text{ Mhos} \approx 81$$

Our calculated gain is ≈ 81, while our measured gain is ≈ 78. These values are very close to each other, and the difference between them is likely explained by our data selection when calculating the lines of best fits.

Compared to the differential-mode voltage gain we calculated in Lab 7 for our simple nMOS differential amplifier (≈ 53 measured, ≈ 47 calculated) our gain for the nMOS current-mirror differential amplifier is much higher. As explained in experiment 1, these differences can be explained by the two additional current mirrors, which allow us to pull down Vout to ground with the nMOS current-mirror differential amplifier, whereas Vout in Lab 7 was not tied to ground.

Experiment 3: Unity-Gain Follower Step Response

We begin this experiment by configuring the amplifier as a unity-gain follower. We connected the output to the inverting input. Additionally, we loaded the output of the amplifier with a 1nF capacitor. We will input different square waves in order to see the response to small and large signals.

The output does not track linearly since there is exponential growth and decay. The measured time constant for the growth (up-going) portion of the response is $2.97e-06$, while the measured time constant for the decay (down-going) portion of the response is $2.73e-06$. The response appears to mostly be symmetrical. The time constants are slightly different but within the scope of the experiment are very close, and the behavior for down-going and up-going portions mirror each other. You can calculate a theoretical time constant using the load capacitance and the differential-mode transconductance gain found in Experiment 2. The relation is given:

$$\tau = \frac{C_{load}}{g_m}$$

We used a capacitor of 1nF, or $1e-09$ F, and the calculated differential-mode transconductance gain was found to be $3.65e-4$ Mhos. That gives us a calculated time constant of $2.7397e-06$, which is very close to the actual measured time constants.

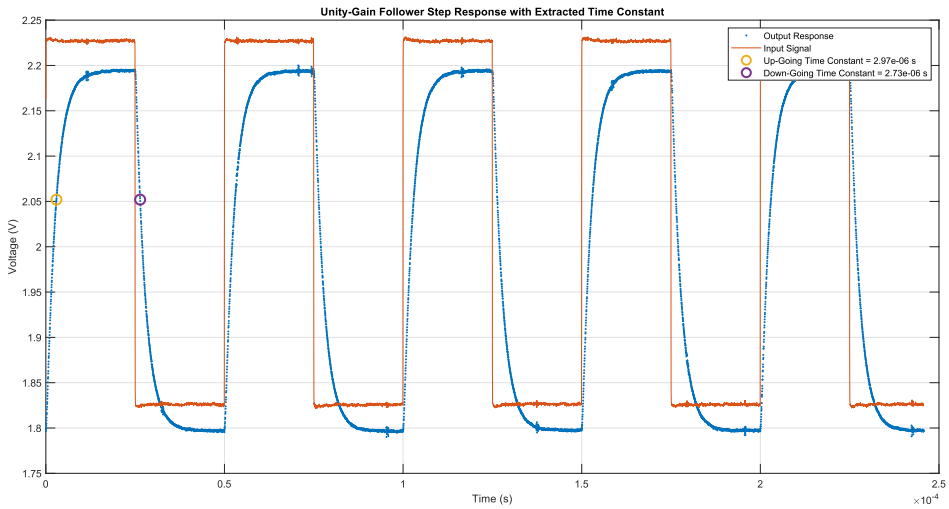

Figure 5: A plot of the Unity-Gain Follower Step Response with a capacitor connected to ground. The input is a square signal, and we measure the output voltage across the capacitor. We can extract the time constants by calculating the time period needed for the voltage to climb 63% or fall down to 37% of the maximum voltage.

For the second part of the experiment, we increased the amplitude of the square wave to 2V, and then raised the DC offset to 2.5V in order to keep the transistor pair in saturation, and adjusted the frequency of the square wave. The response also appears symmetrical. There is a slight difference between the slew rates, but again, within the scope of the project, they are incredibly close. We noted some slewing occurring in the response. By fitting lines to the response, we get measured slew rates of 158590 and 155200 V/S.

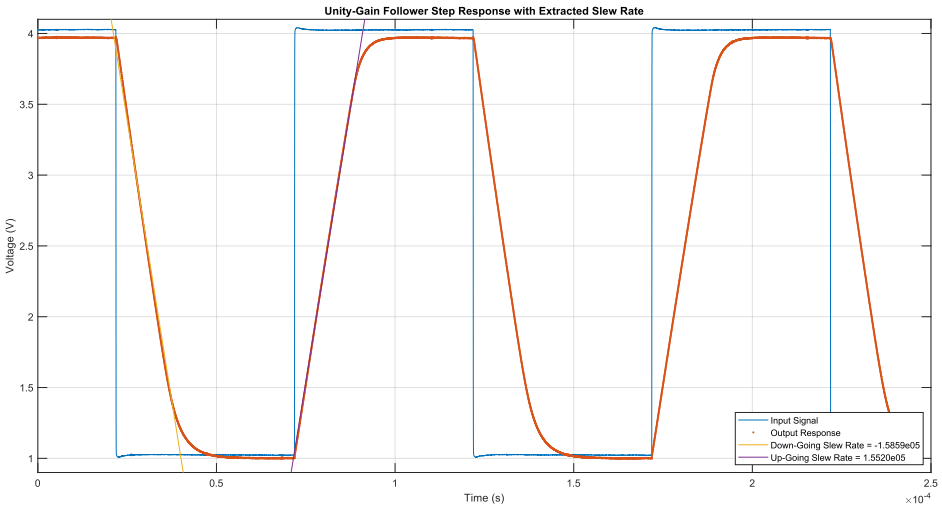

Figure 6: A plot of the Unity-Gain Follower Step Response with a capacitor connected to ground. The input is a square signal, and we measure the output voltage across the capacitor. We can extract the slew rate by taking the slope of the falling and climbing responses.

To calculate a theoretical slew rate, we can take the relation between the maximum output current I_{max} and the load capacitance C_{load},

$$SR = \frac{I_{max}}{C_{load}}$$

Given the maximum output current calculated in Experiment 2 of 166 microamps, and a measured capacitance of 1nF, we get a theoretical slew rate value of 166000 V/S, pretty close to the measured values of 157590 and 155200 V/S.