Circuits Lab 7: A Simple MOS Differential Amplifier

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Experiment 1: Voltage Transfer Characteristics

The objective of this experiment is to analyze the voltage transfer characteristics (VTC) of a differential amplifier with an nMOS differential pair and a pMOS current mirror. The response of the amplifier is examined under different common-mode input voltages and differential-mode input voltages, comparing the behavior in weak/moderate inversion (just at threshold) and strong inversion (above threshold).

To setup the experiment, we need to set up an nMOS differential pair using an ALD1106 quad nMOS transistor array and a pMOS current mirror using an ALD1107 quad pMOS transistor array. We are be able to manually sweep over the differential-mode input voltages.

Part A: At Threshold Bias Current

For the first part of the experiment, we set the bias voltage so the bias current is just at threshold, which meant setting the bias voltage to 0.7 volts using a voltage divider. This sets the bias current to ≈ 1 micro amp.

In order to sweep the differential-mode input voltages, we connected V_2 to a constant voltage source and swept V_1 from 0 to 5 volts. We swept over different values of V_2 as well, running the experiment with V_2 held constant at 2.5, 3.5, and 4.5 volts. Upon sweeping the input voltage, we measured the output voltage, located on the right side between the differential amplifier and the current mirror.

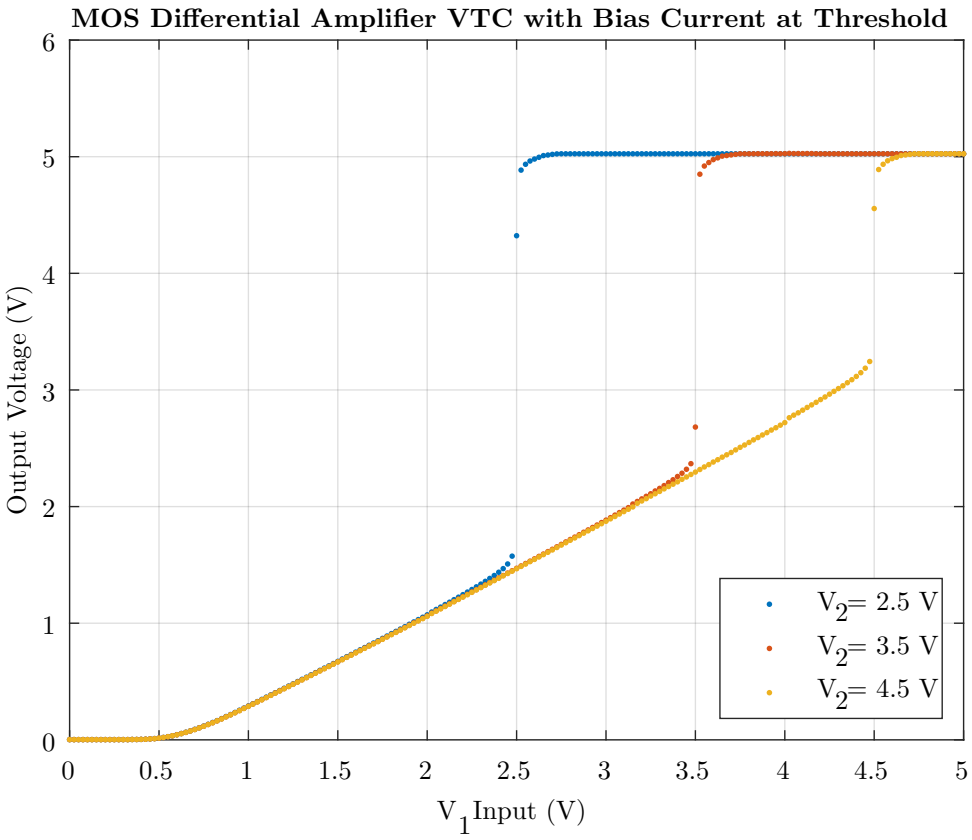

Figure 1: A plot of the input and output voltage of the MOS differential amplifier with bias current held at threshold. The input voltage is swept over V_1 while V_2 is held constant at different values.

Part B: Above Threshold Bias Current

For the second part of the experiment, we repeated the experiment, but made one small change: setting the bias current above the threshold, which meant setting the bias voltage to 1.4 volts. This sets the bias current to ≈ 100 micro amps.

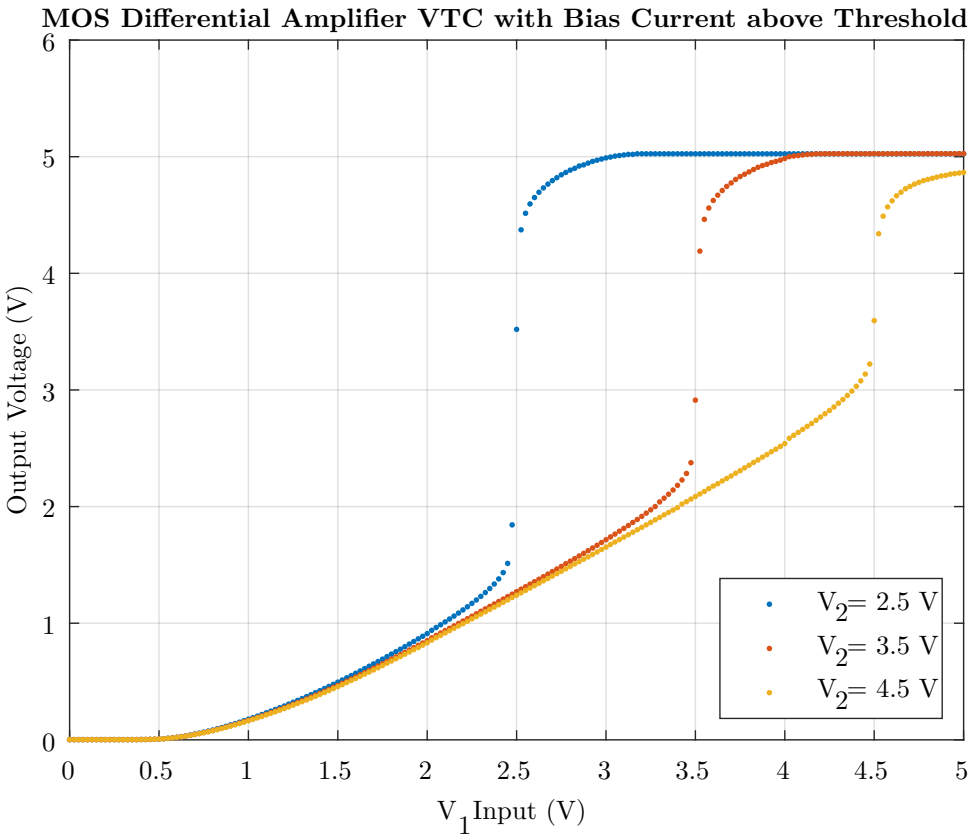

Figure 2: A plot of the input and output voltage of the MOS differential amplifier with bias current held above threshold. The input voltage is swept over V_1 while V_2 is held constant at different values.

Overall, the behavior of the circuit does not differ greatly between when held in moderate or strong inversion. The transition is slightly more smooth and gradual while held in strong inversion (above threshold), but the general behavior is consistent throughout the experiments.

Experiment 2: Transconductance, Resistance, and Gain

In Experiment 2, our goal is to calculate the incremental output resistance, incremental transconductance gain, and differential-mode voltage gain.

Note: for Experiment 2, we set the bias voltage to 1.2 volts, meaning we are operating above threshold for each of the different parts of Experiment 2.

For the first part of part of Experiment 2, we aimed to determine the differential-mode voltage gain directly from our MOS differential amplifier. To do this, we held V_2 at 3.5 Volts using a voltage divider and swept around $V_{dm} = V_1 - V_2$ while measuring V_{out}. Our results are shown in **Figure 3.**

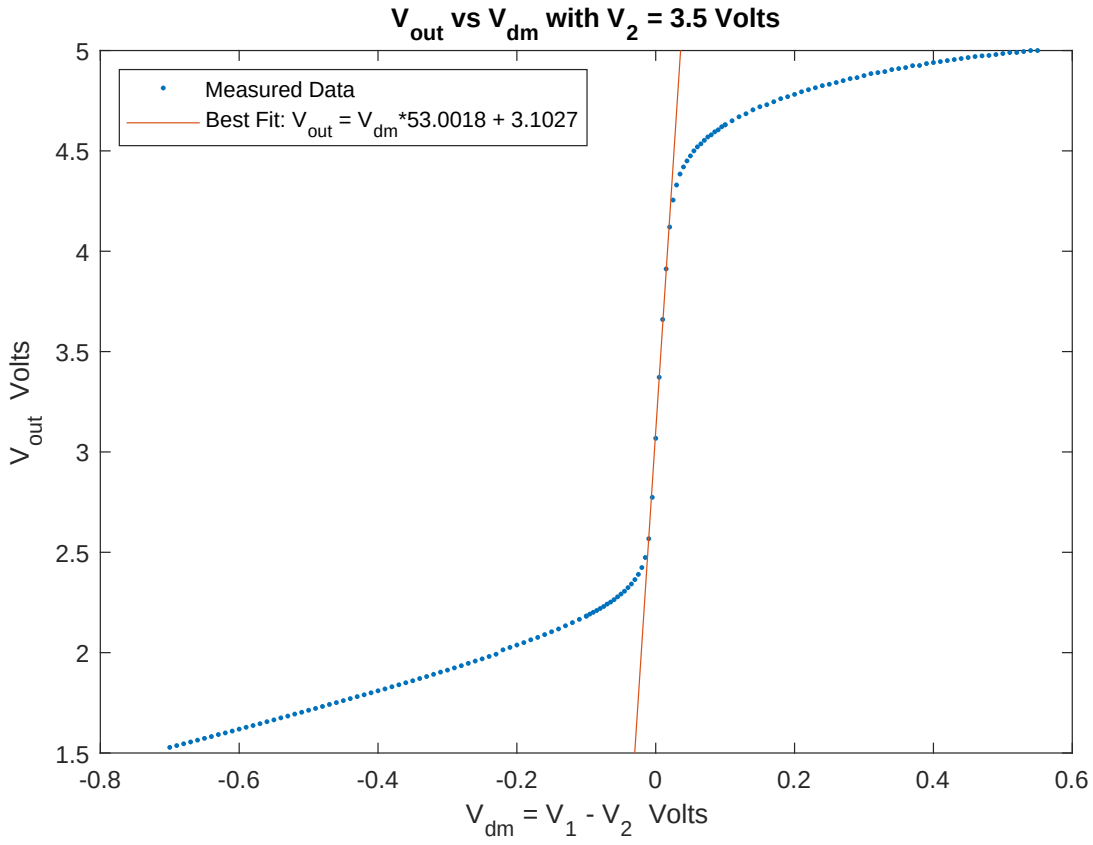

Figure 3: Plot of V_{dm} vs V_{out} with $V_2 = 3.5$ volts for our MOS Differential Amplifier. The line of best fit is around the steepest slope, $V_{dm} = 0$, which corresponds to the highest differential-mode voltage gain.

As we can see from **Figure 3**, differential-mode voltage gain when $V_{dm} \approx 0$ is around 53. This is the steepest slope, which corresponds to the highest voltage gain at $V_{dm} = 0$.

Next, we want to calculate the incremental output resistance. We set V_{dm} to zero volts and swept over V_{out} while measuring I_{out}. Since $V_{dm} = 0$, we can estimate the gain to be high and I_{out} to be zero as long as M2 and M4 are saturated. The slope of this graph will allow us to calculate the incremental output resistance, $R_{out} = \frac{\delta V_{out}}{\delta I_{out}}$. Our results for this experiment are shown in **Figure 4**.

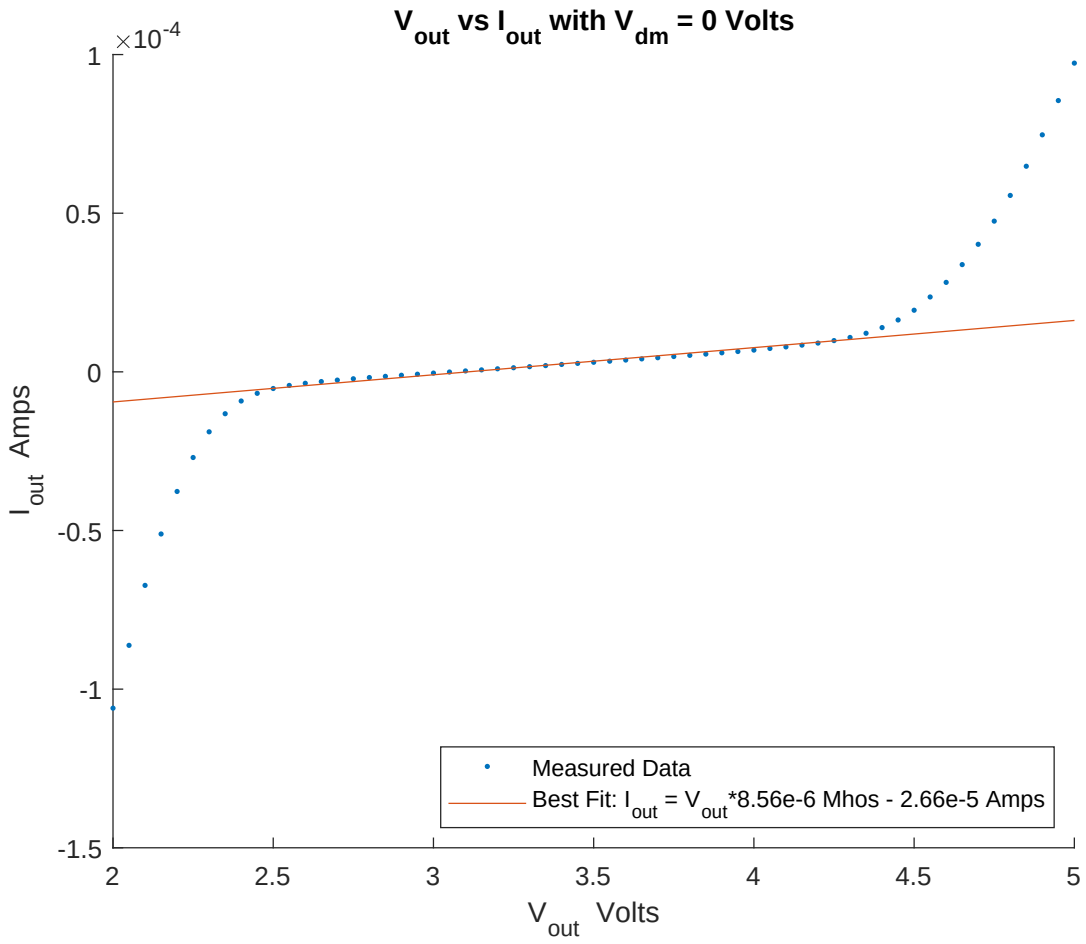

Figure 4: Plot of V_{out} vs I_{out} with V_{dm} held at zero volts for our MOS Differential Amplifier. Our line of best fit is fit to the "shallow" part of the curve, where $I_{out} \approx 0$ and M2 and M4 are saturated.

As we can see in the graph, $I_{out} \approx 0$ between $V_{out} = 2.5$ volts and $V_{out} = 4.5$ volts. This is the range of voltages (of V_{out}) where the gain of the circuit is large (as long as $V_{dm} = 0$.

From the slope of our best fit line, we can also determine our incremental output resistance, R_{out}

$$\text{Given: } \frac{\delta I_{out}}{\delta V_{out}} = 8.56e-6 \text{ Mhos} \rightarrow R_{out} = \frac{\delta V_{out}}{\delta I_{out}} = \frac{1}{8.56e-6} = 116.8\text{k}\Omega$$

to be 116.8kΩ.

For the next part of Experiment 2, we want to calculate the incremental transconductance gain. To do this, we fixed V_{out} at 3.5 volts, where we know the gain is high. Then, we measured I_{out} as we swept V_{dm}. We can then extract G_{dm} from the slope of the line, as $G_{dm} = \frac{\delta I_{out}}{\delta V_{dm}}$. Our results are shown in **Figure 5**.

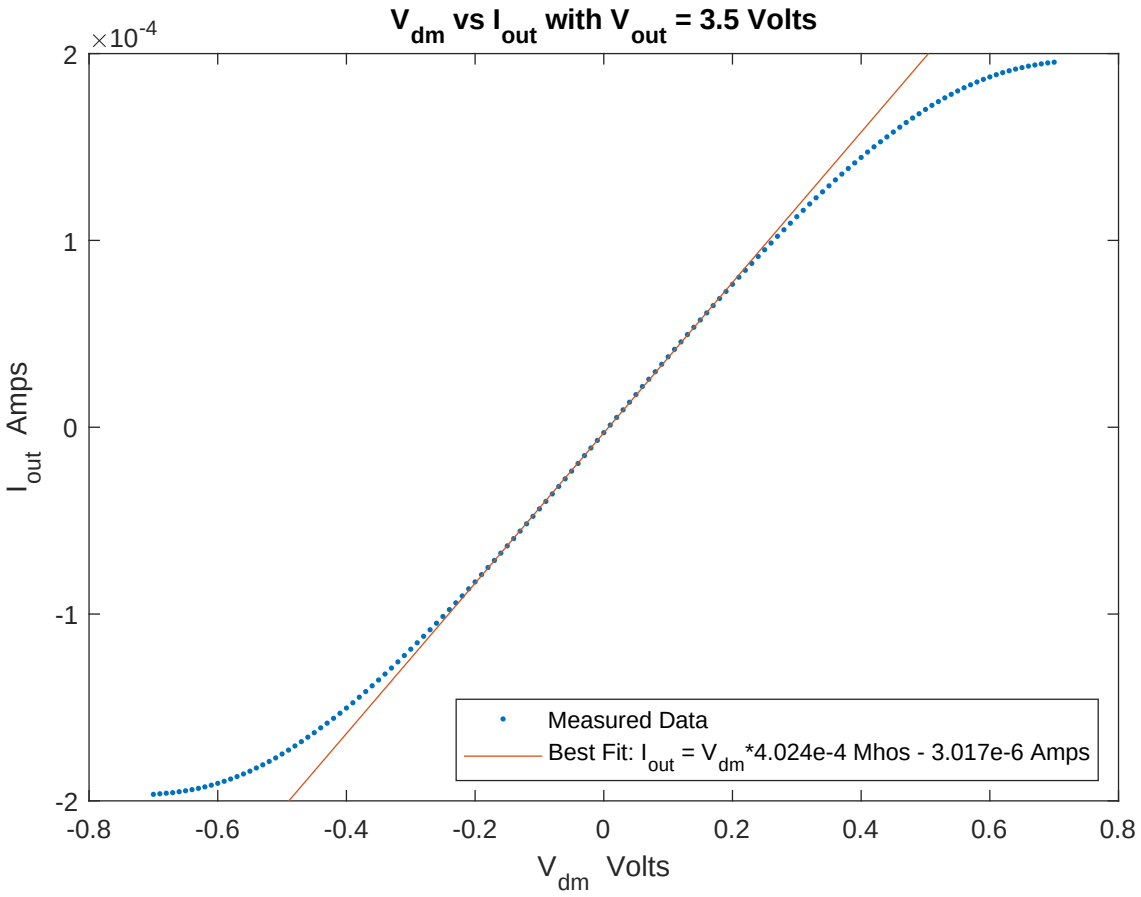

Figure 5: Plot of I_{out} over V_{dm} with V_{out} held at 3.5 volts for our MOS Differential Amplifier. Our line of best fit is fit around $V_{dm} = 0$, the flattest part of our curve.

From **Figure 5** can directly extract our incremental transconductance gain from the slope of our line of best fit as:

$$G_{dm} = \frac{\delta I_{out}}{\delta V_{dm}} = 4.024e-4 \text{ Mhos}$$

Lastly, using out measured incremental output resistance, R_{out}, and incremental transconductance gain, G_{dm}, we can calculate our differential-mode voltage gain when $V_{out} = 3.5$ and $V_{dm} = 0$ (where the gain is highest). We can use the formula:

$$A_{dm} = \frac{\delta V_{out}}{\delta V_{dm}} = \frac{\delta V_{out}}{\delta I_{out}} \cdot \frac{\delta I_{out}}{\delta V_{dm}} = R_{out} \cdot G_{dm} = 116.8 \text{ k}\Omega \cdot 4.024e-4 \text{ Mhos} \approx 47$$

Our calculated gain is ≈ 47, while our measured gain is ≈ 53. These values are very close to each other, and the difference between them is likely explained by our data selection when calculating the lines of best fits.

Experiment 3: Unity-Gain Follower

In this experiment, we configured the differential amplifier to act as a unity-gain follower. A unity-gain follower (also known as a unity-gain amplifier or buffer) is an op-amp circuit which has a voltage gain of 1. They are important to many circuits because they draw very little current and thus, don't

disturb the original circuits they are drawing power from. They can act as "isolation buffers".

To configure this circuit, we connected the output to the inverting input terminal, which we determined in the prelab to be V_2. That means that the input to the circuit is V_1. To measure the behavior of the unity-gain follower circuit, we swept over V_1 as the input and measured the output of the circuit. After measuring the VTC, we created a linear best-fit line to determine the incremental gain, which is the slope of the plot (the ratio of $\frac{V_{out}}{V_{in}}$). The goal is to measure the voltage transfer characteristic (VTC) and verify that the incremental gain is close to unity.

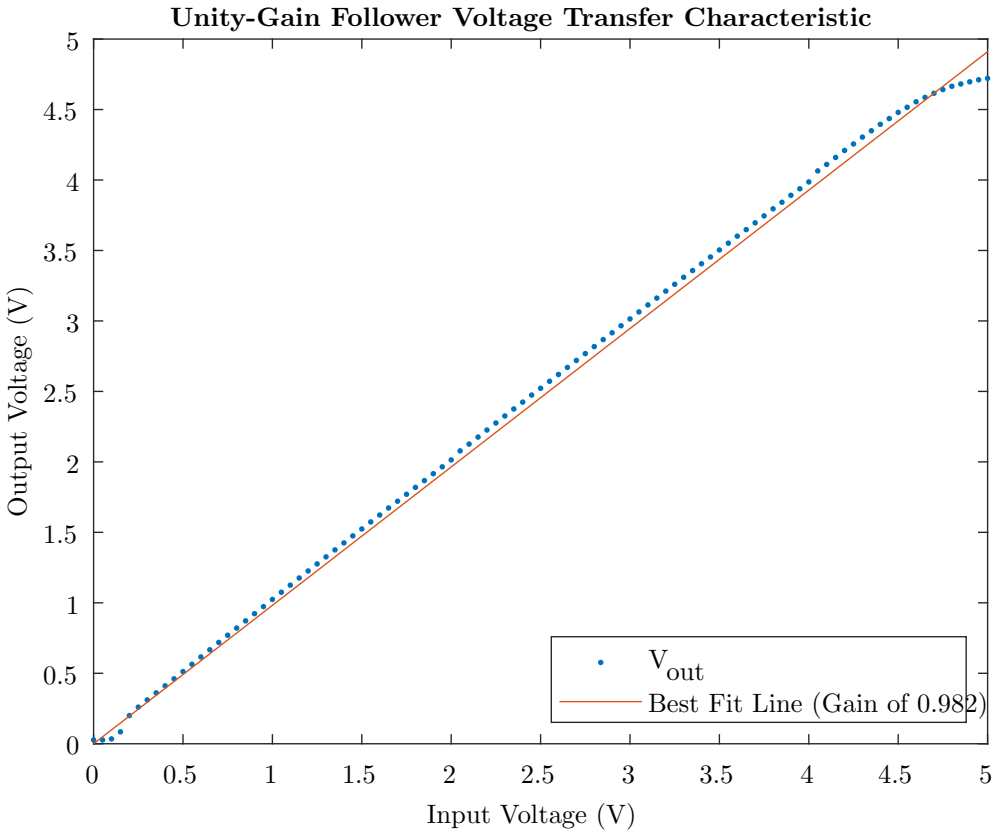

Figure 6: A plot of the input and output voltage of the unity-gain follower circuit.

The plot of V_{out} vs V_{in} showed a nearly linear relationship, which is expected for a unity-gain follower. The slope of the best-fit line was found to be around 0.982, which confirms that the circuit operates close to unity gain.