Circuits Lab 6: The MOS Differential Pair

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Experiment 1: Differential Pair I-V Characteristics

Part A: Below Threshold Bias Current

In this lab, we will examine the current–voltage characteristics of a MOS differential pair, which is widely used as an input stage in operational amplifiers and in many other types of circuits as well.

For the first step of our experiment, we used 3 nMOS transistors from a ALD1106 quad nMOS transistor array to create a nMOS Differential Pair. Using the SMU, we connected ground to pin 4 and $V_{dd} = 5V$ to pin 11 to ensure the array would be working properly.

In constructing our nMOS differential pair, we set the bias voltage, Vb, at 0.50 V, a value obtained from Lab 5 **Figure 1** to make the bias current just below threshold ($I_b \approx 1\mu A$). We did this using a voltage divider from our 5V rail to ground and equivalent resistors valued at $4.5k\Omega$ and $0.5k\Omega$:

$$5V \cdot \frac{0.5k\Omega}{4.5k\Omega + 0.5k\Omega} = 0.5V$$

Additionally, we set up a voltage divider to supply constant voltages of $4.5V$, $3.5V$, or $2.5V$ to V_2.

Lastly, for V_1, we swept across $V_{dm} = V_1 - V_2$ from $-500mv$ to $500mv$. Since V2 is held at a constant voltage, this is the same as sweeping V_1 from five tenths of a volt below V_2 to five tenths of a volt above V_2.

We swept across V_{dm} three times, measuring each of the output currents, I_1 and I_2, and the common-source node voltage across the three different sweeps. Then, we repeated these measurements for our two additional values of V_2, 3.5 and 2.5 volts.

To analyze our results, we plotted I_1, I_2, $I_1 - I_2$, and $I_1 + I_2$ as we swept across V_{dm}. Our results can be seen in **Figure 1**.

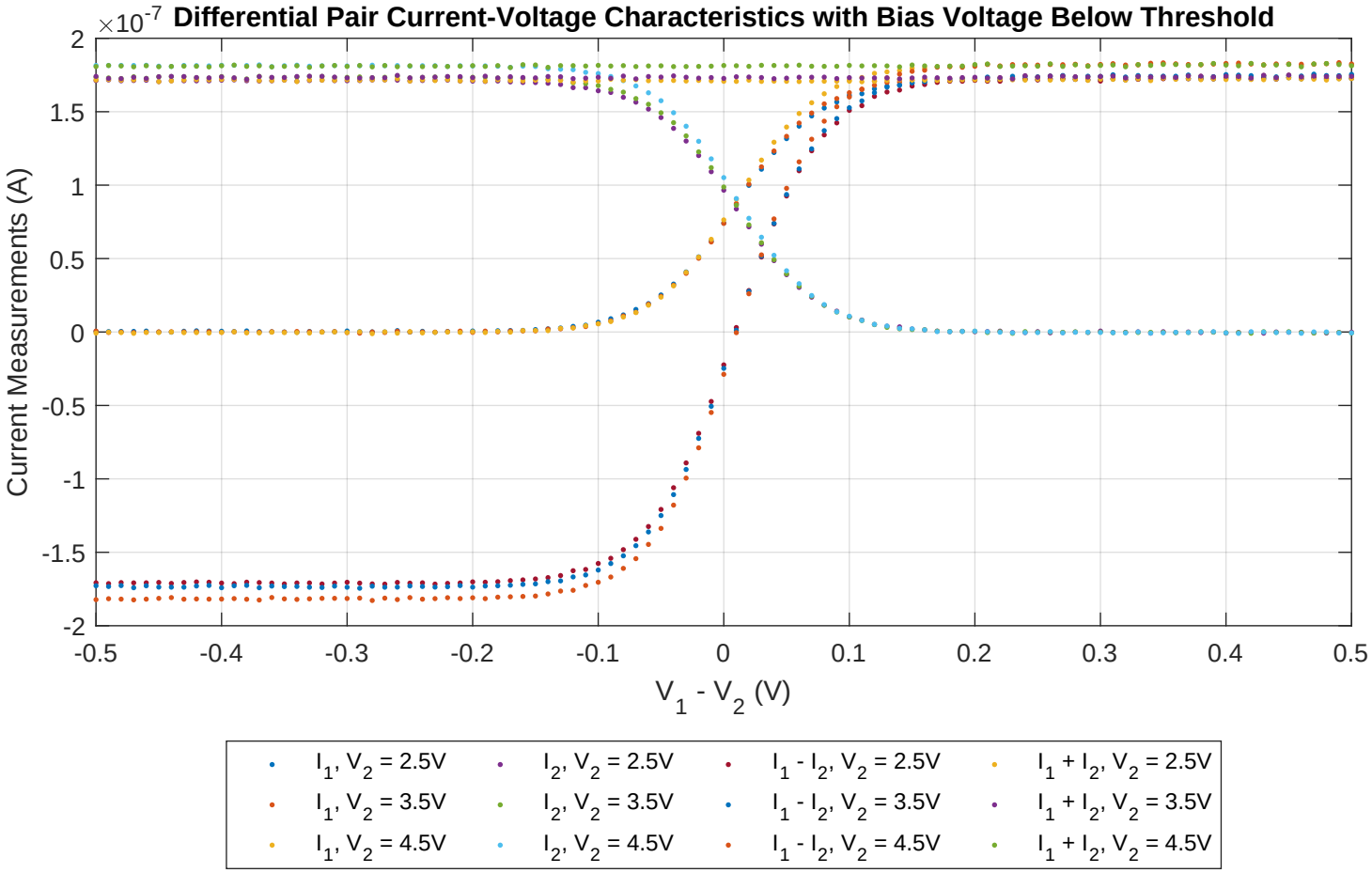

Figure 1: Measurements for I_1, I_2, $I_1 - I_2$, and $I_1 + I_2$ of an nMOS Differential Pair with a bias current BELOW threshold, for each of our three values of V_2. We used our SMU to sweep V_{dm} from $-500mv$ to $500mv$.

As seen in the plots, these measurements do not change significantly as V_2 changes. However, they *do* change significantly as we sweep from below V_2 to above V_2.

Next, we wanted to analyze the common-source node voltage, V , as a function of $V_{dm} = V_1 - V_2$ for all three values of V_2. This can be seen in **Figure 2**.

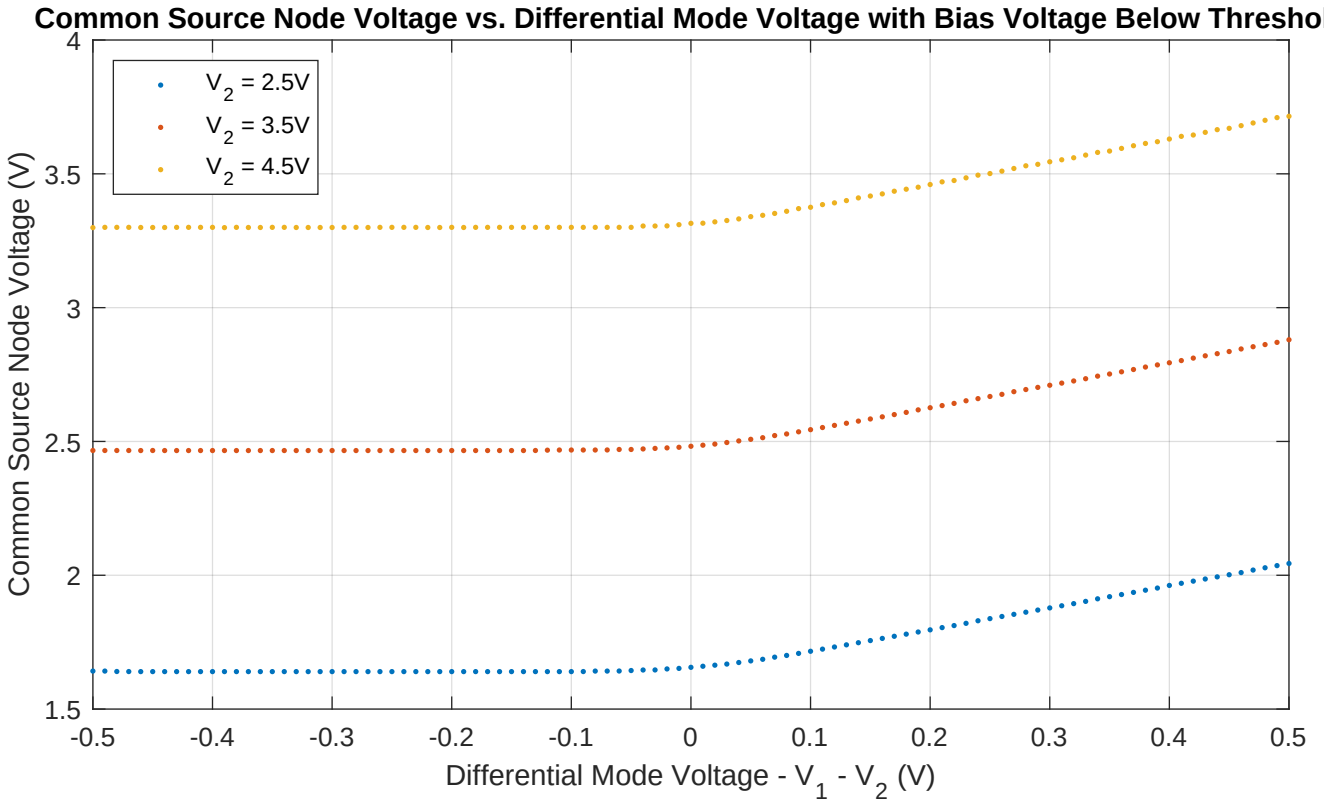

Figure 2: Common Source Node Voltage vs. Differential Mode Voltage of an nMOS Differential Pair with a BELOW threshold bias current swept from $-500mv$ to $500mv$ below/above V_2.

When V_1 is below V_2, we see that V is roughly equivalent to V_2. However, as V_1 rises above V_2, we notice V shift so that V is roughly equivalent to V_1. This matches with what we derived in the prelab for an nMOS differential pair:

$$V = \kappa(max(V_1, V_2) - V_b)$$

where V is dependent on V_1 OR V_2, whichever is bigger.

Lastly, for each of the three values of V_2 that we used, we fit a straight line to the plot of $I_1 - I_2$ as a function of $V_{dm} = V_1 - V_2$ around the region where $V_1 \approx V_2$ (i.e., around where $V_1 - V_2 \approx 0V$). The slope of this line is approximately equal to the (incremental) differential-mode transconductance gain of the differential pair, which is formally given by:

$$G_{dm} = \frac{\delta I_{dm}}{\delta V_{dm}}\bigg|_{V_{dm}=0V} = \frac{\delta I_1 - I_2}{\delta V_1 - V_2}\bigg|_{V_1=V_2}$$

We can estimate the differential-mode transconductance gain by examining the slope of $I_1 - I_2$ as a function of $V_{dm} = V_1 - V_2$, as shown in **Figure 3**.

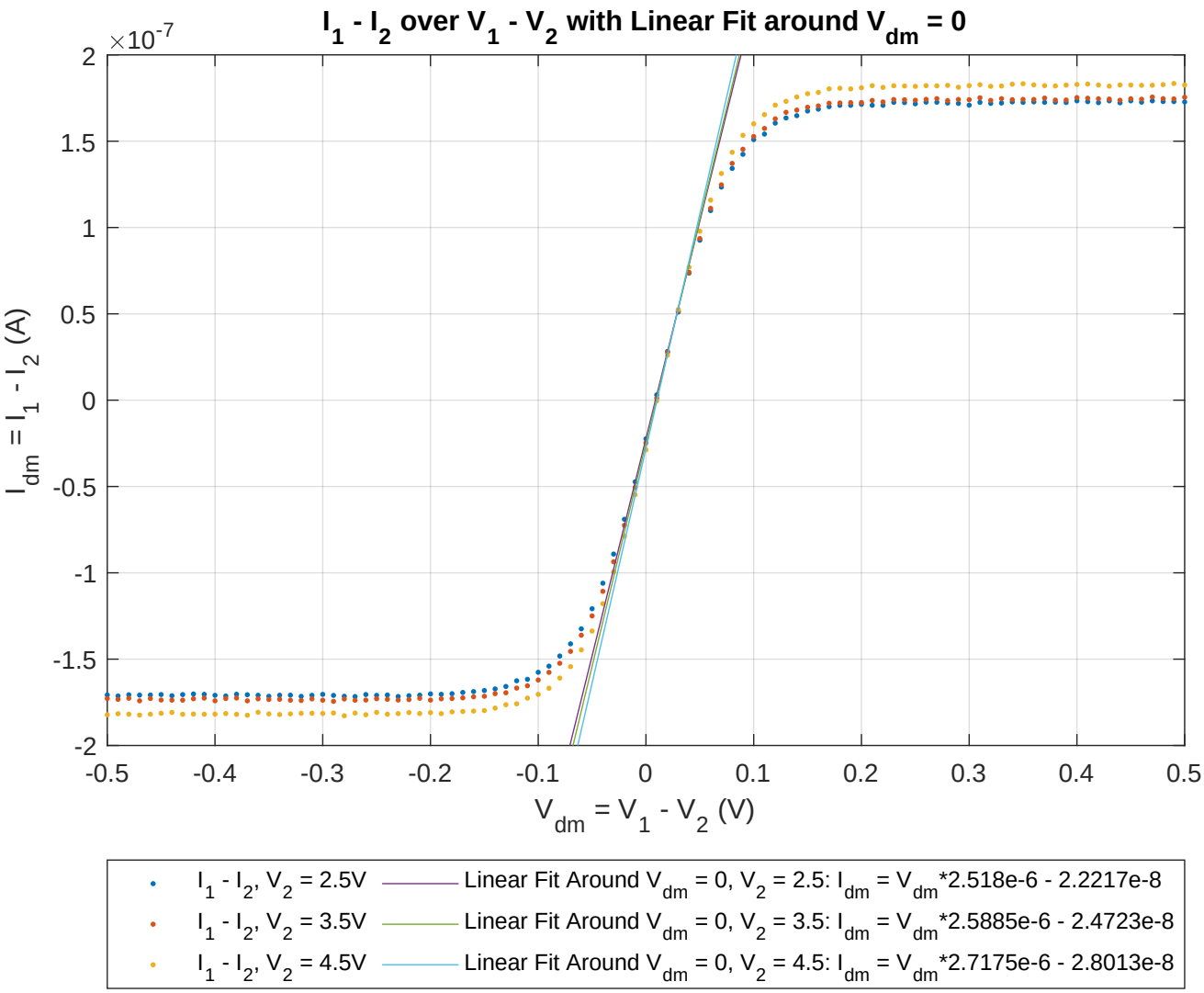

Figure 3: Measurements for $I_1 - I_2$ against V_{dm} of an nMOS Differential Pair, with a BELOW threshold bias current, for each of our three values of V_2. We used our SMU to sweep V_{dm} from $-500mv$ to $500mv$. We have also included the differential-mode transconductance gains, which are the slopes of the best fit lines near $V_{dm} = 0$.

While the the differential-mode transconductance gain does change slightly with different values of V_2, it does not change significantly. The lowest slope is $2.5180e-6$ mhos, while the highest is $2.7175e-6$ mhos.

Part B: Above Threshold Bias Current

For the second part of Experiment 1, we raised our bias current to be above threshold ($I_b \approx 100\mu A$) by raising our bias voltage to be around $1.2V$ using a voltage divider. Then, we repeated the same experiments as we did with the below threshold current using the same values of V_2, $4.5V$, $3.5V$, and $2.5V$

First, we swept across V_{dm} three times, measuring each of the output currents, I_1 and I_2, and the

common-source node voltage across the three different sweeps. Then, we repeated these measurements for our two additional values of V_2, 3.5 and 2.5 volts.

To analyze our results, we plotted I_1, I_2, $I_1 - I_2$, and $I_1 + I_2$ as we swept across V_{dm}. Our results can be seen in **Figure 4**.

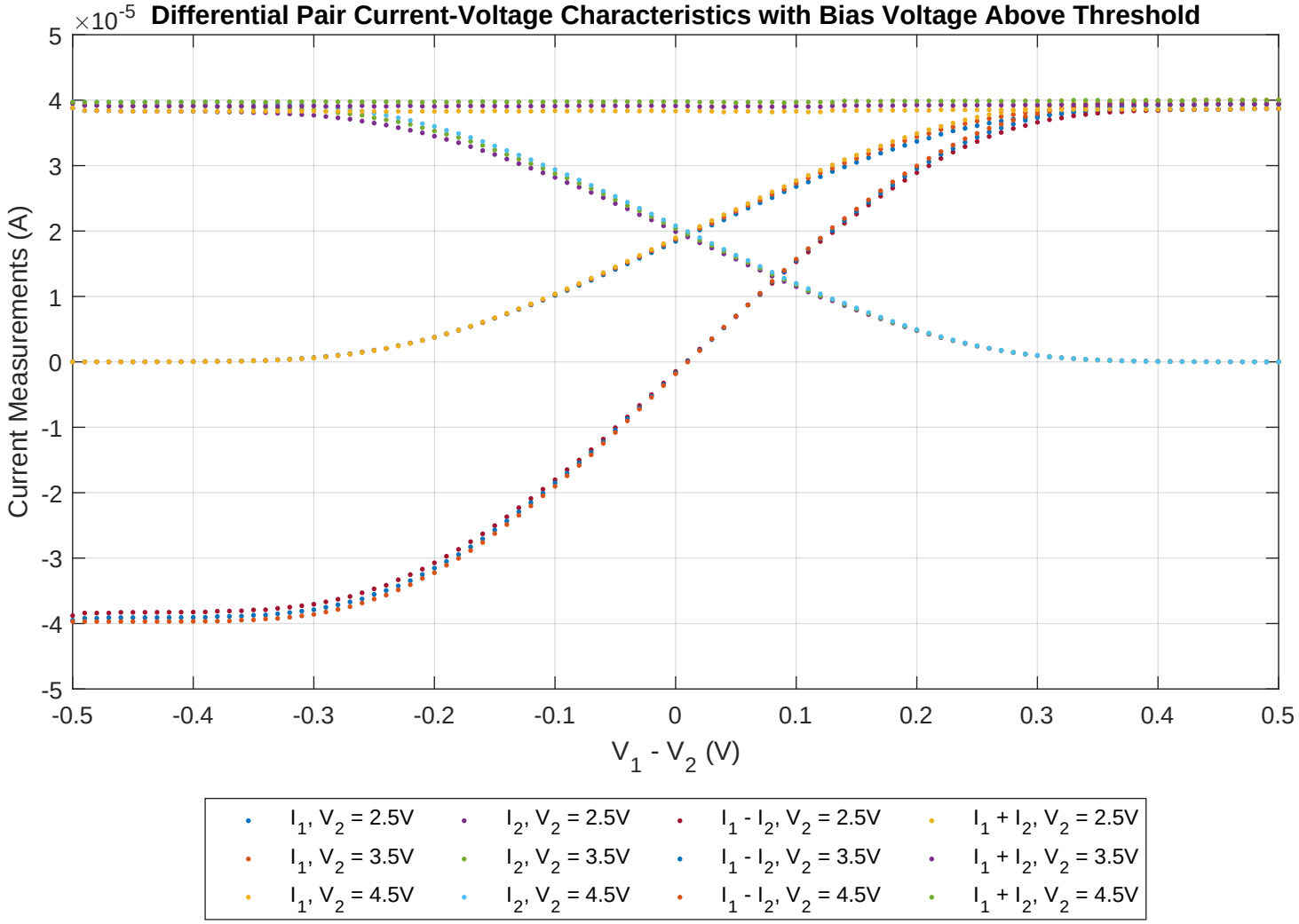

Figure 4: Measurements for I_1, I_2, $I_1 - I_2$, and $I_1 + I_2$ of an nMOS Differential Pair with a bias current ABOVE threshold, for each of our three values of V_2. We used our SMU to sweep V_{dm} from $-500mv$ to $500mv$.

Similarly to the current below threshold, the current readings do not change much for the various voltages of V_2. However, the transition from V_1 being below V_2 to V_1 being above V_2 occurs over a much larger range of voltages, from around $V_{dm} = -0.3V$ to $V_{dm} = 0.3V$ compared to around $V_{dm} = -0.1V$ to $V_{dm} = 0.1V$ for below threshold.

Next, we again analyzed the common-source node voltage, V , as a function of $V_{dm} = V_1 - V_2$ for all three values of V_2, as shown in **Figure 5**.

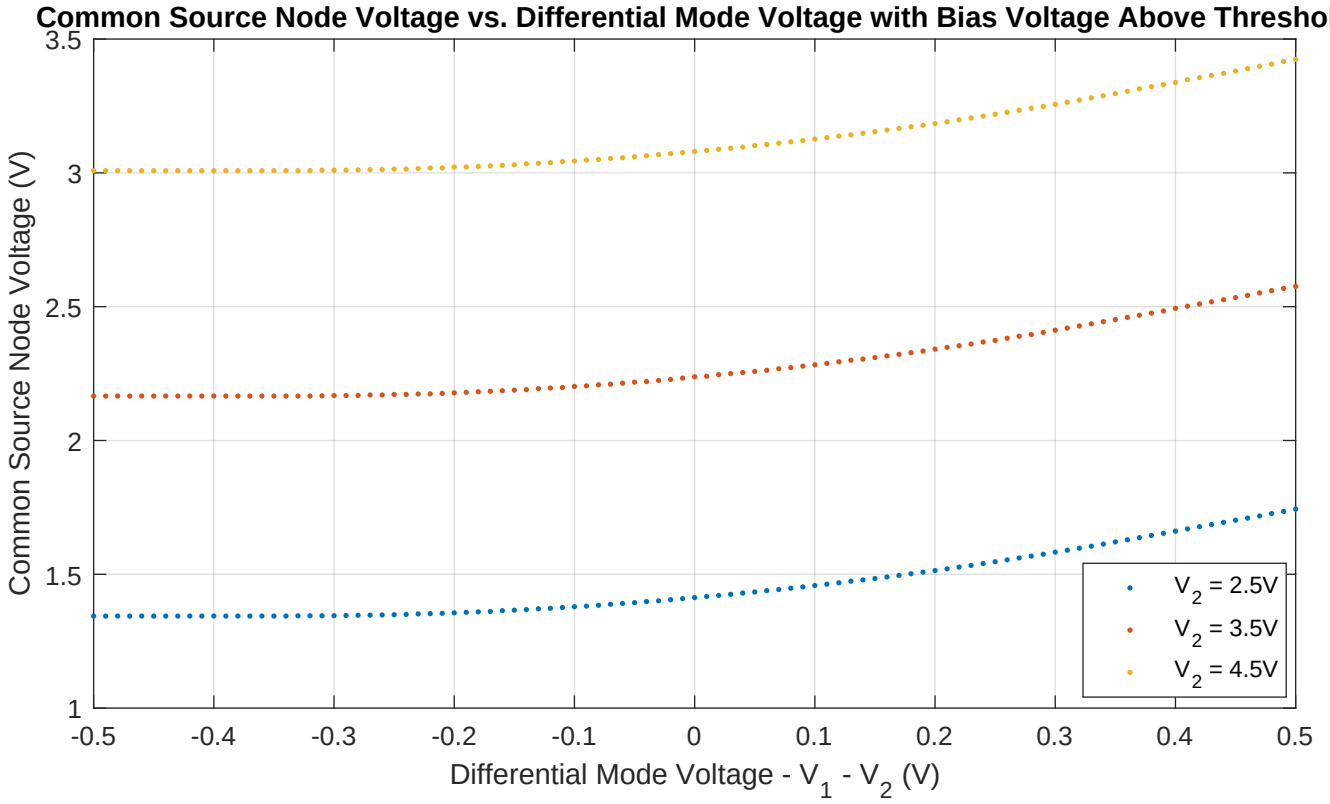

Figure 5: Common Source Node Voltage vs. Differential Mode Voltage of an nMOS Differential Pair with an ABOVE threshold bias current swept from $-500mv$ to $500mv$ below/above V_2.

This time, we see that the common source node voltage is slightly different compared to the below threshold case ($3V$ compared to $3.3V$, $2.2V$ compared to $2.5V$, and $1.8V$ compared to $1.6V$). However, we see a similar pattern of increase as V_1 begins to overtake V_2, although this overtake does start much earlier (around $V_{dm} = -0.2V$ instead of $V_{dm} = 0V$).

Lastly, we again wanted to analyze the differential-mode transconductance gains for each of the three values of V_2 that we used. To do so, we fit a straight line to the plot of $I_1 - I_2$ as a function of $V_{dm} = V_1 - V_2$ around the region where $V_1 \approx V_2$ (i.e., around where $V_1 - V_2 \approx 0V$). This gives us an estimate of the differential-mode transconductance gain as shown in **Figure 6**.

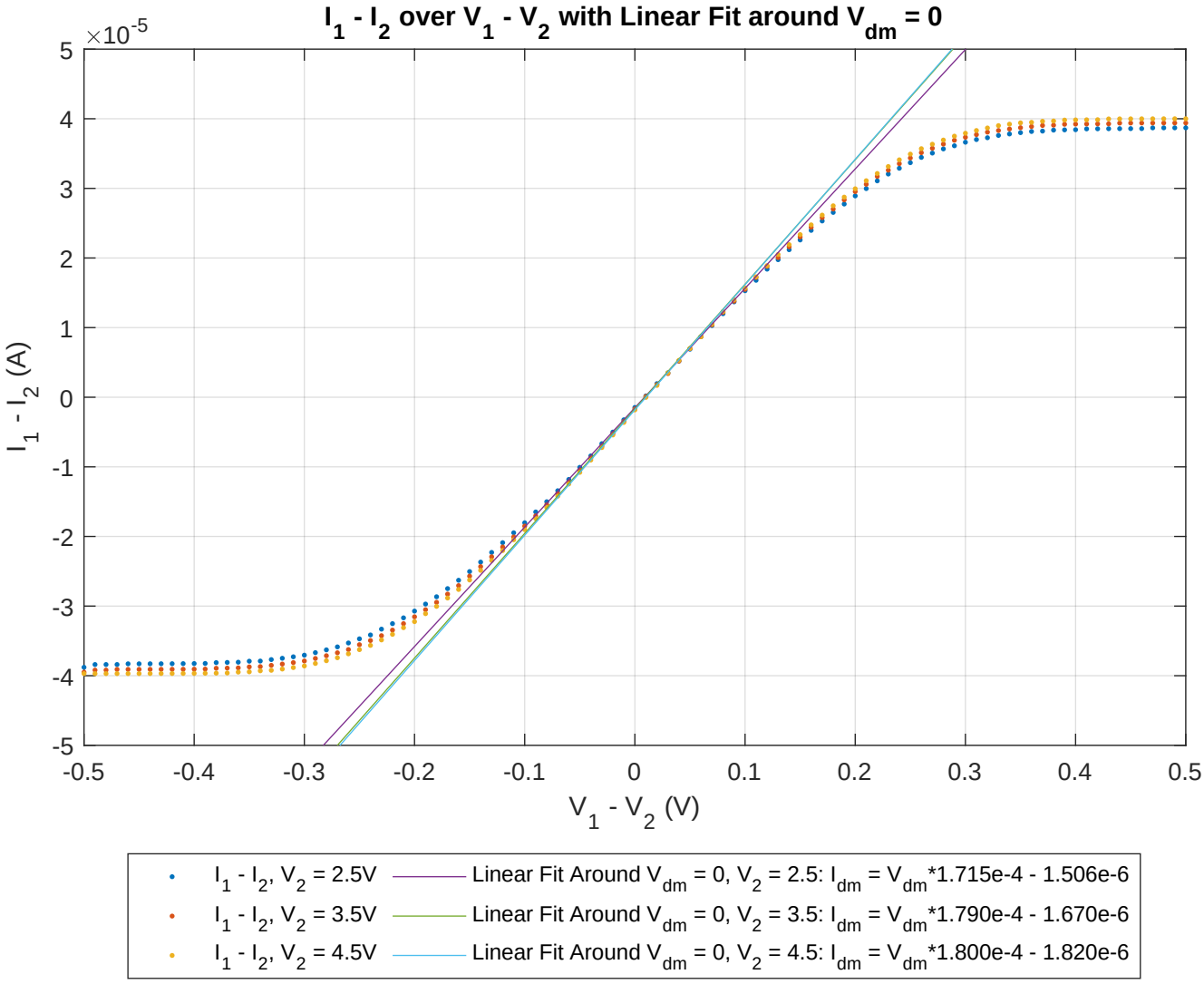

Figure 6: Measurements for $I_1 - I_2$ against V_{dm} of an nMOS Differential Pair with an ABOVE threshold bias current, for each of our three values of V_2. We used our SMU to sweep V_{dm} from $-500mv$ to $500mv$. We have also included the differential-mode transconductance gains, which are the slopes of the best fit lines near $V_{dm} = 0$.

Again, the the differential-mode transconductance gain does change slightly with different values of V_2, it does not change significantly. The lowest slope is $1.715e-4$ mhos, while the highest is $1.800e-4$ mhos.

However, we can note that as the slopes are much more shallow here, that the differential-mode transconductance gain is much lower for an above threshold bias current than for a below threshold bias current.