Circuits Lab 5: MOS Transistor Characteristics and Simple MOS Current Mirrors

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Experiment 1: Input/Gate Characteristics

For the first experiment, we will measure the voltage-current characteristics of four diode-connected nMOS transistors from the same chip array and see how well they match each other.

First, we obtained an ALD1106 quad nMOS transistor array and diode-connected each of the MOSFETs by connecting their respective drains and gates. We then swept over the input current from 10 nA to 1 mA to the drain/gate while measuring the gate voltage.

After measuring the voltage-current characteristics of each MOSFET, we can then use the provided ekgfit function in Matlab to calculate the Is, VT, and kappa values for each MOSFET. These calculated values can be shown in **Table 1**.

MOSFET #	$I_s(A)$	$V_T(V)$	κ
MOSFET 1	$1.9438 \cdot 10^{-}6$	0.6801	0.05644
MOSFET 2	$1.9438 \cdot 10^{-}6$	0.6801	0.05644
MOSFET 3	$1.9438 \cdot 10^{-}6$	0.6801	0.05644
MOSFET 4	$1.9438 \cdot 10^{-}6$	0.6801	0.05644

Table 1: A table with the extracted I_s, V_T and κ values for each resistor using the ekgfit function.

Once we extracted our I_s, V_T and κ values, we can now plot our measured data against a theoretical fit. In order to model our fit, we use the model

$$I = I_s \cdot \log^2(1 + e^{(\kappa \cdot (V_G - V_T)/(2 \cdot U_T))});$$

using $U_T = 0.0258$ and the values of I_s, V_T and κ as seen in **Table 1**. We plot each of the current-voltage characteristics as well as an ideal fit in **Figure 1**, using the gate voltage from MOSFET 1 to create our ideal fit..

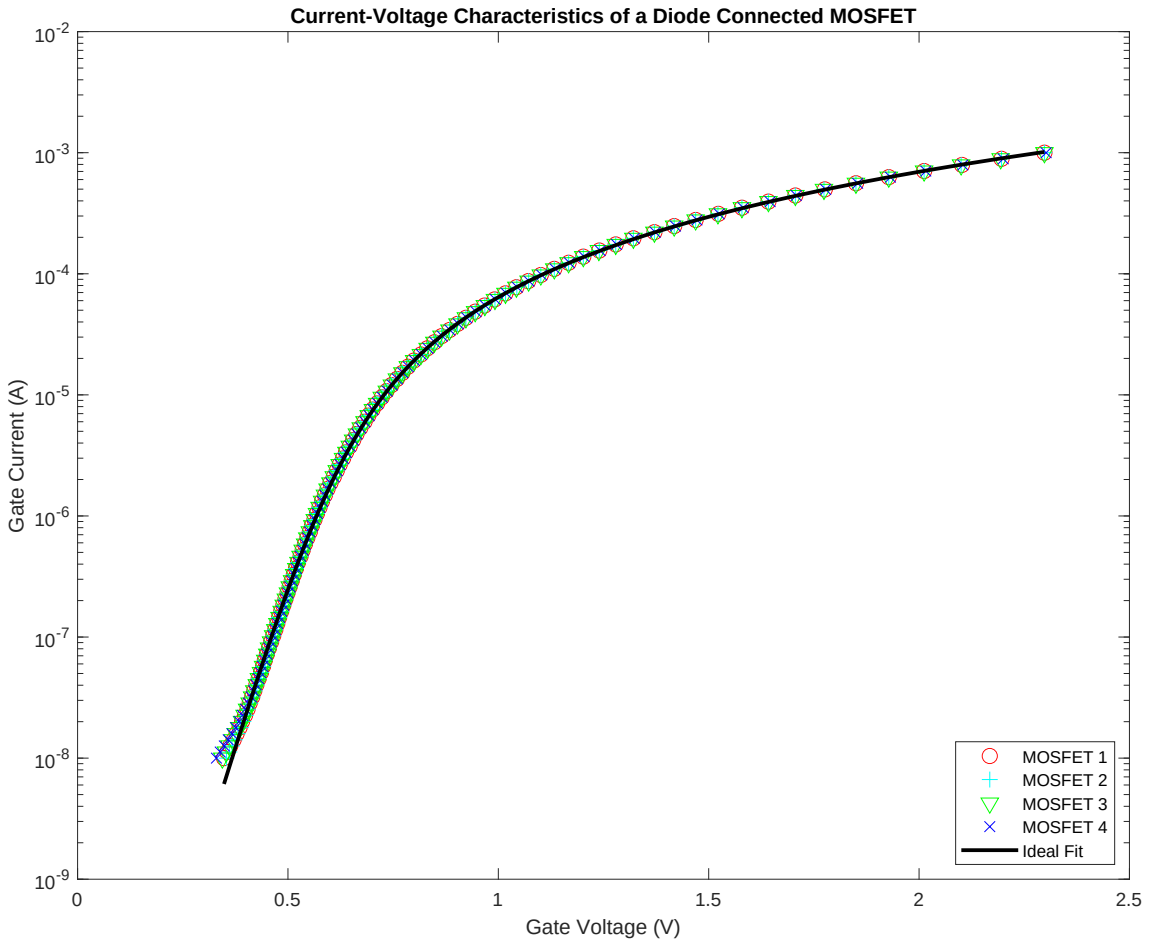

Figure 1: Current Voltage Characteristics of each of the four MOSFETs from our ALD1106 array compared to an ideal fit.

We can see that our current-voltage characteristics are nearly identical between our four MOSFETs.

To further analyze the differences in our transistor array, we wanted to compare each individual transistor's gate voltage with the average gate voltage from all four transistors. We graphed these differences in relation to the input current, as shown in **Figure 2**.

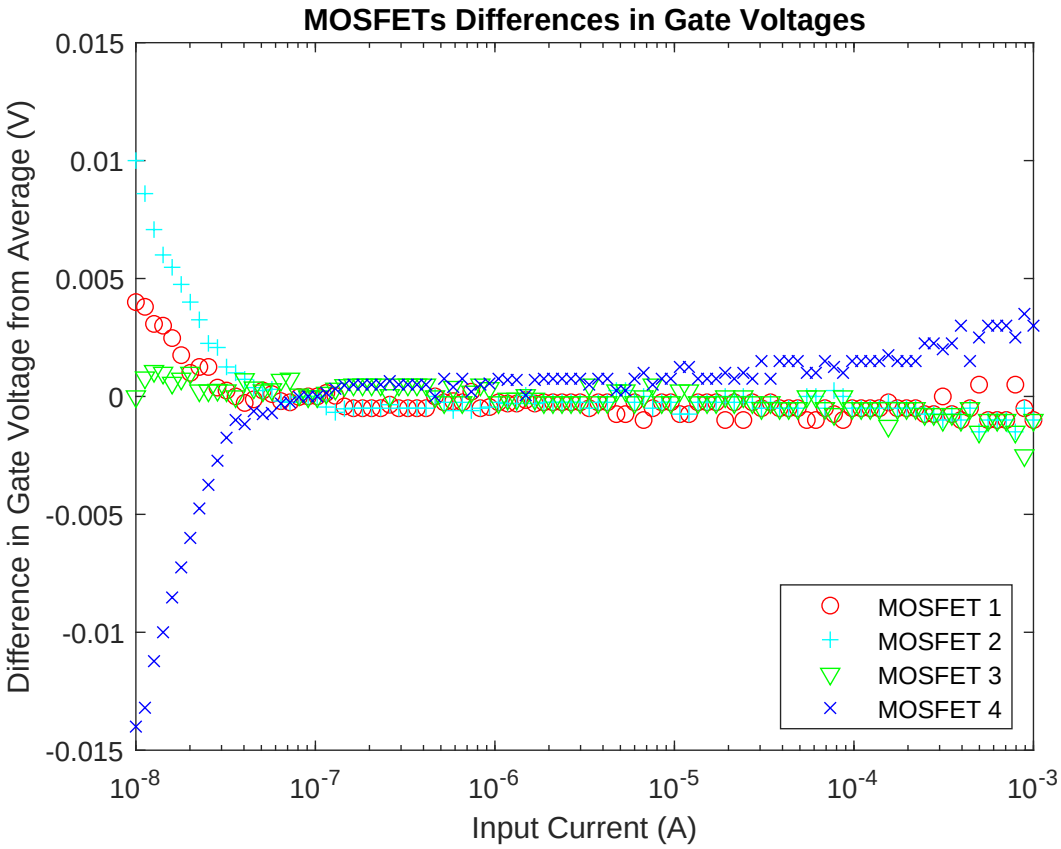

Figure 2: Difference in gate voltage for each MOSFET compared to the average gate voltage.

The characteristics match each other very well, where we have less than a 5mV difference in gate voltage for most of our input currents. Notably, the MOSFETs match best at mid inversion. At weak inversion, the voltages begin to deviate significantly, while at high inversion, the voltages deviate slightly.

For the last part of Experiment 1, we extracted the one of our transistor's incremental trans-conductance gains. We chose MOSFET 3 since it had the most consistent data, as shown in **Figure 2**. In order to extract the incremental transconductance gain, we used the MATLAB command diff to obtain a crude finite-difference approximation of transconductance gain:

$$g_m = (\frac{diff(I_{sat})}{diff(V_G)}))$$

Additionally, we used the formula:

$$g_m = \kappa \cdot g_s = \kappa(\frac{\sqrt{I_s I_{sat}}}{U_T}(1 - e^{-\sqrt{I_s at/I_s}}))$$

to find the ideal fit for the same trans-conductance gain. To compare the ideal and measured fits, we plotted them both with respect to input current, as seen in **Figure 3**.

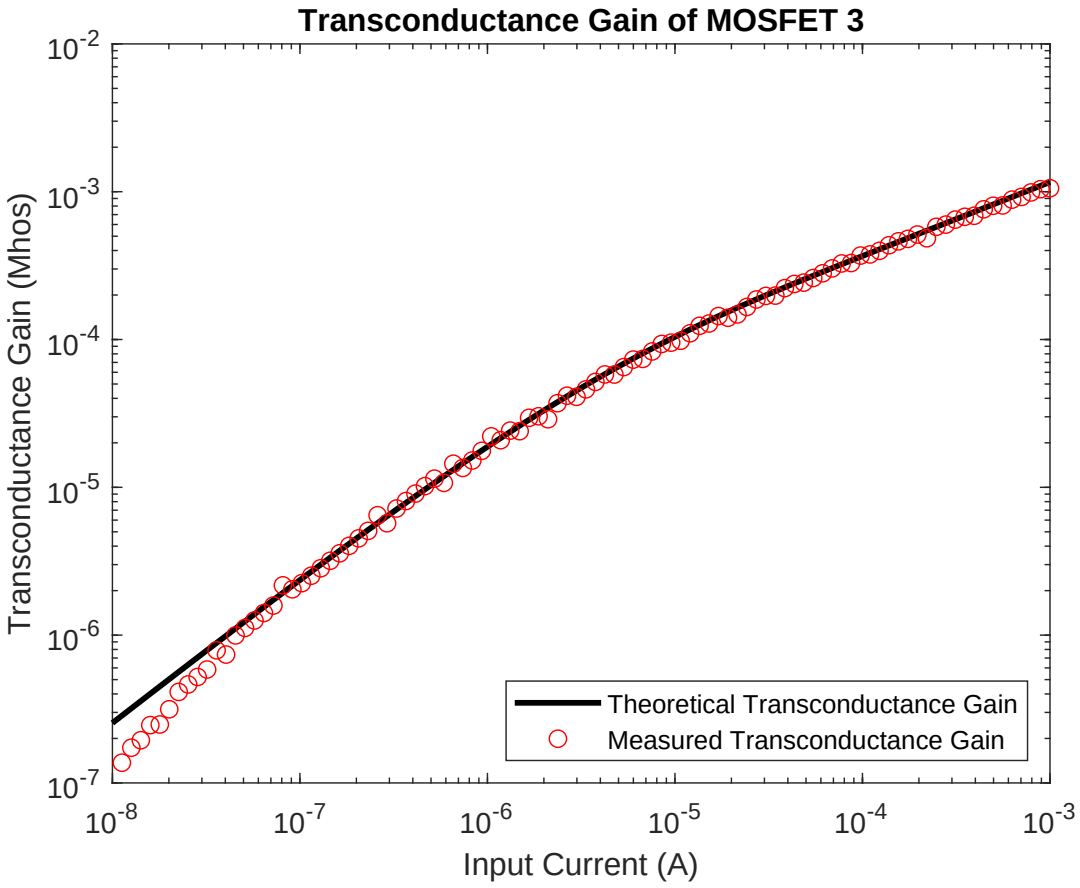

Figure 3: Theoretical and Measured trans-conductance gains for MOSFET 3 with respect to input current.

The measured trans-conductance gain matched the theoretical trans-conductance gain very well. It demonstrates slight deviation in weak induction, but matches the majority of the data perfectly. //

Experiment 2: Current Transfer Characteristics

In this experiment, we will construct and characterize a simple nMOS current mirror using two ALD1106 transistors, measuring its current transfer characteristic over an input current range of 10 nA to 1 mA at an output voltage of +5 V.

For an ideal current mirror, the input current will be equal to the output current, and that is reflected in our theoretical fit.

$$I_{out} = I_{in}$$

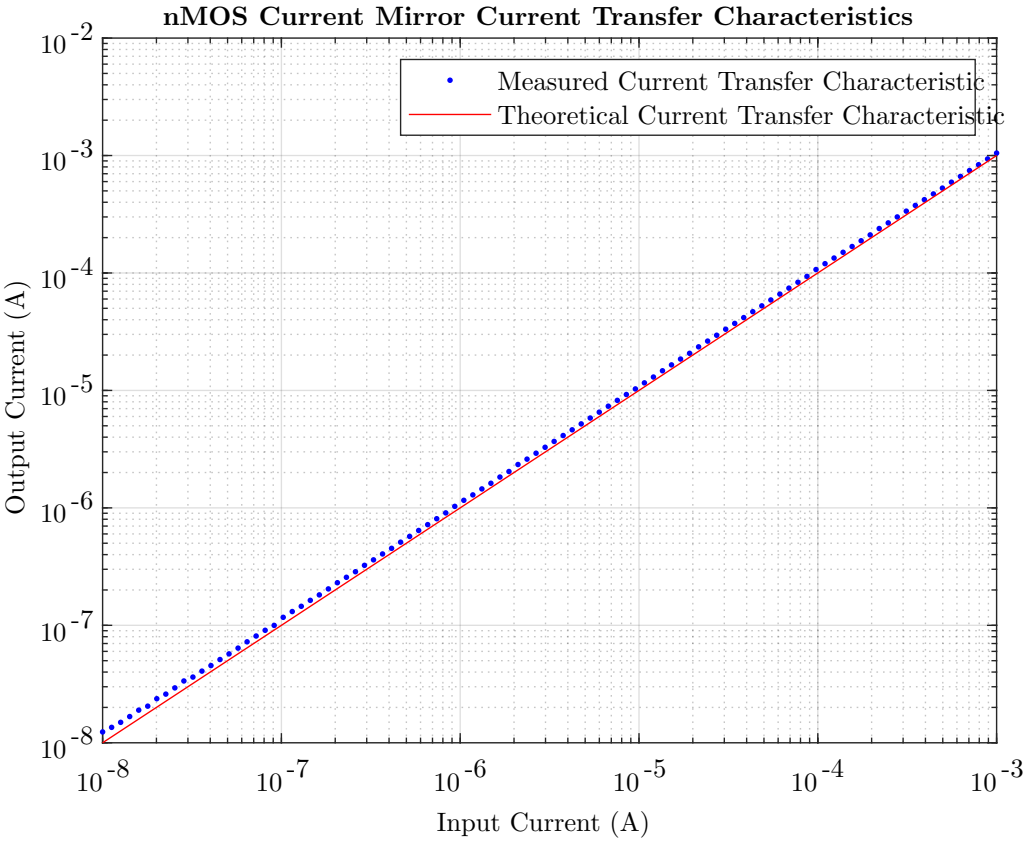

Figure 4: A loglog plot of the input and output current of the nMOS current mirror.

The current mirror works as expected for moderate currents (1 µA–100 µA) but shows slight deviations at very low and very high currents. The log-log plot confirms the expected linear relationship with minor deviations.

Experiment 3: Output/Drain Characteristics

In this lab, we measure the output current-voltage (I-V) characteristics of an nMOS current mirror at three input current levels (100 nA, 1 µA, 100 µA) representing weak, moderate, and strong inversion. Key parameters such as Early voltage (V_A), output resistance (r_o), on-resistance (r_{on}), and intrinsic gain ($\frac{r_o}{r_{on}}$) are extracted to evaluate the validity of the assumption that intrinsic gain is much greater than unity.

We kept the input current stable at the specified three values, and then swept the output voltage, while measuring the drain current.

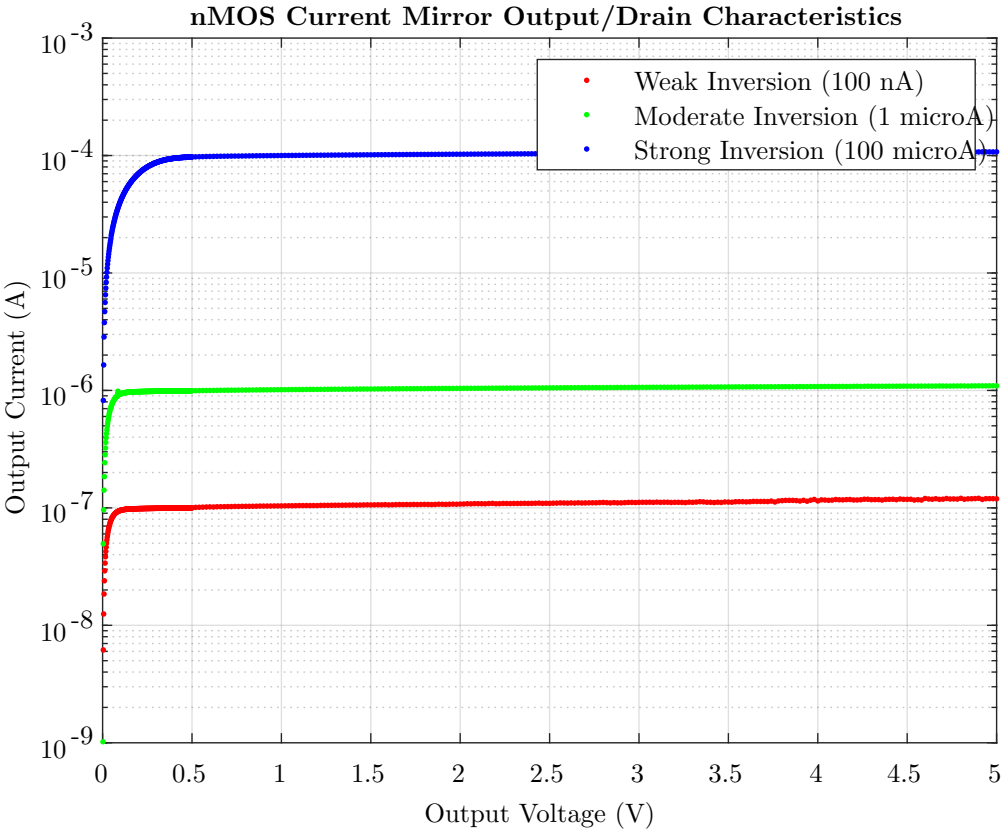

Figure 5: A semilog plot of the output current/voltage characteristics for three different input current values.

Now, we need to extract the values from the data. First, we derived the early voltage V_A. To do so, we created a fit for the saturation region of the current-voltage characteristic and extrapolated it to determine where the drain current would theoretically be zero. Next, to determine the early effect resistance, we divided the early voltage by the saturation current:

$$\frac{V_A}{I_S}$$

Next, to determine the transistor's on resistance, we created a fit of the deep ohmic region of the current-voltage characteristic (where the swept output voltage is very low) and took the inverse of the slope (which is given as current over voltage, so it makes sense that the inverse, voltage over current, gives the transistor's on resistance). Finally, to determine the intrinsic gain of each drain in each inversion, we divided the early effect resistance by the transistor's on resistance.

	Weak Inversion	Moderate Inversion	Strong Inversion
Early Voltage (V)	22.29	39.25	49.44
Early Effect Resistance (Ohms)	1.1467e+07	2.0192e+07	2.5434e+07
Transistor's On Resistance (Ohms)	470990	135840	2960.9
Intrinsic Gain	24.34	148.64	8589.97

The assumption that intrinsic gain $<<$ 1 holds across all inversion levels. The gain does differ in scale across different inversion levels but they are all comfortably above unity for all inversion levels.