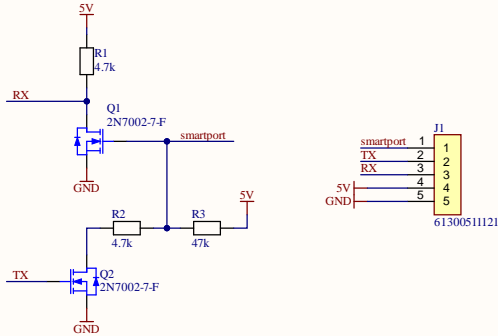


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REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE	PROJECT	Altium	
ENG: -				
DSN: -		PROJECT REVISION	DOCUMENT REVISION	DESIGN ITEM
CHK: -		TITLE		
REFERENCE DOCUMENTS		★		
BOM:				
ASSY DWG:	SIZE	CAGE CODE	DWG NO.	REV
FAB DWG:	A3			
PCB DWG:	SCALE:	FILE NAME	smartport_inverter.SchDoc	
		SHEET	*	OF *

The diagram shows the SmartPort Inverter module with the following components and connections:

- Components:**
 - R1:** A 10kΩ pull-up resistor connected to the TX pin.
 - R2:** A 10kΩ pull-up resistor connected to the RX pin.
 - Q1:** An NPN transistor (2N2222) with its emitter connected to GND and its collector connected to the TX pin.
 - Q2:** An NPN transistor (2N2222) with its emitter connected to GND and its collector connected to the RX pin.
- Pin Connections:**
 - J1:** A 5-pin connector with the following pins:
 - SP:** Serial Port (TX and RX pins).
 - TX:** Transmitter pin.
 - RX:** Receiver pin.
 - 5V:** Power supply pin.
 - GND:** Ground pin.



SmartPort Inverter

Diagram showing the pinout for the SmartPort Inverter module. The module has a 5-pin header (J1) with pins labeled SP, TX, RX, 5V, and GND. The internal circuitry includes two inverters, Q1 and Q2, and three resistors, R1, R2, and R3. The connections are as follows:

- SP is connected to the input of Q1.
- TX is connected to the output of Q1.
- RX is connected to the input of Q2.
- 5V is connected to the output of Q2.
- GND is connected to the common ground of the inverters.

SmartPort Inverter

Diagram showing the pinout for the SmartPort Inverter module. The pins are labeled R3, R2, R1, Q1, Q2, J1, SP, TX, RX, 5V, and GND. The module has a 5-pin header (SP, TX, RX, 5V, GND) and a 6-pin header (R3, R2, R1, Q1, Q2, J1). The internal components are labeled R3, R2, R1, Q1, and Q2.

SmartPort Inverter

R3 R2

R1 Q1 Q2

J1

SP TX RX 5V GND

The diagram shows the SmartPort Inverter module with the following components and connections:

- Components:**
 - R1, R2, R3:** Resistors.
 - Q1, Q2:** Transistors.
 - J1:** A 5-pin connector with pins labeled SP, TX, RX, 5V, and GND.
- Connections:**
 - The **SP** pin of J1 is connected to the base of Q1.
 - The **TX** pin of J1 is connected to the emitter of Q1.
 - The **RX** pin of J1 is connected to the base of Q2.
 - The **5V** pin of J1 is connected to the emitter of Q2.
 - The **GND** pin of J1 is connected to the common ground.

SmartPort Inverter

R3 R2

R1

Q1 Q2

J1

SP TX RX 5V GND

The diagram shows the SmartPort Inverter module with the following components and connections:

- Components:**
 - R1:** A 10kΩ pull-up resistor connected to the TX pin.
 - R2:** A 10kΩ pull-up resistor connected to the RX pin.
 - Q1:** An NPN transistor (2N2222) with its emitter to ground and its collector to the TX pin.
 - Q2:** An NPN transistor (2N2222) with its emitter to ground and its collector to the RX pin.
 - J1:** A 5-pin header with pins labeled SP, TX, RX, 5V, and GND.
- Connections:**
 - The **TX** pin of the header is connected to the collector of Q1 and through R1 to the TX pin of the module.
 - The **RX** pin of the header is connected to the collector of Q2 and through R2 to the RX pin of the module.
 - The **5V** pin of the header is connected to the base of Q1 and Q2, and through a 10kΩ resistor to the TX pin of the module.
 - The **GND** pin of the header is connected to the emitter of Q1 and Q2, and to the GND pin of the module.

SmartPort Inverter

R3 R2

R1

Q1 Q2

J1

SP TX RX 5V GND

SmartPort Inverter

R3 R2

R1 Q1 Q2

J1

SP TX RX 5V GND

The diagram illustrates the SmartPort Inverter circuit. It features two inverters, Q1 and Q2, each represented by a square symbol with a cross inside. Resistor R1 is connected to the input of Q1, R2 to the input of Q2, and R3 to the output of Q2. A 5-pin connector, J1, is shown at the bottom with pins labeled SP, TX, RX, 5V, and GND. The circuit is powered by a 5V supply connected to the 5V pin of J1.

The diagram shows the SmartPort Inverter module with the following components and connections:

- Components:**
 - R1:** A 10kΩ pull-up resistor connected to the 5V supply and the TX pin.
 - R2:** A 10kΩ pull-up resistor connected to the 5V supply and the RX pin.
 - Q1:** An NPN transistor (2N2222) with its emitter to ground, base to TX, and collector to RX.
 - Q2:** A PNP transistor (2N2907) with its emitter to 5V, base to RX, and collector to TX.
- Pin Connections:**
 - J1:** A 5-pin header with pins labeled SP, TX, RX, 5V, and GND.
 - TX:** Connected to the TX pin of the module and the TX pin of J1.
 - RX:** Connected to the RX pin of the module and the RX pin of J1.
 - 5V:** Connected to the 5V pin of J1.
 - GND:** Connected to the GND pin of J1.

SmartPort Inverter

R3 R2

R1 Q1 Q2

J1

SP TX RX 5V GND

The diagram shows the SmartPort Inverter pinout. It includes three resistors (R1, R2, R3) connected to the TX and RX pins of the J1 connector. Two inverters (Q1, Q2) are shown, with their inputs connected to the TX and RX pins of the J1 connector. The J1 connector has five pins: SP, TX, RX, 5V, and GND. The TX and RX pins are connected to the inputs of the inverters Q1 and Q2, respectively. The outputs of the inverters Q1 and Q2 are connected to the TX and RX pins of the J1 connector. The 5V and GND pins are connected to the power and ground pins of the J1 connector.

The diagram shows a 'SmartPort Inverter' circuit. It features a 5-pin D-sub connector labeled J1 with pins SP, TX, RX, 5V, and GND. The SP pin is connected to a square wave signal source. The TX pin is connected to the input of an inverter circuit labeled Q1. The RX pin is connected to the input of another inverter circuit labeled Q2. The 5V pin is connected to the positive supply rail, and the GND pin is connected to the common ground. The output of Q1 is connected to the input of Q2, and the output of Q2 is connected back to the input of Q1, forming a cross-coupled inverter pair. The circuit is powered by a 5V supply and a common ground.

The diagram illustrates the pinout for the SmartPort Inverter. It shows a top view of the component with pins labeled R1, R2, R3, Q1, Q2, and J1. Below the component, a row of five pins is labeled SP, TX, RX, 5V, and GND. The connections are as follows: R1 is connected to SP; R2 is connected to TX; R3 is connected to RX; Q1 is connected to 5V; and Q2 is connected to GND. The J1 pin is shown but has no connection indicated.

SmartPort Inverter

R3 R2

R1 Q1 Q2

J1

SP TX RX 5V GND

Smart-Port Inverter

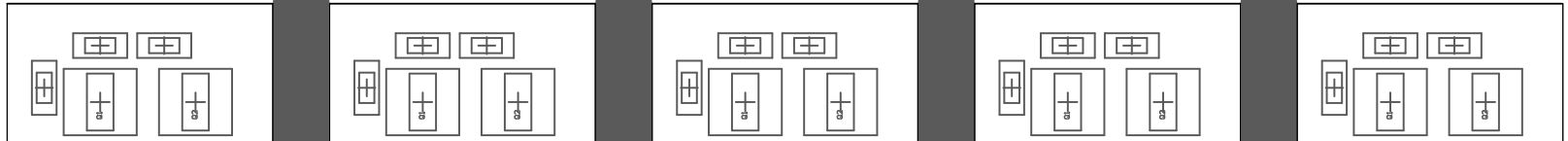
R3 R2 R1

J1

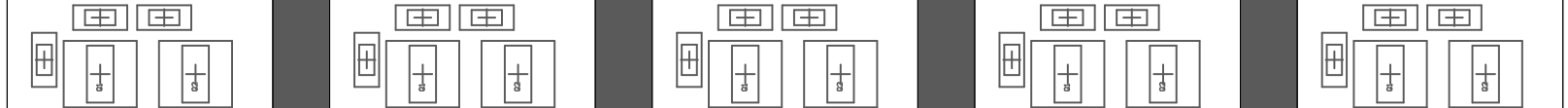
SP TX RX 5V GND



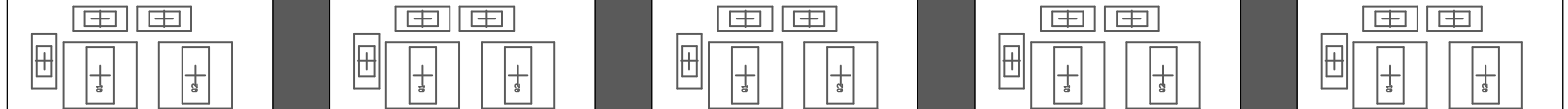
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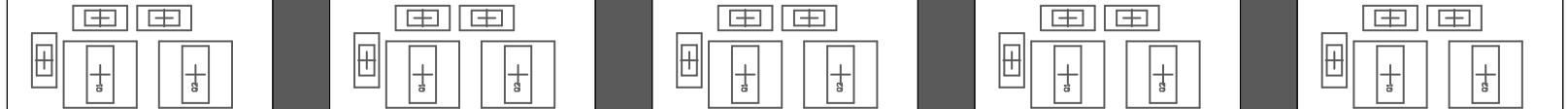
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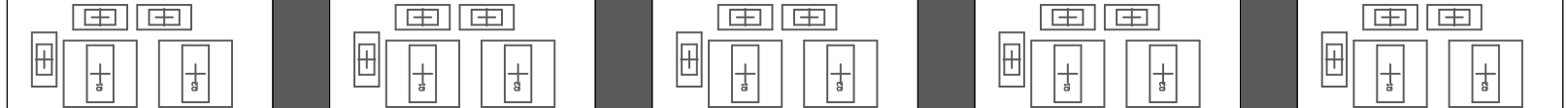
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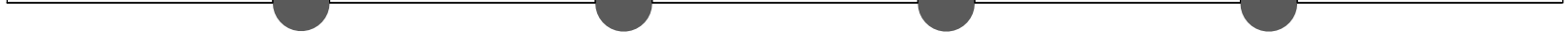
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V-Core both sides full length of pcb

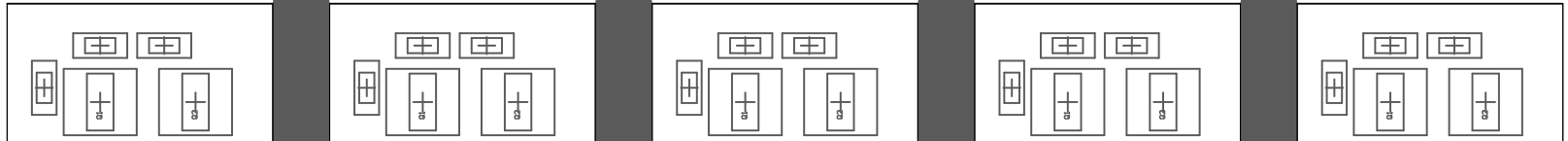


V-Core both sides full length of pcb

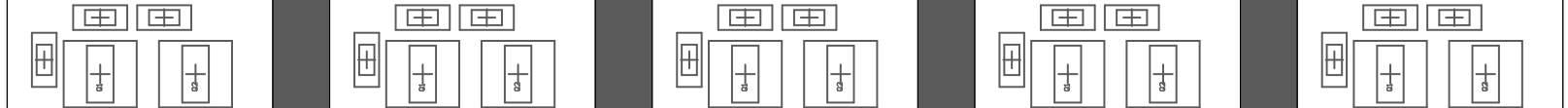




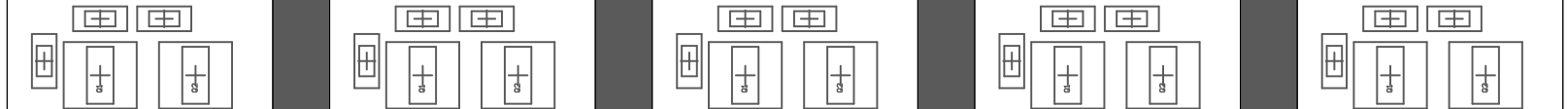
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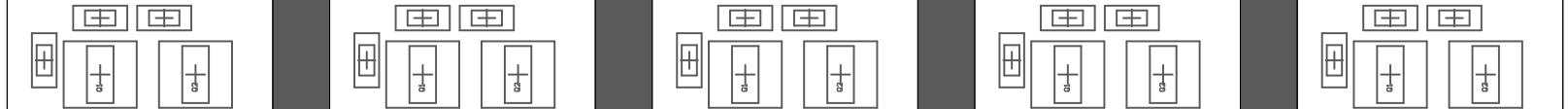
V-Core both sides full length of pcb



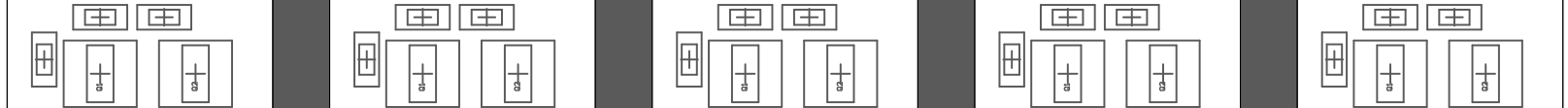
V-Core both sides full length of pcb



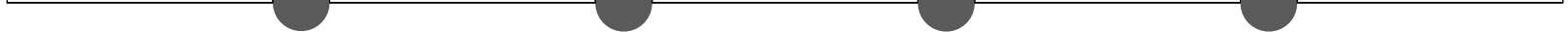
V-Core both sides full length of pcb



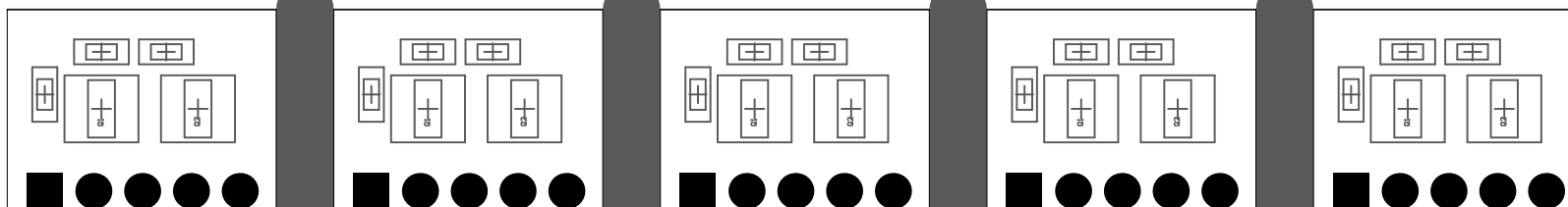
V-Core both sides full length of pcb



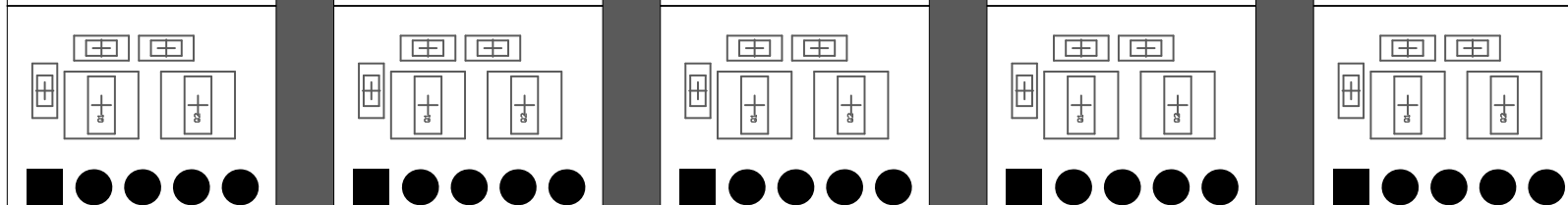
V-Core both sides full length of pcb



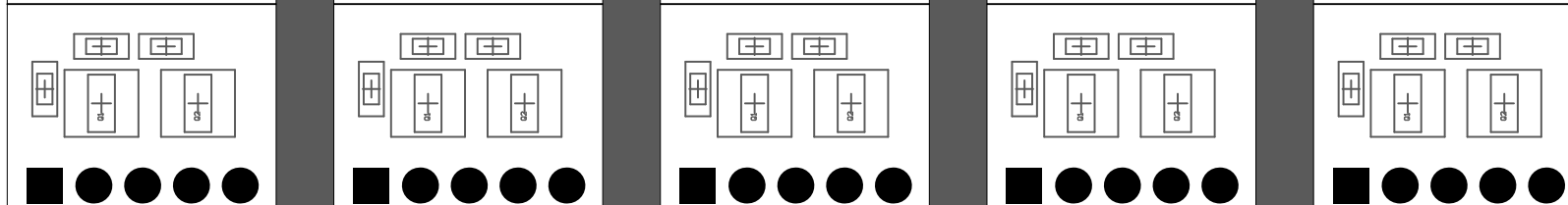
V-Core both sides full length of pcb



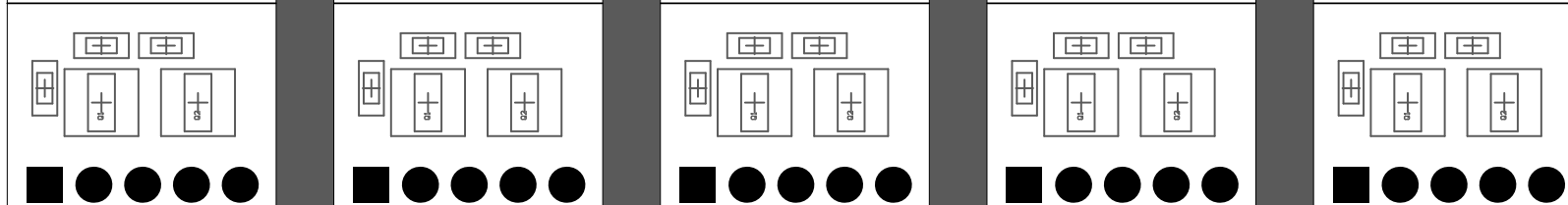
V-Core both sides full length of pcb



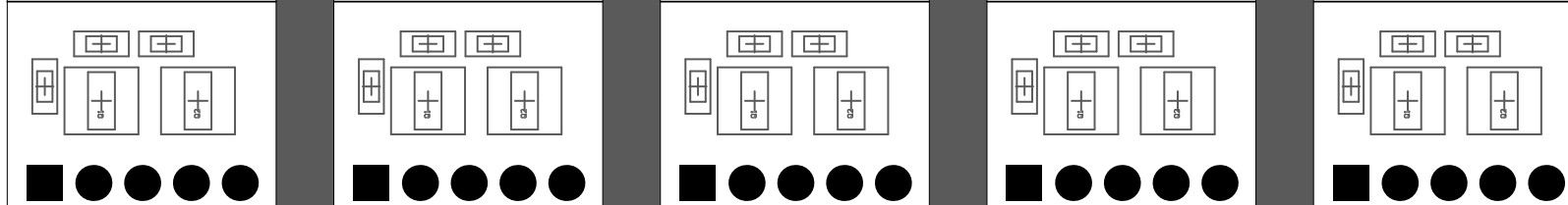
V-Core both sides full length of pcb



V-Core both sides full length of pcb



V-Core both sides full length of pcb



V-Core both sides full length of pcb

Comment	Description	Designator	Footprint	LibRef	Quantity
61300511121	Headers & Wire Housings WR-PHD 2.54mm Hdr 5P Single Str Gold	J1	61300511121	61300511121	1
2N7002-7-F	MOSFET N-CH 60V 200MA SOT23-3	Q1, Q2	SOT23-3N	2N7002-7-F	2
4.7k	Resistor 4.7k 0603 +- 1% 0.1	R1, R2	R0603	RES_YAG_RC0603FR- 074K7L	2
47k	Resistor 47k 0603 +- 1% 0.1	R3	R0603	RES_YAG_RC0603FR- 0747KL	1

Design Rules Verification Report

Filename : C:\github\rcmodel\smartport\smartport_inverter.PcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.35mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint (All)	0
Width Constraint (Min=0.1mm) (Max=1mm) (Preferred=0.15mm) (WithinRoom('BGA'))	0
Width Constraint (Min=0.1mm) (Max=5mm) (Preferred=0.15mm) (All)	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.1mm) (Max=0.16mm) (Preferred=0.1mm) and	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.5mm) (Conductor Width=0.25mm) (Air Gap=0.25mm)	0
Minimum Annular Ring (Minimum=0.1mm) (All)	0
Minimum Annular Ring (Minimum=0.35mm) (OnLayer('Mid-Layer 1'))	0
Minimum Annular Ring (Minimum=0.35mm) (OnLayer('Mid-Layer 2'))	0
Hole Size Constraint (Min=0.2mm) (Max=15mm) (All)	0
Hole Size Constraint (Min=0.1mm) (Max=2.5mm) (isVia And WithinRoom('MCU_IO'))	0
Hole To Hole Clearance (Gap=0.4mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.07mm) (All),(All)	0
Net Antennae (Tolerance=20mm) (InNetClass('JTAG'))	0
Net Antennae (Tolerance=0mm) (All)	0
Matched Lengths(Tolerance=14.2mm) (InDifferentialPair ('USB_D'))	0
Matched Lengths(Tolerance=1.27mm) (InNetClass('Flash'))	0
Matched Lengths(Tolerance=8mm) (InNetClass('RMII'))	0
Matched Lengths(Tolerance=10mm) (InNetClass('XIP'))	0
Matched Lengths(Tolerance=2.3mm) (InDifferentialPairClass('DP_ETH'))	0
Matched Lengths(Tolerance=2mm) (InNetClass('MD'))	0
Matched Lengths(Tolerance=8mm) (InNetClass('SD'))	0
Matched Lengths(Tolerance=10mm) (InNetClass('SSD'))	0
Total	0