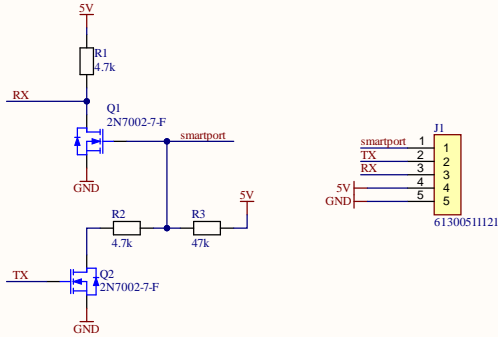


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REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE	PROJECT	Altium	
ENG: -			.	
DSN: -			.	
CHK: -			.	
REFERENCE DOCUMENTS		TITLE		
BOM:		★		
ASSY DWG:		SIZE	CAGE CODE	DWG NO.
FAB DWG:		A3		
PCB DWG:		SCALE:	FILE NAME	SHEET * OF *
			smartport_inverter.SchDoc	

SmartPort Inverter

R3 R2

R1

J1 Q1 Q2

SP TX RX 5V GND

The diagram shows a 'SmartPort Inverter' circuit. It includes three 3-pin headers: R1, R2, and R3. R1 is on the left, R2 is on the right, and R3 is at the top. Two 4-pin headers, J1 and J2, are at the bottom. J1 has pins labeled SP, TX, RX, 5V, and GND. J2 has pins labeled SP, TX, RX, 5V, and GND. The circuit contains two inverters, Q1 and Q2, which are 74VHC14 hex inverters. Q1 is connected to R1 and J1. Q2 is connected to R2 and J2. The output of Q1 is connected to the TX pin of J1. The output of Q2 is connected to the TX pin of J2. The SP pin of J1 is connected to the SP pin of J2. The 5V pin of J1 is connected to the 5V pin of J2. The GND pin of J1 is connected to the GND pin of J2.

SmartPort Inverter

Diagram showing the components and their connections for the SmartPort Inverter:

- R1**: A 10k resistor connected between J1 pin 1 and ground.
- R2**: A 10k resistor connected between J1 pin 2 and ground.
- R3**: A 10k resistor connected between J1 pin 3 and ground.
- Q1**: A 2N2222 transistor connected between J1 pin 4 and ground.
- Q2**: A 2N2222 transistor connected between J1 pin 5 and ground.
- J1**: A 5-pin connector with pins labeled SP, TX, RX, 5V, and GND.

The diagram shows the SmartPort Inverter module with the following components and connections:

- Components:**
 - R1, R2, R3:** Resistors.
 - Q1, Q2:** Transistors.
 - J1:** A 5-pin connector with pins labeled SP, TX, RX, 5V, and GND.
- Connections:**
 - The **SP** pin of J1 is connected to the base of Q1.
 - The **TX** pin of J1 is connected to the base of Q2.
 - The **RX** pin of J1 is connected to the collector of Q1.
 - The **5V** pin of J1 is connected to the emitter of Q1 and the emitter of Q2.
 - The **GND** pin of J1 is connected to the collector of Q2.

SmartPort Inverter

R3 R2

R1

Q1 Q2

J1

SP TX RX 5V GND

SmartPort Inverter

Diagram showing the pinout for the SmartPort Inverter module. The module has a 5-pin header (J1) and a 5-pin connector (SP). The pins are labeled R1, R2, R3, Q1, and Q2. The connector pins are labeled SP, TX, RX, 5V, and GND.

Connections:

- R1 is connected to SP.
- R2 is connected to TX.
- R3 is connected to RX.
- Q1 is connected to 5V.
- Q2 is connected to GND.

The diagram shows the SmartPort Inverter module with the following components and connections:

- Components:**
 - R1:** A 10kΩ pull-up resistor connected between the TX pin and the TX+ pin.
 - R2:** A 10kΩ pull-up resistor connected between the RX pin and the RX+ pin.
 - Q1:** An NPN transistor (2N2222) with its emitter connected to GND and its collector connected to the TX pin.
 - Q2:** An NPN transistor (2N2222) with its emitter connected to GND and its collector connected to the RX pin.
- Pin Connections:**
 - SP:** Serial Port connector.
 - TX:** Transmitter pin.
 - RX:** Receiver pin.
 - 5V:** Power supply pin.
 - GND:** Ground pin.

SmartPort Inverter

R3 R2

R1 Q1 Q2

J1

SP TX RX 5V GND

SmartPort Inverter

Diagram illustrating the internal circuitry of the SmartPort Inverter. The circuit includes resistors R1, R2, and R3, and transistors Q1 and Q2. The pins are labeled J1, SP, TX, RX, 5V, and GND.

SmartPort Inverter

R3 R2

R1 Q1 Q2

J1

SP TX RX 5V GND

SmartPort Inverter

R3 R2

R1 Q1 Q2

J1

SP TX RX 5V GND

SmartPort Inverter

R3 R2

R1 Q1 Q2

J1

SP TX RX 5V GND

The diagram shows a 'SmartPort Inverter' circuit. It includes a 5V power source (J1) connected to a 5V pin. A 10k resistor (R1) is connected between the 5V pin and the base of a 2N2222A NPN transistor (Q1). The emitter of Q1 is grounded. The collector of Q1 is connected to the base of a 2N2222A PNP transistor (Q2). The emitter of Q2 is connected to the 5V pin. The collector of Q2 is connected to the TX pin. A 10k resistor (R2) is connected between the TX pin and ground. A 10k resistor (R3) is connected between the TX pin and the 5V pin. The RX pin is connected to ground. The 5V and GND pins are connected to the 5V and GND pins of the SmartPort connector.

SmartPort Inverter

Diagram showing the pinout for the SmartPort Inverter module. The pins are labeled R3, R2, R1, Q1, Q2, J1, SP, TX, RX, 5V, and GND. The module has a 5-pin header (SP, TX, RX, 5V, GND) and a 6-pin header (R3, R2, R1, Q1, Q2, J1). The internal circuitry shows a 5V regulator and a 10k pull-up resistor.

SmartPort Inverter

R3 R2

R1

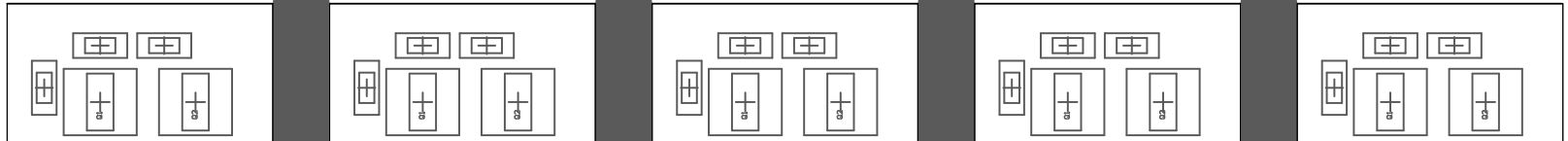
J1

Q1 Q2

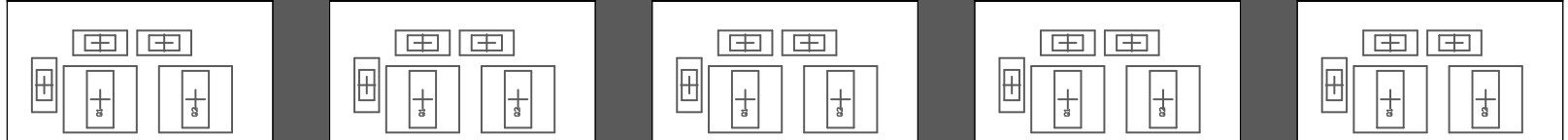
SP TX RX 5V GND



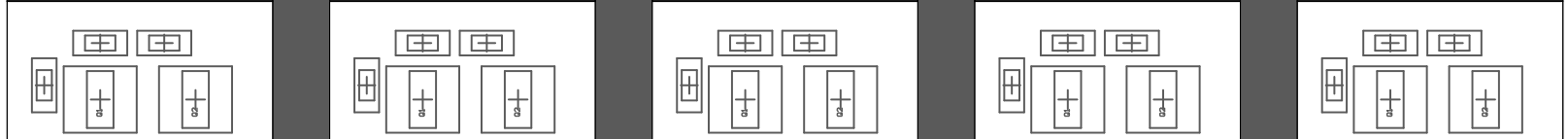
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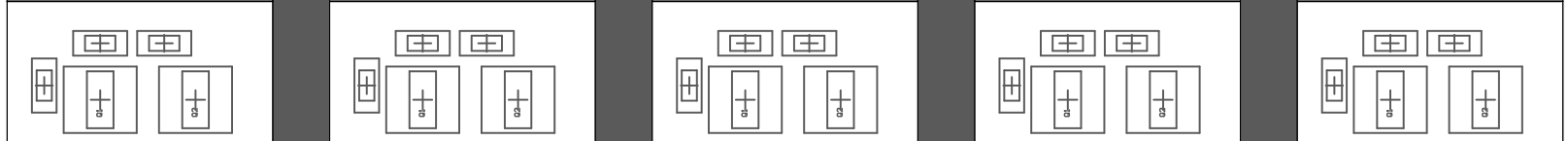
V-Core both sides full length of pcb



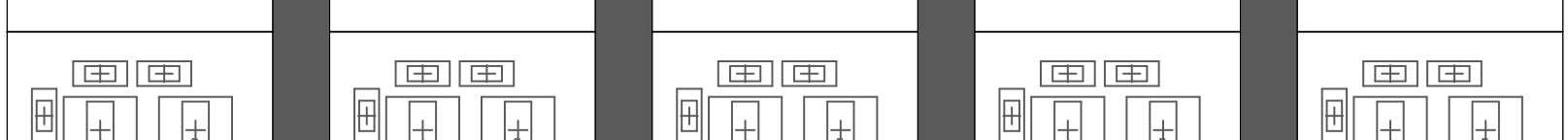
V-Core both sides full length of pcb



V-Core both sides full length of pcb



V-Core both sides full length of pcb

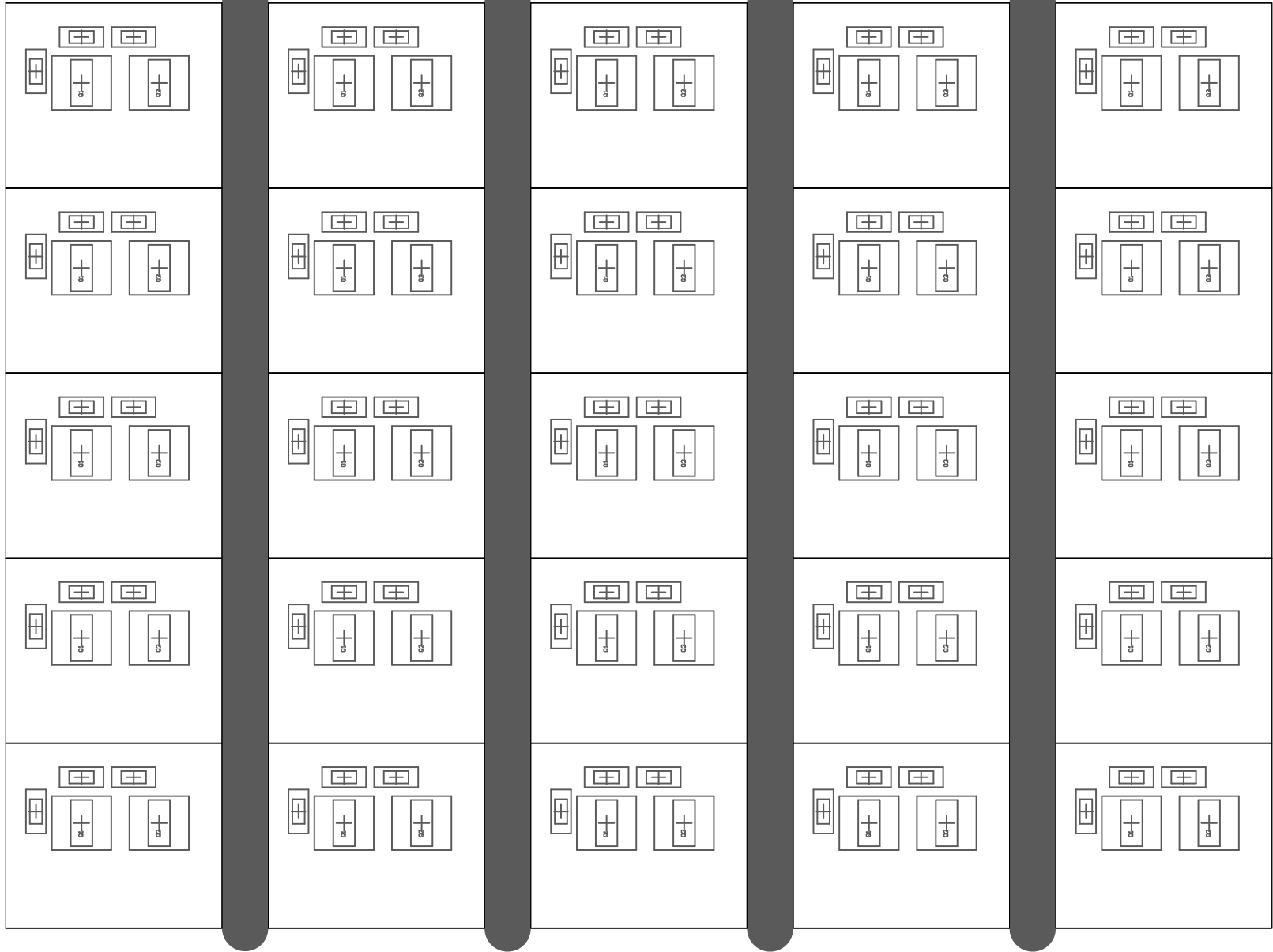


V-Core both sides full length of pcb





V-Core both sides full length of pcb



V-Core both sides full length of pcb

V-Core both sides full length of pcb

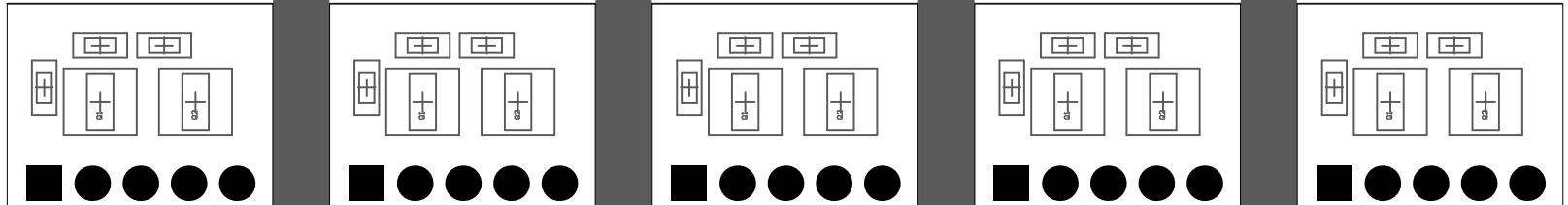
V-Core both sides full length of pcb

V-Core both sides full length of pcb

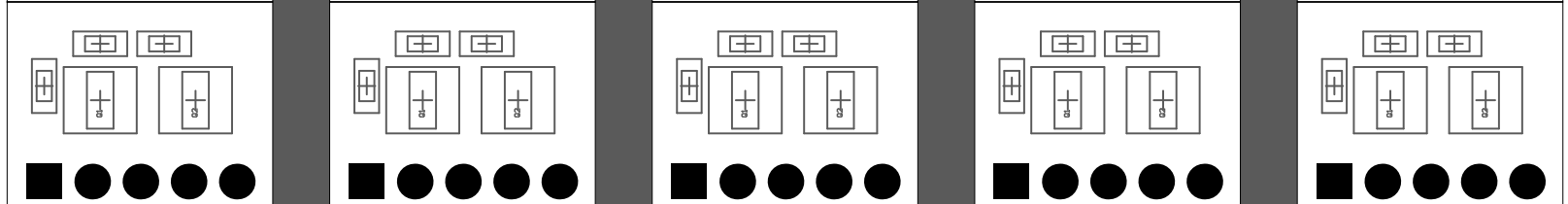
V-Core both sides full length of pcb



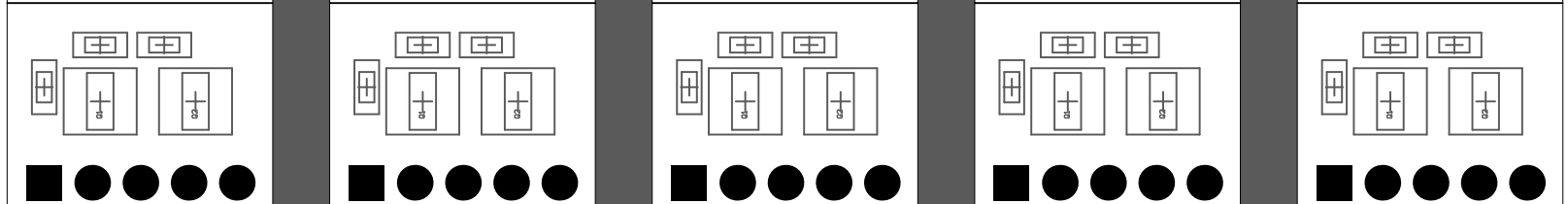
V-Core both sides full length of pcb



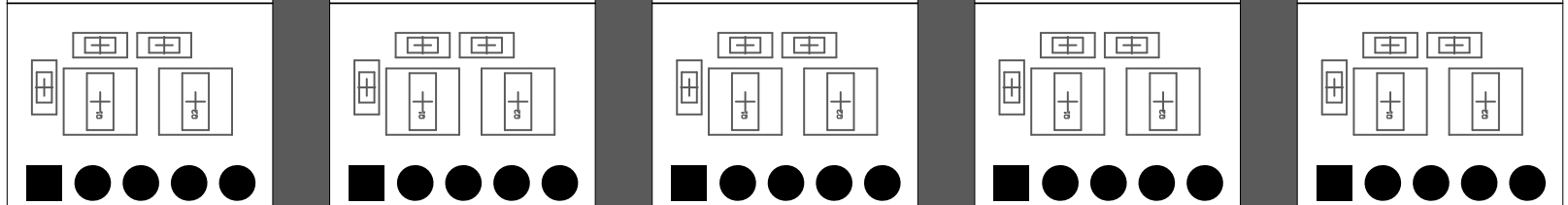
V-Core both sides full length of pcb



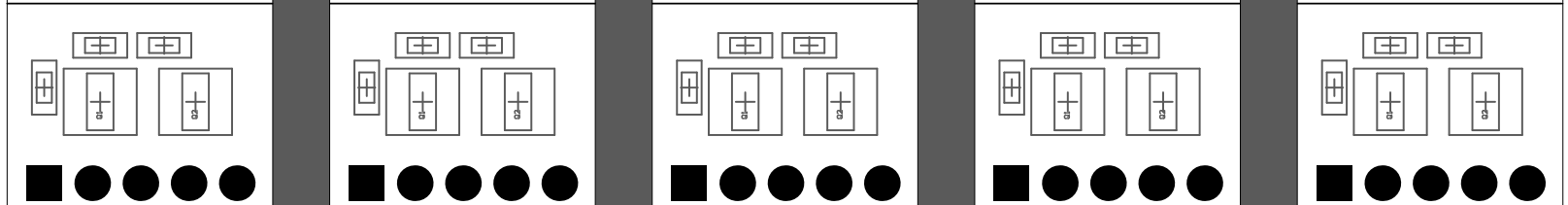
V-Core both sides full length of pcb



V-Core both sides full length of pcb



V-Core both sides full length of pcb



V-Core both sides full length of pcb

Comment	Description	Designator	Footprint	LibRef	Quantity
61300511121	Headers & Wire Housings WR-PHD 2.54mm Hdr 5P Single Str Gold	J1	61300511121	61300511121	1
2N7002-7-F	MOSFET N-CH 60V 200MA SOT23-3	Q1, Q2	SOT23-3N	2N7002-7-F	2
4.7k	Resistor 4.7k 0603 +- 1% 0.1	R1, R2	R0603	RES_YAG_RC0603FR- 074K7L	2
47k	Resistor 47k 0603 +- 1% 0.1	R3	R0603	RES_YAG_RC0603FR- 0747KL	1

Design Rules Verification Report

Filename : C:\github\rcmodel\smartport\smartport_inverter_Panel5X5.PcbDoc

Warnings 0
Rule Violations 6

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.35mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint (All)	3
Width Constraint (Min=0.1mm) (Max=5mm) (Preferred=0.15mm) (All)	0
Width Constraint (Min=0.1mm) (Max=1mm) (Preferred=0.15mm) (WithinRoom('BGA'))	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.1mm) (Max=10mm) (Preferred=0.1mm) and	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.1mm) (Max=0.16mm) (Preferred=0.1mm) and	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.1mm) (Max=10mm) (Preferred=0.1mm) and	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.1mm) (Max=10mm) (Preferred=0.1mm) and	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.1mm) (Max=10mm) (Preferred=0.1mm) and	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.5mm) (Conductor Width=0.25mm) (Air Gap=0.25mm)	0
Minimum Annular Ring (Minimum=0.35mm) (OnLayer('Mid-Layer 2'))	0
Minimum Annular Ring (Minimum=0.1mm) (All)	3
Minimum Annular Ring (Minimum=0.35mm) (OnLayer('Mid-Layer 1'))	0
Hole Size Constraint (Min=0.2mm) (Max=15mm) (All)	0
Hole Size Constraint (Min=0.1mm) (Max=2.5mm) (isVia And WithinRoom('MCU_IO'))	0
Hole To Hole Clearance (Gap=0.4mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.07mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Net Antennae (Tolerance=20mm) (InNetClass('JTAG'))	0
Matched Lengths(Tolerance=8mm) (InNetClass('RMII'))	0
Matched Lengths(Tolerance=14.2mm) (InDifferentialPair ('USB_D'))	0
Matched Lengths(Tolerance=1.27mm) (InNetClass('Flash'))	0
Matched Lengths(Tolerance=2.3mm) (InDifferentialPairClass('DP_ETH'))	0
Matched Lengths(Tolerance=10mm) (InNetClass('SSD'))	0
Matched Lengths(Tolerance=10mm) (InNetClass('XIP'))	0
Matched Lengths(Tolerance=8mm) (InNetClass('SD'))	0
Matched Lengths(Tolerance=2mm) (InNetClass('MD'))	0
Total	6

Un-Routed Net Constraint (All)	
Un-Routed Net Constraint: Via (75.725mm,-3mm) from Top Layer to Bottom Layer Dead Copper - Net Not Assigned.	
Un-Routed Net Constraint: Via (7mm,-3.4mm) from Top Layer to Bottom Layer Dead Copper - Net Not Assigned.	
Un-Routed Net Constraint: Via (7mm,62.875mm) from Top Layer to Bottom Layer Dead Copper - Net Not Assigned.	

Minimum Annular Ring (Minimum=0.1mm) (All)	
Minimum Annular Ring: (No Ring) Via (75.725mm,-3mm) from Top Layer to Bottom Layer (Annular Ring missing on Top Layer)	
Minimum Annular Ring: (No Ring) Via (7mm,-3.4mm) from Top Layer to Bottom Layer (Annular Ring missing on Top Layer)	
Minimum Annular Ring: (No Ring) Via (7mm,62.875mm) from Top Layer to Bottom Layer (Annular Ring missing on Top Layer)	