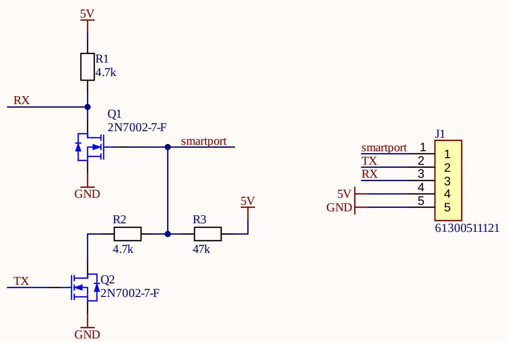
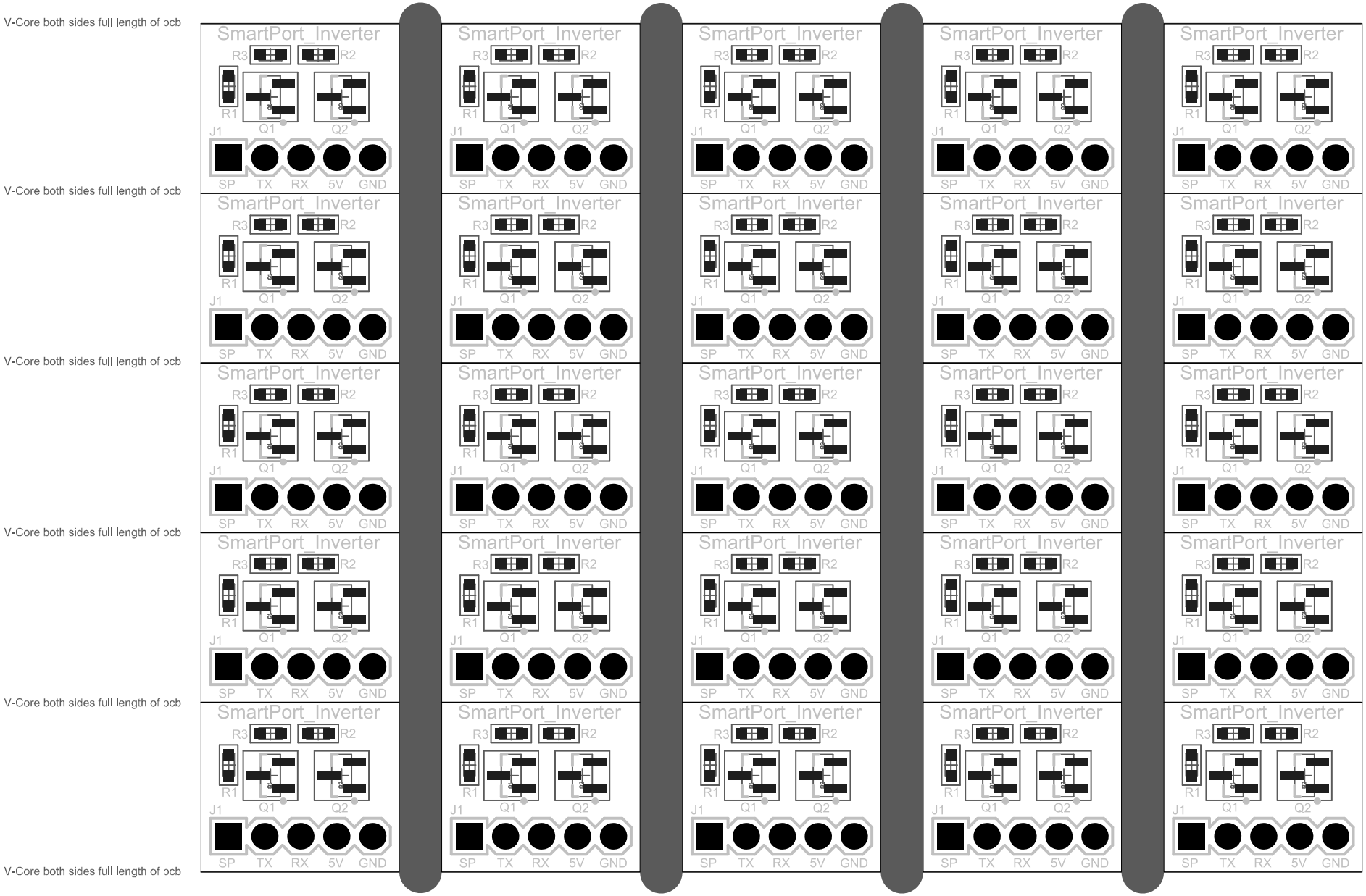
REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
ENG: *	
DSN: *	
CHK: *	

REFERENCE DOCUMENTS
BOM:
ASSY DWG:
FAB DWG:
PCB DWG:

PROJECT
Altium
PROJECT REVISION: 1f984ed06d77d23c2cc8004ff5b4b95dbfb3d50195
DOCUMENT REVISION:
DESIGN ITEM:
TITLE
*
SIZE A3 | CAGE CODE | DWG NO. | REV
SCALE: | FILE NAME smartport_inverter.SchDoc | SHEET * OF *


V-Core both sides full length of pcb
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SmartPort_Inverter
R3
R2
R1
Q1
Q2
J1
SP
TX
RX
5V
GND


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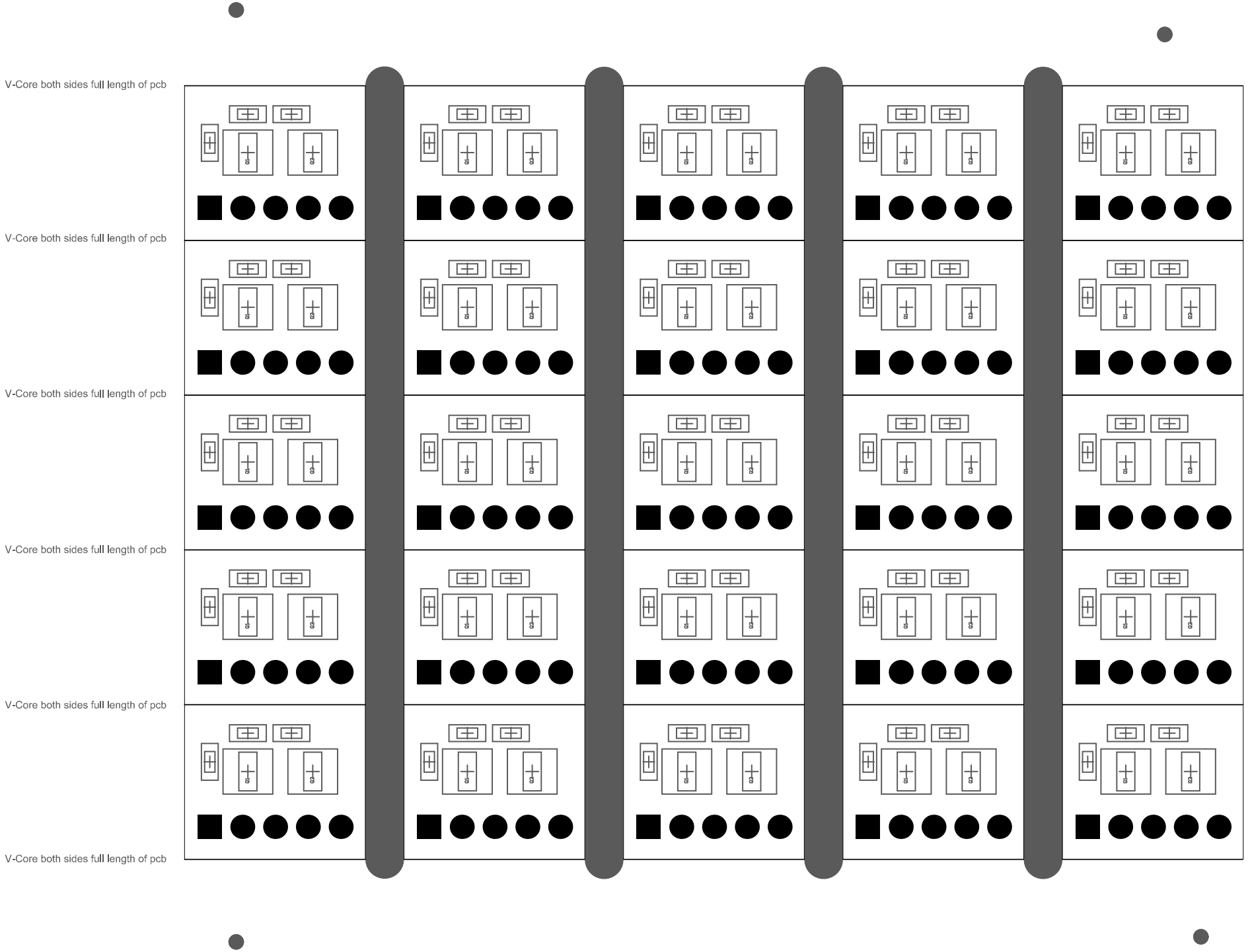
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Comment	Description	Designator	Footprint	LibRef	Quantity
61300511121	Headers & Wire Housings WR-PHD 2.54mm Hdr 5P Single Str Gold	J1	61300511121	61300511121	1
2N7002-7-F	MOSFET N-CH 60V 200MA SOT23-3	Q1, Q2	SOT23-3N	2N7002-7-F	2
4.7k	Resistor 4.7k 0603 +- 1% 0.1	R1, R2	R0603	RES_YAG_RC0603FR-074K7L	2
47k	Resistor 47k 0603 +- 1% 0.1	R3	R0603	RES_YAG_RC0603FR-0747KL	1

Design Rules Verification Report

Filename : C:\github\rcmodel\smartport\smartport_inverter_Panel5X5.PcbDoc

Warnings 0
Rule Violations 6

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.35mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	3
Width Constraint (Min=0.1mm) (Max=5mm) (Preferred=0.15mm) (All)	0
Width Constraint (Min=0.1mm) (Max=1mm) (Preferred=0.15mm) (WithinRoom('BGA'))	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.1mm) (Max=10mm) (Prefered=0.1mm) and	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.1mm) (Max=0.16mm) (Prefered=0.1mm) and	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.1mm) (Max=10mm) (Prefered=0.1mm) and	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.1mm) (Max=10mm) (Prefered=0.1mm) and	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.1mm) (Max=10mm) (Prefered=0.1mm) and	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.5mm) (Conductor Width=0.25mm) (Air Gap=0.25mm)	0
Minimum Annular Ring (Minimum=0.35mm) (OnLayer('Mid-Layer 2'))	0
Minimum Annular Ring (Minimum=0.1mm) (All)	3
Minimum Annular Ring (Minimum=0.35mm) (OnLayer('Mid-Layer 1'))	0
Hole Size Constraint (Min=0.2mm) (Max=15mm) (All)	0
Hole Size Constraint (Min=0.1mm) (Max=2.5mm) (isVia And WithinRoom('MCU_IO'))	0
Hole To Hole Clearance (Gap=0.4mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.07mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Net Antennae (Tolerance=20mm) (InNetClass('JTAG'))	0
Matched Lengths(Tolerance=8mm) (InNetClass('RMII'))	0
Matched Lengths(Tolerance=14.2mm) (InDifferentialPair ('USB_D'))	0
Matched Lengths(Tolerance=1.27mm) (InNetClass('Flash'))	0
Matched Lengths(Tolerance=2.3mm) (InDifferentialPairClass('DP_ETH'))	0
Matched Lengths(Tolerance=10mm) (InNetClass('SSD'))	0
Matched Lengths(Tolerance=10mm) (InNetClass('XIP'))	0
Matched Lengths(Tolerance=8mm) (InNetClass('SD'))	0
Matched Lengths(Tolerance=2mm) (InNetClass('MD'))	0
Total	6

Un-Routed Net Constraint ((All))
Un-Routed Net Constraint: Via (75.725mm,-3mm) from Top Layer to Bottom Layer Dead Copper - Net Not Assigned.
Un-Routed Net Constraint: Via (7mm,-3.4mm) from Top Layer to Bottom Layer Dead Copper - Net Not Assigned.
Un-Routed Net Constraint: Via (7mm,62.875mm) from Top Layer to Bottom Layer Dead Copper - Net Not Assigned.

Minimum Annular Ring (Minimum=0.1mm) (All)
Minimum Annular Ring: (No Ring) Via (75.725mm,-3mm) from Top Layer to Bottom Layer (Annular Ring missing on Top Layer)
Minimum Annular Ring: (No Ring) Via (7mm,-3.4mm) from Top Layer to Bottom Layer (Annular Ring missing on Top Layer)
Minimum Annular Ring: (No Ring) Via (7mm,62.875mm) from Top Layer to Bottom Layer (Annular Ring missing on Top Layer)