SYNCOAM Co., Ltd

Version: 1.8
Date: Dec. 10th, 2008

SEPS114A

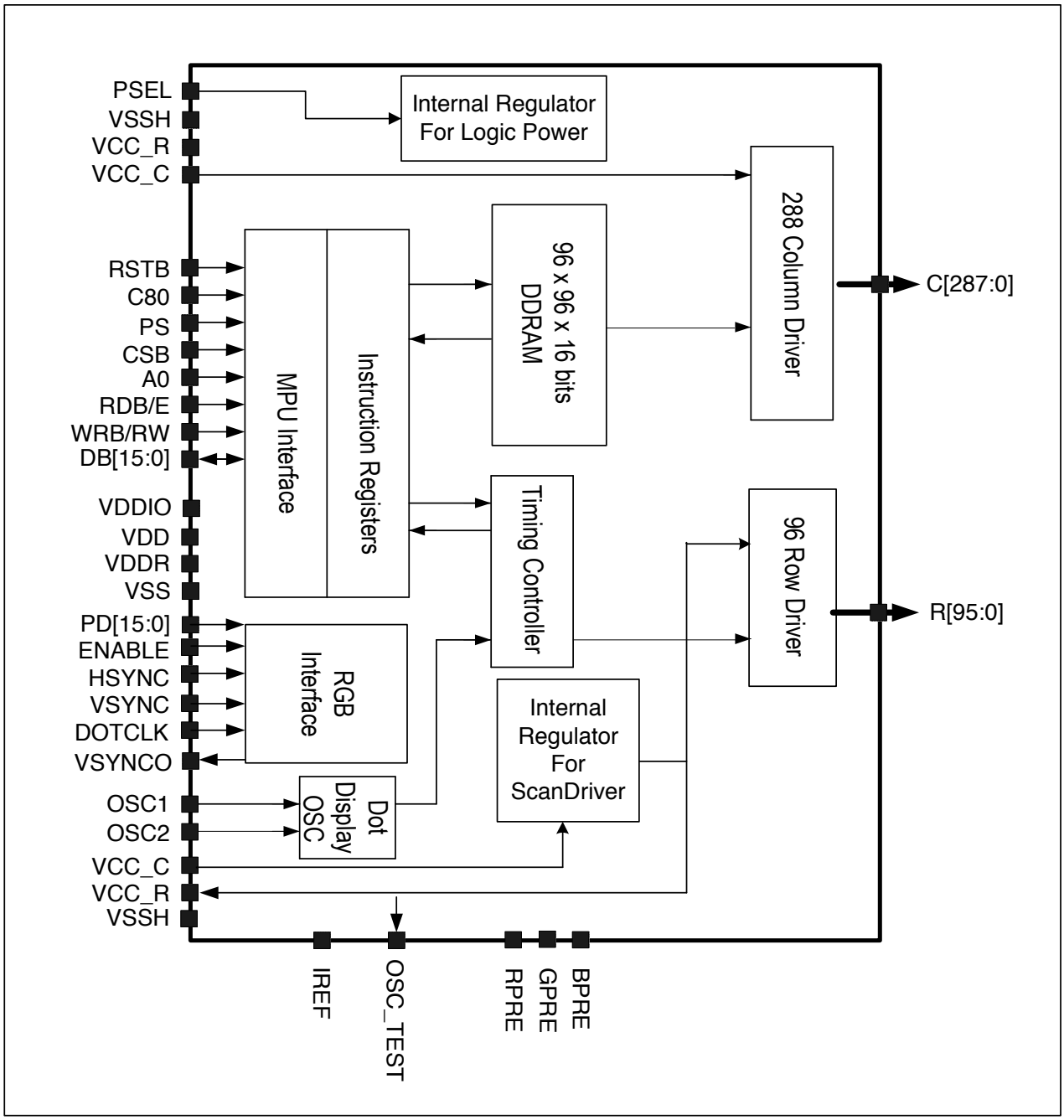
96 x 96 Dots, 65K Colors PM-OLED Display Driver and Controller

1. Product Preview

- 65k colors OLED single chip display driver IC
- Data Interface
  - Parallel interface : 68/80series MPU(8/16/6(RGB)/6(BGR)-bit)
  - Serial interface : SPI 4-wire interface
  - RGB interface : 8/16/6(RGB)/6(BGR)-bit
- Driver Output
  - 96× RGB columns(288), 96 rows
- Display RAM Capacity
  - 96 × 16(RGB) × 96 = 147,456 bits
- Various Instructions Set
  - Power save mode
  - Reduced current driving available
  - Window mode
  - Partial display : programmable panel display size
  - Screen Saver (Vertical scroll, Horizontal panning, Fade in/out)
- OLED Column drive
  - Discharge time control : Discharge time(0clock ~ 30clocks) with internal oscillator clock
  - Pre-charge peak control :
    - Peak pulse delay time : (0clock ~ 15clocks) with internal oscillator clock
    - Peak pulse width time : (0clock ~ 31clocks) with internal oscillator clock
  - Pre-charge current control : 8-bit, 0uA ~ 1020uA by 4uA step control
  - Driving current control : 8-bit, 0uA ~ 188.7uA by 0.74uA step control
- OLED Row drive
  - Current sink : Max 50mA
- Oscillator Circuit
  - Internal / External clock selectable
  - Frame rate : 95 frames/sec (80.0 ~ 140.0 frames/sec adjustable)
- Supply Voltage
  - VDDIO: 1.65V ~ 3.3V
  - VDD : 2.4V ~ 3.3V
  - VCC : 8.0V ~ 18.0V
- Package : Au Bumped
- Ordering information

SEPS114AF	COF Package
SEPS114AG	COG Package

2. Block Diagram



3. Pin Description

<table>
<tr><th>Pin Name</th><th>Pins</th><th>I/O</th><th>Connected To</th><th>Description</th></tr>
<tr><td>C80</td><td>1</td><td>I</td><td>VSS or VDDIO</td><td>Selects the MPU type
Low : 80-Series Interface, High : 68-Series Interface</td></tr>
<tr><td>PS</td><td>1</td><td>I</td><td>VSS or VDDIO</td><td>Selects parallel/Serial interface type
Low : serial, High : parallel</td></tr>
<tr><td>CSB</td><td>1</td><td>I</td><td>MPU</td><td>Selects the SEPS114A
Low : SEPS114A is selected and can be accessed
High : SEPS114A is not selected and cannot be accessed</td></tr>
<tr><td>A0</td><td>1</td><td>I</td><td>MPU</td><td>Selects the data / command
Low : command, High : parameter / data</td></tr>
<tr><td>RDB/E</td><td>1</td><td>I</td><td>MPU</td><td>For an 80-serise bus interface, read strobe signal (active low)
For an 68-serise bus interface, bus enable strobe (active high)
When using SPI, fix it to VDDIO or VSS level</td></tr>
<tr><td>WRB/RW</td><td>1</td><td>I</td><td>MPU</td><td>For an 80-serise bus interface, write strobe signal (active low)
For an 68-serise bus interface, read/write select
Low : Write, High : Read
When using SPI, fix it to VDDIO or VSS level</td></tr>
<tr><td>RSTB</td><td>1</td><td>I</td><td>MPU</td><td>Reset SEPS114A(active low)</td></tr>
<tr><td>DB[15:0]</td><td>16</td><td>I/O</td><td>MPU</td><td>Serves as a 16_bit bi-directional data bus
<table>
<tr><th>PS</th><th>Description</th></tr>
<tr><td>1</td><td>8_bit bus : DB[7:0]
16_bit bus : DB[15:0]
6_bit bus : DB[5:0] for RGB/BGR</td></tr>
<tr><td>0</td><td>DB[0] SCL : Serial clock input
DB[1] SDI : Serial data input
DB[2] SDO : Serial data output
DB[3] R/W : Serial Read/Write
0 : Write, 1 : Read</td></tr>
</table>
Fix unused pins to the VSS level</td></tr>
<tr><td>PD[15:0]</td><td>16</td><td>I</td><td>RGB Interface</td><td>8_bit RGB bus : PD[7:0], 16_bit RGB bus : PD[15:0]
6_bit RGB bus : PD[5:0], 6_bit GBR bus : PD[5:0]</td></tr>
<tr><td>OSC1</td><td>1</td><td>I</td><td rowspan="2">Oscillation-Resistor</td><td rowspan="2">Fine adjustment for oscillation
Tie 27 kΩ to OSC1 between OSC2
When the external clock mode is selected, OSC1 is used external clock input</td></tr>
<tr><td>OSC2</td><td>1</td><td>O</td></tr>
<tr><td>OSC TEST</td><td>1</td><td>O</td><td>Floating</td><td>OSC Test</td></tr>
<tr><td>C[287:0]</td><td>288</td><td>O</td><td>PANEL</td><td>SEPS114A Display column outputs</td></tr>
<tr><td>R[95:0]</td><td>96</td><td>O</td><td>PANEL</td><td>SEPS114A Display row outputs</td></tr>
<tr><td>VCC_C</td><td>2</td><td>P</td><td>POWER</td><td>Data Driver Power Supply(8V ~ 18V)</td></tr>
<tr><td>VCC_R</td><td>2</td><td>P</td><td>POWER</td><td>Power Supply for Scan Driver</td></tr>
<tr><td>VDDR</td><td>1</td><td>P</td><td>POWER</td><td>Logic Power Supply2</td></tr>
<tr><td>VDD</td><td>1</td><td>P</td><td>POWER</td><td>Logic Power Supply(2.4V ~ 3.3V)</td></tr>
<tr><td>PSEL</td><td>1</td><td>I</td><td>VDD or VSS</td><td>Regulator Enable/Disable for Logic Power Supply2</td></tr>
<tr><td>VSS</td><td>4</td><td>P</td><td>POWER</td><td>Ground for VDD/VDDR</td></tr>
<tr><td>VSSH</td><td>4</td><td>P</td><td>POWER</td><td>Ground for VCC_C/VCC_R</td></tr>
<tr><td>VDDIO</td><td>2</td><td>P</td><td>POWER</td><td>MPU I/F PAD Power Supply(1.65V ~ 3.3V)
VDDIO should be lower than VDD or the same as VDD.</td></tr>
<tr><td>IREF</td><td>1</td><td>-</td><td>Resister</td><td>Tie 39 kΩ to VSS</td></tr>
<tr><td>BPRE</td><td>1</td><td>-</td><td>Zener or VSSH</td><td>Pre-Charge Voltage for Bule</td></tr>
<tr><td>GPRE</td><td>1</td><td>-</td><td>Zener or VSSH</td><td>Pre-Charge Voltage for Green</td></tr>
<tr><td>RPRE</td><td>1</td><td>-</td><td>Zener or VSSH</td><td>Pre-Charge Voltage for Red</td></tr>
<tr><td>VSYNCO</td><td>1</td><td>O</td><td>Floating</td><td>Vertical Sync. Output</td></tr>
<tr><td>VSYNC</td><td>1</td><td>I</td><td>MPU or VDDIO</td><td>Vertical Sync. Input when RGB mode is selected</td></tr>
<tr><td>HSYNC</td><td>1</td><td>I</td><td>MPU or VDDIO</td><td>Horizontal Sync. Input when RGB mode is selected</td></tr>
<tr><td>DOTCLK</td><td>1</td><td>I</td><td>MPU or VDDIO</td><td>Dot clock Input when RGB mode is selected</td></tr>
<tr><td>ENABLE</td><td>1</td><td>I</td><td>MPU or VDDIO</td><td>Video enable Input when RGB mode is selected</td></tr>
</table>

4. Functional Description

MPU Interface

The SEPS114A has three high-speed system interface : a 68-serise, an 80-serise 8/16/6(RGB/BGR) bit bus, and a clock synchronous serial SPI (Serial Peripheral Interface). Among the interface modes, a specific mode is selected by the setting of PS pin and CPU_IF register(0Dh).

The SEPS114A has 3-type registers : an index register(IR) 8-bits, a write data register(WDR), and a read data register(RDR). The IR stores index information for the control registers and the DDRAM. The WDR temporarily stores data to be written into control registers and the DDRAM.

The RDR temporarily stores data read from the DDRAM.

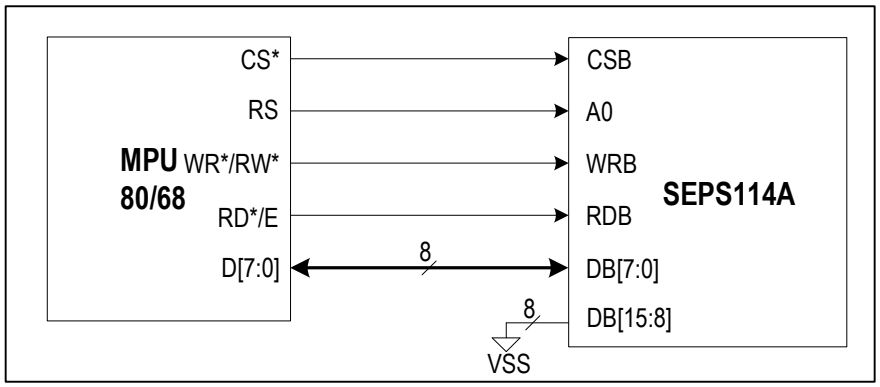
Data written into the DDRAM from the MPU is first written into the WDR and then it is automatically written into the DDRAM by internal operation. Data is read through the RDR when reading from the DDRAM, and the first read data is invalid and the second and the following data are valid.

Truth Table of Parallel Interface

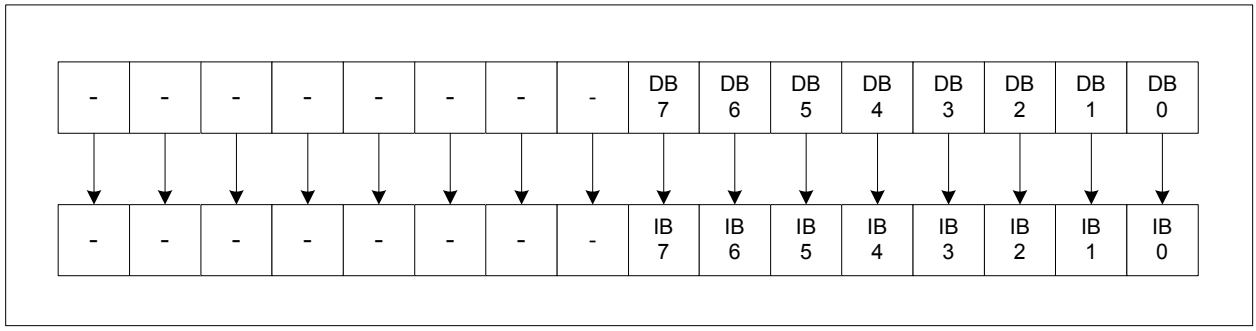
80-series		68-series		A0	C80	Operation
WRB	RDB	RW	E			
0	1	-	-	0	0	Write command(indexes) into IR
0	1	-	-	1	0	Write into control registers and DDRAM through WDR
1	0	-	-	1	0	Read from control registers and DDRAM through RDR
-	-	0	1	0	1	Write command(indexes) into IR
-	-	0	1	1	1	Write into control registers and DDRAM through WDR
-	-	1	1	1	1	Read from DDRAM through RDR

1) 8-bit Bus Interface

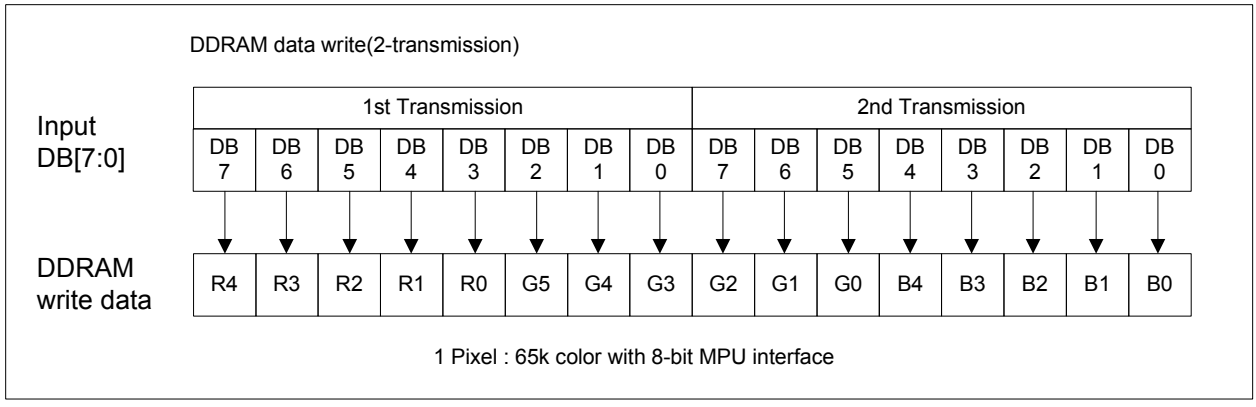
CIF1	CIF0	Operation(0Dh)
0	0	8-bit bus operation



Index/Command Write

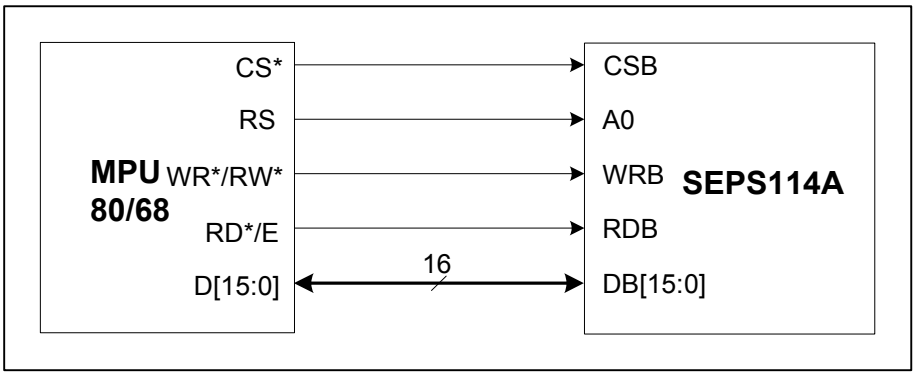


DDRAM Read/Write

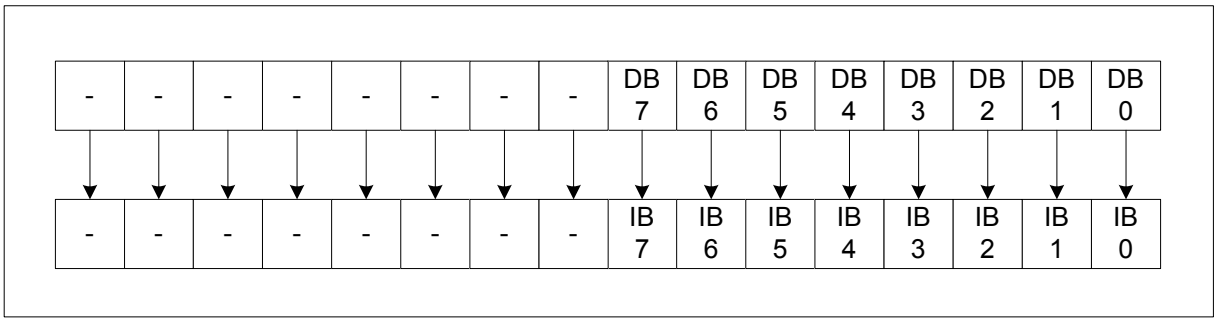


2) 16-bit Bus Interface

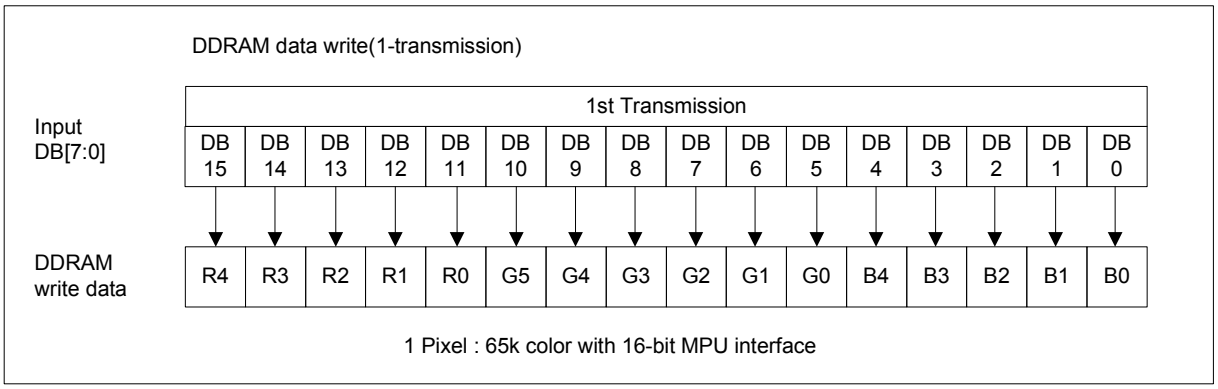
CIF1	CIF0	Operation(0Dh)
0	1	16-bit bus operation



Index/Command Write

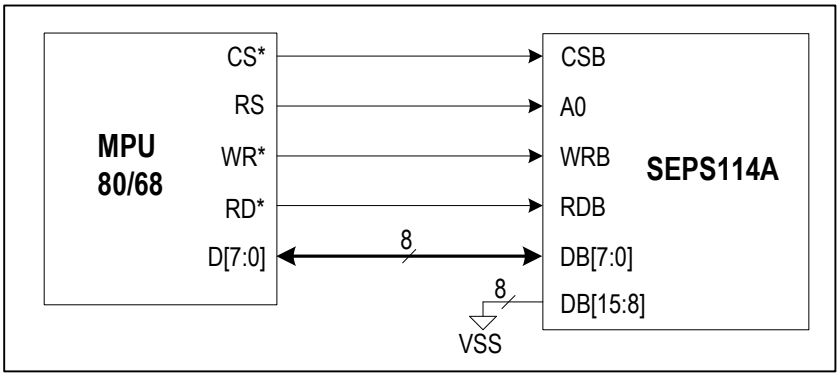


DDRAM Read/Write

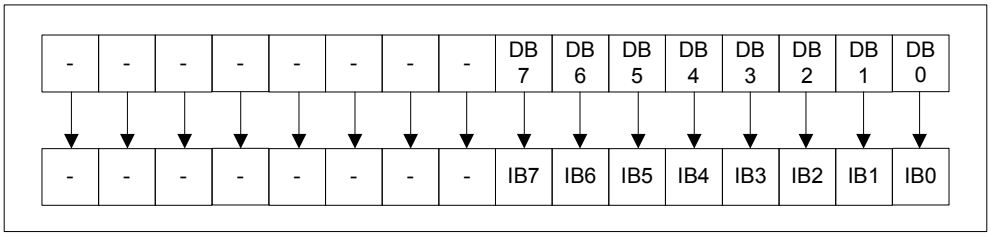


3) 6-bit Bus Interface

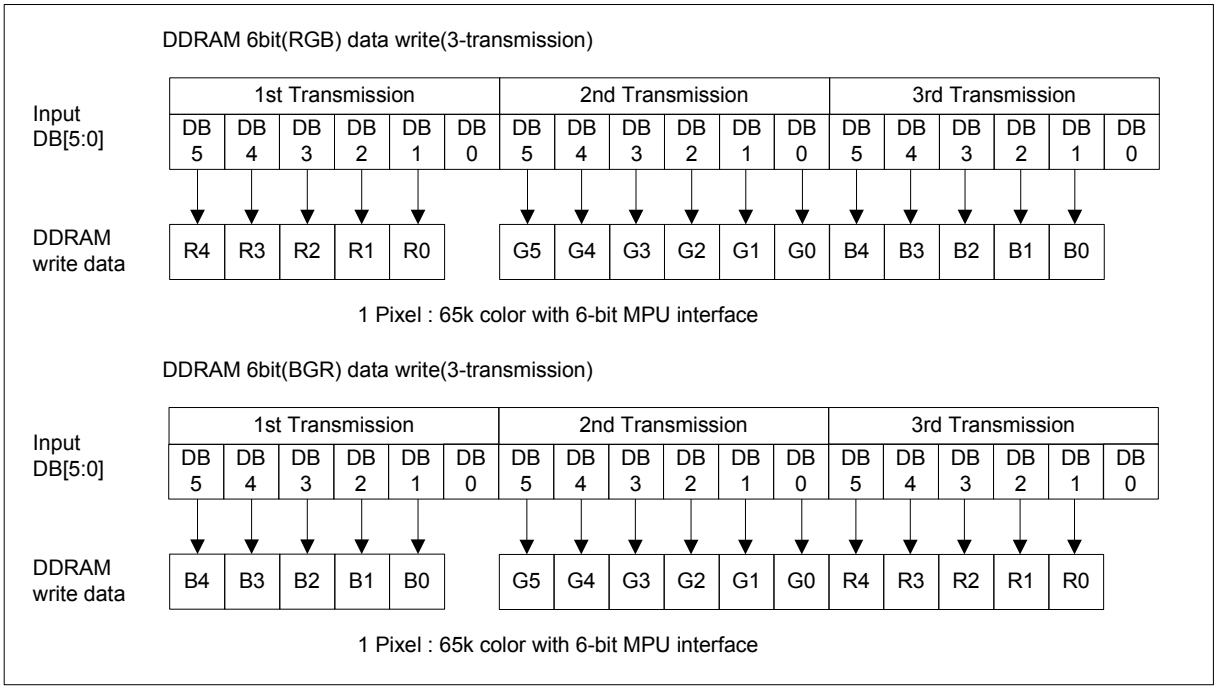
CIF1	CIF0	Operation(0Dh)
1	0	6-bit(RGB) bus operation
1	1	6-bit(BGR) bus operation



Index/Command Write



DDRAM Write/Read



5) Clock Synchronized Serial Interface (SPI)

Setting PS to the '0' level allows clock synchronized serial data(SPI) transfer, using the chip select pin(CSB) , A0 pin, serial clock pin(SCL) and serial data input(SDI).

When chip is not selected, internal shift register and counter are reset to initial value. Input data through SDI pin are latched at the rising edge of serial clock(SCL) in the sequence of MSB first and converted to 8 -bit parallel data and handled at the rising edge of last serial clock.

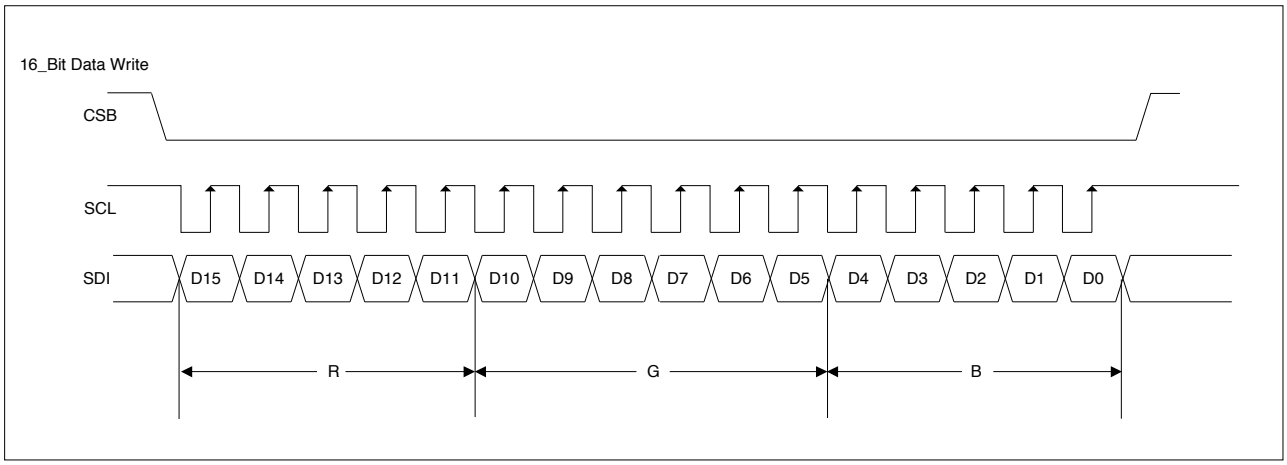
Serial data input (SDI) are identified to display data or command by A0 bit data at the rising of first serial clock(SCL).

A0	Function
L	Command
H	Parameter/ Data

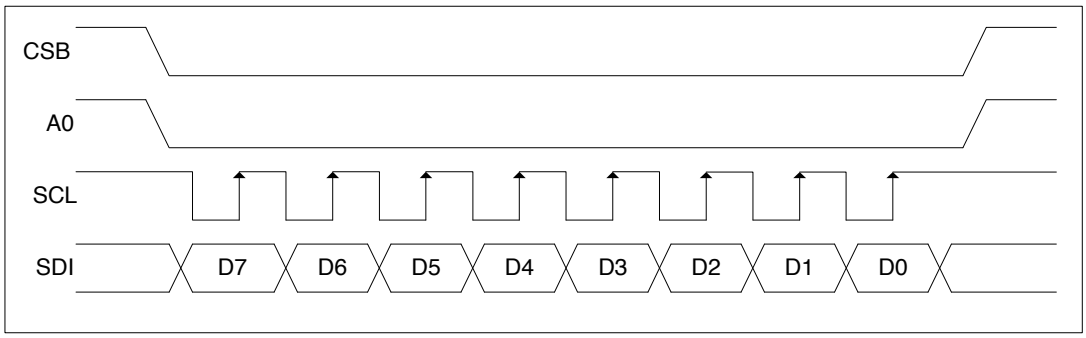
After 16-bit data transfer, serial clock(SCL) should be high-level at the non-access period. SDI and SCL signals are sensitive to external noise. To prevent miss operation chip select state should be released(CSB = "H") after 16-bit data transfer as shown in the following.

*Note : When the SPI mode is selected, DB[2]-SDO pin must be unconnected.

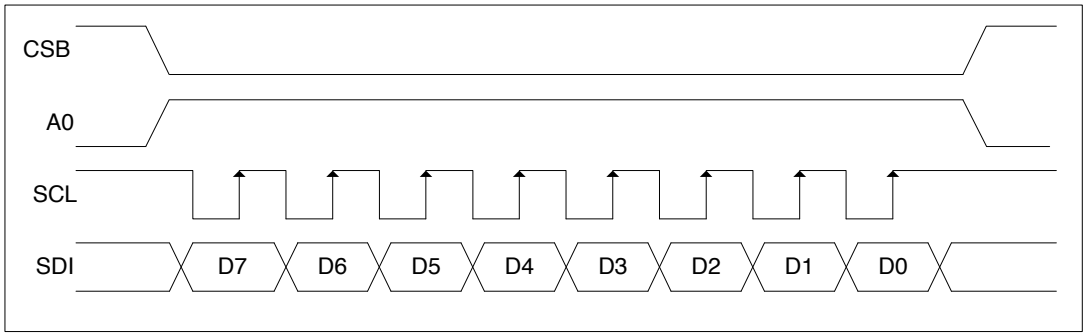
PS = "0"



INDEX REGISTER WRITE

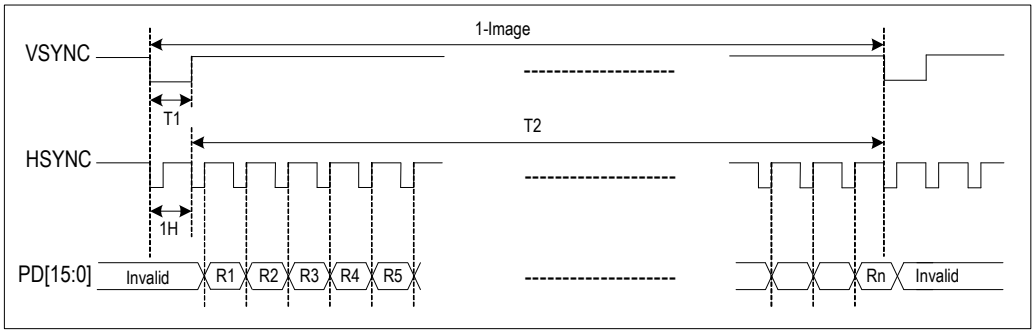


CONTROL REGISTER WRITE



6) RGB Interface

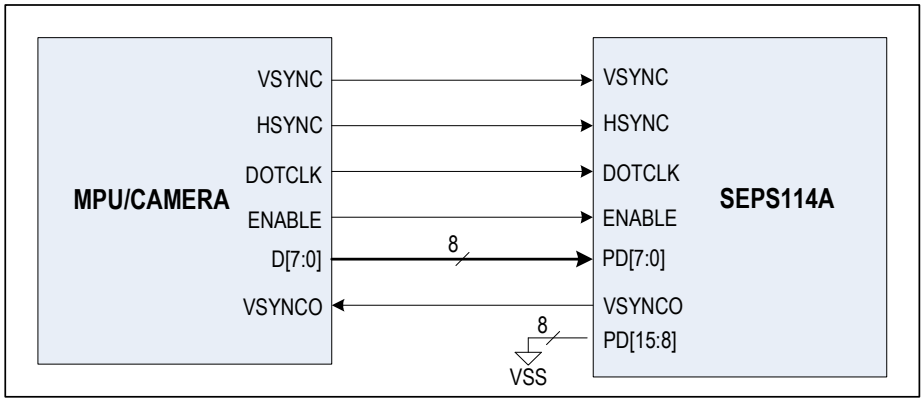
When the RGB_IF register(E0h) bit0 is set to "1", SEPS114A enters into the RGB interface mode and DDRAM write cycle is synchronized by DOTCLK.



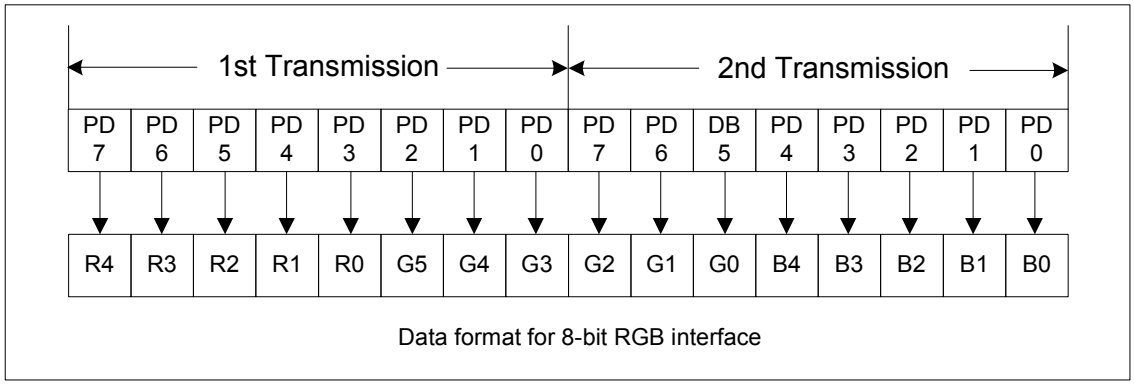
Symbol	Description	Remark
T1	VSYNC Pulse Width	≥ 1H, n*1H
T2	DDRAM Write Width	≤ 96H

8-bit RGB interface

The 8-bit RGB interface is selected by setting RIM[1:0] bits to "00". DDRAM write operation is synchronized with DOTCLK and ENABLE. Display data are transmitted to DDRAM in synchronization with 8-bit RGB data bus(PD[7:0]) and the data enable(ENABLE).

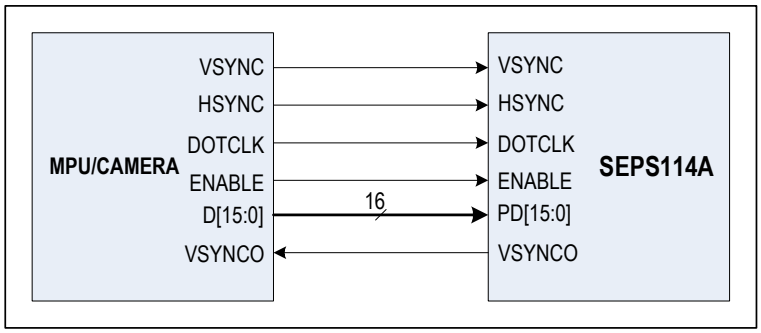


DDRAM Write

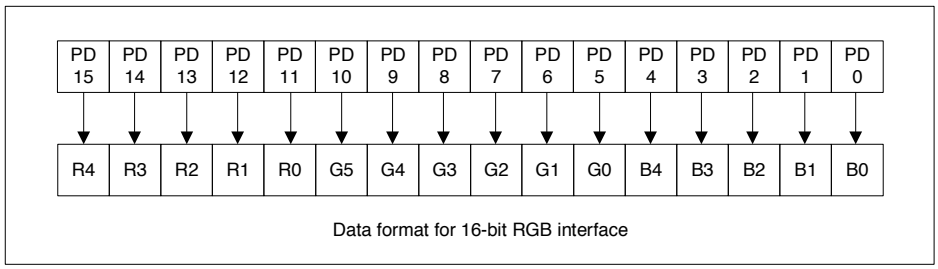


16-bit RGB interface

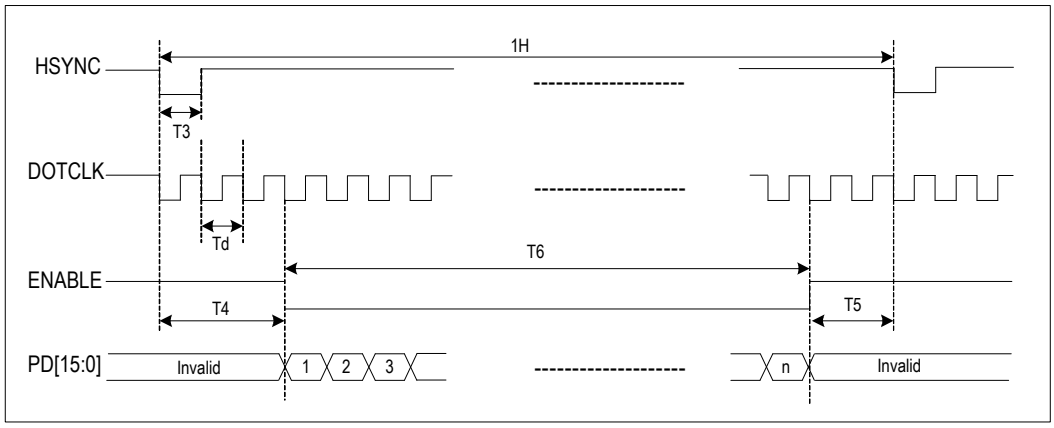
The 16-bit RGB interface is selected by setting RIM[1:0] bits to "01". DDRAM write operation is synchronized with DOTCLK and ENABLE. Display data are transmitted to DDRAM in synchronization with 16-bit RGB data bus (PD[15:0]) and the data enable (ENABLE).



DDRAM Write



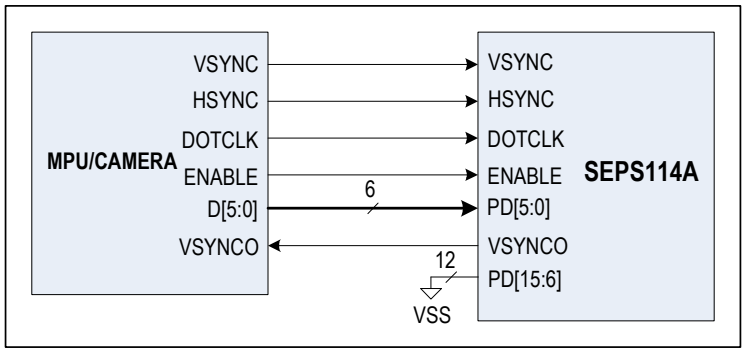
16-bit RGB interface timing



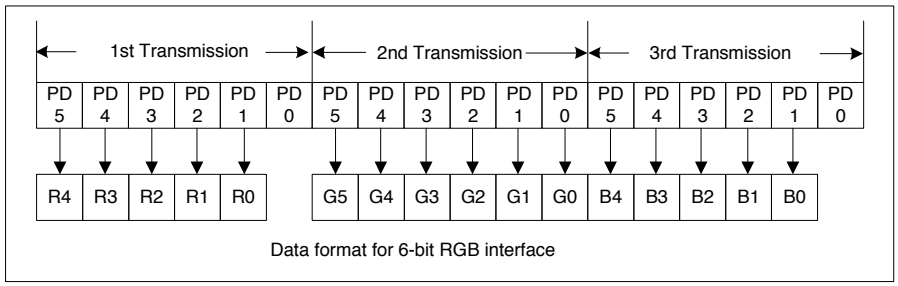
Symbol	Description	Remark
T3	HSYNC Pulse Width	≥ Td, n*Td
T4	Setup time for Data transfer	≥ 2Td, T4>T3
T5	Hold time for Data transfer	≥ 2Td, T5>T3
T6	DDRAM Write Width	≤ 96Td
T6 = n, Td ≥ 100ns		

6-bit RGB interface

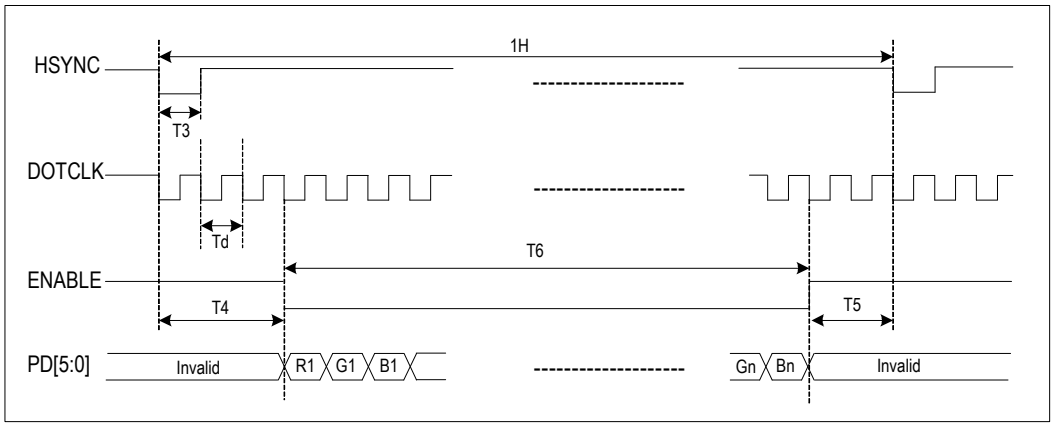
The 6-bit RGB interface is selected by setting RIM[1:0] bits to "10". DDRAM write operation is synchronized with DOTCLK and ENABLE. Display data are transmitted to DDRAM in synchronization with 6-bit RGB data bus(PD[5:0]) and the data enable(ENABLE).



DDRAM Write



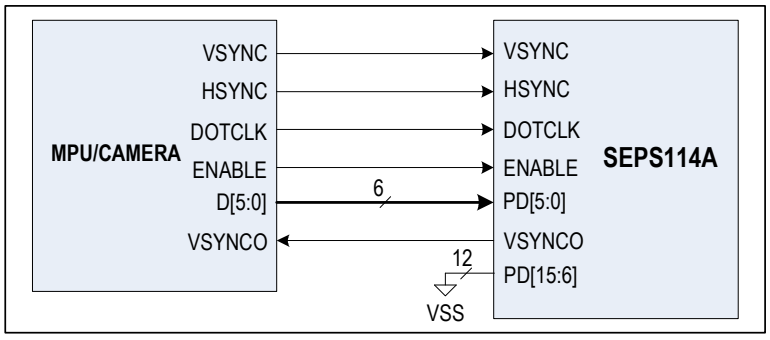
6-bit RGB interface timing



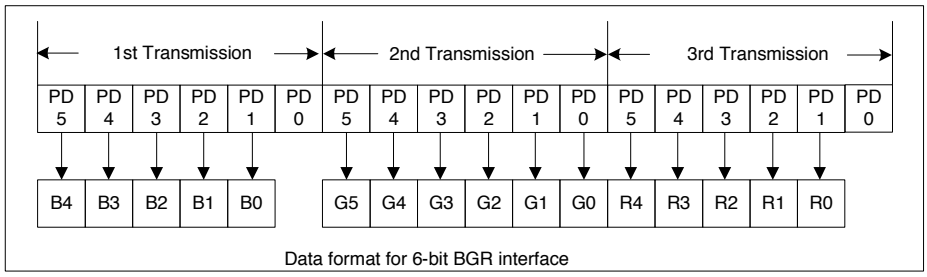
Symbol	Description	Remark
T3	HSYNC Pulse Width	≥ Td, n*Td
T4	Setup time for Data transfer	≥ 2Td, T4>T3
T5	Hold time for Data transfer	≥ 2Td, T5>T3
T6	DDRAM Write Width	≤ 288Td
T6 = 3n, Td ≥ 100ns		

6-bit BGR interface

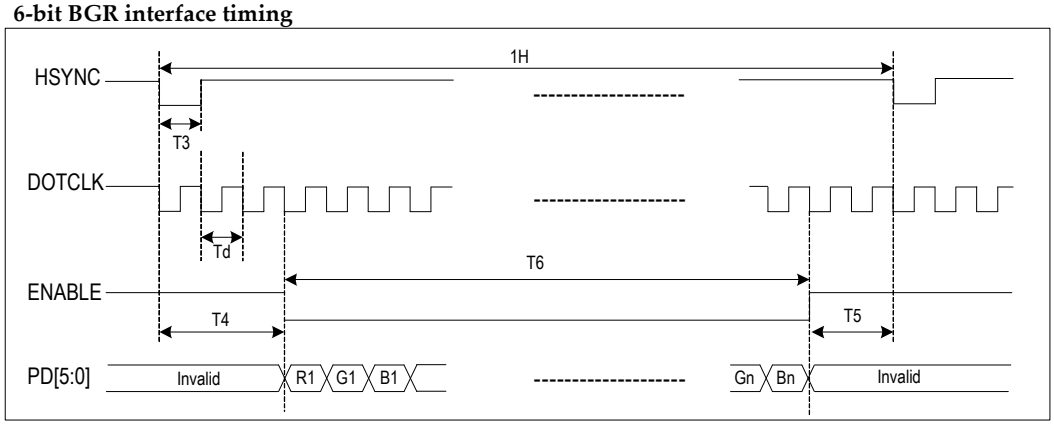
The 6-bit BGR interface is selected by setting RIM[1:0] bits to "11". DDRAM write operation is synchronized with DOTCLK and ENABLE. Display data are transmitted to DDRAM in synchronization with 6-bit RGB data bus(PD[5:0]) and the data enable(ENABLE).



DDRAM Write



6-bit BGR interface timing



Symbol	Description	Remark
T3	HSYNC Pulse Width	≥ Td, n*Td
T4	Setup time for Data transfer	≥ 2Td, T4>T3
T5	Hold time for Data transfer	≥ 2Td, T5>T3
T6	DDRAM Write Width	≤ 288Td
T6 = 3n, Td ≥ 100ns		

DDRAM(Display Data RAM) Addressing

The DDRAM stores pixel data for the display. It is composed of 96-row by 96-column x 16-bit addressable array. Address counter provides row and column address to DDRAM for access display pixel data from MPU.

Relationship between DDRAM Address and Display Position

SCAND=0	SCAND=2	Column Data	0	1	2	3	----------	92	93	94	95
G0	G95	00h					----------				
G1	G94	01h									
G2	G93	02h									
G3	G92	03h									
G4	G91	04h									
G5	G90	05h									
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
G90	G5	59h									
G91	G4	5Ah									
G92	G3	5Bh									
G93	G2	5Ch									
G94	G1	5Eh									
G95	G0	5Fh									

D0	D1	D2	D3	----------	D92	D93	D94	D95
C0	C1	C2				C285	C286	C287

SCAND[1:0] : Row scan direction register(09h).

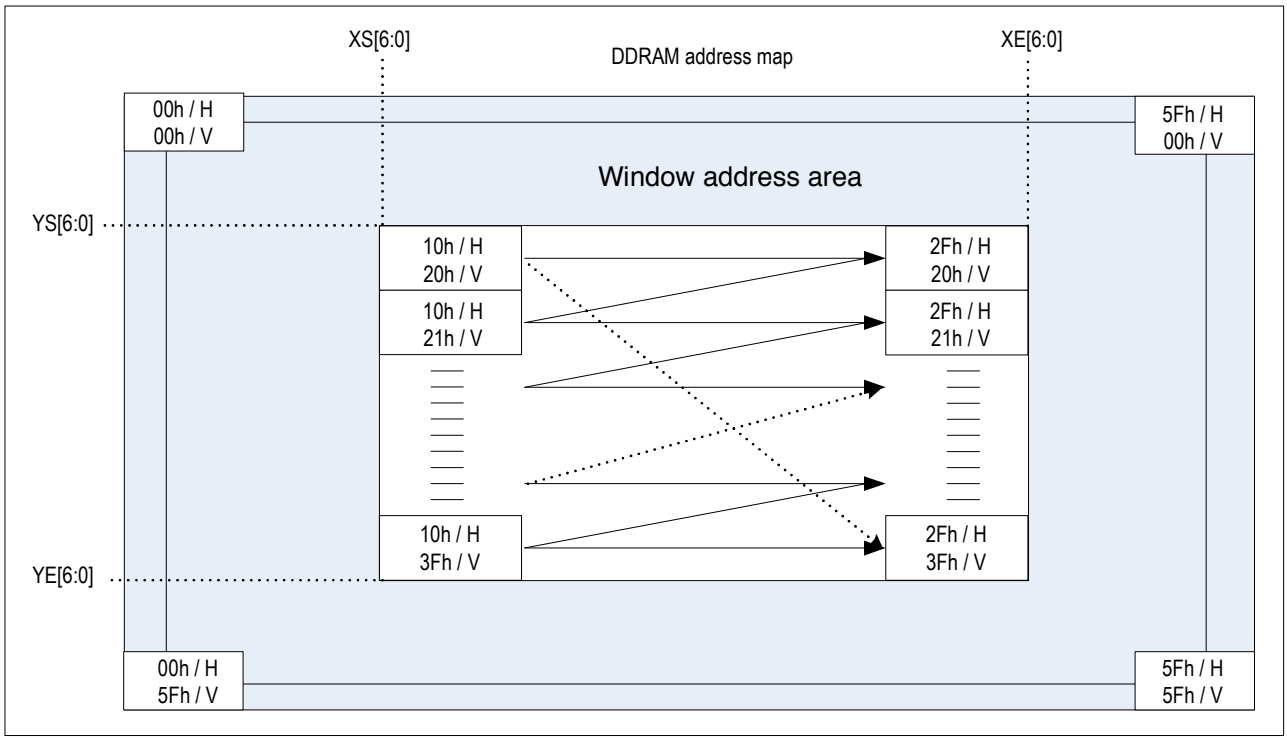
Window Address Function for DDRAM Write

When data is written to the on-chip DDRAM, a window address-range which is specified by the horizontal address register(start : XS[6:0], end : XE[6:0]) or the vertical address register(start : YS[6:0], end : YE[6:0]) can be written to consecutively. Data is written to addresses in the direction specified by the MDIR1, MDIR0(increment/decrement), and VH bit(V or H direction). When the image data is being written, data can be written consecutively without thinking of a data wrap by doing this.
The window must be specified within the DDRAM address area described below, Addresses must be set within the window address.

[Restriction on window address-range setting]
(horizontal direction) 00h≤ XS[6:0] < XE[6:0] ≤ 5Fh
(vertical direction) 00h ≤ YS[6:0] < YE[6:0] ≤ 5Fh

Window address-range specification.
XS [6:0] = 10h, XE [6:0] = 2Fh MDIR1, MDIR0 = 0,0 (increment)
YS [6:0] = 20h, YE [6:0] = 3Fh VH = 0 (horizontal writing)

Example of Address Operation in the Window Address Specification



Reset Status

The **SEPS114A** is initialized as following description when RSTB pin is set to "L". Usually RSTB pin is connected reset pin of MPU, so that the chip can be initialized simultaneously with MPU. The **SEPS114A** should be initialized when the power is on.

INITIAL SETTING CONDITION (default setting)

1. Standby mode : ON
2. Frame frequency : 95Hz
3. OSC mode : internal OSC
4. Internal OSC : OFF
5. DDRAM write horizontal address : XS = 00h, XE = 5Fh
6. DDRAM write vertical address : YS = 00h, YE = 5Fh
7. Display data RAM write : MDIR1 = 0, MDIR0 = 0, VH = 0
8. Row scan direction : R0, R1, … , R94, R95
9. Column data direction : C0, C1, … , C286, C287
10. Display ON/OFF : OFF
11. Panel display size : FX = 00h, TX = 5Fh, FY = 00h, TY = 5Fh
12. Display data RAM read column/row address : DX = 00h, DY = 00h
13. Discharge time : 8 clock
14. Peak pulse delay : 5 clock
15. Peak pulse width time (R/G/B) : 5 clock
16. Precharge current (R/G/B) : 0 uA
17. Driving current (R/G/B) : 0 uA

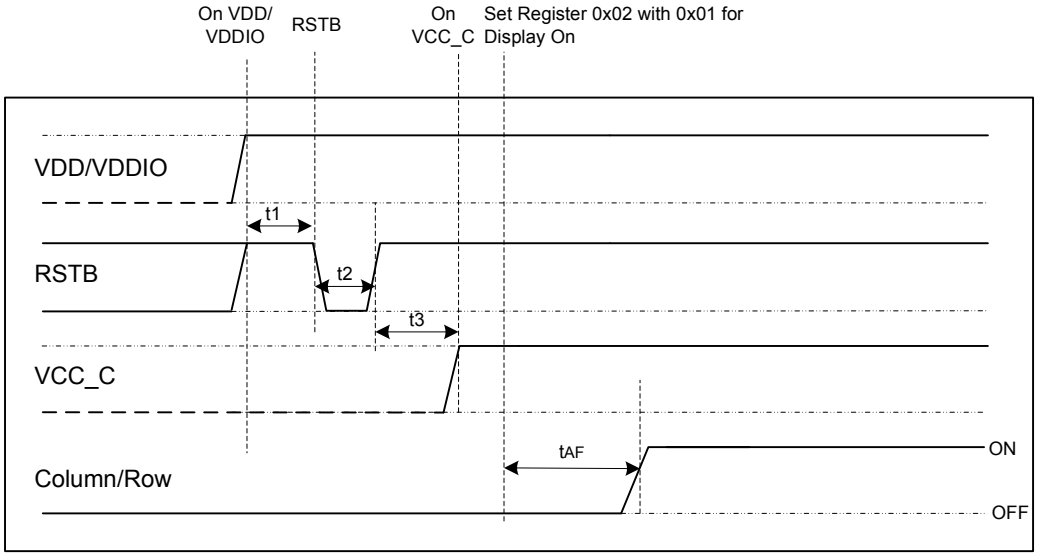
POWER ON/OFF SEQUENCE

Power ON sequence

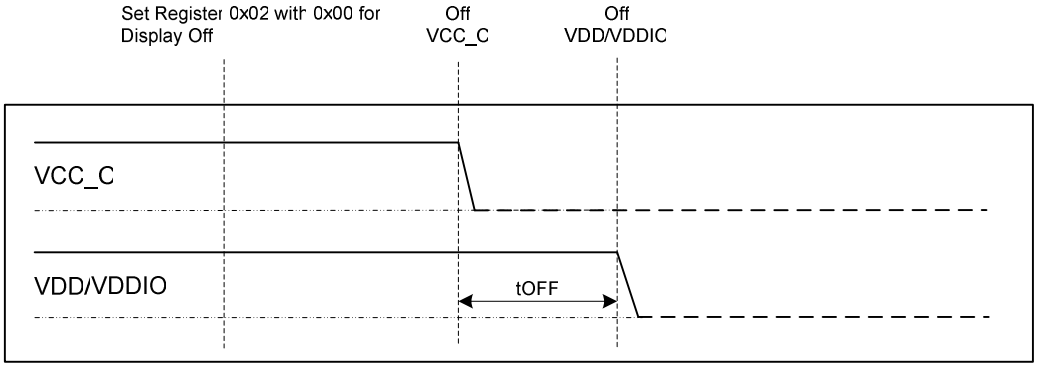
(1) Power ON VDD, VDDIO.
(2) After VDD, VDDIO become stable and wait for 100ms(t1), set RSTB pin LOW (logic low) for at least 1ms (t2) and then HIGH(logic high).
(3) After set RSTB pin HIGH (logic high), wait for at least 50ms (t3). Then Power ON VCC_C
(4) After VCC_C become stable, set register 0x02 with value 0x01 for display ON. Data/Scan will be ON after 200ms (tAF).

Power OFF sequence

(1) Set register 0x02 with value 0x00 for display OFF.
(2) Power OFF VCC_C
(3) Wait for tOFF. Power OFF VDD, VDDIO (where Minimum tOFF=0ms, Typical tOFF=100ms)



<Power On Sequence>



<Power Off Sequence>

Note :

Since ESD protection circuit is connected between VDD, VDDIO and VCC_C, VCC_C becomes lower than VDD whenever VDD, VDDIO is ON and VCC_C is OFF. VCC_C should be kept disable when it is OFF.

5. Instruction Description

Normal Display

ADDR	RW	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	Description	Default
01h	W	IDX[7]	IDX[6]	IDX[5]	IDX[4]	IDX[3]	IDX[2]	IDX[1]	IDX[0]	SOFT_RESET	00h
02h	R/W	-	-	-	-	-	-	-	DON	DISP_ON_OFF	00h
0Fh	R/W	SELEXP	SELRES	SELCLK	-	-	-	-	IREF	ANALOG_CONTROL	80h
14h	R/W	-	-	-	-	-	-	-	STB	STANDBY_ON_OFF	01h
1Ah	R/W	-	-	-	-	FR[3]	FR[2]	FR[1]	FR[0]	OSC_ADJUST	03h
09h	R/W	-	-	-	-	-	-	SCAND[1]	SCAND[0]	ROW_SCAN_DIRECTION	00h
30h	R/W	-	FX[6]	FX[5]	FX[4]	FX[3]	FX[2]	FX[1]	FX[0]	DISPLAY_X1	00h
31h	R/W	-	TX[6]	TX[5]	TX[4]	TX[3]	TX[2]	TX[1]	TX[0]	DISPLAY_X2	5Fh
32h	R/W	-	FY[6]	FY[5]	FY[4]	FY[3]	FY[2]	FY[1]	FY[0]	DISPLAY_Y1	00h
33h	R/W	-	TY[6]	TY[5]	TY[4]	TY[3]	TY[2]	TY[1]	TY[0]	DISPLAY_Y2	5Fh
38h	R/W	-	DX[6]	DX[5]	DX[4]	DX[3]	DX[2]	DX[1]	DX[0]	DISPLAYSTART_X	00h
39h	R/W	-	DY[6]	DY[5]	DY[4]	DY[3]	DY[2]	DY[1]	DY[0]	DISPLAYSTART_Y	00h
0Dh	R/W	-	-	-	-	-	-	CIF[1]	CIF[0]	CPU_IF	00h
34h	R/W	-	XS[6]	XS[5]	XS[4]	XS[3]	XS[2]	XS[1]	XS[0]	MEM_X1	00h
35h	R/W		XE[6]	XE[5]	XE[4]	XE[3]	XE[2]	XE[1]	XE[0]	MEM_X2	5Fh
36h	R/W		YS[6]	YS[5]	YS[4]	YS[3]	YS[2]	YS[1]	YS[0]	MEM_Y1	00h
37h	R/W		YE[6]	YE[5]	YE[4]	YE[3]	YE[2]	YE[1]	YE[0]	MEM_Y2	5Fh
1Dh	R/W						VH	MDIR[1]	MDIR[0]	MEMORY_WRITE/READ	00h
08h	R/W	DDRAM[15:0]								DDRAM_DATA_ACCESS_PORT	00h
18h	R/W				DIS[4]	DIS[3]	DIS[2]	DIS[1]	DIS[0]	DISCHARGE_TIME	08h
16h	R/W					PDLY[3]	PDLY[2]	PDLY[1]	PDLY[0]	PEAK_PULSE_DELAY	05h
3Ah	R/W				PWR[4]	PWR[3]	PWR[2]	PWR[1]	PWR[0]	PEAK_PULSE_WIDTH _R	05h
3Bh	R/W				PWG[4]	PWG[3]	PWG[2]	PWG[1]	PWG[0]	PEAK_PULSE_WIDTH _G	05h
3Ch	R/W				PWB[4]	PWB[3]	PWB[2]	PWB[1]	PWB[0]	PEAK_PULSE_WIDTH _B	05h
3Dh	R/W	PCR[7]	PCR[6]	PCR[5]	PCR[4]	PCR[3]	PCR[2]	PCR[1]	PCR[0]	PRECHARGE_CURRENT_R	00h
3Eh	R/W	PCG[7]	PCG[6]	PCG[5]	PCG[4]	PCG[3]	PCG[2]	PCG[1]	PCG[0]	PRECHARGE_CURRENT_G	00h
3Fh	R/W	PCB[7]	PCB[6]	PCB[5]	PCB[4]	PCB[3]	PCB[2]	PCB[1]	PCB[0]	PRECHARGE_CURRENT_B	00h
40h	R/W	DCR[7]	DCR[6]	DCR[5]	DCR[4]	DCR[3]	DCR[2]	DCR[1]	DCR[0]	COLUMN_CURRENT_R	00h
41h	R/W	DCG[7]	DCG[6]	DCG[5]	DCG[4]	DCG[3]	DCG[2]	DCG[1]	DCG[0]	COLUMN_CURRENT_G	00h
42h	R/W	DCB[7]	DCB[6]	DCB[5]	DCB[4]	DCB[3]	DCB[2]	DCB[1]	DCB[0]	COLUMN_CURRENT_B	00h
48h	R/W							ROW[1]	ROW[0]	ROW_OVERLAP	00h
49h	R/W					SOFF[3]	SOFF[2]	SOFF[1]	SOFF[0]	SCAN_OFF_LEVEL	04h
17h	R/W								SC_ON	ROW_SCAN_ON/OFF	00h
13h	R/W								SCM[0]	ROW_SCAN_MODE	00h
D0h	R/W	SMON			SLON					SCREEN_SAVER_CONTROL	00h
D1h	R/W	STIM[7]	STIM[6]	STIM[5]	STIM[4]	STIM[3]	STIM[2]	STIM[1]	STIM[0]	SS_SLEEP_TIMER	00h
D2h	R/W						SM[2]	SM[1]	SM[0]	SCREEN_SAVER_MODE	00h
D3h	R/W	SSUT[7]	SSUT[6]	SSUT[5]	SSUT[4]	SSUT[3]	SSUT[2]	SSUT[1]	SSUT[0]	SS_UPDATE_TIMER	00h
E0h	R/W			RIM[1]	RIM[0]				EIM	RGB_IF	00h
E1h	R/W	VSOEN	VSOP			VSP	HSP	ENP	DOTP	RGB_POL	00h
E5h	R/W	SWAP		RC[1]	RC[0]			DC[1]	DC[0]	DISPLAY_MODE_CONTROL	00h

SOFT_RESET (01h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
W	IDX7	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0
Default	-	-	-	-	-	-	-	-

Soft Reset	Actions						
ON	Standby	Display	Internal OSC	GRAM	ALL Reg	Row	Col
	ON	OFF	STOP	Keep	Default	GND	Zener

DISPLAY_ON_OFF (02h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	-	-	-	-	-	-	DON
Default	-	-	-	-	-	-	-	0

DON : Display ON/OFF.

DON	Actions						
0 : OFF	Internal OSC	GRAM	ALL Reg	Row	Col	Data Transfer	Analog Logic
	RUN	Keep	Keep	GND	Zener	STOP	Reset

ANALOG_CONTROL (0Fh)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	SELEXP	SELRES	SELCLK	-	-	-	-	IREF
Default	1	0	0	-	-	-	-	0

SELEXP	EXPORT1
0	Internal clock
1	0

SELRES	Resister
0	External
1	Internal

SELCLK	Clock Source
0	OSC
1	External CLK

IREF	Resister
0	External
1	Internal

STANDBY ON/OFF (14h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	-	-	-	-	-	-	STB
Default	-	-	-	-	-	-	-	1

STB : STANDBY ON/OFF

STB	Function	Actions						
1	STANDBY ON	Display	Internal OSC	GRAM	ALL Reg	Latched Data	Row	Col
		OFF	STOP	Keep	Keep	Clear	GND	Zener
0	STANDBY OFF	OFF	START	Keep	Keep	Clear	GND	Zener

OSC Adjust (1Ah)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	-	-	-	FR3	FR2	FR1	FR0
Default	-	-	-	-	0	0	1	1

FR : OSC frequency setting.

FR[3:0]	Frame Rate
0	80 Hz
1	85 Hz
2	90 Hz
3	**95 Hz**
4	100 Hz
5	105 Hz
6	110 Hz
7	115 Hz

FR[3:0]	Frame Rate
8	120 Hz
9	125 Hz
A	130 Hz
B	135 Hz
C	140 Hz
D	140 Hz
E	140 Hz
F	140 Hz

ROW_SCAN_DIRECTION(09h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	-	-	-	-	-	SCAND1	SCAND0
Default	-	-	-	-	-	-	0	0

SCAND[1:0]	COL	ROW
0Xb	0 -> MAX	0 -> MAX
1Xb	0 -> MAX	MAX -> 0

DISPLAY_X1 (30h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	FX6	FX5	FX4	FX3	FX2	FX1	FX0
Default	-	0	0	0	0	0	0	0

DISPLAY_X2 (31h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	TX6	TX5	TX4	TX3	TX2	TX1	TX0
Default	-	1	0	1	1	1	1	1

DISPLAY_Y1 (32h)

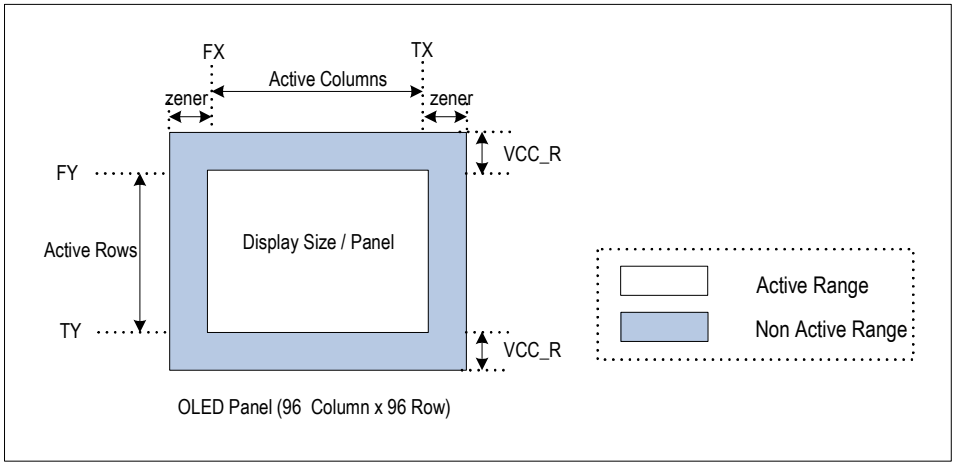
	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	FY6	FY5	FY4	FY3	FY2	FY1	FY0
Default	-	0	0	0	0	0	0	0

DISPLAY_Y2 (33h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	TY6	TY5	TY4	TY3	TY2	TY1	TY0
Default	-	1	0	1	1	1	1	1

FX[6:0] / TX[6:0] : The start/end address of active column outputs for the first screen (00h ~ 5Fh).
(FX[6:0] < TX[6:0])

FY[6:0] / TY[6:0] : The start/end address of active row outputs for the second screen (00h ~ 5Fh).
(FY[6:0] < TY[6:0])



The row outputs out of active area are always VCC_R excluding display off.

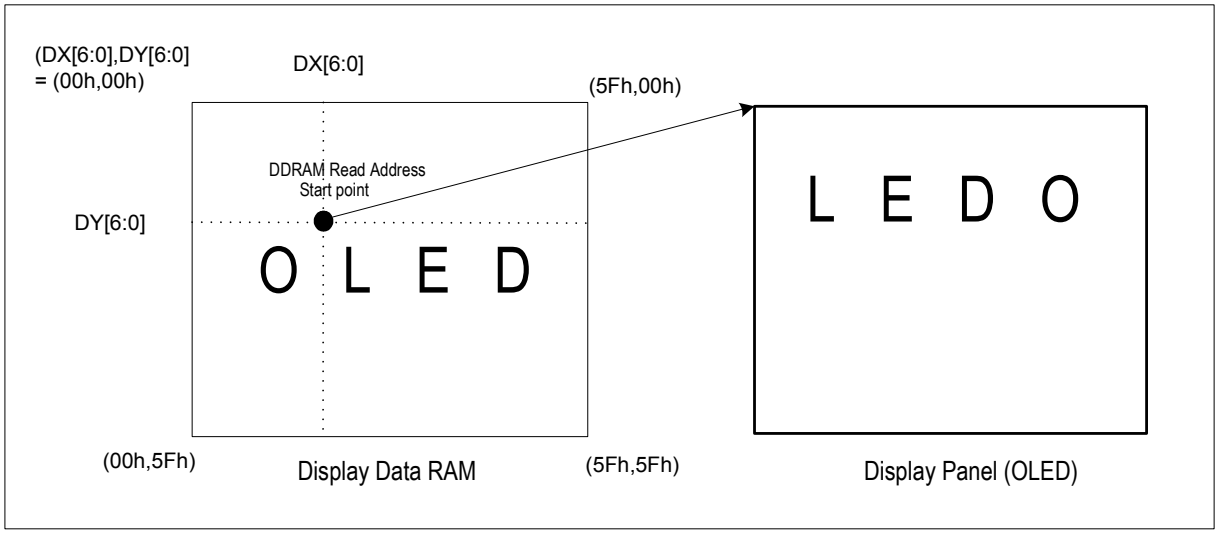
DISPLAYSTART_X (38h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	DX6	DX5	DX4	DX3	DX2	DX1	DX0
Default	-	0	0	0	0	0	0	0

DISPLAYSTART_Y (39h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	DY6	DY5	DY4	DY3	DY2	DY1	DY0
Default	-	0	0	0	0	0	0	0

DX[6:0] : Horizontal address for display.
DY[6:0] : Vertical address for display.



CPU_IF (0Dh)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	-	-	-	-	-	CIF1	CIF0
Default	-	-	-	-	-	-	0	0

CIF[1:0]	CPU Interface Format
0	8_Bit
1	16_Bit
2	6_Bit (RGB)
3	6_Bit (BGR)

MEM_X1 (34h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	XS6	XS5	XS4	XS3	XS2	XS1	XS0
Default	-	0	0	0	0	0	0	0

MEM_X2 (35h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	XE6	XE5	XE4	XE3	XE2	XE1	XE0
Default	-	1	0	1	1	1	1	1

MEM_Y1 (36h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	YS6	YS5	YS4	YS3	YS2	YS1	YS0
Default	-	0	0	0	0	0	0	0

MEM_Y2 (37h)

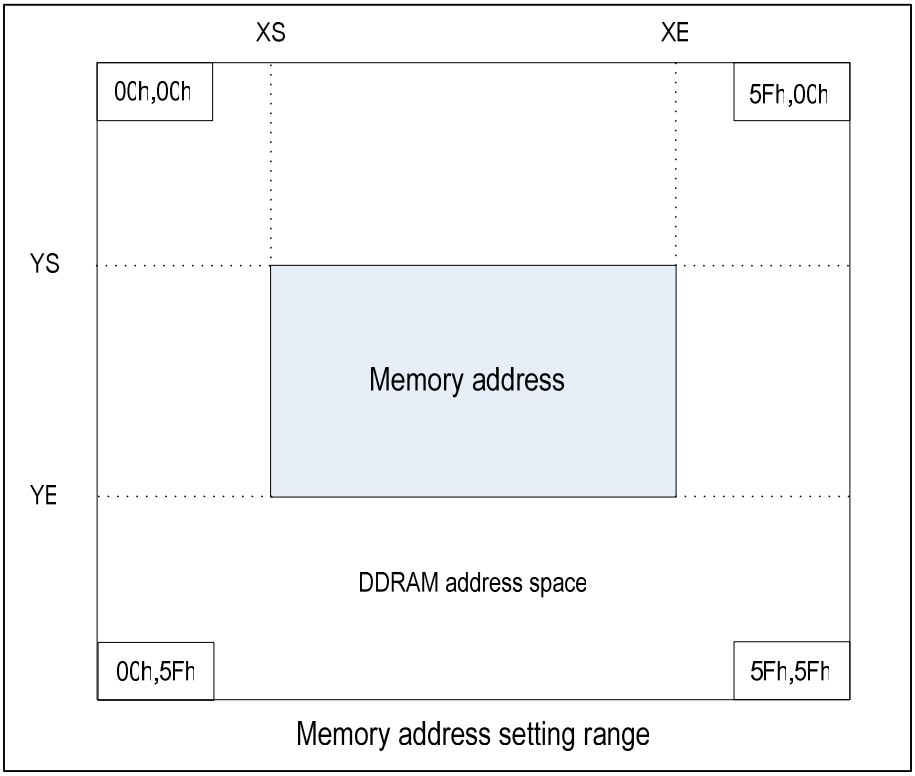
	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	YE6	YE5	YE4	YE3	YE2	YE1	YE0
Default	-	1	0	1	1	1	1	1

XS[6:0] / XE[6:0] (XS[6:0] < XE[6:0])

Specify the horizontal start/end position of a window for access in memory. Data can be written to DDRAM from the address specified by XS[6:0] to the address specified by XE[6:0].

YS[6:0] / YE[6:0] (YS[6:0] < YE[6:0])

Specify the vertical start/end position of a window for access in memory. Data can be written to DDRAM from the address specified by YS[6:0] to the address specified by YE[6:0].



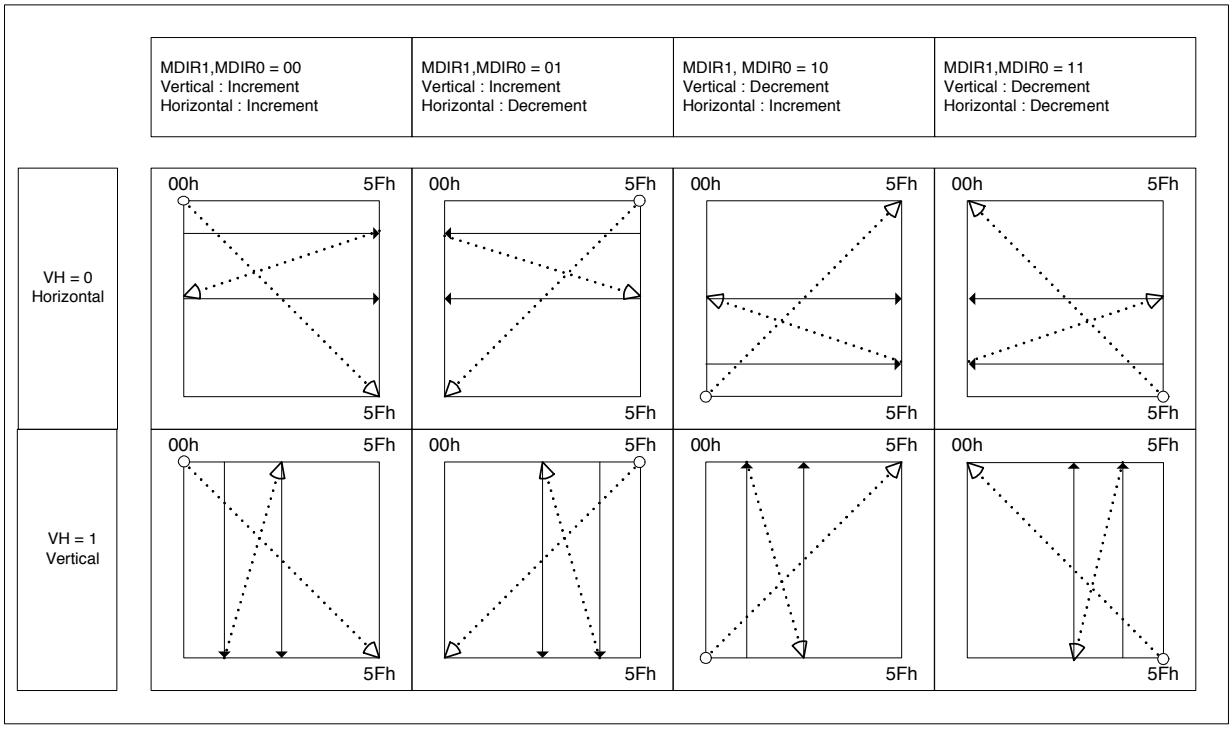
MEMORY_WRITE/READ (1Dh)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	-	-	-	-	VH	MDIR1	MDIR0
Default	0	0	0	0	0	0	0	0

VH : Set the automatic update method of the AC after the data is written to the DDRAM.
When VH= 0, The data is continuously written horizontally
When VH= 1, The data is continuously written vertically

MDIR1 : Vertical address increment/decrement.
When MDIR1= 0, Vertical address counter is increased.
When MDIR1= 1, Vertical address counter is decreased.

MDIR0 : Horizontal address increment/decrement.
When MDIR0= 0, Horizontal address counter is increased.
When MDIR0= 1, Horizontal address counter is decreased.



DDRAM_DATA_ACCESS_PORT (08h)

	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Default	R					G						B				

DDRAM[15:0] : After index register 08h is selected, Internal DDRAM memory can be accessed.

0x08 16-bit

	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
R/W	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

0x08 8-bit

	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
R/W	-	-	-	-	-	-	-	-	R4	R3	R2	R1	R0	G5	G4	G3
	-	-	-	-	-	-	-	-	G2	G1	G0	B4	B3	B2	B1	B0

0x08 6-bit

	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
R/W	-	-	-	-	-	-	-	-	-	-	R4	R3	R2	R1	R0	-
	-	-	-	-	-	-	-	-	-	-	G5	G4	G3	G2	G1	G0
	-	-	-	-	-	-	-	-	-	-	B4	B3	B2	B1	B0	-

0x08 6-bit

	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
R/W	-	-	-	-	-	-	-	-	-	-	B4	B3	B2	B1	B0	-
	-	-	-	-	-	-	-	-	-	-	G5	G4	G3	G2	G1	G0
	-	-	-	-	-	-	-	-	-	-	R4	R3	R2	R1	R0	-

DISCHARGE_TIME (18h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	-	-	DIS4	DIS3	DIS2	DIS1	DIS0-
Default	-	-	-	0	1	0	0	0

DIS[4:0]	Discharge Time
0	0 clock
1	1 clock
:	:
1D	29 clock
1E	30 clock

DIS[4:0] : Discharge time.

0x00-0x1E	Normal Dis-Charge	
0x1F	All COL = Zener Level	All Row = normal SCAN

PEAK_PULSE_DELAY (16h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	-	-	-	PDLY3	PDLY2	PDLY1	PDLY0
Default	-	-	-	-	0	1	0	1

PDLY[3:0]	Peak Pulse Delay
0	0 clock
1	1 clock
:	:
E	14 clock
F	15 clock

PEAK_PULSE_WIDTH _R (3Ah)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	-	-	PWR4	PWR3	PWR2	PWR1	PWR0
Default	-	-	-	0	0	1	0	1

PEAK_PULSE_WIDTH_G (3Bh)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	-	-	PWG4	PWG3	PWG2	PWG1	PWG0
Default	0	0	0	0	0	1	0	1

PEAK_PULSE_WIDTH _B (3Ch)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	-	-	PWB4	PWB3	PWB2	PWB1	PWB0
Default	0	0	0	0	0	1	0	1

PW[4:0]	Peak Pulse Width
0	0 clock
1	1 clock
:	:
1E	30 clock
1F	31 clock

PWR[4:0] : Precharge time R.
PWG[4:0] : Precharge time G.
PWB[4:0] : Precharge time B.

The range is from 0 to 31 based on internal OSC.

PRECHARGE_CURRENT_R (3Dh)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	PCR7	PCR6	PCR5	PCR4	PCR3	PCR2	PCR1	PCR0
Default	0	0	0	0	0	0	0	0

PRECHARGE_CURRENT_G (3Eh)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	PCG7	PCG6	PCG5	PCG4	PCG3	PCG2	PCG1	PCG0
Default	0	0	0	0	0	0	0	0

PRECHARGE_CURRENT_B (3Fh)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	PCB7	PCB6	PCB5	PCB4	PCB3	PCB2	PCB1	PCB0
Default	0	0	0	0	0	0	0	0

PC[7:0]	Output Current (Default 0 uA)
0	0 uA
1	4 uA
:	:
FE	1016 uA
FF	1020 uA

PCR[7:0] : Precharge current R.
PCG[7:0] : Precharge current G.
PCB[7:0] : Precharge current B.

* Precharge current = setting value * 4uA.

COLUMN_CURRENT_R (40h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	DCR7	DCR6	DCR5	DCR4	DCR3	DCR2	DCR1	DCR0
Default	0	0	0	0	0	0	0	0

COLUMN _CURRENT_G (41h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	DCG7	DCG6	DCG5	DCG4	DCG3	DCG2	DCG1	DCG0
Default	0	0	0	0	0	0	0	0

COLUMN _CURRENT_B (42h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	DCB7	DCB6	DCB5	DCB4	DCB3	DCB2	DCB1	DCB0
Default	0	0	0	0	0	0	0	0

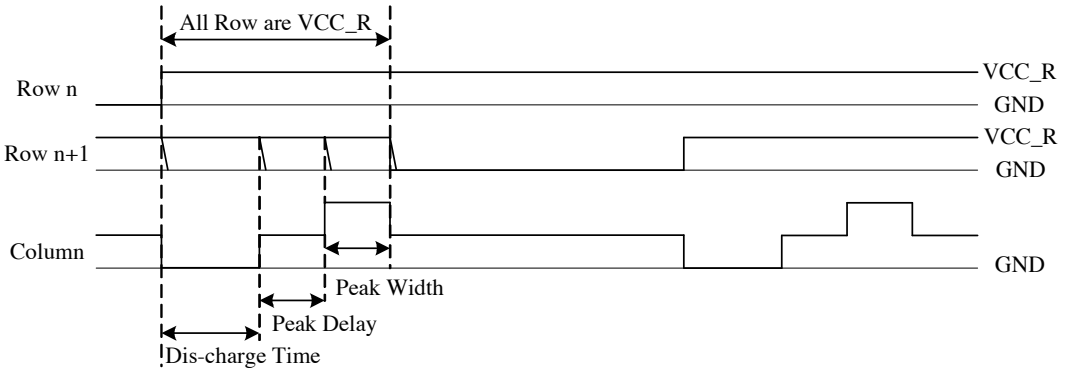
DC[7:0]	Output Current (Default 0 uA)
00	0 uA
01	0.74 uA
:	:
FE	187.96 uA
FF	188.7 uA

DCR[7:0] : DCR driving current R.
DCG[7:0] : DCG driving current G.
DCB[7:0] : DCB driving current B.

* Driving current = setting value * 0.74 uA.

ROW_OVERLAP (48h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	-	-	-	-	-	ROW1	ROW0
Default	-	-	-	-	-	-	0	0



ROW[1:0]	Row VCC_R Time
00	None(Band Gap Only)
01	Dis-charge Time
10	Dis-charge + Peak Delay
11	Dis-charge + Peak Delay + Peak Width

SCAN_OFF_LEVEL(49h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	-	-	-	SOFF3	SOFF2	SOFF1	SOFF0
Default	-	-	-	-	0	1	0	0

SOFF[3:0]	VCC_R
0	VCC_C*0.95
1	VCC_C *0.90
2	VCC_C *0.85
3	VCC_C *0.80
4	VCC_C *0.75
5	VCC_C *0.70
6	VCC_C *0.65
7	VCC_C *0.60

SOFF[3:0]	VCC_R
8	VCC_C *0.55
9	VCC_C *0.50
A	VCC_C *0.45
B	VCC_C *0.40
C	INVALID
D	INVALID
E	INVALID
F	VCC_C *1.00

ROW_SCAN_ON/OFF (17h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	-	-	-	-	-	-	SC_ON
Default	-	-	-	-	-	-	-	0

SC_ON: SCAN ON.

0	Normal Row Scan
1	All Row go to GND

ROW_SCAN_MODE (13h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	-	-	-	-	-	-	SCM0
Default	-	-	-	-	-	-	-	0

SCM[0]	SCAN Mode	Display Direction	
0	Alternate scan mode	0	0,1,2,⋯,94,95,0,1,2,...
		2	95,94,⋯,1,0,95,94,...
1	Alternate scan mode1	0	1,0,3,2,5,4…
		2	94,95,92,93…

SCREEN_SAVER_CONTEROL (D0h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	SMON	-	-	SLON	-	-	-	-
Default	0	-	-	0	-	-	-	-

SMON	Saver Mode On/Off
0	OFF
1	ON

SLON	Saver Sleep Mode
0	OFF
1	ON

SS_SLEEP_TIMER (D1h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	STIM7	STIM6	STIM5	STIM4	STIM3	STIM2	STIM1	STIM0
Default	0	0	0	0	0	0	0	0

Note) Based on 180 frame(2 Second)

SCREEN_SAVER_MODE (D2h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	-	-	-	-	SM2	SM1	SM0
Default	-	-	-	-	-	0	0	0

SM2	SM1	SM0	Saver1 Mode
0	0	0	Left Panning
0	0	1	Right Panning
0	1	0	Down Scroll
0	1	1	Up Scroll
1	0	0	Fades in
1	0	1	Fades out
1	1	0	Fades Out/in
1	1	1	Pixel Vibration

SS_UPDATE_TIMER (D3h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	SSUT7	SSUT6	SSUT5	SSUT4	SSUT3	SSUT2	SSUT1	SSUT0
Default	0	0	0	0	0	0	0	0

RGB_IF (E0h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	-	-	RIM1	RIM0	-	-	-	EIM
Default	-	-	0	0	-	-	-	0

RIM1	RIM0	
0	0	8_Bit RGB
0	1	16_Bit RGB
1	0	6_Bit RGB
1	1	6_Bit BGR

EIM	
0	MCU I/F
1	RGB I/F

RGB_POL (E1h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	VSOEN	VSOP	-	-	VSP	HSP	ENP	DOTP
Default	0	0	-	-	0	0	0	0

VSOEN	VSYNC Output Enable

VSYNC Output Polarity	
0	Active Low
1	Active High

Bit[3:0]	
0	Active Low
1	Active High

VSOEN : Vsync. Output enable.
VSOP : Vsync. Output polarity.
DOTP : Dot clock polarity.
ENP : Enable polarity.
HSP : Hsync. Polarity.
VSP : Vsync. Polarity.

DISPLAY_MODE_CONTROL(E5h)

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	SWAP	-	RC1	RC0	-	-	DC1	DC0
Default	0	-	0	0	-	-	0	0

SWAP	Input	Output
0	RGB	RGB
1	RGB	BGR

RC	REDUCE CURRENT
00	Normal
01	1/2 Current
10	1/4 Current
11	1/8 Current

DC1	DC0	
0	0	Normal
0	1	All Low
1	0	All High
1	1	Half PWM

6. Electric Characteristics

1) Absolute Maximum Rating

ITEM	SYMBOL	CONDITION	PORT	RATINGS	UNIT
Supply voltage	VDD	VSS(0V) Reference Ta = +25℃	VDD	- 0.3 ~ +4.0	V
	VCC		VCC	- 0.3 ~ +19.5	V
	VDDIO		VDDIO	- 0.3 ~ +4.0	V
Input voltage	VI		*1	- 0.3 ~ +VDD+0.3	V
Storage temperature	Tstg			- 65 ~ +150	℃

1* : DB[15:0], CPU, PS, CSB, A0, RDB, WRB, RSTB.

2) Recommended Operation Conditions

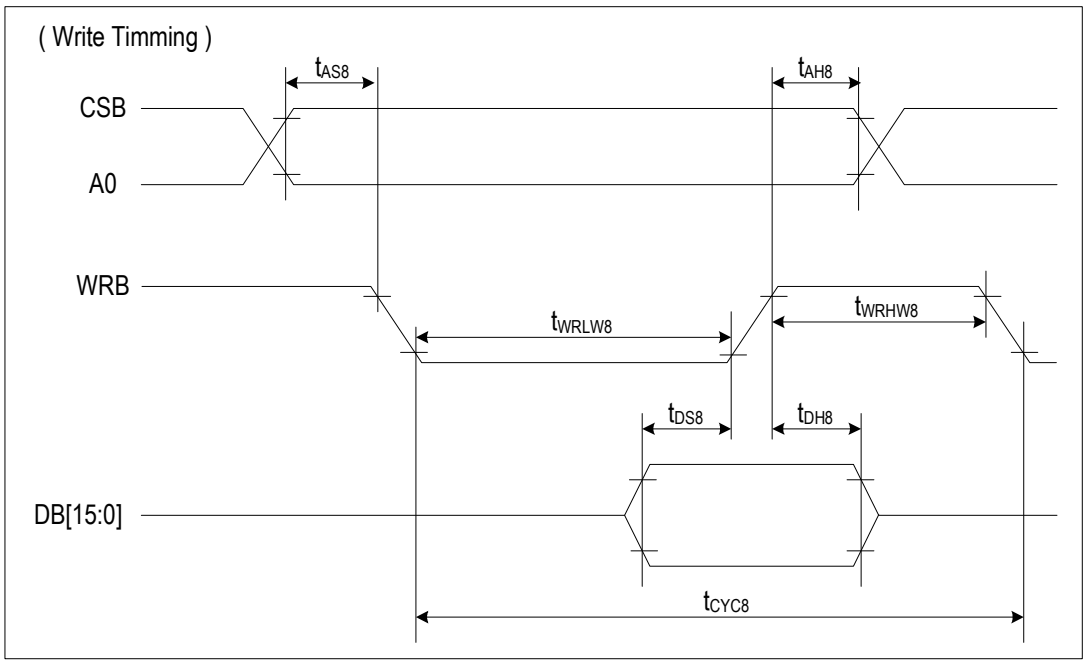
ITEM	SYMBOL	PORT	MIN	TYP	MAX	UNIT	REMARK
Supply voltage	VDD	VDD	2.4	2.8	3.3	V	
	VCC	VCC	8.0	16	18.0	V	
	VDDIO	VDDIO	1.65	-	3.3	V	
Operating voltage	VDC	C[287:0]	0	16	18.0	V	
Operation temperature	Topr		- 40		85	℃	

3) DC Characteristics

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	PORT
High level input voltage	VIH		0.8XVDDIO		VDDIO	V	
Low level input voltage	VIL		0		0.4	V	
High level output voltage	VOH	IOH = -0.1mA	VDDIO-0.4			V	
Low level output voltage	VOL	IOL = -0.1mA			0.4	V	
Input leakage current	ILI	VI = VSS or VDDIO	-1		1	uA	
Output leakage current	ILO	VI = VSS or VDDIO	-1		1	uA	
Static current	ISB	CSB = VDDIO, VDD = 2.8V Ta = 25℃, Power save mode			5	uA	
Current Consumption	IVDD	VDD = 2.8V, IDC = 50uA		0.5	2	mA	
	IVDDIO	VDD = 2.8V, IDC = 50uA		0.8	2	mA	
	IVCC	VDD = 2.8V, IDC = 50uA		20	30	mA	
Oscillator frequency	FOSCI	VDD = 2.8V, Ta = 25℃			3	MHz	
Oscillator frequency By external resistor	FOSCE	RF = 27kΩ@ CP Test			3	MHz	
Oscillator frequency match	FOSCV	VDD = 2.8V, Ta = 25℃	-6		6	%	
Frame scan rate	Frame	VDD = 2.8V, Ta = 25℃	80	95	140	Hz	
Column output current range	IDC	4 < VDC < VCC -2V Max Column current = 0xFF (for R,G,B)	0		188.7	uA	
Column output current match	DEV	VDD=2.8V, VCC=16V Idrv=100uA, Ipre=100uA Without Panel, 20kΩ load, display on	-4		4	%	
	ADJ. DEV		-2		2	%	
Row switch on current sink	IDR	Common is on Idrv =188.7uA			50	mA	
Row switch on resistance	RDR	Common is on, VDC IFM = max 50mA		20	40	Ω	

4) AC Characteristics

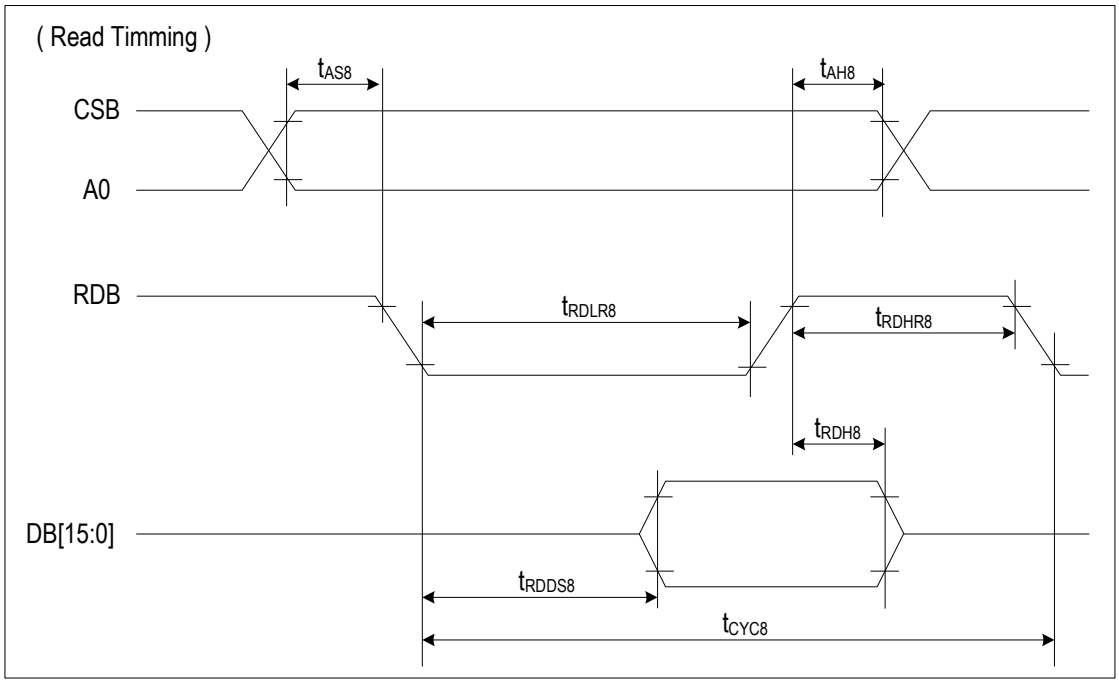
4-1) System BUS Read/Write Timing (80 series CPU interface)



(VDD = 2.8V, Ta = 25℃)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	t_{AH8}	-	5	-	ns	CSB
Address setup timing	t_{AS8}		5		ns	A0
System cycle timing	t_{CYC8}	-	100	-	ns	WRB
Write "L" pulse width	t_{WRLW8}		45		ns	
Write "H" pulse width	t_{WRHW8}		45		ns	
Data setup timing	t_{DS8}	-	30	-	ns	DB[15:0]
Data hold timing	t_{DH8}		10		ns	

notice) All the timing reference is 10% and 90% of VDDIO.

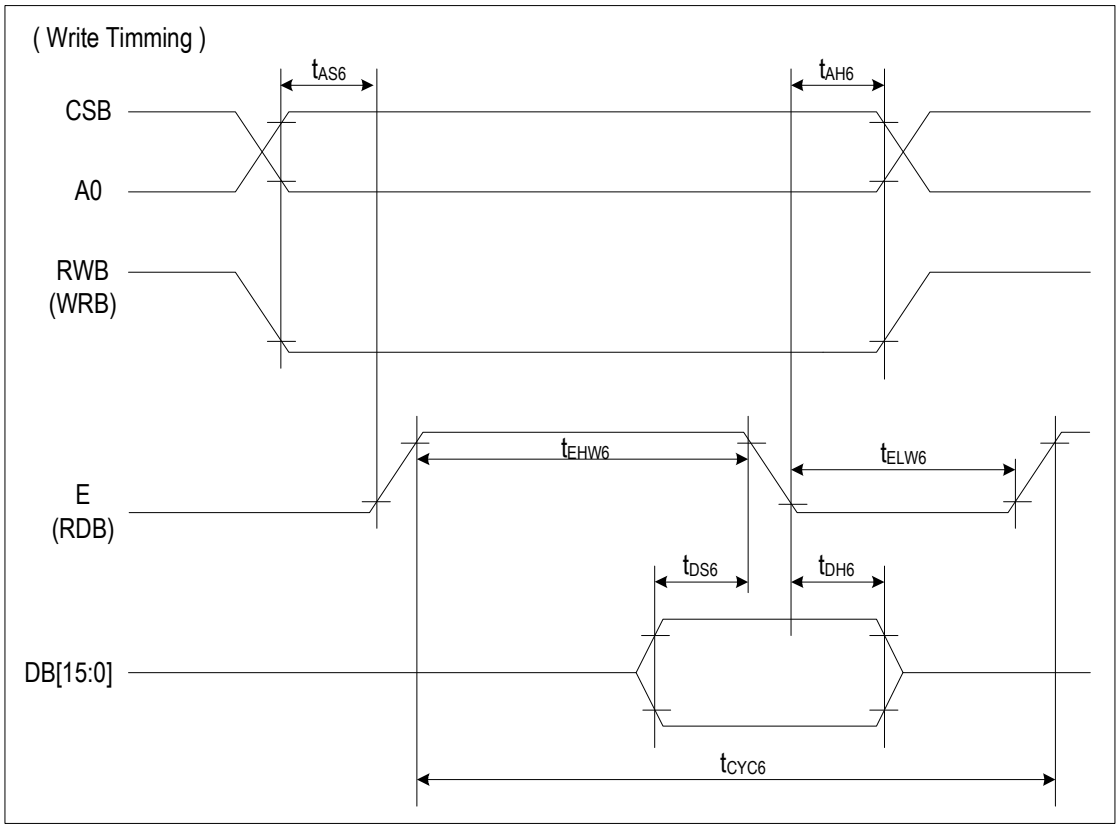


(VDD = 2.8V, Ta = 25℃)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	t_{AH8}	-	5	-	ns	CSB
Address setup timing	t_{AS8}		5		ns	A0
System cycle timing	t_{CYC8}	-	200	-	ns	RDB
Read "L" pulse width	t_{RDLR8}		90		ns	
Read "H" pulse width	t_{RDHR8}		90		ns	
Read data output delay time	t_{RDD8}	CL = 15 pF	-	60	ns	DB[15:0]
Data hold timing	t_{RDH8}		0		ns	

Notice) All the timing reference is 10% and 90% of VDDIO.

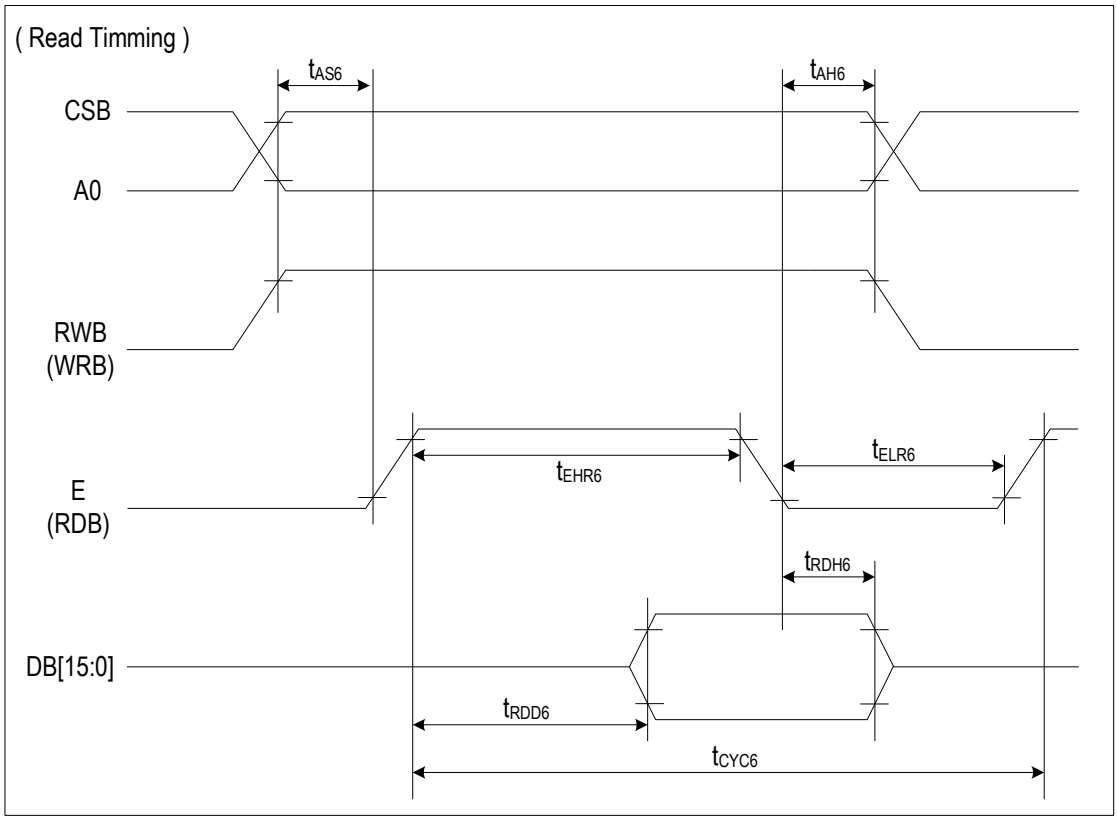
4-2) System BUS Read/Write Timing (68 series CPU interface)



(VDD = 2.8V, Ta = 25℃)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	t_{AH6}	-	5	-	ns	CSB
Address setup timing	t_{AS6}		5		ns	A0
System cycle timing	t_{CYC6}	-	100	-	ns	E
Write "L" pulse width	t_{ELW6}		45		ns	
Write "H" pulse width	t_{EHW6}		45		ns	
Data setup timing	t_{DS6}	-	40	-	ns	DB[15:0]
Data hold timing	t_{DH6}		10		ns	

Notice) All the timing reference is 10% and 90% of VDDIO.

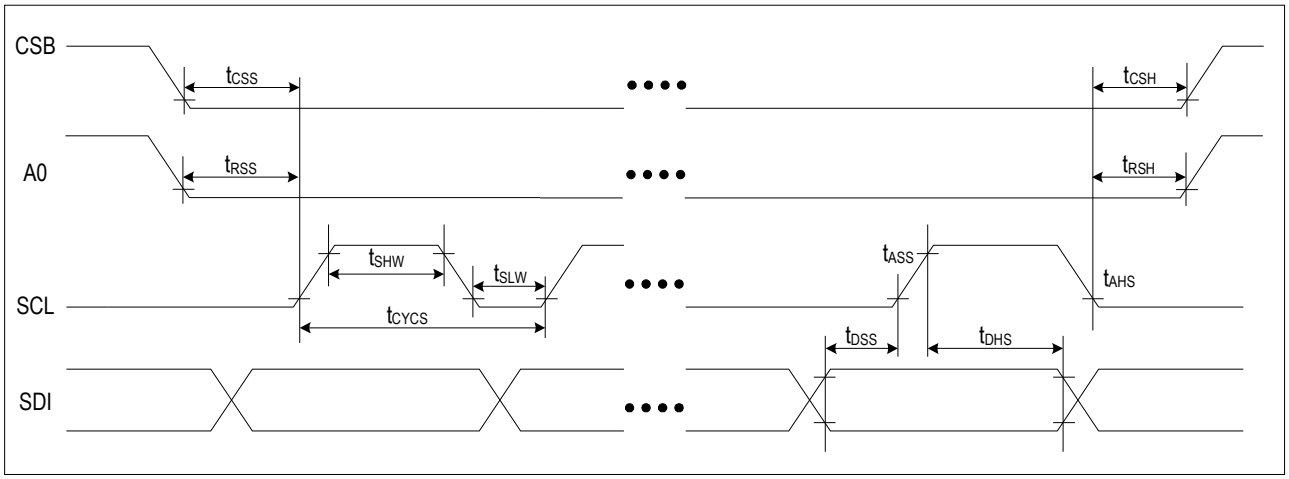


(VDD = 2.8V, Ta = 25℃)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	t_{AH6}	-	10	-	ns	CSB
Address setup timing	t_{AS6}		10		ns	A0
System cycle timing	t_{CYC6}		200		ns	
Read "L" pulse width	t_{ELR6}	-	90	-	ns	E
Read "H" pulse width	t_{EHR6}		90		ns	
Read data output delay time	t_{RDD6}	CL = 15 pF	0	70	ns	DB[15:0]
Data hold timing	t_{RDH6}				ns	

Notice) All the timing reference is 10% and 90% of VDDIO.

4-3) Serial Interface Timing

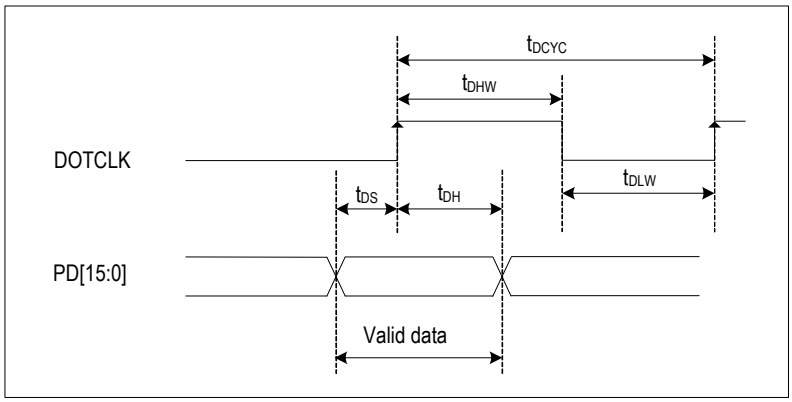


(VDD = 2.8V, Ta = 25℃)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Serial clock cycle	t_{CYCS}	-	200	-	ns	SCL
SCL "H" pulse width	t_{SHW}		90		ns	
SCL "L" pulse width	t_{SLW}		90		ns	
Data setup timing	t_{DSS}	-	25	-	ns	SDI
Data hold timing	t_{DHS}		25		ns	
CSB-SCL timing	t_{CSS}	-	25	-	ns	CSB
CSB-hold timing	t_{CSH}		25		ns	
RS-SCL timing	T_{RSS}	-	25	-	ns	RS
RS-hold timing	T_{RSH}		25		ns	

Notice) All the timing reference is 10% and 90% of VDDIO.

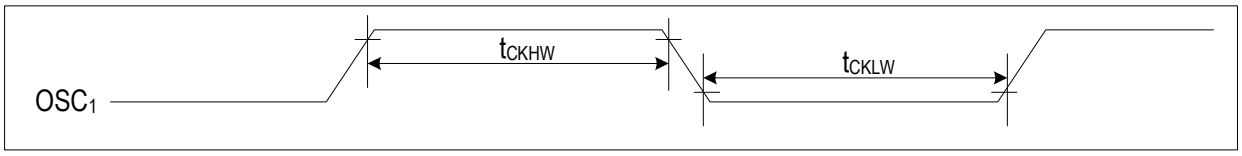
4-4) RGB Interface Timing



(VDD = 2.8V, Ta = 25℃)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Dot clock cycle	t_{DCYC}	-	100	-	ns	DOTCLK
Dot "H" pulse width	t_{DHW}		45		ns	
Dot "L" pulse width	t_{DLW}		45		ns	
Data setup timing	t_{DS}	-	5	-	ns	PD[15:0]
Data hold timing	t_{DH}		5		ns	

4-5) External Clock Input Timing

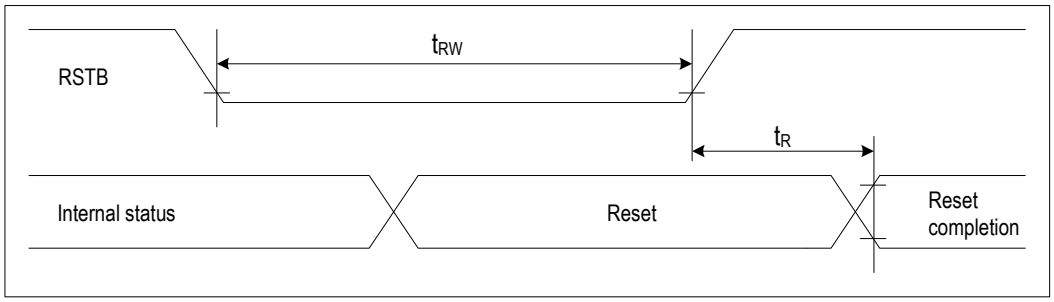


(VDD = 2.8V, Ta = 25℃)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Osc1 Duty Ratio	Dextclk		30	70	%	OSC1
Osc1 'H' pulse width	t_{CKHW}		-	-	us	
Osc1 'L' pulse width	t_{CKLW}		-	-	us	

*Note : 1. Osc1 Duty Ratio : Dextclk = t_{CKLW} / (t_{CKHW} + t_{CKLW})

4-6) Reset Input Timing



(VDD = 2.8V, Ta = 25℃)

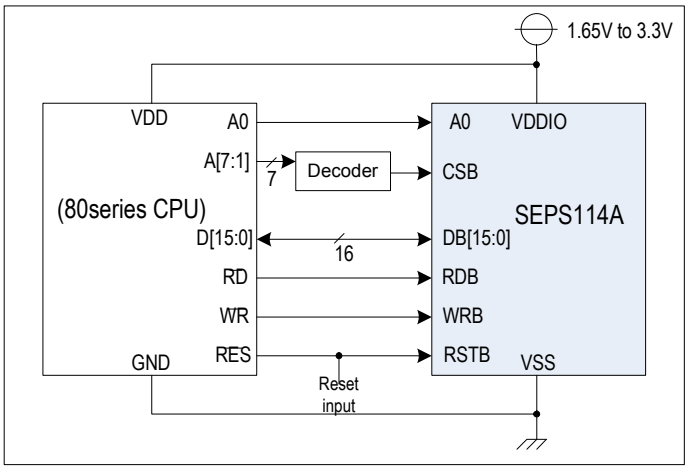
ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Reset time	t_R			1.5	us	
RSTB "L" pulse width	t_{RW}		5		us	RSTB

7. Application Example

1) Connection With MPU

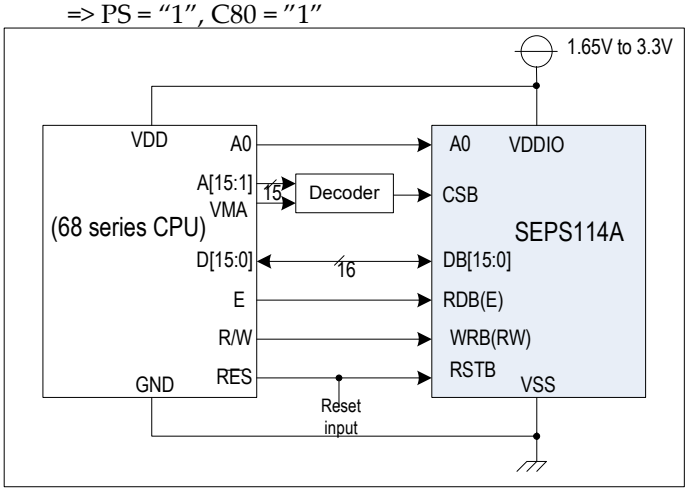
1-1) 80 Series Interface(16-bit bus)

=> PS = "1", C80 = "0"

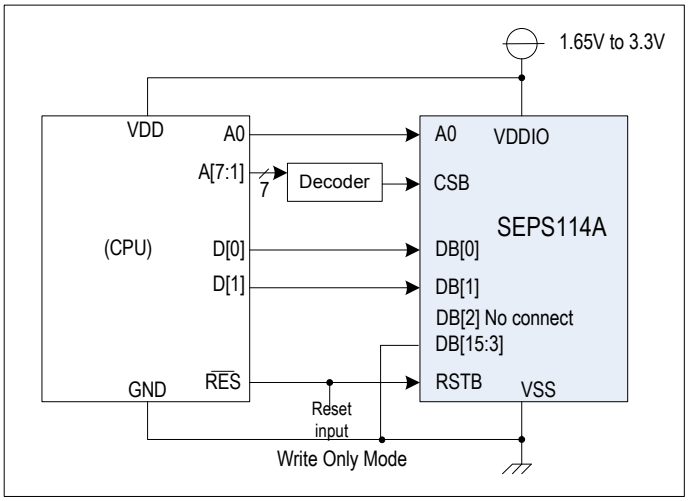


1-2) 68 Series Interface(16-bit bus)

=> PS = "1", C80 = "1"



1-3) MPU Connection with Serial Interface



Revision Record

Rev.	Data	Page No.	Contents of Modification	
0.0	2007.01.25		First issue	Name
0.1	2007.03.13	32	DC Characteristics → DC Characteristics item insert	
0.2	2007.03.16	26 ~ 27	11h, 12h Register → 11h, 12h Register Value revised	
0.3	2007.05.21	3	External OSC Resistance 39 kΩ → 20 kΩ	
		29	Row Scan Mode SCM[1] deleted	
0.5	2007.08.03	22	MEMORY_WRITE/READ modified(Vertical↔Horizontal)	DH Kim
0.6	2007.10.15	1	Frame rate/Current step modified	GJ Lee
		2	Block Diagram modified	
		3	External OSC Resistance 20 kΩ → 27 kΩ	
			VSS modified	
		15	Power ON Sequence inserted	
		17	SELRES/IREF deleted	
		18	Oscillator frequency adjusted	
		32	Static current(1) deleted and Static current(2) renamed as Static current	
			External OSC Resistance 20 kΩ → 27 kΩ	
			Current consumption TBD updated. Category modified	
		39	Osc1 TBD updated. Osc1 Duty Ratio category inserted	
1.0	2007.11.19	1,25	Discharge time (0~31clock) → (0~30clock)	KY Kim/
		1,19	Frame rate(75Hz~150Hz) → (80Hz~140Hz)	BS Ahn/
		1,28	Driving current(0~188.7uA,0.74uA step) modified.	MS Kim
		2	Block Diagram modified.	
		3	Pin Description modified.	
		13	6-bit BGR interface inserted.	
		16	Initial Setting Condition modified, Power Sequence modified.	
		18	Analog control modified.	
		23	Memory Write/Read modified.	
		33	DC characteristic modified.	
		37	RWB->RW corrected.	
		41	Application Example modified.	
1.1	2008. 2. 5	17	Power OFF Sequence added.	GJ Lee
			Power ON/OFF modified.	
1.2	2008. 2. 20	34	FOSCE modified.	GJ Lee
1.3	2008. 3. 21	17	Power off Sequence modified.(0ms deleted and changed)	GJ Lee
1.4	2008. 7. 23	34	FOSCV, Chip to Chip, DEV, ADJ. DEV modified.	GJ Lee
1.5	2008. 7. 30	34	Chip to Chip deleted. Deviation is modified.	GJ Lee
1.6	2008. 7. 31	34	Column current Test condition modified.	GJ Lee
1.7	2008.10.09	12	Note 2) deleted.	Andy Kim
	2008.10.13	8	SCL signal modified.	
		11,12,13	DTST maximum time inserted	Andy Kim
1.8	2008.11.06	10,11,12,13	RGB Interface timing modified	Andy Kim
	2008.12.10	17	Power ON/OFF modified	Antonius/Andy