Cortex ARMv7 Family
Cortex-A8 Pipeline

References:
- The ARM Architecture: https://www.arm.com/files/pdf/ARM_Arch_A8.pdf
- ARM Cortex-A* Series Processors, Haoyang Lu, Zheng Lu, Yong Li, James Cortese : https://pdfs.semanticscholar.org/c480/d8b1533a1341c9ca9aeb79a86eaaaff71291.pdf
- ARM Cortex A8 Pipeline, Wei Wang : http://www.ece.tufts.edu/~karen/classes/final_presentation/ARM_A8_pipeline_Wei.pptx
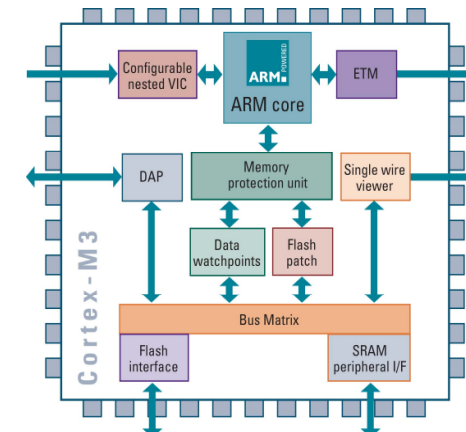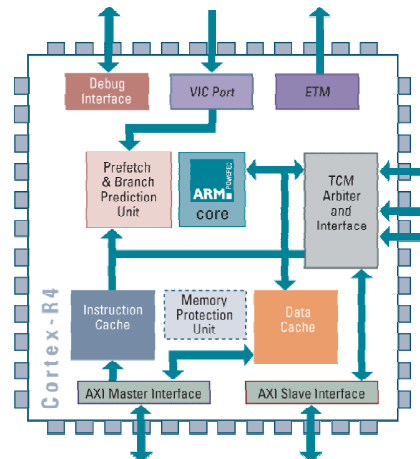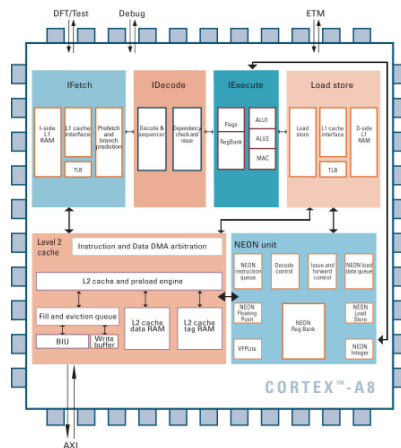
Cortex family

Cortex-A8

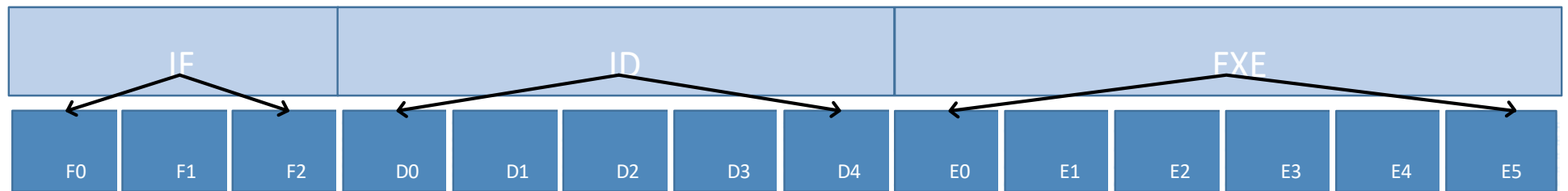- Architecture v7A
- MMU
- AXI
- VFP & NEON support

Cortex-R4

- Architecture v7R
- MPU (optional)
- AXI
- Dual Issue

Cortex-M3

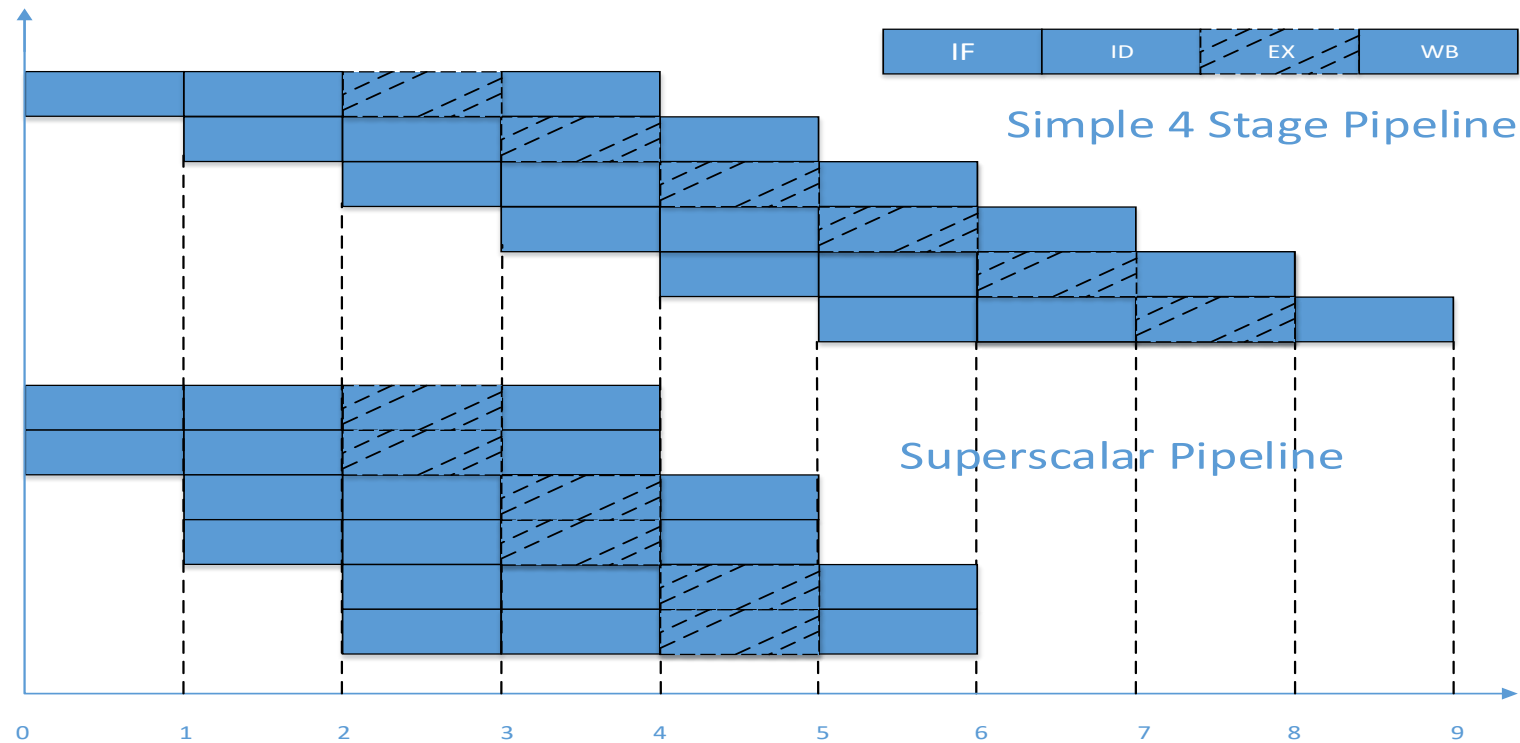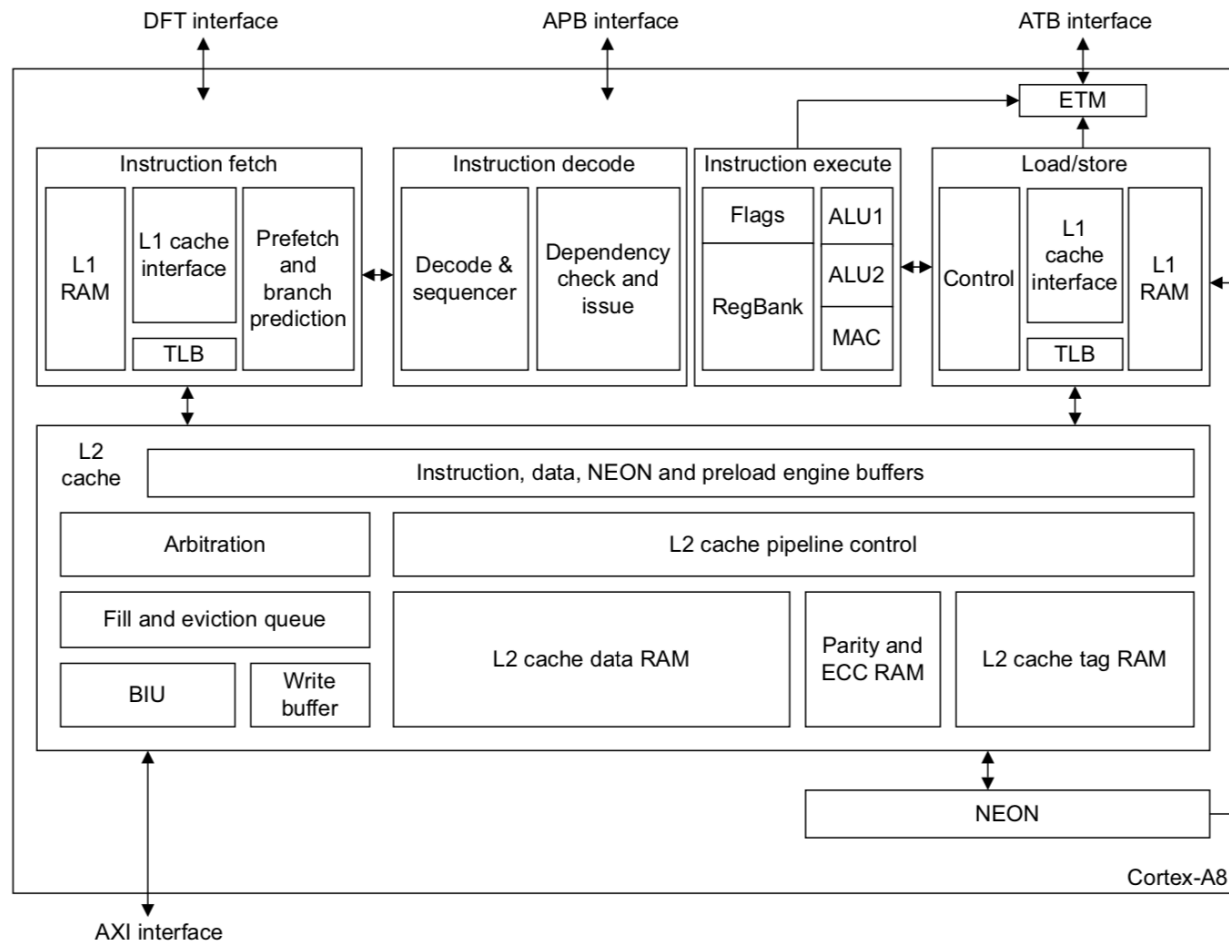- Architecture v7M
- MPU (optional)
- AHB Lite & APB

The Architecture for the Digital World® **ARM**®

Deeper Pipeline

IF			ID					EXE					
F0	F1	F2	D0	D1	D2	D3	D4	E0	E1	E2	E3	E4	E5

Superscalar Pipeline

IF	ID	EX	WB

Simple 4 Stage Pipeline

Superscalar Pipeline

0   1   2   3   4   5   6   7   8   9

Two instructions executed at the same time

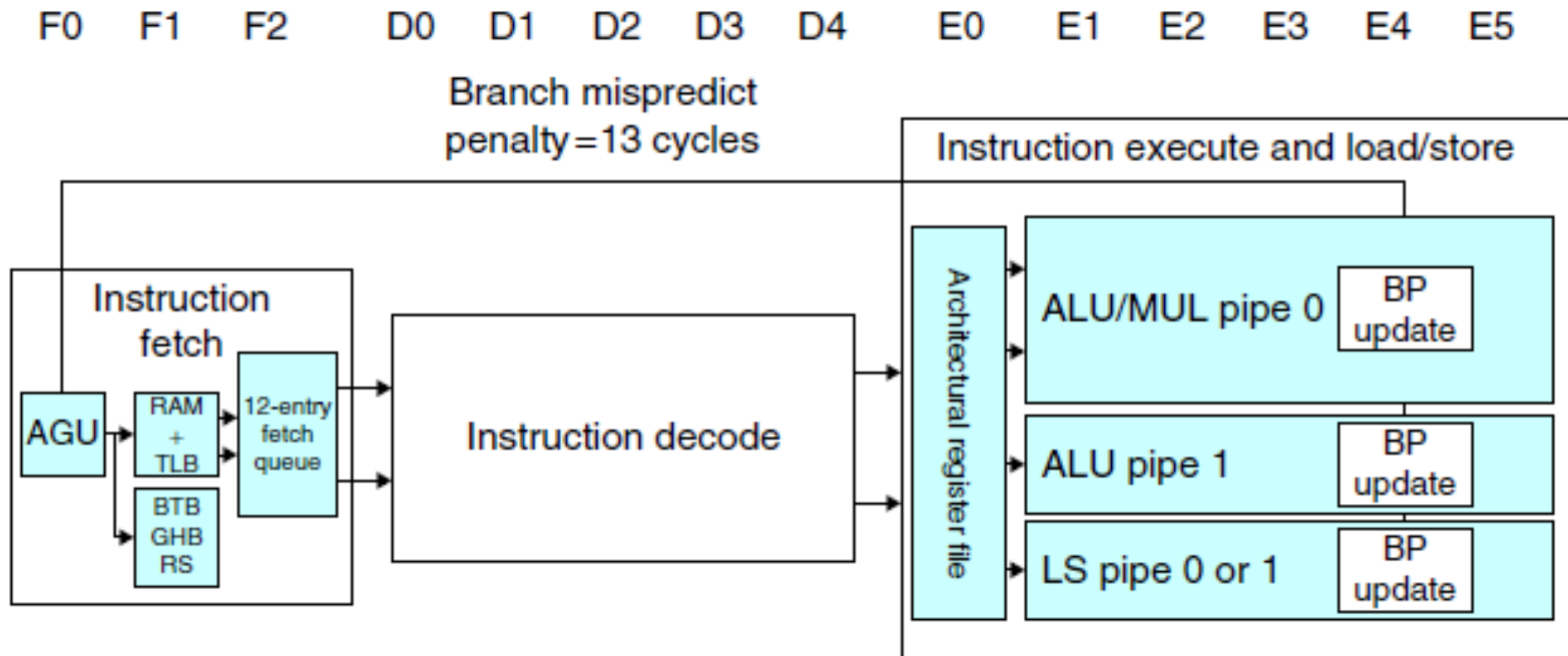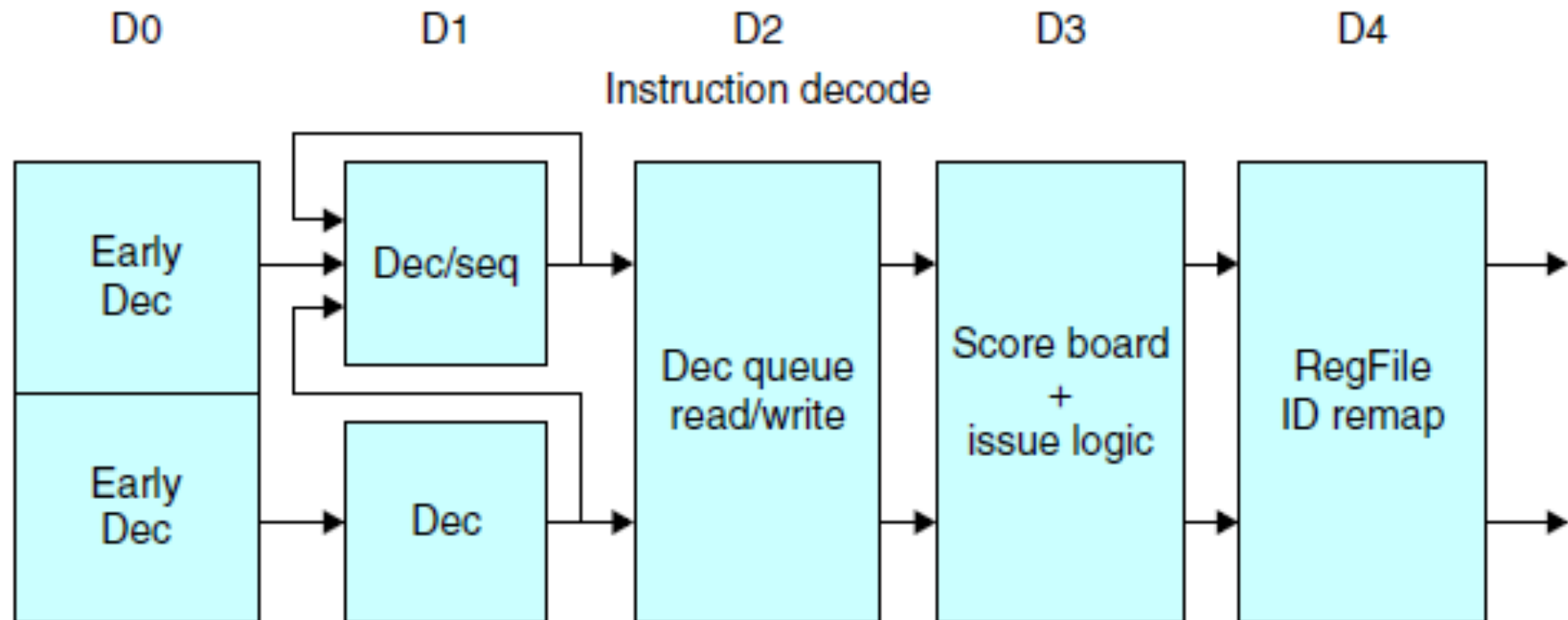# Cortex-A8 Internal Architecture

Cortex-A8 Instruction Fetch Pipeline

Cortex-A8 Instruction Decode Pipeline

Cortex-A8 Instruction Execute Pipeline