SYNCOAM

Synergetic Combination of ASIC & Memory

SEPS114A

Application Note

96 x 96 Dots, 65K Colors
PM-OLED Display Driver and Controller

Version : 1.0
Date : Dec, 2008

CONTENTS

1. Introduction

This application note serves as a design and application guideline for SEPS114A. The SEPS114A drives a PMOLED panel of 96RGB x 96 dots with incorporated RAM that is compliant with a graphics display of 96RGB x 96 dots at maximum, and can handle 65,536 colors.

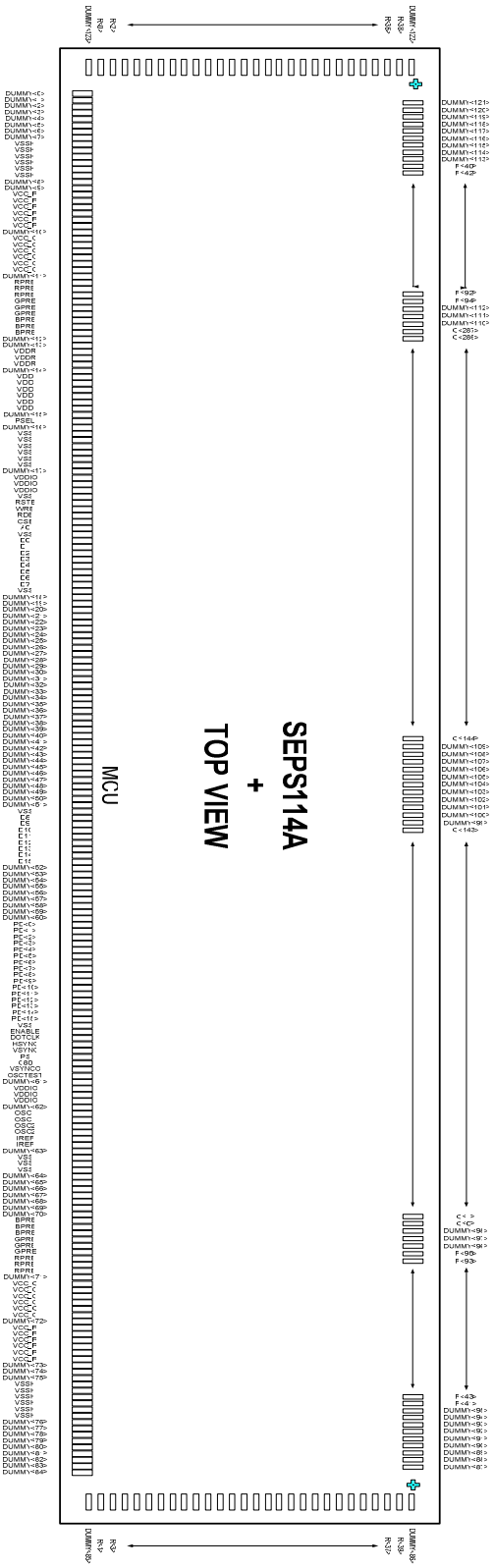
This note covers device operation, programming parameters, and interfacing to MCU. For the detailed characteristics of the IC, please refer to SEPS114A datasheet.

2. Features

- 65k colors OLED single chip display driver IC
- Data Interface
  - Parallel interface : 68/80series MPU(16/8/6-bit)
  - Serial interface : SPI 4-wire interface
  - RGB interface : 16/8/6 bits interface
- Driver Output : 96× RGB columns(288), 96 rows
- Display RAM Capacity : 96 × 16(RGB) × 96 = 147,456 bits
- Various Instructions Set
  - Power save mode
  - Reduced current driving available
  - Window mode
  - Partial display : programmable panel display size
- OLED Column Drive
  - Dis_charge time control : Dis_charge time(0clock ~ 30clocks) with internal oscillator clock
  - Pre_charge peak control :
    - Peak pulse delay time : (0clock ~ 15clocks) with internal oscillator clock
    - Peak pulse width time : (0clock ~ 31clocks) with internal oscillator clock
  - Pre_charge current control : 8-bit, 0uA ~ 1020uA by 4uA step control
  - Driving current control : 8-bit, 0uA ~ 188.7uA by 0.74uA step control
- OLED Row Drive : Current sink - Max 50mA
- Internal Oscillator Circuit
  - Internal / External clock selectable
  - Frame rate : 95 frames/sec (80.0 ~ 140.0 frames/sec adjustable)
- Supply Voltage
  - VDDIO : 1.65 ~ 3.3V
  - VDD : 2.4 ~ 3.3V
  - VCC : 8.0 ~ 18.0V

3. Hardware Configuration

3.1 Pin Configuration



3.2 Pin Description

<table>
<tr><th>Pin Name</th><th>Pins</th><th>I/O</th><th>Connected To</th><th>Description</th></tr>
<tr><td>C80</td><td>1</td><td>I</td><td>VSS or VDDIO</td><td>Selects the MPU type
Low : 80-Series Interface, High : 68-Series Interface</td></tr>
<tr><td>PS</td><td>1</td><td>I</td><td>VSS or VDDIO</td><td>Selects parallel/Serial interface type
Low : serial, High : parallel</td></tr>
<tr><td>CSB</td><td>1</td><td>I</td><td>MPU</td><td>Selects the SEPS114A
Low : SEPS114A is selected and can be accessed
High : SEPS114A is not selected and cannot be accessed</td></tr>
<tr><td>A0</td><td>1</td><td>I</td><td>MPU</td><td>Selects the data / command
Low : command, High : parameter / data</td></tr>
<tr><td>RDB/E</td><td>1</td><td>I</td><td>MPU</td><td>For an 80-serise bus interface, read strobe signal (active low)
For an 68-serise bus interface, bus enable strobe (active high)
When using SPI, fix it to VDDIO or VSS level</td></tr>
<tr><td>WRB/RW</td><td>1</td><td>I</td><td>MPU</td><td>For an 80-serise bus interface, write strobe signal (active low)
For an 68-serise bus interface, read/write select
Low : Write, High : Read
When using SPI, fix it to VDDIO or VSS level</td></tr>
<tr><td>RSTB</td><td>1</td><td>I</td><td>MPU</td><td>Reset SEPS114A(active low)</td></tr>
<tr><td>DB[15:0]</td><td>16</td><td>I/O</td><td>MPU</td><td>Serves as a 16_bit bi-directional data bus
<table>
<tr><th>PS</th><th>Description</th></tr>
<tr><td>1</td><td>8_bit bus : DB[7:0]
16_bit bus : DB[15:0]
6_bit bus : DB[5:0] for RGB/BGR</td></tr>
<tr><td>0</td><td>DB[0] SCL : Serial clock input
DB[1] SDI : Serial data input
DB[2] SDO : Serial data output
DB[3] R/W : Serial Read/Write
0 : Write, 1 : Read</td></tr>
</table>
Fix unused pins to the VSS level</td></tr>
<tr><td>PD[15:0]</td><td>16</td><td>I</td><td>RGB Interface</td><td>8_bit RGB bus : PD[7:0], 16_bit RGB bus : PD[15:0]
6_bit RGB bus : PD[5:0], 6_bit GBR bus : PD[5:0]</td></tr>
<tr><td>OSC1</td><td>1</td><td>I</td><td rowspan="2">Oscillation-Resistor</td><td rowspan="2">Fine adjustment for oscillation
Tie 27 kΩ to OSC1 between OSC2
When the external clock mode is selected, OSC1 is used external clock input</td></tr>
<tr><td>OSC2</td><td>1</td><td>O</td></tr>
<tr><td>OSC TEST</td><td>1</td><td>O</td><td>Floating</td><td>OSC Test</td></tr>
<tr><td>C[287:0]</td><td>288</td><td>O</td><td>PANEL</td><td>SEPS114A Display column outputs</td></tr>
<tr><td>R[95:0]</td><td>96</td><td>O</td><td>PANEL</td><td>SEPS114A Display row outputs</td></tr>
<tr><td>VCC_C</td><td>2</td><td>P</td><td>POWER</td><td>Data Driver Power Supply(8V ~ 18V)</td></tr>
<tr><td>VCC_R</td><td>2</td><td>P</td><td>POWER</td><td>Power Supply for Scan Driver</td></tr>
<tr><td>VDDR</td><td>1</td><td>P</td><td>POWER</td><td>Logic Power Supply2</td></tr>
<tr><td>VDD</td><td>1</td><td>P</td><td>POWER</td><td>Logic Power Supply(2.4V ~ 3.3V)</td></tr>
<tr><td>PSEL</td><td>1</td><td>I</td><td>VDD or VSS</td><td>Regulator Enable/Disable for Logic Power Supply2</td></tr>
<tr><td>VSS</td><td>4</td><td>P</td><td>POWER</td><td>Ground for VDD/VDDR</td></tr>
<tr><td>VSSH</td><td>4</td><td>P</td><td>POWER</td><td>Ground for VCC_C/VCC_R</td></tr>
<tr><td>VDDIO</td><td>2</td><td>P</td><td>POWER</td><td>MPU I/F PAD Power Supply(1.65V ~ 3.3V)
VDDIO should be lower than VDD or the same as VDD.</td></tr>
<tr><td>IREF</td><td>1</td><td>-</td><td>Resister</td><td>Tie 39 kΩ to VSS</td></tr>
<tr><td>BPRE</td><td>1</td><td>-</td><td>Zener or VSSH</td><td>Pre-Charge Voltage for Blue</td></tr>
<tr><td>GPRE</td><td>1</td><td>-</td><td>Zener or VSSH</td><td>Pre-Charge Voltage for Green</td></tr>
<tr><td>RPRE</td><td>1</td><td>-</td><td>Zener or VSSH</td><td>Pre-Charge Voltage for Red</td></tr>
<tr><td>VSYNCO</td><td>1</td><td>O</td><td>Floating</td><td>Vertical Sync. Output</td></tr>
<tr><td>VSYNC</td><td>1</td><td>I</td><td>MPU or VDDIO</td><td>Vertical Sync. Input when RGB mode is selected</td></tr>
<tr><td>HSYNC</td><td>1</td><td>I</td><td>MPU or VDDIO</td><td>Horizontal Sync. Input when RGB mode is selected</td></tr>
<tr><td>DOTCLK</td><td>1</td><td>I</td><td>MPU or VDDIO</td><td>Dot clock Input when RGB mode is selected</td></tr>
<tr><td>ENABLE</td><td>1</td><td>I</td><td>MPU or VDDIO</td><td>Video enable Input when RGB mode is selected</td></tr>
</table>

3.3 Application Block Diagram

The SEPS114A's external connection block can be classified into four blocks ; PMOLED Panel, Power supply, MCU interface, OSC block.

PMOLED Panel is connected with SEPS114A through column output(C[287:0]), row output(R[95:0]).

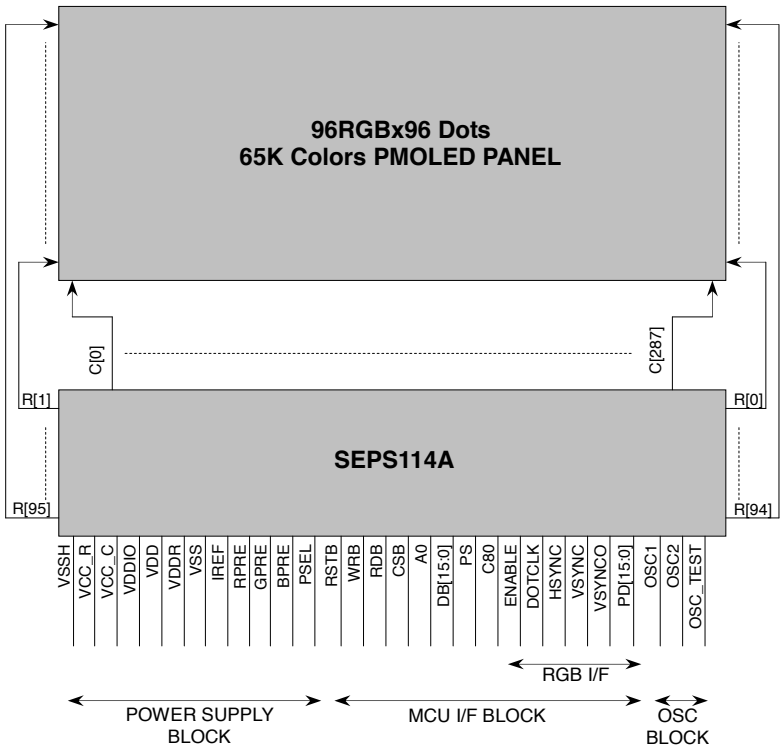


Figure 1. Application block diagram

3.3.1 Power Supply Block

VDDR, VDDIO, VDD, VCC_R and VCC_C pins supply power to SEPS114A.

Pin name	Description	Power level
VDDR	Logic Power Supply2	1.7V
VDDIO	MPU I/F PAD Power Supply VDDIO must be lower than VDD or the same as VDD.	1.65V ~ 3.3V
VDD	Logic Power Supply	2.4V ~ 3.3V
VCC_R	Scan Driver Power Supply	0.4*VCC_C ~ VCC_C
VCC_C	Data Driver Power Supply	8V ~ 18V
VSSH	Scan/Data Driver Ground	-
VSS	Logic ground	-

Table 1. Power pin description

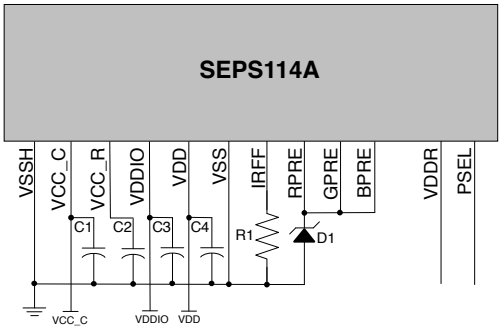


Figure 2. Power supply block

VCC_R is Scan driver power supply pin. Its level can be varied by a setting value of SCAN_OFF_LEVEL register (49h). The following table indicates VCC_R level according to a setting value.

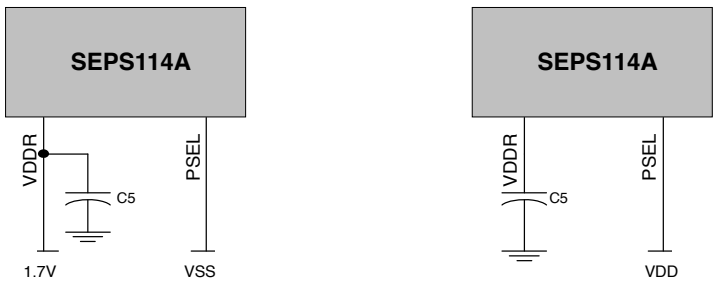
SOFF[3:0]	VCC_R Level	SOFF[3:0]	VCC_R Level	SOFF[3:0]	VCC_R Level
0x00	VCC_C*0.95	0x05	VCC_C*0.70	0x0A	VCC_C*0.45
0x01	VCC_C*0.90	0x06	VCC_C*0.65	0x0B	VCC_C*0.40
0x02	VCC_C*0.85	0x07	VCC_C*0.60	0x0F	VCC_C*1.00
0x03	VCC_C*0.80	0x08	VCC_C*0.55		
0x04	VCC_C*0.75	0x09	VCC_C*0.50		

Table 2. VCC_R Voltage Level

IREF is Iref current output pin and connected with resistor(R1). Iref is a reference current to generate the pre-charge and driving current.

RPRE, GPRE and BPRE are pre-charge voltage for Red, Green and Blue each. These pins are connected to the cathode of zener diode. The voltage level of zener diode is determined by a panel characteristics.

VDDR pin is for supply voltage(1.7V) to the memory and digital logic of SEPS114A. This voltage is generated by the internal regulator or supplied by an external voltage supplier. It is selected by PSEL pin whether using the internal regulator or an external voltage supplier. If PSEL is VDD, the internal regulator is used. Otherwise, an external voltage supplier is used. Please refer to the following figure 3.



<External voltage supply> <Internal regulator>

Figure 3. VDDR & PSEL Configuration

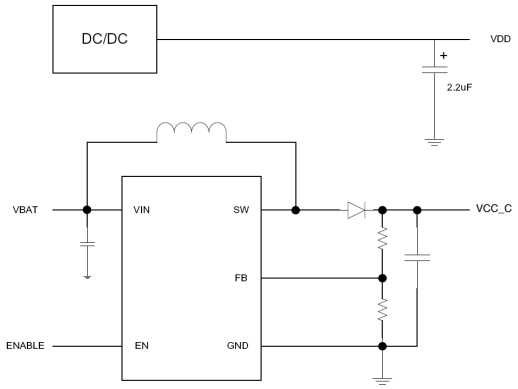
The external components value of power supply block is as the below table.

Item	Description
C1	Capacitor - 1μF/25V
C2	Capacitor - 4.7μF/25V
C3	Capacitor - 0.1μF/16V
C4	Capacitor - 0.1μF/16V
C5	Capacitor – 2.2μF/16V
R1	Resistor - 39kΩ, 1%

Table 3. External component value

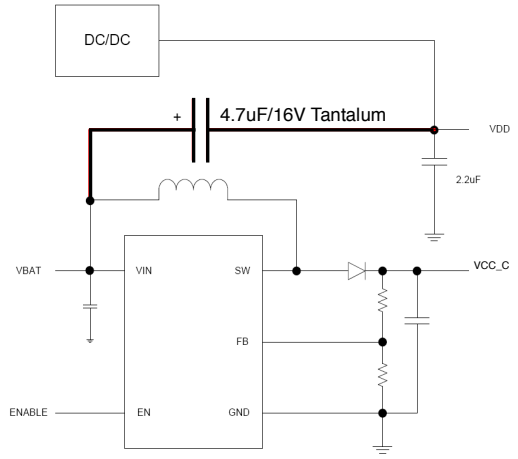
3.3.2 Leakage Current on Abnormal Power Sequence

The leakage current(High voltage current, Ivcc_c) could be created in case of specific application condition. For example, once battery of cell phone is removed and put on again, Vbat is supplied like picture 4. In that case, if VDD/Input pins are floated or grounded at the same time with Vbat supplying, the leakage current in the VCC_C is created.



Picture 4. Power supply block on a application system

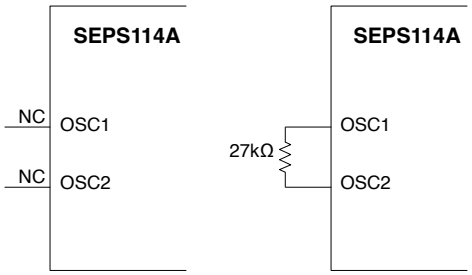
To prevent this leakage current, a capacitor should be added between VDD and VBAT. It is recommended that the 4.7uF/16V tantalum capacitor is used. Please refer to the following picture 5.



Picture 5. Prevent from leakage current

3.3.3 OSC Block

OSC1 and OSC2 are pins to connect a resistor for RC oscillation, or pins for external clock input. Figure 4 is the application that uses a resistor for RC oscillation. It allows fine adjustment for oscillation.
When the external clock mode is selected, OSCA1 is used for external clock input.



<Internal Resistor> <External Resistor>

Figure 6. Internal Clock Mode

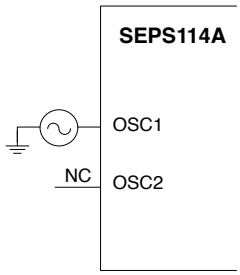


Figure 7. External Clock Mode

3.3.4 MCU Interface Block

The SEPS114A has three high-speed system interface : a 68-series, an 80-series 6/8/16 bit bus and a clock synchronous serial(SPI : Serial Peripheral Interface). A specific mode is selected by the setting of PS pin and CPU_IF register(0x0D).

Interface Mode	80-Series				68-Series				SPI
	6bit (RGB)	6bit (BGR)	8bit	16bit	6bit (RGB)	6bit (BGR)	8bit	16bit	-
CPU_IF(0x0D)	0x02	0x03	0x00	0x01	0x02	0x03	0x00	0x01	Don't care
PS pin connection	High(VDDIO)				High(VDDIO)				Low(VSS)
C80 pin connection	Low(VSS)				High(VDDIO)				Don't care

Table 4. MCU Interface configuration

Table 5 is the Read/Write operation control signal of each MCU mode. When 'A0' signal is low, data is command. Otherwise, data is parameter or DDRAM data.

A0	80 mode		68 mode		Operation
	RDB	WRB	RW	E	
0	0	1	1	1	Reads internal status
0	1	0	0	1	Writes indexes into IR
1	0	1	1	1	Reads from DDRAM through RDR
1	1	0	0	1	Writes into control registers and DDRAM through WDR

Table 5. Read/Write Operation Signal

For the detail operation description of MCU interface, please refer to the SEPS114A datasheet.

1) 80 Series MCU Interface => PS pin = “high”, C80 pin = ”low”

▣ 16-bit bus mode

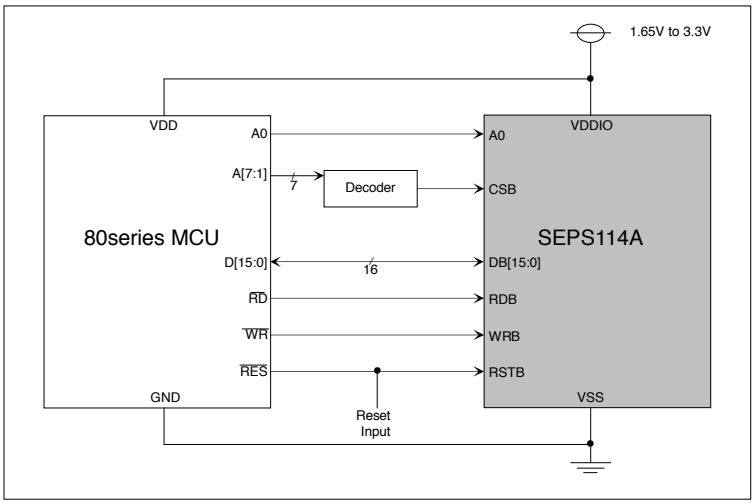


Figure 8. 80 Series MCU 16-bit Interface

► Index/Command Write

-	-	-	-	-	-	-	-	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
-	-	-	-	-	-	-	-	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0

► DDRAM Read/Write

	1st Transmission															
Input Data	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
DDRAM Data	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

▣ 8-bit/6-bit bus mode

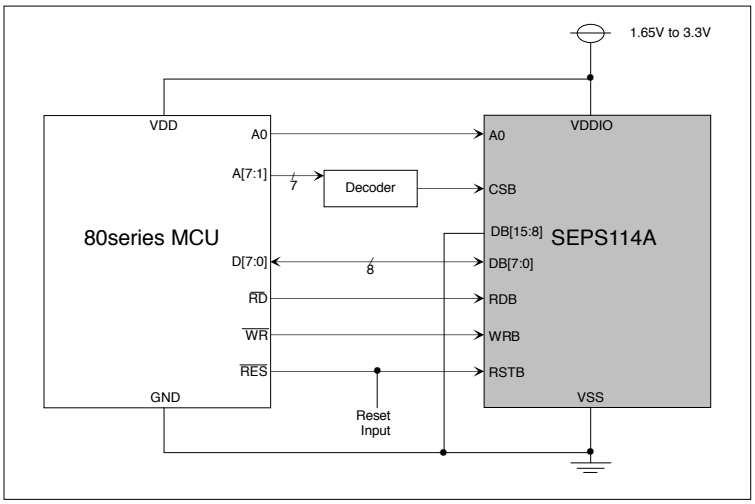
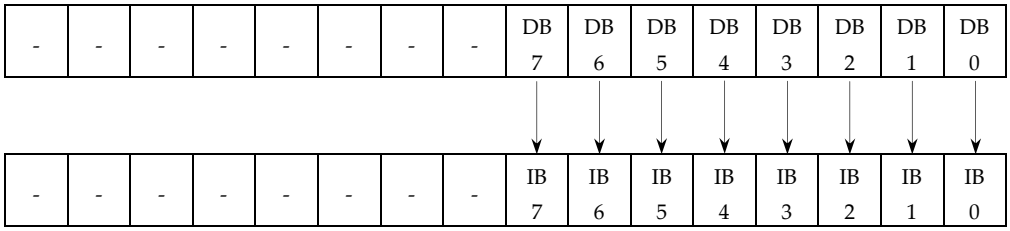
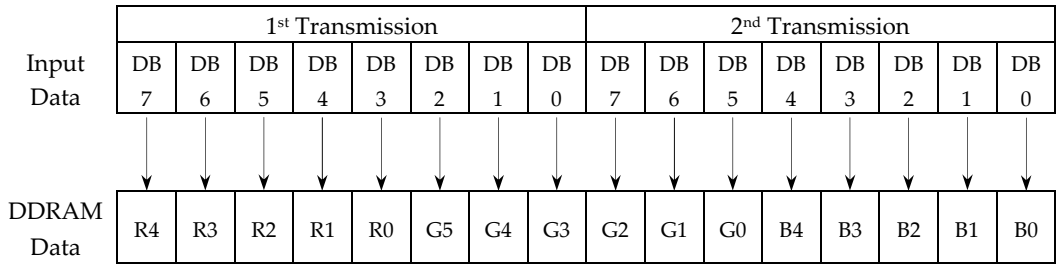


Figure 9. 80 Series MCU 8-bit/6-bit bus Interface

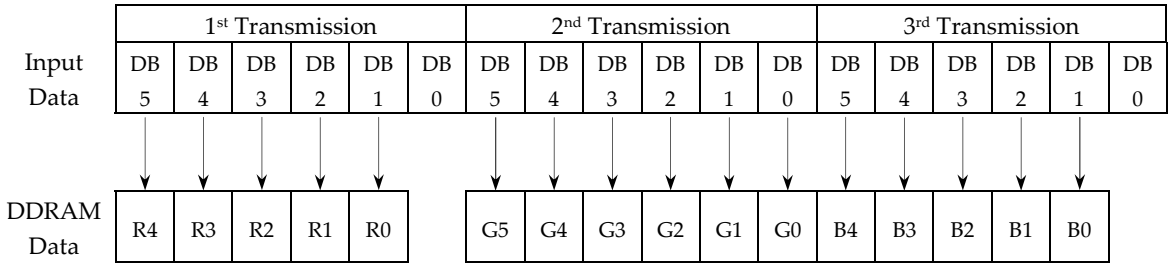
► Index/Command Write



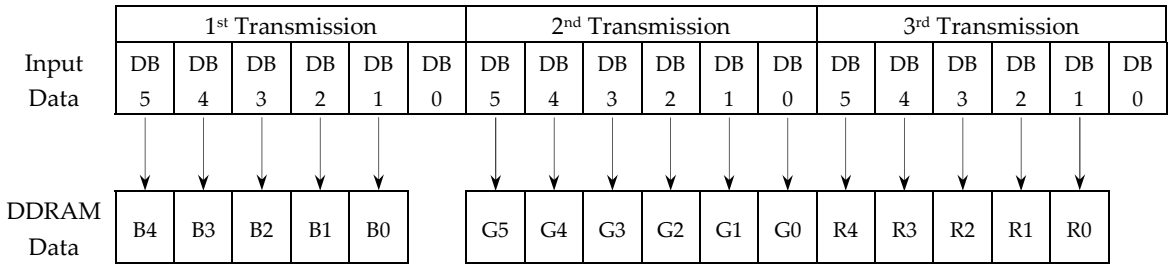
► DDRAM Read/Write(8bit bus interface)



► DDRAM Read/Write(6bit bus interface : RGB)



► DDRAM Read/Write(6bit bus interface : BGR)



◎ System BUS Read/Write Timing

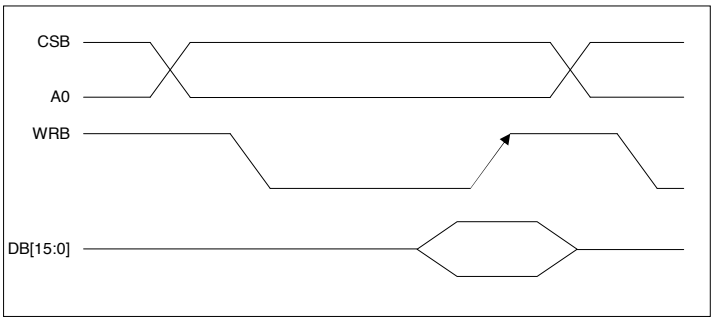


Figure 10. Write timing

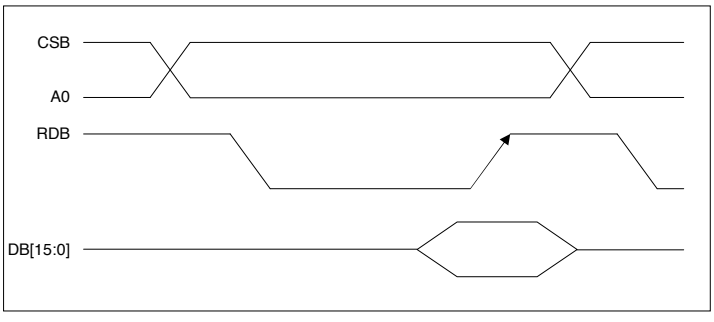


Figure 11. Read timing

2) 68 Series MCU Interface => PS pin = “high”, C80 pin = ”high”

▣ 16-bit bus mode

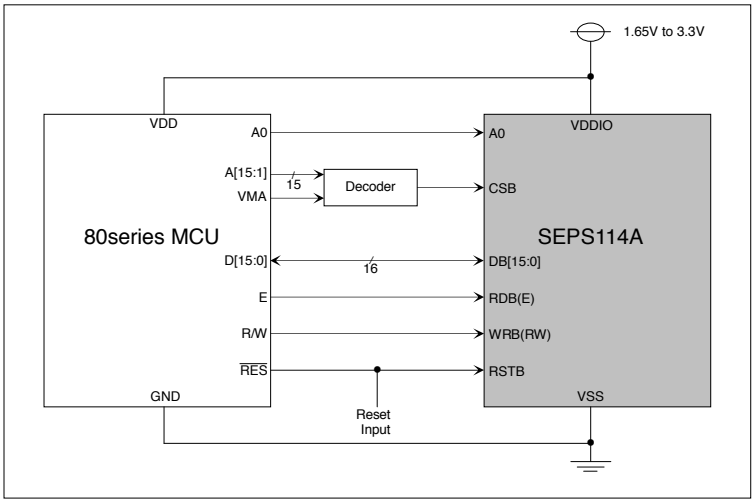


Figure 12. 68 Series MCU 16-bit bus Interface

▣ 8-bit/6-bit bus mode

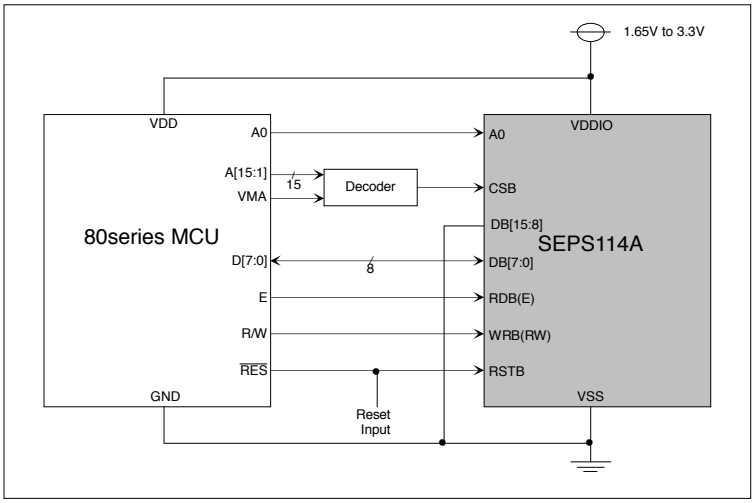


Figure 13. 68 Series MCU 8-bit/6-bit bus Interface

◎ System BUS Read/Write Timing

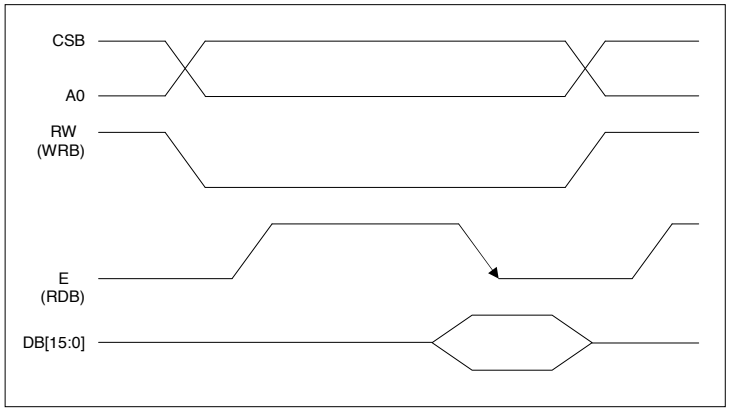


Figure 14. Write timing

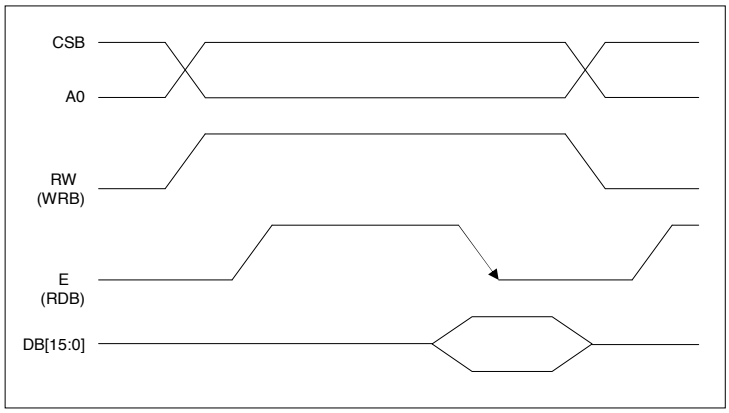


Figure 15. Read timing

3) MCU Connection With Serial Interface => PS = "low", C80 = don't care

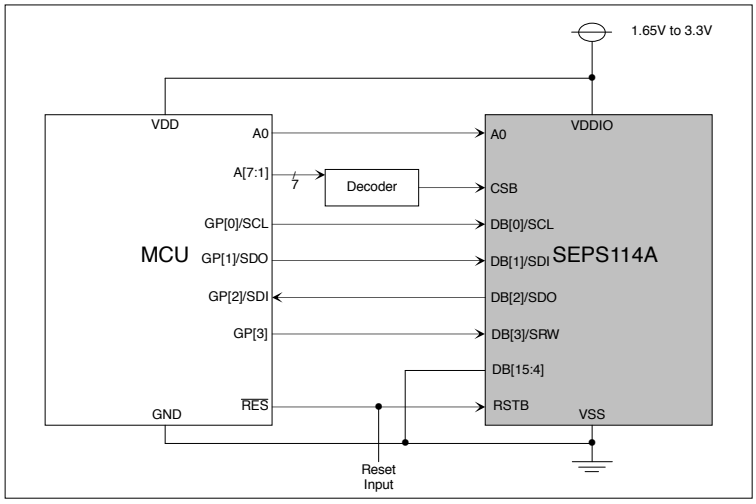


Figure 16. SPI Interface

If you don't use the SDO and SRW, make the SDO open and connect the SRW with VDDIO or VSS.

- Serial Interface Timing

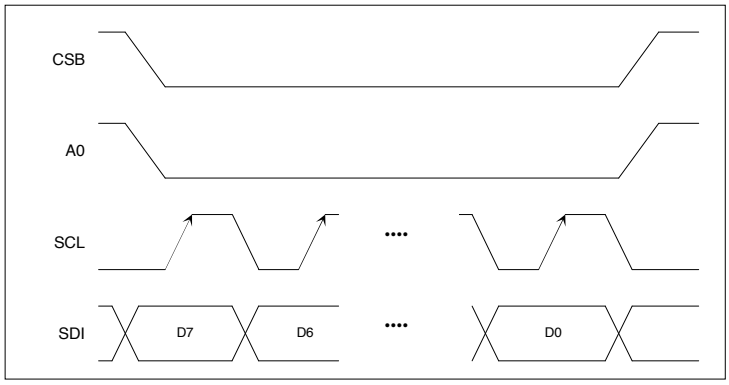


Figure 17. Index Register Write Timing

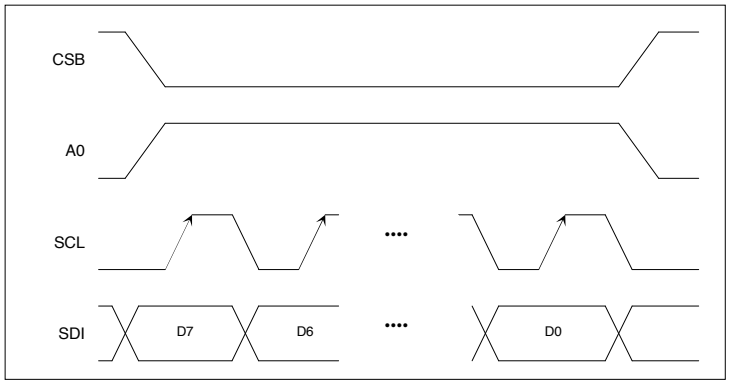


Figure 18. Control Register Timing

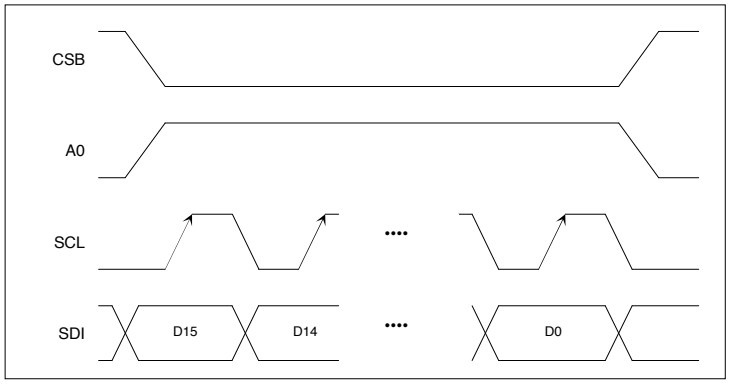


Figure 19. Memory Write Timing

3.3.5 MCU Interface Block

When the RGB_IF register(E0h) bit0 is set to "1", the SEPS114A enters the RGB interface mode and DDRAM write cycle is synchronized by DOTCLK. And the data format of RGB Interface is selected by RIM[1:0] of the RGB_IF register.

EIM	RIM1	RIM0	Interface
1	0	0	8 bit RGB
	0	1	16 bit RGB
	1	0	6 bit RGB
	1	1	6 bit BGR
0	Don't care	Don't care	MCU interface

1) RGB Interface + SPI : RGB 6bit

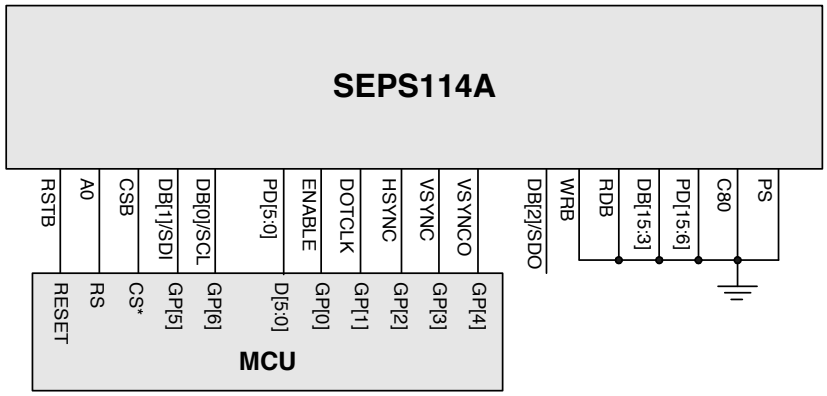


Figure 20. RGB & SPI

2) RGB Interface + Parallel Interface : RGB 6bit and Parallel 8bit(80 MCU series)

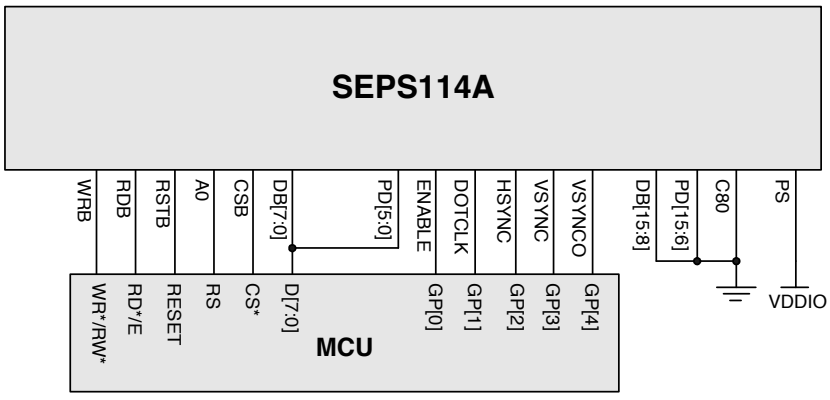
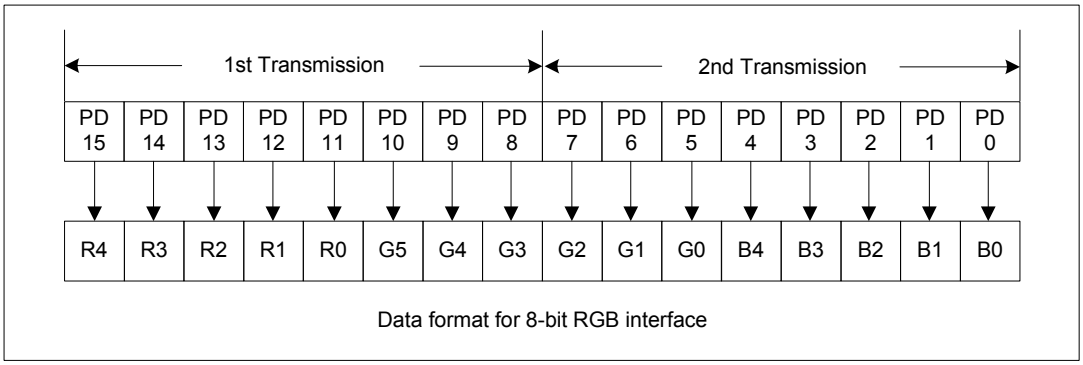
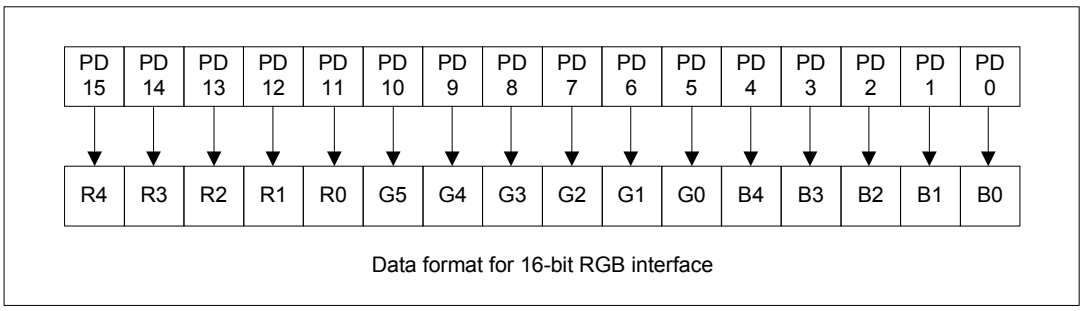


Figure 21. RGB & Parallel Interface

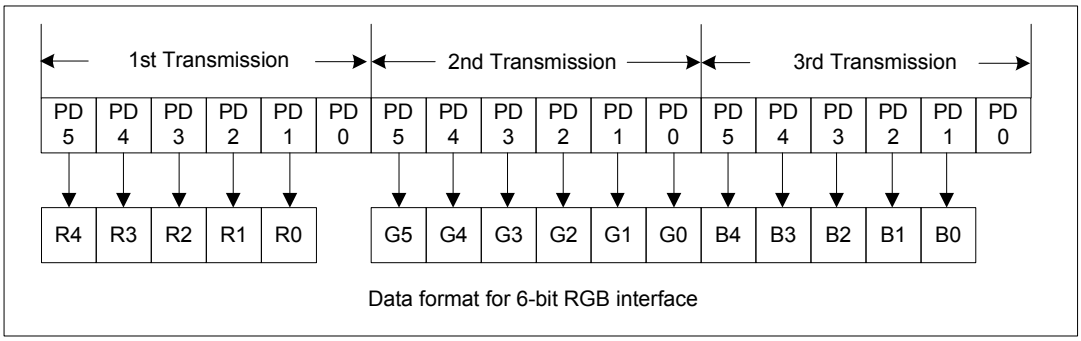
3) RGB Interface Data Format



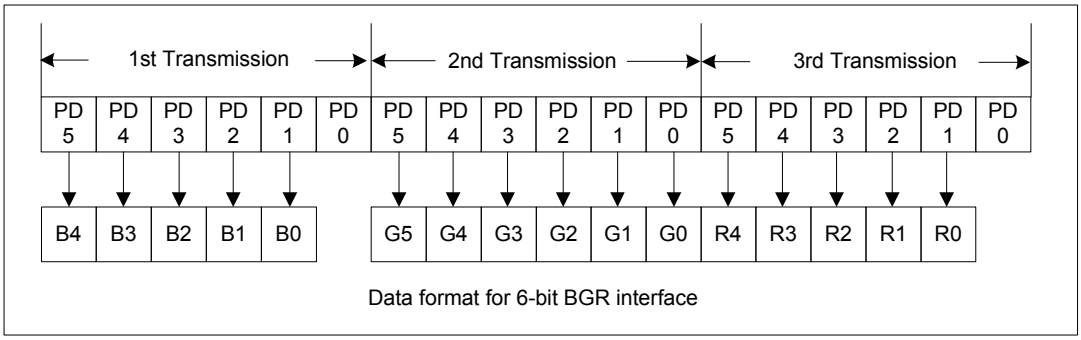
Data format for 8-bit RGB interface



Data format for 16-bit RGB interface

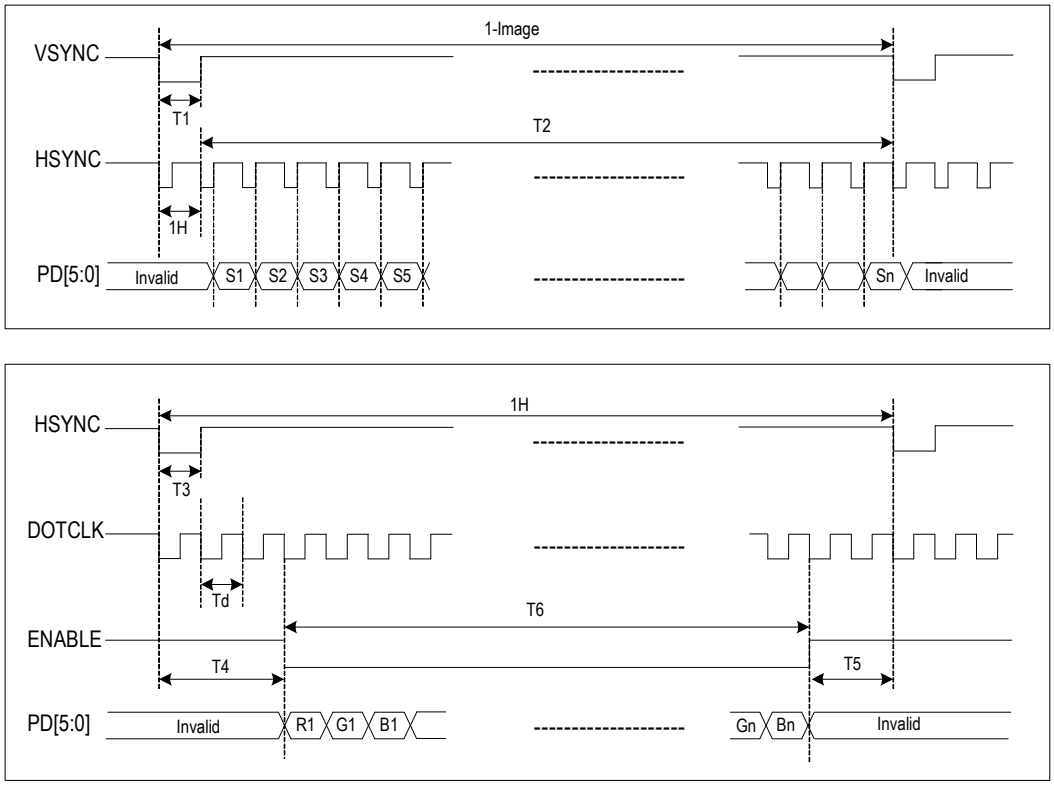


Data format for 6-bit RGB interface



Data format for 6-bit BGR interface

4) RGB Interface Timing : 6 bit interface



Symbol	Description	Remark
T1	VSYNC Pulse Width	≥ 1H, n*1H
T2	DDRAM Write Width	≤ 96H
T3	HSYNC Pulse Width	≥ Td, n*Td
T4	Setup time for Data transfer	≥ 2Td, T4>T3
T5	Hold time for Data transfer	≥ 2Td, T5>T3
T6	DDRAM Write Width	≤ 288Td
T6 = 3n, Td ≥ 100ns		

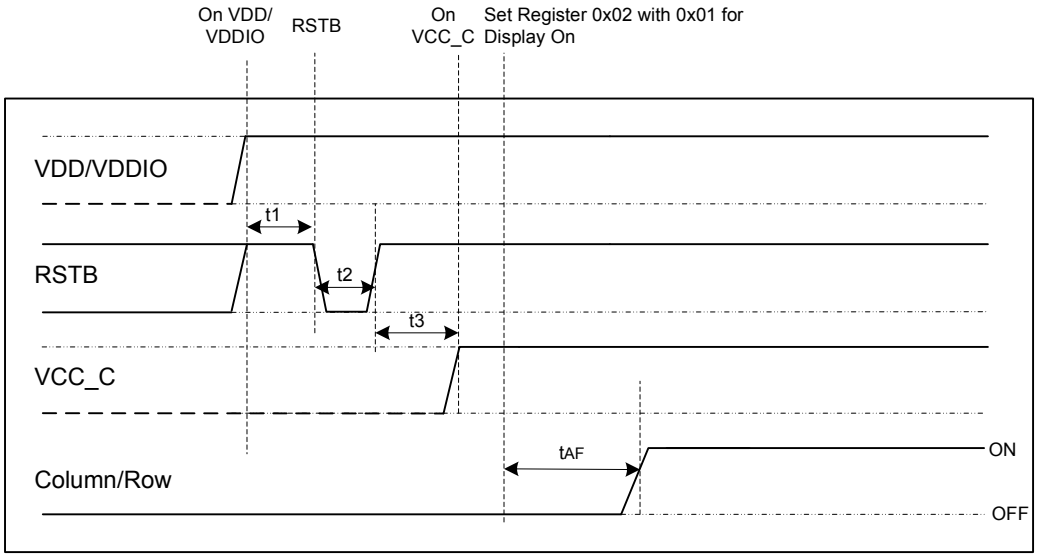
* In case of 8/16 bit interface, T6 ≤ 96Td and T6 = n.

Please refer to the SEPS114A datasheet's AC characteristics for a detail timing margin of each interface.

4. Power ON Sequence

Power ON sequence

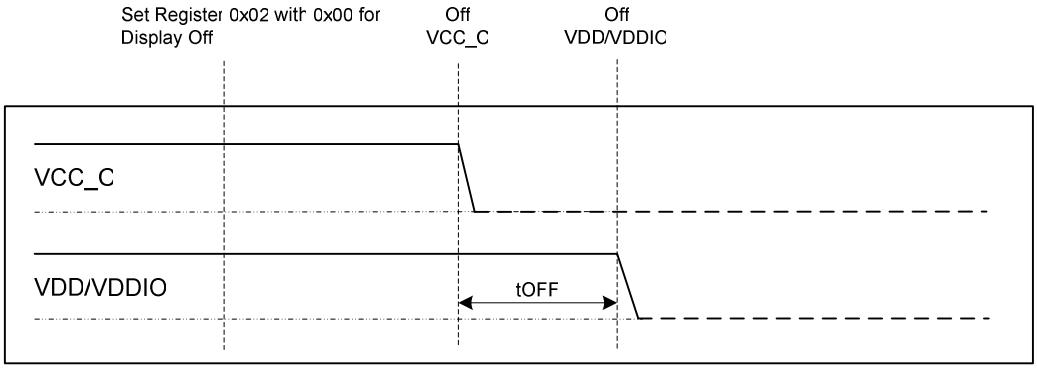
(1) Power ON VDD, VDDIO.
(2) After VDD, VDDIO become stable and wait for 100ms(t1), set RSTB pin LOW (logic low) for at least 1ms (t2) and then HIGH(logic high).
(3) After set RSTB pin HIGH (logic high), wait for at least 50ms (t3). Then Power ON VCC_C
(4) After VCC_C become stable, set register 0x02 with value 0x01 for display ON. Data/Scan will be ON after 200ms (tAF).



<Power On Sequence>

Power OFF sequence

(1) Set register 0x02 with value 0x00 for display OFF.
(2) Power OFF VCC_C
(3) Wait for tOFF. Power OFF VDD, VDDIO (where Minimum tOFF=0ms, Typical tOFF=100ms)



<Power Off Sequence>

Note :
Since ESD protection circuit is connected between VDD, VDDIO and VCC_C, VCC_C becomes lower than VDD whenever VDD, VDDIO is ON and VCC_C is OFF. VCC_C should be kept disable when it is OFF.

5. Software Configuration

The sample program as below '5.1 SEPS114A Initialization' runs under the following table of condition.

Item	Condition	Register index	Reset Value	Setting Value
Standby On/Off	Standby off	0x14	0x01	0x00
Analog Control	RC OSC. : External Resistor, CLK Mode : Internal OSC ON IREF Resistor : External	0x0F	0x80	0x00
Frame rate	90Hz	0x1A	0x03	0x02
CPU I/F	16 Bit bus interface	0x0D	0x00	0x01
Discharge Time	8 Clock	0x18	0x08	Default
Peak Pulse Delay	5 Clock	0x16	0x05	Default
Peak Pulse Width	5 Clock	0x3A, 0x3B, 0x3C	0x05	Default
Precharge Current	-	0x3D, 0x3E, 0x3F	0x00	0x5F
Column Current	-	0x40, 0x41, 0x42	0x00	0x5F
Row Scan Direction	0 → Max(Column/Row)	0x09	0x00	Default
Row Overlap	None(Band Gap Only)	0x48	0x00	Default
Scan Off Level	VCC*0.75	0x49	0x04	Default
Row Scan Mode	Alternate scan mode	0x13	0x00	Default
Display Mode Control	SWAP : RGB, Reduce current : Normal, DC[1:0] : Normal	0xE5	0x00	Default
Memory R/W Mode	Horizontally write, Vertical/Horizontal Inc	0x1D	0x00	Default
Memory Address	Horizontal start position : 0	0x34	0x00	Default
	Horizontal end position : 95	0x35	0x5F	Default
	Vertical start position : 0	0x36	0x00	Default
	Vertical end position : 95	0x37	0x5F	Default
Memory Access Point	Horizontal start position : 0	0x38	0x00	Default
	Vertical start position : 0	0x39	0x00	Default
Active Display Area	Start address of active column : 0	0x30	0x00	Default
	End address of active column : 95	0x31	0x5F	Default
	Start address of active row : 0	0x32	0x00	Default
	End address of active row : 95	0x33	0x5F	Default
Display ON	Display On	0x02	0x00	0x01

5.1 SEPS114A Initialization

After power on reset, the SEPS114A should be initialized to operate properly. The below initial routine is recommended.

```
void init_SEPS114A(void)
{
    /* Standby off */
    comm_write(0x14, 0x00);
    wait(1);                        // wait for 1ms

    /* Set Oscillator operation */
    comm_write(0x0F, 0x00);         // using external resistor and internal OSC

    /* Set frame rate */
    comm_write(0x1A, 0x02);         // frame rate : 90Hz

    /* Set MCU   Interface */
    comm_write(0x0D, 0x01);         // MPU External interface mode, 16bits

    /* Set discharge time */
    comm_write(0x18, 0x08);         // Discharge time : normal discharge

    /* Set peak pulse delay */
    comm_write(0x16, 0x05);

    /* Set peak pulse width   */
    comm_write(0x3A, 0x05);
    comm_write(0x3B, 0x05);
    comm_write(0x3C, 0x05);

    /* Set precharge current */
    comm_write(0x3D, 0x1F);
    comm_write(0x3E, 0x1F);
    comm_write(0x3F, 0x1F);

    /* Set column current */
    comm_write(0x40, 0x5F);
    comm_write(0x41, 0x5F);
    comm_write(0x42, 0x5F);

    /* Set row scan direction */
    comm_write(0x09, 0x00);         // Column : 0 → Max, Row : 0 → Max

    /* Set row overlap */
    comm_write(0x48, 0x00);         // Band gap only

    /* Set scan off level */
    comm_write(0x49, 0x04);         //VCC_C*0.75
```

```
    /* Set row scan mode */
    comm_write(0x13, 0x00);                 // Alternate scan mode

    /* Set display mode control */
    comm_write(0xE5, 0x00);                 //SWAP:RGB, Reduce current : Normal, DC[1:0] : Normal

    /* Set Memory Read/Write mode */
    comm_write(0x1D, 0x00);

    /* Set memory area(address) to write a display data */
    comm_write(0x34, 0x00);
    comm_write(0x35, 0x5F);
    comm_write(0x36, 0x00);
    comm_write(0x37, 0x5F);

    /* Set memory access point */
    comm_write(0x38, 0x00);
    comm_write(0x39, 0x00);

    /* Set active display area of panel */
    comm_write(0x30, 0x00);
    comm_write(0x31, 0x5F);
    comm_write(0x32, 0x00);
    comm_write(0x33, 0x5F);

    /* Display ON */
    comm_write(0x02, 0x01);
}
```

5.2 Write Command to Register of SEPS114A

When a command is written to the SEPS114A register, the control signal A0 indicates whether the current data is index or command. In this example the SEPS114A's A0 pin is connected to address line 2, A2. And accessing the address 0x80xx_xxxx, the control signal CS becomes 'low'.

So when user write a data(0x02) to DISP_COM that is defined below, A0 signal and CS signal become 'low' and SEPS114A indicates this data(0x02) as index.

And when data(0x01) is written to DISP_DATA, A0 is 'high' and CS is 'low', so this data(0x01) is command.

```
#define DISP_COM        *((volatile unsigned *)0x80000000)
#define DISP_DATA       *((volatile unsigned *)0x80000004)      /* A2 : OLED A0 Pin */

void comm_write(unsigned char index, unsigned char command)
{
        DISP_COM = index;                       // index write
        DISP_DATA = command;                    // command write
}
```

5.3 Write Display Data to Data RAM

This routine is to write a image data(96*96) to DDRAM by 16-bit bus interface. Firstly we should set the DDRAM access port(0x08).

```
#define HEIGHT          96
#define WIDTH           96

unsigned int img_data[HEIGHT*WIDTH];        // Image data buffer

void image_write(void)
{
        unsigned i;

        DISP_COM = 0x08;                        // Set DDRAM Access port

        for(i=0;i++;i<HEIGHT*WIDTH)
                DISP_DATA = img_data[i];        // write data to DDRAM
}
```

5.4 RGB Interface Example Program

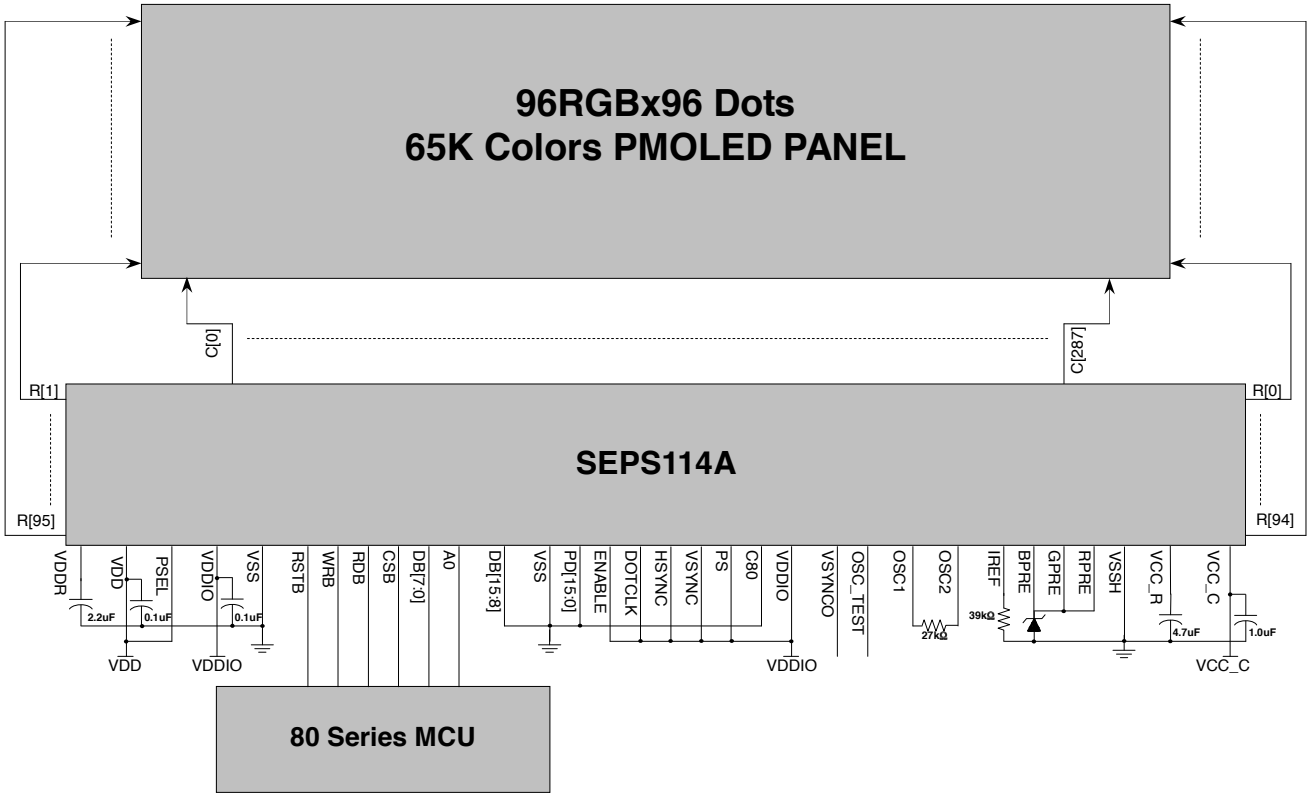
This program is an example program for 6 bit RGB interface, controlling the SEPS114A through SPI.

```
/* Select the RGB data format and set the initial state of RGB interface port */
void init_rgbif(void)
{
        reg_write_spi(0xE0, 0x21);                              /* RGB 6bit interface */

        out_signal = 1<<ENABLE|1<<HSYNC|1<<VSYNC|1<<DOTCLK;
        OUTPORT = out_signal;
}

void rgb_display(uint16_t red, uint16_t green, uint16_t blue)
{
        unsigned short i, j;

        /* SEPS114A Initialization */
        // To Do :: Initialize SEPS114A(Display size, Memory area, Frame Rate, ETC……..)
        // Using "reg_write_spi()" function(SPI Interface) to initialize

        init_rgbif();

        signal_assert(VSYNC, 0);
        signal_assert(HSYNC, 0);

        signal_assert(DOTCLK, 0);
        signal_assert(DOTCLK, 1);

        signal_assert(VSYNC, 1);
        signal_assert(HSYNC, 1);

        signal_assert(ENABLE, 0);

        /* Memory(graphic ram) port setting */
        INDEXDATA = 0x08;

        /* transfer the first row data */
        while(1)
        {
                signal_assert(VSYNC, 1);

                for(i=0;i<96;i++)
                {
                        signal_assert(HSYNC, 1);

                        for(j=0;j<96;j++)
                        {
                                CONTROLDATA = red<<1;
                                signal_assert(DOTCLK, 0);
                                signal_assert(DOTCLK, 1);
```

```
                        CONTROLDATA = green<<0;
                        signal_assert(DOTCLK, 0);
                        signal_assert(DOTCLK, 1);

                        CONTROLDATA = blue<<1;
                        signal_assert(DOTCLK, 0);
                        signal_assert(DOTCLK, 1);
                }

                signal_assert(HSYNC, 0);
        }

        signal_assert(VSYNC, 0);
    }
}


void reg_write_spi(uint32_t addr, uint32_t data)
{
    spi_write(INDEX, addr);
    spi_write(COMMAND, data);
}


void spi_write(uint8_t ch, uint32_t data)
{
    unsigned char i;
    unsigned short temp=0;

    signal_assert(CS, 0);

    if(ch == INDEX)     signal_assert(A0, 0);
    else                signal_assert(A0, 1);

    for(i=0;i<8;i++)
    {
        temp = data&(0x80>>i);

        signal_assert(SCL, 0);

        if(temp)                signal_assert(SDI, 1);
        else                    signal_assert(SDI, 0);

      signal_assert(SCL, 1);
    }
    delay(5);

    signal_assert(CS, 1);
    delay(10);
}
```

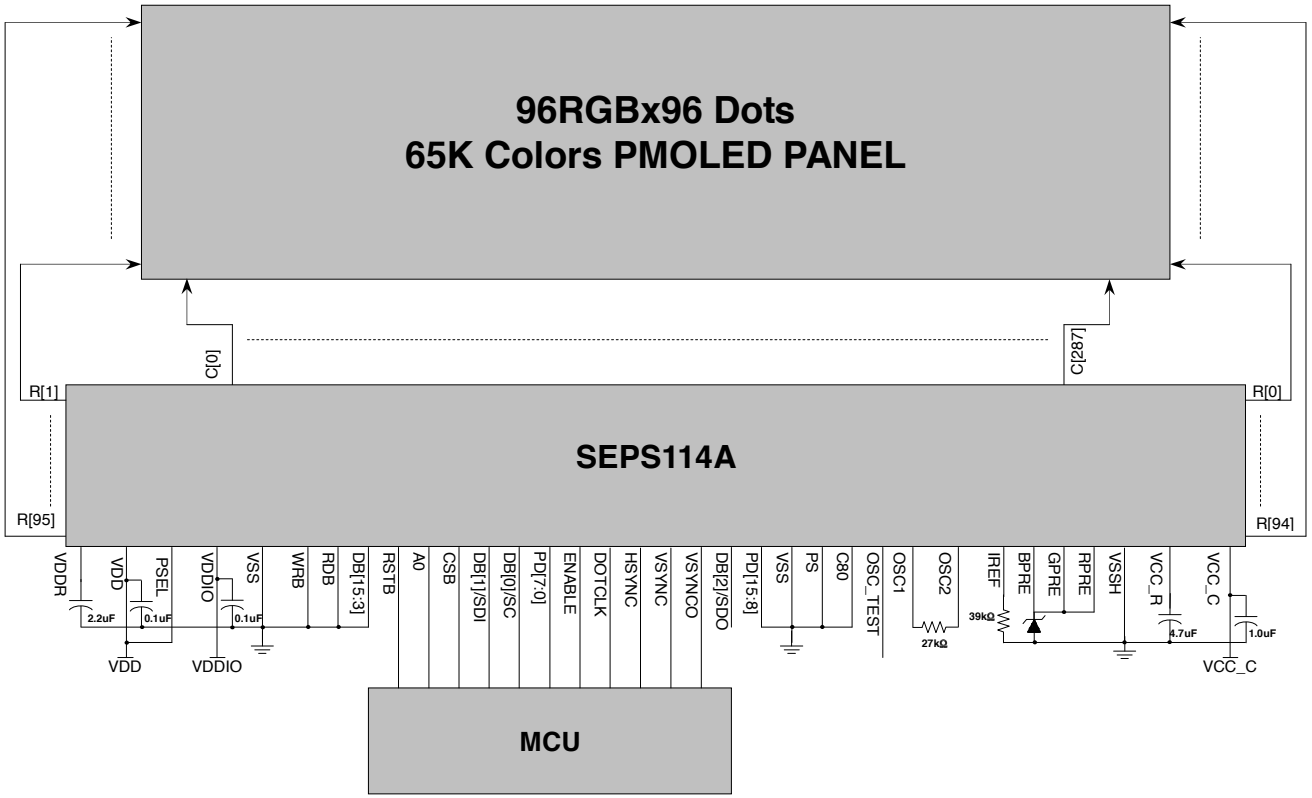
▣ APPENDIX 1. Application Circuit Example 1

- ◆ 80 Series MCU, 8bit Interface
- ◆ OSC resistor : External, IREF resistor : External
- ◆ VDDR : Internal Regulator

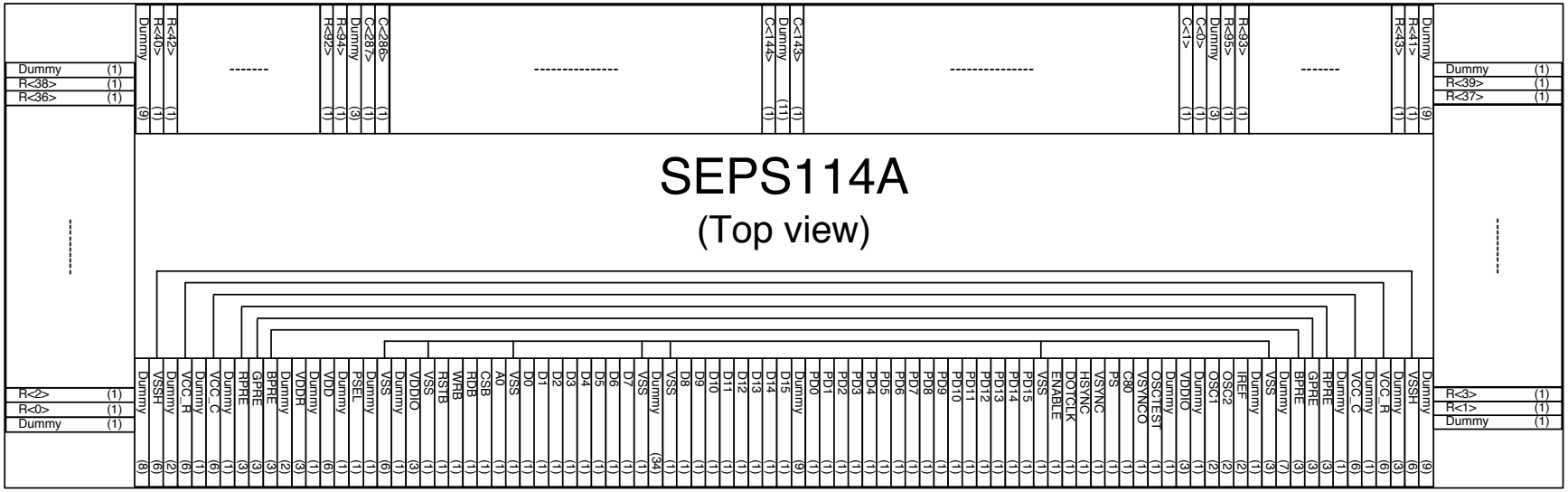


▣ APPENDIX 2. Application Circuit Example 2

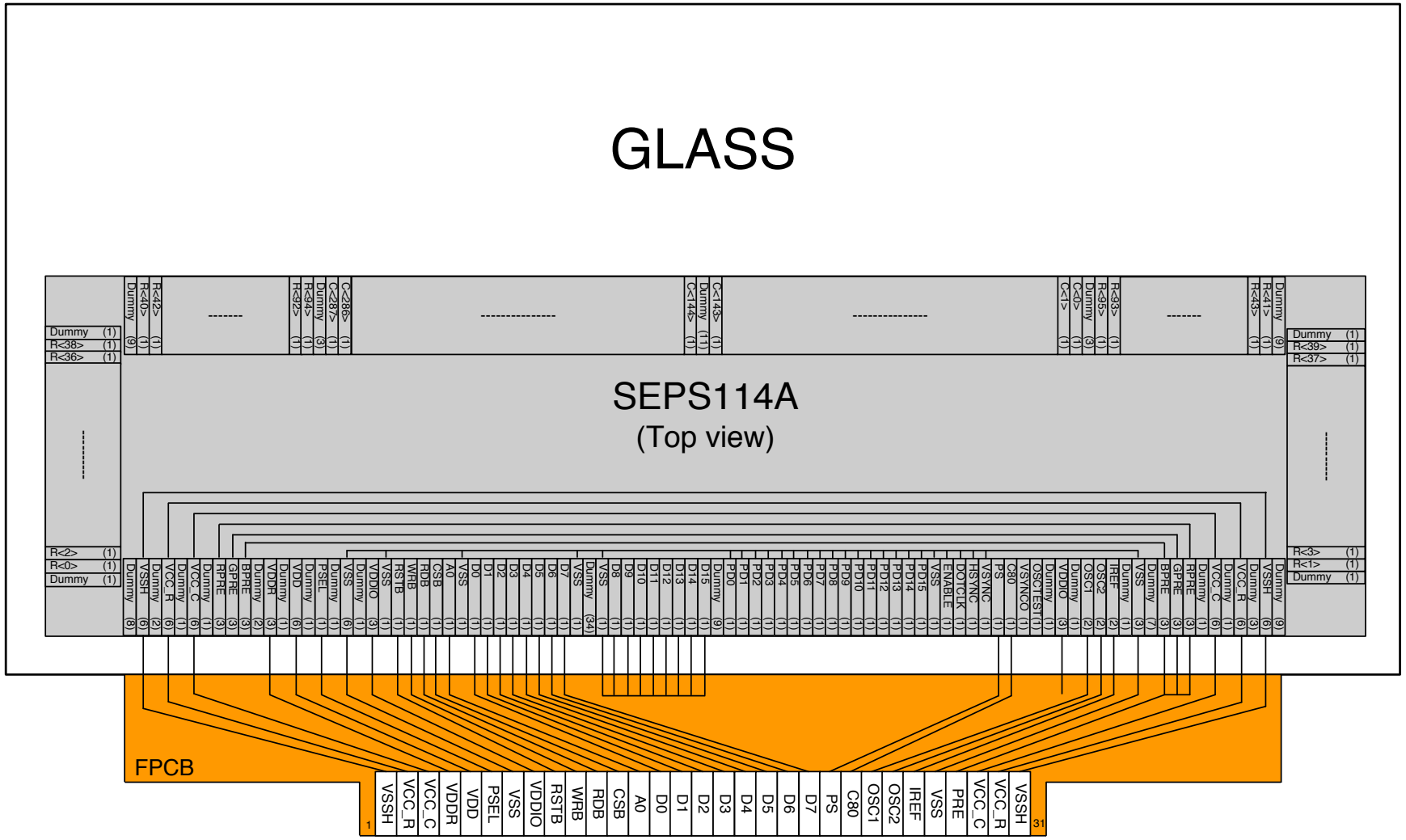
- ◆ Index/Command Write : SPI, Graphic RAM Write : RGB 8bit Interface
- ◆ OSC resistor : External, IREF resistor : External
- ◆ VDDR : Internal Regulator
- ◆ Serial Data Output unused : DB[2]/SDO → Open, DB[3]/SRW → VSS



▣ APPENDIX 3. Power PAD Connection Example



▣ APPENDIX 4. Glass & FPCB Connection Example



REVISION RECORD

Rev.	Data	Page No.	Contents of Modification	Name
0.0	2007.07.31		First issue	Andy Kim
0.1	2007.10.15	3	Driving Current Control : 153uA -> 188.7uA, 0.6uA Step -> 0.7uA Step	Andy Kim
		3	Frame Rate : 75.0 ~ 150.0 -> 80.0 ~ 140.0	
		16	Power Sequence Added	
		17	Frame Rate Setting Value : Default -> 0x02	
0.2	2007.11.21	5	Pin Description modified	Andy Kim
		16	Power Sequence modified	
0.3	2008.01.02	17, 19	ROW_SCAN_ON/OFF Index deleted	Andy Kim
0.4	2008.01.17	4	'VSS' pin is inserted between 'A0' and 'D0'	Andy Kim
		5, 7, 21, 22	PSEL connection is modified	
0.5	2008.02.11	8	'3.3.2 leakage current on abnormal power sequence' inserted	Andy Kim
0.6	2008.03.20	16	Power off sequence is inserted	Andy Kim
0.7	2008.09.10	7, 21, 22	VCC_R Connection is modified	Andy Kim
1.0	2008.12.10	23/24	Appendix 3/4 inserted	Andy Kim
		19	Power Sequence modified	
		16	RGB Interface Block inserted	
		24	RGB Interface Example Program inserted	