SEMESTER – II

Faculty of Information and Communication Engineering

M.E. VLSI Design

215VLP01 - VLSI Design Laboratory - II

(Requirement for a batch of 16 students)

Sl. No	Description of Equipment	Quantity required	Quantity available	Deficiency %
1	OMAP 3530 Processor (ARM Cortex – A8 Processor + C64X DSP)	18	20	NIL
2	PROGRAMMABLE Logic (Xilinx SPARTAN 6 FPGA)	18	20	NIL
3	Touch Screen TFT LCD Display	18	20	NIL
4	Industry Standard Peripherals like JTAG, SD card Interface, 10/100 Mbps Ethernet, UART's, USB OTG, ADC & DAC	18	20	NIL
5	Interface Debugging, Communication and I/O expansions	18	20	NIL
6	Drivers for supporting application software development on the kit	18	20	NIL
7	Embedded Linux ported on the ULK board	18	20	NIL
8	GNU Eclipse based GUI for Flash / FPGA Programming	18	20	NIL
9	Enclosure and External keypad for Processor	18	20	NIL

Adhiyamaan College of Engineering – Autonomous		Regulation		R2015
Department	Electronics and Communication Engineering	Programme Name		M.E VLSI

SEMESTER I

Course code	Course name	Hours/week			Credit	Maximum mark		
		L	T	P	C	CA	EA	Total
115VLP01	VLSI DESIGN LABORATORY I	0	0	3	2	50	50	100

Objective(s)

- To design Multiplexers, Decoders, Comparators, Counters and Shift registers
- To design FIR Filter, High Speed Multipliers, ALU using FPGA
- To realize the Universal Modulator, Real Time Clock, Traffic Light Controller and Stepper motor using FPGA
- To monitor the temperature using FPGA

Prerequisites

LIST OF EXPERIMENTS

1. Design of Multiplexers, Decoders, Comparators, Counters and Shift Registers using HDL.
2. Design of FIR Filter using HDL.
3. Design of High Speed Multipliers using HDL.
4. Design of ALU using HDL.
5. Design of Universal Modulator using HDL.
6. Realization of Real Time Clock using FPGA.
7. Realization of Traffic Light Controller using FPGA.
8. Realization of Stepper Motor using FPGA.
9. Write a VHDL Code to display messages on the given 7 Segment display accepting Hex keypad input data using FPGA.
10. Temperature monitoring using sensor through LCD Display using FPGA.
11. Realization of LED Display using FPGA.
12. Realization of Waveform Generation using FPGA.

Course outcomes

- Ability to design Multiplexers, Decoders, Comparators, Counters and Shift registers
- Ability to design FIR Filter, High Speed Multipliers, ALU using FPGA
- Ability to realize the Universal Modulator, Real Time Clock, Traffic Light Controller and Stepper motor using FPGA
- Monitoring the temperature using FPGA

Professor and Head
Department of Electronics and Communication Engineering
Adhiyamaan College of Engineering (Autonomous)
HOSUR - 635 109. Krishnagiri Dt., Tamil Nadu

Adhiyamaan College of Engineering – Autonomous		Regulation				R2015		
Department	Electronics and Communication Engineering		Programme Name			M.E VLSI DESIGN		
SEMESTER II								
Course code	Course name	Hours/week			Credit	Maximum mark		
		L	T	P	C	CA	EA	Total
215VLP01	VLSI DESIGN LABORATORY II	0	0	3	2	50	50	100
Objective(s)	• To design FIFO, MAC Unit, Vetribi decoder, AES using UTLP. • To Realize ADC, I^2C Bus, LCD (Touch and Character) using UTLP. • To Realize FFT, convolution filter using UTLP.							
Prerequisites	Nil							

LIST OF EXPERIMENTS

1. Design & implementation of high speed FIFO.
2. Design & implementation of MAC unit.
3. Design & implementation of vetribi decoder.
4. Realization of Analog to Digital Converter.
5. Implementation of Ethernet protocol.
6. Design & implementation of IIR filter.
7. Realization of Finite Fourier Transforms (FFT).
8. Design & implementation of Advanced Encryption Standard (AES).
9. Realization of Inter-Integrated Circuit (I^2C) Bus.
10. Realization of the given message through character Liquid Crystal Display (LCD).
11. Realization of convolution filter.
12. Realize the process of the given image through Touch Liquid Crystal Display (LCD) using ARM processor.

Course Outcomes

- Ability to design FIFO, MAC Unit, Vetribi decoder.
- Ability to Realize ADC, I^2C Bus, LCD (Touch and Character).
- Ability to Realize FFT, convolution filter

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ADHIYAMAAN COLLEGE OF ENGINEERING

(Autonomous)

Affiliated to Anna University- Chennai. Approved by AICTE - New Delhi
Accredited by NBA, AICTE & NAAC with 'A' Grade - UGC - New Delhi.
(An ISO 9001:2008 Certified Institution)

Dr. M.G.R. Nagar, HOSUR - 635 109, Krishnagiri (Dist.), Tamil Nadu, India.

Phone : Off. : 04344 - 260570, 261001-3, 261020
Website : www.adhiyamaan.ac.in
Fax : 04344 - 260573
E-mail : principal@adhiyamaan.ac.in

PO No:432/2014 Date: 07.05.2014

To,

iWave Systems Technologies Pvt Ltd.
No. 7/B, 29th Main, BTM Layout 2nd Stage,
Bangalore - 560 076, India.

Dear Sir,

Sub: Purchase order for the 20 sets of Unified Technology Learning Platform (UTLP) – Reg

With reference to the above, we are pleased to issue the purchase order for the supply of 20 UTLP sets as per the following agreed terms and conditions.

S.No.	Description	Qty	Unit price	Amount
	Unified Technology Learning Platform **Specifications:** • OMAP 3530 Processor (ARM Cortex-A8 Processor + C64X DSP) • Programmable logic (Xilinx SPARTAN 6 FPGA) • Touch screen TFT LCD Display • Industry standard peripherals like JTAG, SD Card Interface, 10/100 Mbps Ethernet, UART's, USB OTG, ADC & DAC • Interfaces Debugging, Communication & I/O expansions • Drivers for supporting application software development on the kit • Embedded Linux ported on the ULK board • GNU Eclipse based GUI for Flash/FPGA programming and application development Enclosure and external keypad	20 Nos	30,000	6,00,000.00
			Total	6,00,000.00
			Add: Excise Duty @ 12.36%	74,160.00
			Add: VAT @ 5.5%	37,079.00
			Grand Total	**7,11,239.00**

(Rupees Seven Lakhs Eleven Thousand Two Hundred and Thirty Nine Only)

DESPATCHED
19.3.14

Principal
Adhiyamaan College of Engineering
Dr. M.G.R. Nagar, HOSUR - 635 109

இந்தியன் ஓவர்சீஸ் வங்கி

इण्डियन ओवरसीज़ बैंक Indian Overseas Bank

K. Palli .... கிளை शाखा Branch

07-03- 2014

வ.டு./அ.வ.மா/ डी डी/एमटी/दे जो

DD/MT on .... Bangalore .... पर आहरित हो

(மாவட்டத்தையும் குறிப்பிடுக)(जिला का नाम भी लिखें Indicate District also)

பெயர் नाम Favouring .... inware systems

Technologies Pvt. Ltd

	ரூ. Rs.	ைபெ. P.
தொகை रकम Amonut	3,55,206	-
பரிமாற்றம் विनिमय Exchange	34	-
மொத்தம் कुल Total	3,55,240	-

TRANSFER

விண்ணப்பதாரர் பெயர் முகவரி ....

आवेदक का नाम व पता .... ACE

Applicant's Name and Address .... Hosur

UTR NO: IOBAH14066110667

காசாளர்
खजांची Cashier

துணை மேலாளர்
उप-प्रबंधक Dy. Manager

(Vertical margin text:) இந்த பகுதி சீட்டானது வங்கியின் அலுவலர் ஒருவரால் கையொப்பமிடப்படவில்லை என்றால் செல்லுபடியாகாது ... यह प्रतिपर्ण बैंक के किसी अधिकारी (नकदी जमा करने के मामले में खजांची के साथ-साथ) द्वारा हस्ताक्षरित नहीं होने पर विधिमान्य नहीं होगा। This Counterfoil is not valid unless signed by an official of the Bank (in addition to the cashier in case of deposit by cash)

(On Letter Head)

Purchase Order No: Date:

To,

iWave Systems Technologies Pvt Ltd.
No. 7/B, 29th Main, BTM Layout 2nd Stage,
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2.	Excise Duty @ 12.36%			**Rs. 74,160/-**
3.	VAT @ 5.5%			**Rs.37,079/-**
	TOTAL			**Rs. 7,11,239/-**