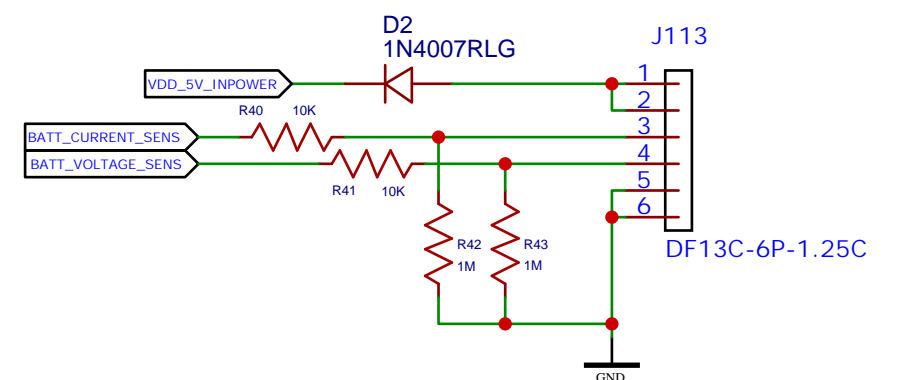
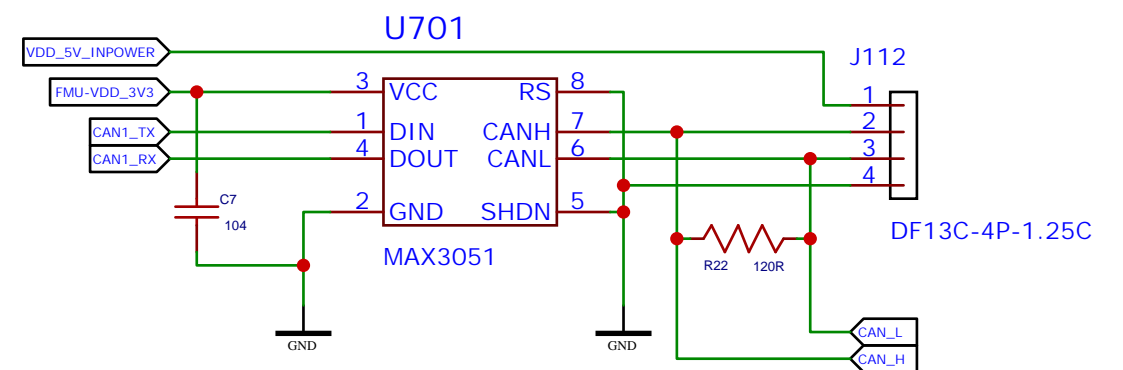
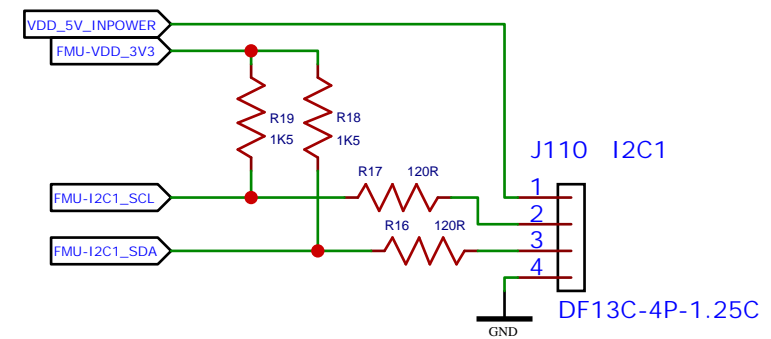
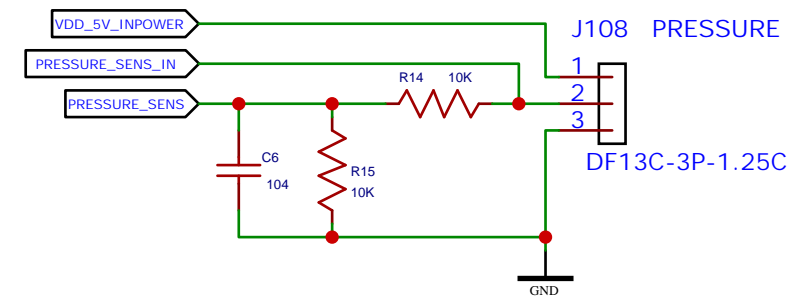
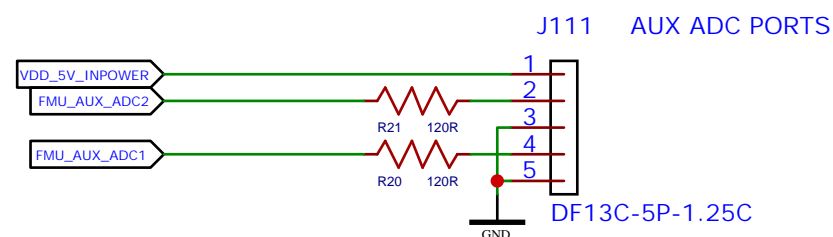
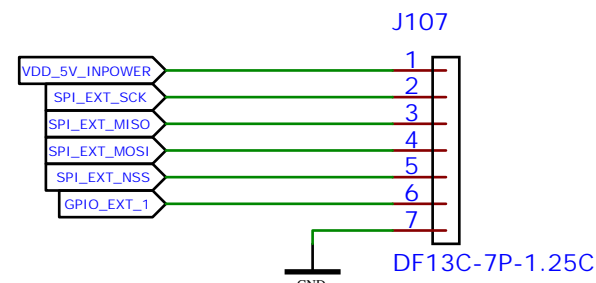
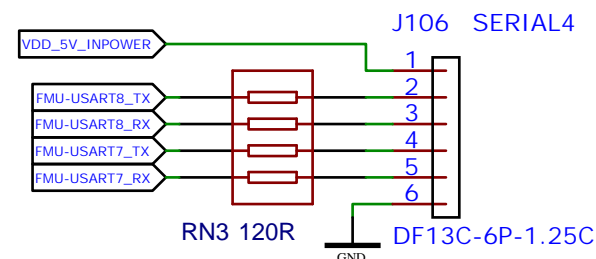
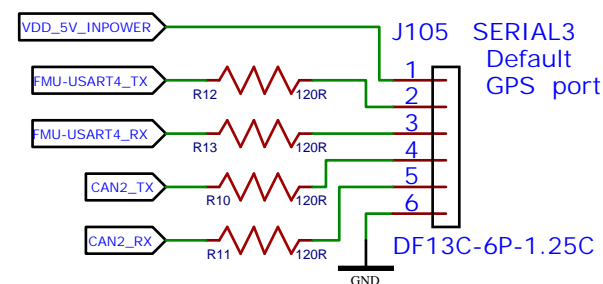
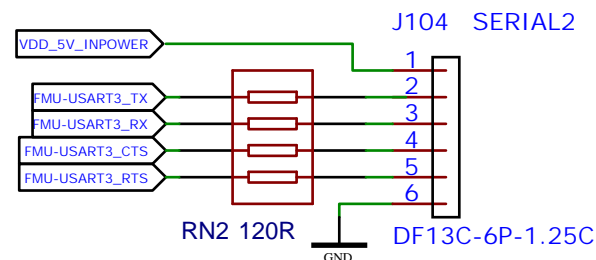
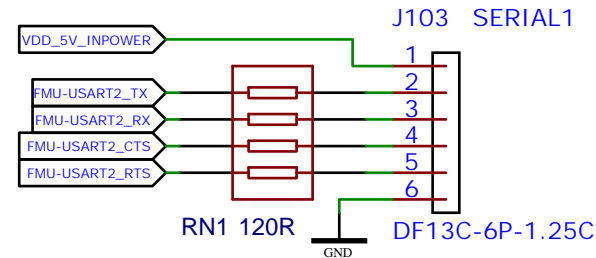
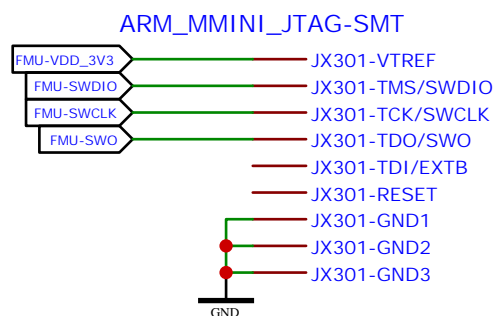
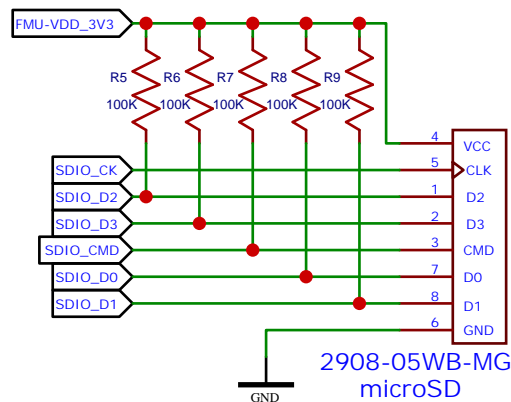
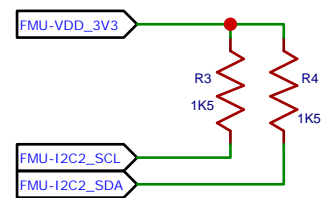
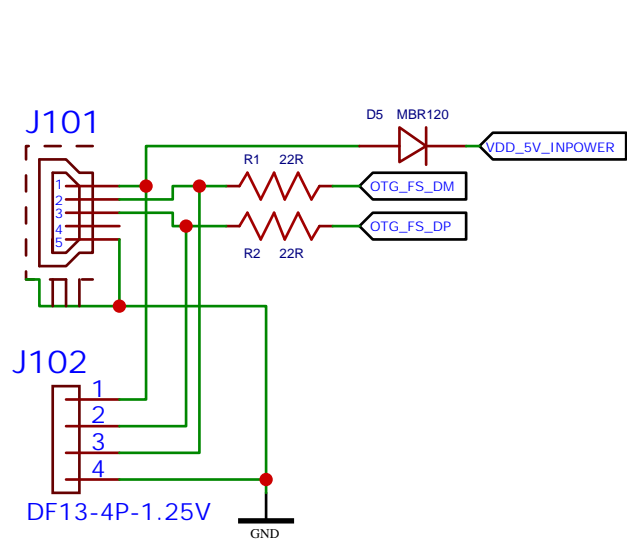
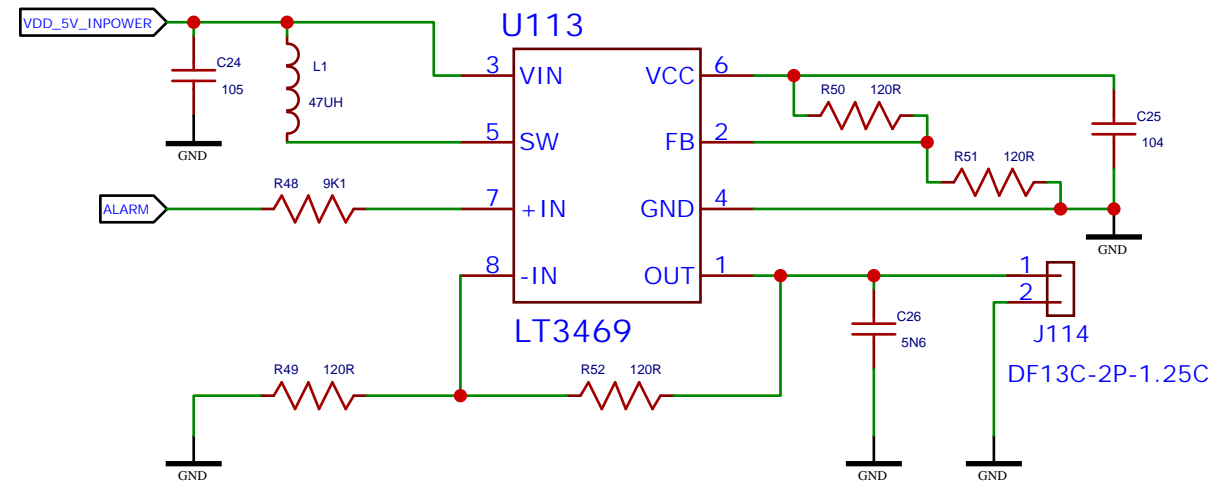


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Figure 1 illustrates the 14-channel FMU system. Each channel (FMU-CH1 to FMU-CH14) is connected to a 120R resistor (R23 to R36) and a corresponding J901 connector (J901-1 to J901-14).

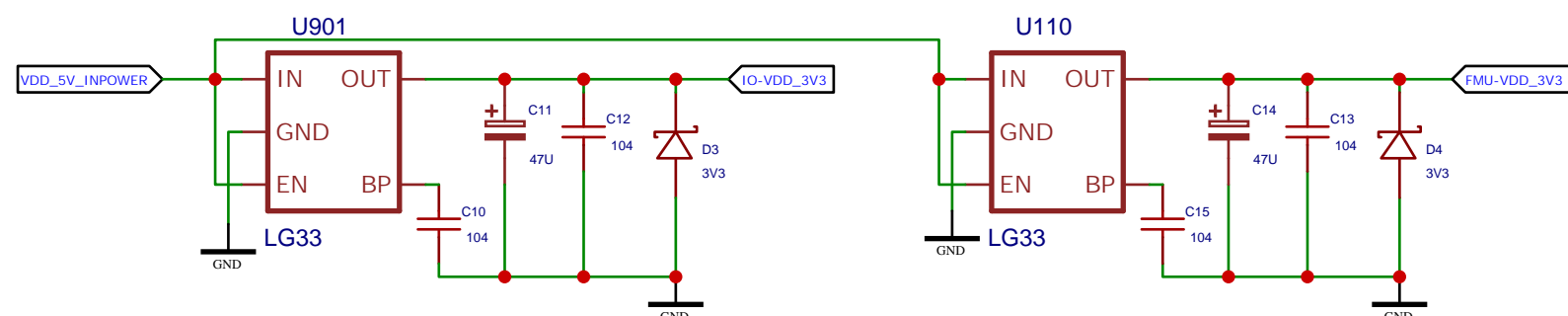
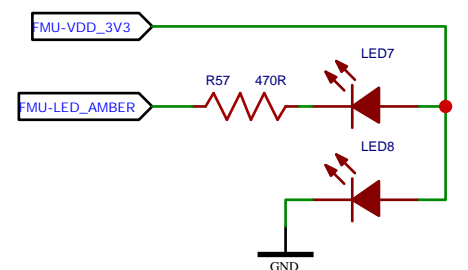
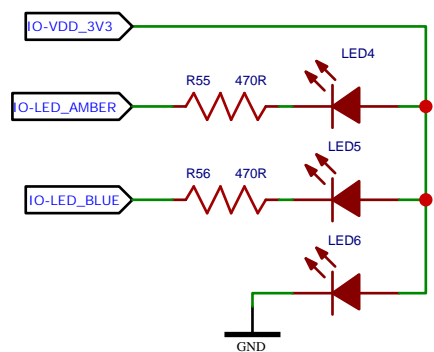


The schematic diagram shows the U801 component, a 74LVC2G240, which is a dual in-line package (DIP) with 14 pins. The pins are labeled as follows:

- Pin 1: 1OE
- Pin 2: 1A
- Pin 3: 1Y
- Pin 4: GND
- Pin 5: 2A
- Pin 6: 2Y
- Pin 7: 2OE
- Pin 8: VCC
- Pin 9: 1OE
- Pin 10: 1A
- Pin 11: 1Y
- Pin 12: GND
- Pin 13: 2A
- Pin 14: 2Y

The component is connected to various signals and power sources:

- Signal Inputs:** PPM\_INPUT, SBUS\_INPUT, IO-VDD\_3V3, SUBS\_OUTPUT, SUBS\_OUTPUT\_EN, and RSSI\_IN.
- Power and Grounding:** VCC (Pin 8) is connected to a 3.3V supply (IO-VDD\_3V3). GND (Pin 4) is connected to ground. A 104 capacitor (C8) is connected between the VCC and GND pins.
- Output Connections:** The output pins (1Y, 2Y, 1OE, 2OE) are connected to various signals and power sources. Pin 1Y is connected to a 120R resistor (R37) and a 120R resistor (R38). Pin 2Y is connected to a 120R resistor (R39) and a 120R resistor (R38). Pin 1OE is connected to a 120R resistor (R37) and a 120R resistor (R38). Pin 2OE is connected to a 120R resistor (R39) and a 120R resistor (R38).
- Power and Grounding (Bottom Section):** VDD\_5V\_INPOWER is connected to a 5V supply. A 47Ux3 capacitor (C9) is connected between the VDD\_5V\_INPOWER and ground. A diode (D1, MBR120) is connected between the VDD\_5V\_INPOWER and ground. A 120R resistor (R38) is connected between the VDD\_5V\_INPOWER and ground.



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