Code:

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 10:42:27 10/07/2019

// Design Name:

// Module Name: mod10\_11\_dwmsy

// Project Name:

// Target Devices:

// Tool versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module mod10\_11\_dwmsy(

input t,

output [3:0]q,

input clk,

input reset

);

wire a,b,c,d;

tff f0(t,clr,q[0],clk,reset);

tff f1(q[0],clr,q[1],clk,reset);

and(a,q[1],q[0]);

tff f2(a,clr,q[2],clk,reset);

and(b,a,q[2]);

tff f3(b,clr,q[3],clk,reset);

and(c,q[0],~q[1]);

and(d,~q[2],q[3]);

assign clr=c&d;

endmodule

Testbench:

`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 19:44:16 11/11/2019

// Design Name: mod10\_11\_dwmsy

// Module Name: C:/Users/swapnil/Desktop/121933011/MOd10\_syn/test\_mod10.v

// Project Name: MOd10\_syn

// Target Device:

// Tool versions:

// Description:

//

// Verilog Test Fixture created by ISE for module: mod10\_11\_dwmsy

// Dependencies:

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

module test\_mod10;

// Inputs

reg t;

reg clk;

reg reset;

// Outputs

wire [3:0] q;

// Instantiate the Unit Under Test (UUT)

mod10\_11\_dwmsy uut (

.t(t),

.q(q),

.clk(clk),

.reset(reset)

);

always #5 clk=~clk;

initial begin

// Initialize Inputs

t = 0;

clk = 0;

reset = 1;

#10

reset = 0;

#10;

t=1;

end

endmodule