

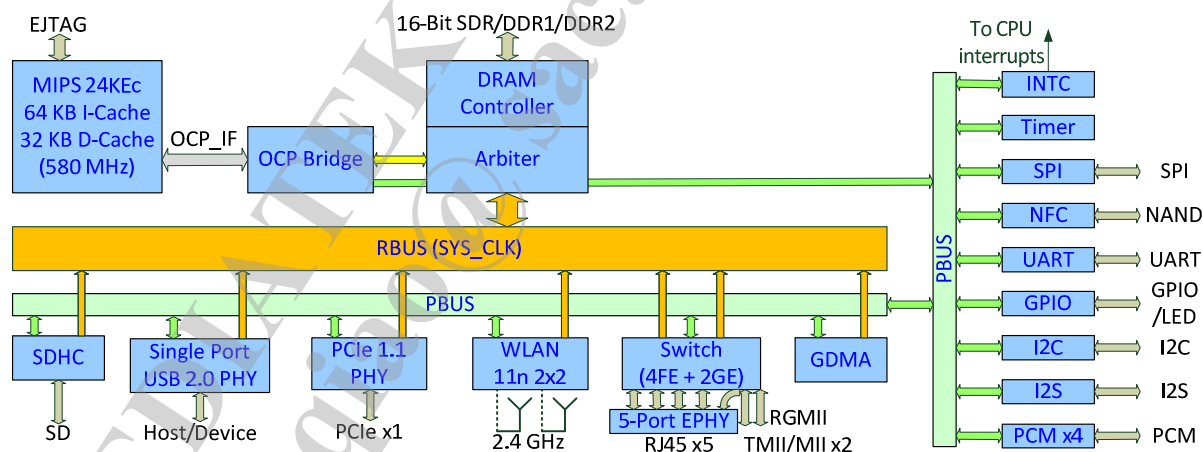
# MT7620 DATASHEET

Integrated 802.11n MAC/BBP and 2.4 GHz RF/FEM Router-on-a-Chip



The MT7620 router-on-a-chip includes an 802.11n MAC and baseband, a 2.4 GHz radio and FEM, a 580 MHz MIPS® 24K™ CPU core, a 5-port 10/100 switch and two RGMII. The MT7620 includes everything needed to build an AP router from a single chip. The embedded high performance CPU can process advanced applications effortlessly, such as routing, security and VoIP. The MT7620 also includes a selection of interfaces to support a variety of applications, such as a USB port for accessing external storage.

- Embedded MIPS24KEc (580 MHz) with 64 KB I-Cache and 32 KB D-Cache
- 2T2R 2.4 GHz with 300 Mbps PHY data rate
- Legacy 802.11b/g and HT 802.11n modes
- 20/40 MHz channel bandwidth
- Legacy 802.11b/g and HT 802.11n modes
- Reverse Data Grant (RDG)
- Maximal Ratio Combining (MRC)
- Space Time Block Coding (STBC)
- 16-bit SDRAM up to 64 Mbytes
- 16-bit DDR1/2 up to 128/256 Mbytes (MT7620A)
- SPI, NAND Flash/SD-XC
- 1x USB 2.0, 1x PCIe host/device
- 5-port 10/100 SW and two RGMII
- An optimized PMU
- Green AP
  - Intelligent Clock Scaling (exclusive)
  - DDR1: ODT off, Self-refresh mode
  - SDRAM: Pre-charge power down
- I2C, I2S, SPI, PCM, UART, JTAG, MDC, MDIO, GPIO
- Hardware NAT with IPv6 and 2 Gbps wired speed
- 16 Multiple BSSID
- WEP64/128, TKIP, AES, WPA, WPA2, WAPI
- QoS: WMM, WMM-PS
- WPS: PBC, PIN
- Voice Enterprise: 802.11k+r
- AP Firmware: Linux 2.6 SDK, eCOS with IPv6
- RGMII iNIC Driver: Linux 2.4/2.6



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| Part Number | Package<br>(Green/RoHS Compliant) |
|-------------|-----------------------------------|
| MT7620A     | TFBGA 265 ball<br>(11 mm x 11 mm) |
| MT7620N     | DR-QFN 148 pin<br>(12 mm x 12 mm) |

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## 1. Main Features

The following table covers the main features offered by the MT7620N and MT7620A. Overall, the MT7620N supports the requirements of an entry-level AP/router, while the more advanced MT7620A supports a number of interfaces together with a large maximum RAM capacity.

| Features                | MT7620N  | MT7620A   |
|-------------------------|--|---|
| <b>CPU</b>              | MIPS24KEc (600/580 MHz)                                  | MIPS24KEc (580 MHz)   |
| <b>Total DMIPs</b>      | 580 x 1.6 DMIPs  | 580 x 1.6 DMIPs   |
| <b>I-Cache, D-Cache</b> | 64 KB, 32 KB   | 64 KB, 32 KB  |
| <b>L2 Cache</b>         | n/a  | n/a   |
| <b>HNAT/HQoS</b>        | HNAT   | HNAT 2 Gbps forwarding  |
| <b>Memory</b>           |  |   |
| <b>DRAM Controller</b>  | 16 b   | 16 b  |
| <b>SDRAM</b>            | 512 Mb, 120 MHz  | n/a   |
| <b>DDR1</b>             | 512 Mb, 193 MHz  | n/a   |
| <b>DDR2</b>             | 512 Mb, 193 MHz  | 2 Gb, 193 MHz   |
| <b>NAND</b>             | n/a  | Small page 512Byte (max 512M bit)<br>Large page 2Kbyte (max 8G bit) |
| <b>SPI Flash</b>        | 3B addr mode (max 128Mbit)<br>4B addr mode (max 512Mbit) | 3B addr mode (max 128Mbit)<br>4B addr mode (max 512Mbit)            |
| <b>SD</b>               | n/a  | SD-XC (class 10)  |
| <b>RF</b>               | 2T2R 802.11n 2.4 GHz                                     | 2T2R 802.11n 2.4 GHz  |
| <b>PCIe</b>             | n/a  | 1   |
| <b>USB 2.0</b>          | 1  | 1   |
| <b>Switch</b>           | 5p FE SW   | 5p FE SW + RGMII(1)<br>4p FE SW + RGMII(2)                          |
| <b>I2S</b>              | n/a  | 1   |
| <b>PCM</b>              | n/a  | 1   |
| <b>I2C</b>              | 1  | 1   |
| <b>UART</b>             | 1 (Lite)   | 2 (Lite/Full)   |
| <b>JTAG</b>             | 1  | 1   |
| <b>Package</b>          | DRQFN148- 12 mm x 12 mm                                  | TFBGA265- 11 mm x 11 mm   |

Table 1-1 Main Features

## 2. Pins

### 2.1 TFBGA (11 mm x 11 mm) 265 Ball Package Diagram

#### 2.1.1 DDR2 Ball Map

| 26<br>5 | 1                 | 2                | 3                | 4                   | 5            | 6         | 7            | 8            | 9            | 10            | 11           | 12         | 13            | 14        | 15         | 16         | 17          |   |
|---------|-------------------|------------------|------------------|---------------------|--------------|-----------|--------------|--------------|--------------|---------------|--------------|------------|---------------|-----------|------------|------------|-------------|---|
| A       | RF0_OUT_P         | RF0_PA2_V33N     | RF0_I_N          | BG_EXTR             | XTAL_XI      | XTAL_XO   | BBPLL_V12A   | SPI_MOSI     | PCIE_RXP     | PCIE_TXN      | APCK_RFCK_OP |            | FB            | DCDC_V33D | UGAT_E     | VFB_DDR    | VFB_DIG     | A |
| B       | RF0_PA1_V33A      | RF0_OUT_N        | RF0_VX_LDO       | PLL_VC_CAP          | XTAL_V12A    |           | SPI_WP       | SPI_HOLD     | PCIE_RXN     | PCIE_TXP      | APCK_RFCK_ON |            |               | LGAT_E    | NC         | DCDC_V33A  | EXT_LDO_DIG | B |
| C       | RF1_I_N           | GND              |                  | GND                 | ADC_VX_LDO   | PORST_N   | SPI_CS0      | SPI_MISO     | SPI_CS1      | PCIE_REXT     | PCIE_RFCKP   | UPHY0_V12D |               | COMP      | UPHY0_VRES | UPHY0_PADM | UPHY0_PADP  | C |
| D       | RF1_OUT_P         | GND              | RF1_VX_LDO       | BG_V33A             | ANT_TRN      | WDT_RST_N | GPIIO0       | SPI_CLK      | SOC_I0_V33D0 | PERST_N       | PCIE_RFCK_N  | APCK_V12A  |               | GE2_RXCLK | GE2_RXDV   | GE1_RXDV   | GE1_RXCLK   | D |
| E       | RF1_OUT_N         | RF1_PA2_V33N     | RF1_PA1_V33A     | ANT_TRNB            | PA_PE_GO     | PA_PEG1   | SOC_C0_V12D1 | SOC_C0_V12D0 | APCK_V12A    | PCIE_V33A     |              |            | UPHY0_V33A    | GE2_RXD3  | GE2_RXD1   | GE1_RXD1   | GE1_RXD0    | E |
| F       |                   | GND              |                  |                     |              |           | GND          | GND          | GND          | GND           | GND          | GND        | GE2_I0_V33D   | GE2_RXD2  | GE2_RXD0   | GE1_RXD3   | GE1_RXD2    | F |
| G       |                   |                  |                  | WLED_N              | SOC_I0_V33D1 | GND       | GND          | GND          | GND          | GND           | GND          | GND        | GE2_I0_V33D   | GE2_TXEN  | GE2_TXCLK  | GE1_TXEN   | GE1_TXCLK   | G |
| H       | EPHY_LED3_N_JTCLK | EPHY_LED2_N_JTMS | EPHY_LED1_N_JTDI | EPHY_LED0_N_JTDO    | DDR_I0_V18D  | GND       | GND          | GND          | GND          | GND           | GND          | GND        |               | GE2_TXD2  | GE2_TXD3   | GE1_TXD1   | GE1_TXD0    | H |
| J       | MD14              | MD9              | MODT             | EPHY_LED4_N_JTRST_N | DDR_I0_V18D  | GND       | GND          | GND          | GND          | GND           | GND          | GND        |               | GE2_TXD1  | GE2_TXD0   | GE1_TXD3   | GE1_TXD2    | J |
| K       | MD12              | MD11             | MCS_N            | GND                 | DDR_I0_V18D  | GND       | GND          | GND          | GND          | GND           | GND          | GND        | SOC_C0_V12D3  | MDC       | MDIO       |            |             | K |
| L       | MD10              | MD13             | MRAS_N           | MA0                 | DDR_I0_VREF  | GND       | GND          | GND          | GND          | GND           | GND          | GND        | SOC_C0_V12D3  | EPHY_V12A | EPHY_V12A  |            |             | L |
| M       | MD8               | MD15             | MCAS_N           | MA2                 | DDR_IOC_V12D | GND       | GND          | GND          | SOC_C0_V12D2 | SOC_IOC_V33D2 | GND          | GND        | EPHY_PLL_V12A | MDI_RN_P3 | MDI_RP_P3  | MDI_TP_P4  | MDI_TN_P4   | M |

| 26<br>5 | 1         | 2         | 3    | 4                    | 5    | 6                       | 7                   | 8                      | 9                                      | 10                        | 11                  | 12                 | 13            | 14                | 15                   | 16                | 17                |   |
|---------|-----------|-----------|------|----------------------|------|-------------------------|---------------------|------------------------|--|---------------------------|---------------------|--------------------|---------------|-------------------|----------------------|-------------------|-------------------|---|
| N       | MDQ<br>S1 | MDQ<br>M1 | MA4  | DDR<br>_IOC<br>_V12D | MA13 | DDR_I<br>O<br>_V18<br>D |                     |                        | SOC_C<br>O<br>_V12D<br>_2              | SOC<br>_IO<br>_V33D<br>_2 | GND                 | EPHY<br>_V33<br>_A | EPHY<br>_V33A | MDI<br>_TN<br>_P3 | MDI<br>_TP_P<br>_3   | MDI<br>_RP<br>_P4 | MDI<br>_RN<br>_P4 | N |
| P       | MCK_<br>P | MCK_<br>N | MA6  | MA8                  | MA12 | MA7                     | DDR<br>_IO<br>_V18D | ND_CS<br>_N            | ND_CL<br>E/ SD<br>_CARD<br>_DETE<br>CT | ND_W<br>P/ SD<br>_WP      | DSR_N               | RXD                | TXD2          | MDI<br>_TP<br>_P2 | MDI<br>_TN<br>_P2    | MDI<br>_RP<br>_P2 | MDI<br>_RN<br>_P2 | P |
| R       | MD5       | MD2       | MA11 | MA9                  | MA5  | MA3                     | MBA2                | ND_RB<br>_N/<br>SD_CLK | ND_RE<br>_N                            | ND_AL<br>E/<br>SD_CM<br>D | ND<br>_WE<br>_N     | TXD                | RTS_N         | RXD2              | EPHY<br>_RES<br>_VBG | MDI<br>_RP<br>_P1 | MDI<br>_RN<br>_P1 | R |
| T       | MD0       | MD6       | MD4  | MDQ50                | MA1  | MBA1                    | MWE<br>_N           | ND_D6/<br>BT<br>_WACT  | ND_D4<br>/<br>BT_ST<br>AT              | ND_D2<br>/<br>SD_D2       | ND<br>_D0/<br>SD_D0 | DCD<br>_N          | RIN           | I2C_S<br>D        | MDI<br>_RN<br>_P0    | MDI<br>_TP<br>_P1 | MDI<br>_TN<br>_P1 | T |
| U       | MD7       | MD1       | MD3  | MDQM<br>0            | MA10 | MBA0                    | MCKE                | ND_D7/<br>BT_ANT       | ND_D5<br>/<br>BT_AU<br>X               | ND_D3<br>/<br>SD_D3       | ND<br>_D1/<br>SD_D1 | DTR<br>_N          | CTS_N         | I2C<br>_SCLK      | MDI<br>_RP<br>_P0    | MDI<br>_TP_P<br>0 | MDI<br>_TN<br>_P0 | U |
|         | 1         | 2         | 3    | 4                    | 5    | 6                       | 7                   | 8                      | 9                                      | 10                        | 11                  | 12                 | 13            | 14                | 15                   | 16                | 17                |   |

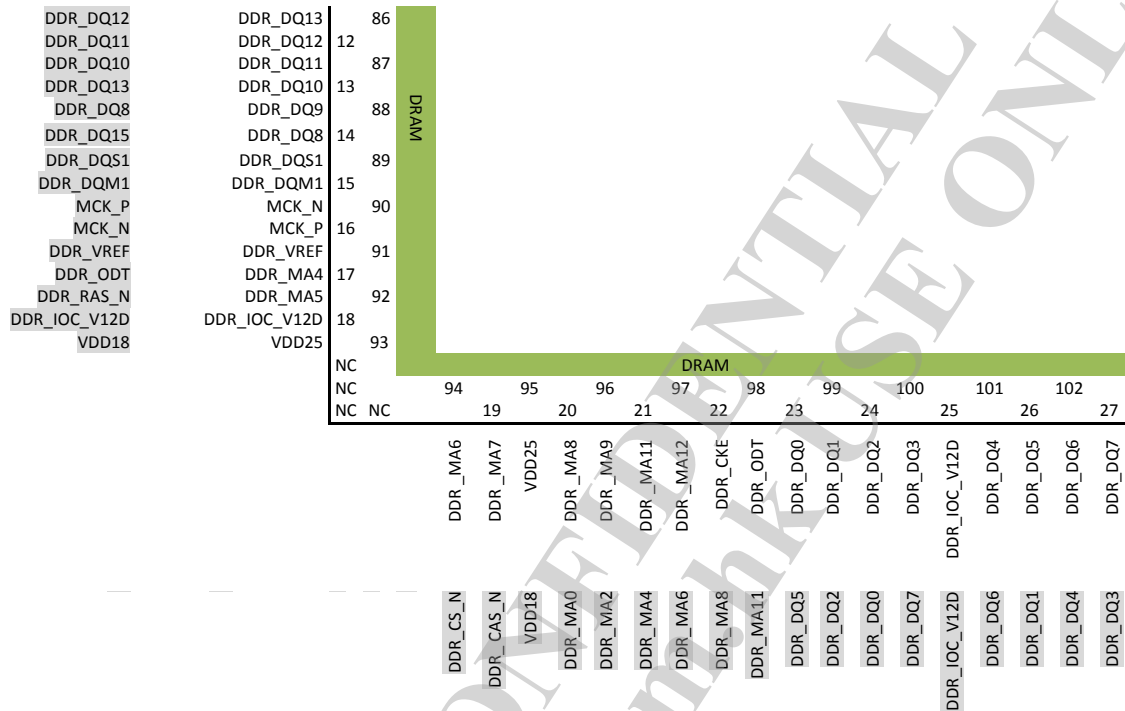
Table 2-1 DDR2 Ball Map

## 2.2 DR-QFN (12 mm x 12 mm) 148-Pin Package Diagram

### 2.2.1 Left side view







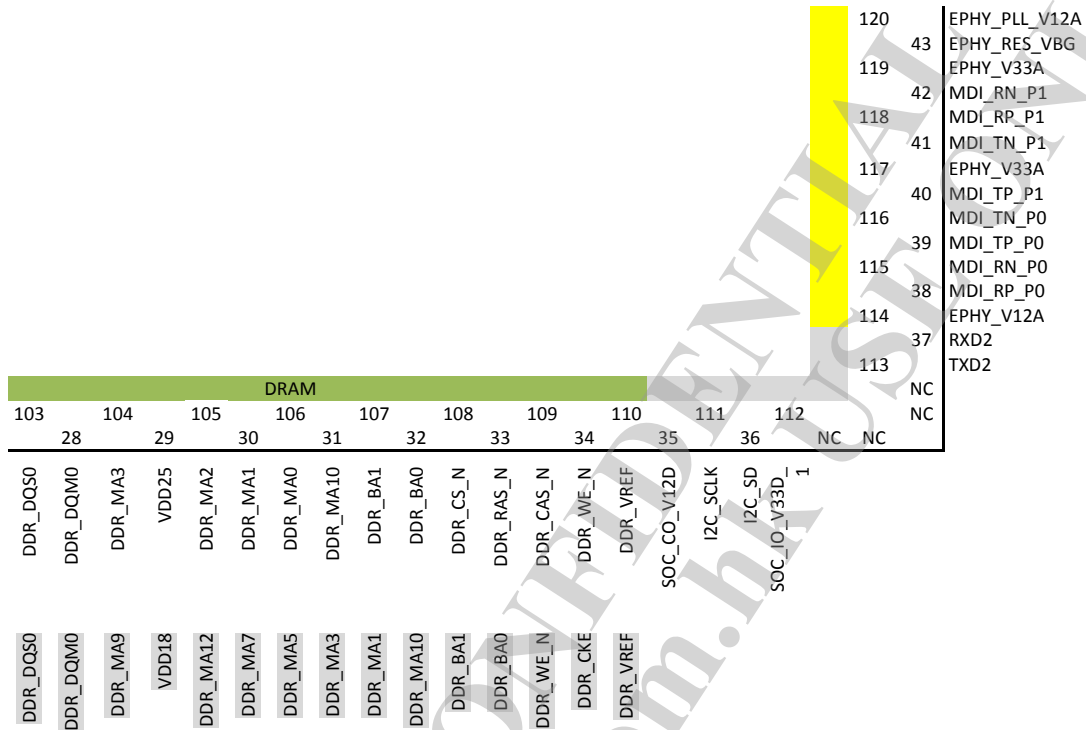


Figure 2-2 DR-QFN Pin Diagram (right side view)

Note: DR-QFN support SDR/DDR1 and DDR2 pin shuffle depend on the bootstrap. For DDR2 pin assignment, please refer to left column and bottom row using DDR\_ format.

### 2.3 Pin Descriptions (TFBGA)

| Pin                       | Name      | Type     | Driv. | Description                               |
|---------------------------|-----------|----------|-------|---|
| <b>WLAN LED</b>           |           |          |       |   |
| G4                        | WLED_N    | O, IPU   | 4 mA  | WLAN Activity LED                         |
| <b>UART Lite</b>          |           |          |       |   |
| R14                       | RXD2      | I, IPU   | 4 mA  | UART Lite RXD                             |
| P13                       | TXD2      | O, IPU   | 4 mA  | UART Lite TXD                             |
| <b>UART Full *</b>        |           |          |       |   |
| P12                       | RXD       | I, IPD   | 4 mA  | UART RXD.                                 |
| T13                       | RIN       | I, IPD   | 4 mA  | UART RIN.                                 |
| U13                       | CTS_N     | I, IPD   | 4 mA  | UART CTS_N.                               |
| P11                       | DSR_N     | I, IPD   | 4 mA  | UART DSR_N.                               |
| T12                       | DCD_N     | I, IPD   | 4 mA  | UART DCD_N.                               |
| R12                       | TXD       | O, IPD   | 4 mA  | UART TXD.                                 |
| U12                       | DTR_N     | O, IPD   | 4 mA  | UART DTR.                                 |
| R13                       | RTS_N     | O, IPD   | 4 mA  | UART RTS.                                 |
| <b>SPI</b>                |           |          |       |   |
| C8                        | SPI_MISO  | I/O, IPD | 4 mA  | Master input/Slave output                 |
| A8                        | SPI_MOSI  | I/O, IPD | 4 mA  | Master output/Slave input                 |
| B7                        | SPI_WP    | O, IPD   | 4 mA  | GOP function                              |
| B8                        | SPI_HOLD  | O, IPD   | 4 mA  | GOP function                              |
| D8                        | SPI_CLK   | O, IPD   | 4 mA  | SPI clock                                 |
| C7                        | SPI_CS0   | O, IPU   | 4 mA  | SPI chip select0                          |
| C9                        | SPI_CS1   | O, IPU   | 4 mA  | SPI chip select1                          |
| <b>I2C</b>                |           |          |       |   |
| U14                       | I2C_SCLK  | I/O, IPU | 4 mA  | I <sup>2</sup> C Clock                    |
| T14                       | I2C_SD    | O, IPU   | 4 mA  | I <sup>2</sup> C Data                     |
| <b>RGMII/MII (3.3 V)*</b> |           |          |       |   |
| D17                       | GE1_RXCLK | I/O      | 8 mA  | RGMII1 /GMII Rx Clock                     |
| D16                       | GE1_RXDV  | I        | 8 mA  | RGMII1 /GMII Rx Data Valid                |
| E17                       | GE1_RXD0  | I        | 8 mA  | RGMII1 Rx Data bit #0/GMII Rx Data bit #0 |
| E16                       | GE1_RXD1  | I        | 8 mA  | RGMII1 Rx Data bit #1/GMII Rx Data bit #1 |
| F17                       | GE1_RXD2  | I        | 8 mA  | RGMII1 Rx Data bit #2/GMII Rx Data bit #2 |
| F16                       | GE1_RXD3  | I        | 8 mA  | RGMII1 Rx Data bit #3/GMII Rx Data bit #3 |
| G17                       | GE1_TXCLK | I/O      | 8 mA  | RGMII1 /GMII Tx Clock                     |
| G16                       | GE1_TXEN  | O        | 8 mA  | RGMII1 /GMII Tx Data Valid                |
| H17                       | GE1_TXD0  | O        | 8 mA  | RGMII1 Tx Data bit #0/GMII Tx Data bit #0 |
| H16                       | GE1_TXD1  | O        | 8 mA  | RGMII1 Tx Data bit #1/GMII Tx Data bit #1 |
| J17                       | GE1_TXD2  | O        | 8 mA  | RGMII1 Tx Data bit #2/GMII Tx Data bit #2 |
| J16                       | GE1_TXD3  | O        | 8 mA  | RGMII1 Tx Data bit #3/GMII Tx Data bit #3 |
| D14                       | GE2_RXCLK | I/O      | 8 mA  | RGMII2 /GMII Rx Clock                     |
| D15                       | GE2_RXDV  | I        | 8 mA  | RGMII2 /GMII Rx Data Valid                |

| Pin                            | Name                | Type     | Driv. | Description  |
|--------------------------------|---------------------|----------|-------|--|
| F15                            | GE2_RXD0            | I        | 8 mA  | RGMII2 Rx Data bit #0/GMII Rx Data bit #0                        |
| E15                            | GE2_RXD1            | I        | 8 mA  | RGMII2 Rx Data bit #1/GMII Rx Data bit #1                        |
| F14                            | GE2_RXD2            | I        | 8 mA  | RGMII2 Rx Data bit #2/GMII Rx Data bit #2                        |
| E14                            | GE2_RXD3            | I        | 8 mA  | RGMII2 Rx Data bit #3/GMII Rx Data bit #3                        |
| G15                            | GE2_TXCLK           | I/O      | 8 mA  | RGMII2 /GMII Tx Clock  |
| G14                            | GE2_TXEN            | O        | 8 mA  | RGMII2 /GMII Tx Data Valid                                       |
| J15                            | GE2_TXD0            | O        | 8 mA  | RGMII2 Tx Data bit #0/GMII Tx Data bit #0                        |
| J14                            | GE2_TXD1            | O        | 8 mA  | RGMII2 Tx Data bit #1/GMII Tx Data bit #1                        |
| H14                            | GE2_TXD2            | O        | 8 mA  | RGMII2 Tx Data bit #2/GMII Tx Data bit #2                        |
| H15                            | GE2_TXD3            | O        | 8 mA  | RGMII2 Tx Data bit #3/GMII Tx Data bit #3                        |
| <b>PHY Management ( 3.3 V)</b> |                     |          |       |  |
| K14                            | MDC                 | O        | 8 mA  | PHY Management Clock. Shared with GPIO23                         |
| K15                            | MDIO                | I/O      | 8 mA  | PHY Management Data. Shared with GPIO22                          |
| <b>GPIO</b>                    |                     |          |       |  |
| D7                             | GPIO0               | O, IPD   | 8 mA  | GPO0 (output only)   |
| <b>5-Port PHY</b>              |                     |          |       |  |
| H4                             | EPHY_LED0_N_JTDO    | O, IPD   | 4 mA  | 10/100 PHY Port #0 activity LED, JTAG_TDO                        |
| H3                             | EPHY_LED1_N_JTDI    | I/O, IPD | 4 mA  | 10/100 PHY Port #1 activity LED, JTAG_TDI                        |
| H2                             | EPHY_LED2_N_JTMS    | I/O, IPD | 4 mA  | 10/100 PHY Port #2 activity LED, JTAG_TMS                        |
| H1                             | EPHY_LED3_N_JTCLK   | I/O, IPD | 4 mA  | 10/100 PHY Port #3 activity LED, JTAG_CLK                        |
| J4                             | EPHY_LED4_N_JTRST_N | I/O, IPU | 4 mA  | 10/100 PHY Port #4 activity LED, JTAG_TRST_N                     |
| R15                            | EPHY_RES_VBG        | A        |       | Connect to an external resistor to provide accurate bias current |
| T15                            | MDI_RN_P0           | I        |       | 10/100 PHY Port #0 RXN   |
| U15                            | MDI_RP_P0           | I        |       | 10/100 PHY Port #0 RXP   |
| U17                            | MDI_TN_P0           | O        |       | 10/100 PHY Port #0 TXN   |
| U16                            | MDI_TP_P0           | O        |       | 10/100 PHY Port #0 TXP   |
| R17                            | MDI_RN_P1           | I        |       | 10/100 PHY Port #1 RXN   |
| R16                            | MDI_RP_P1           | I        |       | 10/100 PHY Port #1 RXP   |
| T17                            | MDI_TN_P1           | O        |       | 10/100 PHY Port #1 TXN   |
| T16                            | MDI_TP_P1           | O        |       | 10/100 PHY Port #1 TXP   |
| P17                            | MDI_RN_P2           | I        |       | 10/100 PHY Port #2 RXN   |
| P16                            | MDI_RP_P2           | I        |       | 10/100 PHY Port #2 RXP   |
| P15                            | MDI_TN_P2           | O        |       | 10/100 PHY Port #2 TXN   |
| P14                            | MDI_TP_P2           | O        |       | 10/100 PHY Port #2 TXP   |
| M14                            | MDI_RN_P3           | I        |       | 10/100 PHY Port #3 RXN   |
| M15                            | MDI_RP_P3           | I        |       | 10/100 PHY Port #3 RXP   |
| N14                            | MDI_TN_P3           | O        |       | 10/100 PHY Port #3 TXN   |

| Pin                | Name       | Type     | Driv. | Description   |
|--------------------|------------|----------|-------|---|
| N15                | MDI_TP_P3  | O        |       | 10/100 PHY Port #3 TXP  |
| N17                | MDI_RN_P4  | I        |       | 10/100 PHY Port #4 RXN  |
| N16                | MDI_RP_P4  | I        |       | 10/100 PHY Port #4 RXP  |
| M17                | MDI_TN_P4  | O        |       | 10/100 PHY Port #4 TXN  |
| M16                | MDI_TP_P4  | O        |       | 10/100 PHY Port #4 TXP  |
| <b>NAND Flash*</b> |            |          |       |   |
| P8                 | ND_CS_N    | O, IPD   | 4 mA  | NAND Flash Chip Select  |
| R9                 | ND_RE_N    | O, IPD   | 4 mA  | NAND Flash Read Enable  |
| R11                | ND_WE_N    | O, IPD   | 4 mA  | NAND Flash Write Enable   |
| P10                | ND_WP      | O, IPD   | 4 mA  | NAND Flash Write Protect  |
| P9                 | ND_CLE     | O, IPD   | 4 mA  | NAND Flash Command Latch Enable                                       |
| R10                | ND_ALE     | O, IPD   | 4 mA  | NAND Flash ALE Latch Enable   |
| T11                | ND_D0      | I/O, IPD | 4 mA  | NAND Flash Data0  |
| U11                | ND_D1      | I/O, IPD | 4 mA  | NAND Flash Data1  |
| T10                | ND_D2      | I/O, IPD | 4 mA  | NAND Flash Data2  |
| U10                | ND_D3      | I/O, IPD | 4 mA  | NAND Flash Data3  |
| T9                 | ND_D4      | I/O, IPD | 4 mA  | NAND Flash Data4  |
| U9                 | ND_D5      | I/O, IPD | 4 mA  | NAND Flash Data5  |
| T8                 | ND_D6      | I/O, IPD | 4 mA  | NAND Flash Data6  |
| U8                 | ND_D7      | I/O, IPD | 4 mA  | NAND Flash Data7  |
| R8                 | ND_RB_N    | I, IPD   | 4 mA  | NAND Flash Ready/Busy   |
| <b>Misc.</b>       |            |          |       |   |
| C6                 | PORST_N    | I, IPU   | 4 mA  | Power on reset  |
| E5                 | PA_PE_G0   | O, I PD  | 16 mA | 0 V to 3.3 V control for external PA0                                 |
| E6                 | PA_PE_G1   | O, IPD   | 16 mA | 0 V to 3.3 V control for external PA1                                 |
| D5                 | ANT_TRN    | O, IPD   | 8 mA  | Positive signal for antenna T/R switch                                |
| E4                 | ANT_TRNB   | O, IPD   | 8 mA  | Negative signal for antenna T/R switch                                |
| D6                 | WDT_RST_N  | O, IPU   | 4 mA  | Watchdog Reset  |
| <b>USB PHY</b>     |            |          |       |   |
| E13                | UPHY0_V33A | P        |       | 3.3 V USB PHY analog power supply                                     |
| C12                | UPHY0_V12D | P        |       | 1.2 V USB PHY digital power supply                                    |
| C15                | UPHY0_VRES | I/O      |       | Connect to an external 8.2 kΩ resistor for band-gap reference circuit |
| C16                | UPHY0_PADM | I/O      |       | USB Port0 data pin Data-  |
| C17                | UPHY0_PADP | I/O      |       | USB Port0 data pin Data+  |
| <b>DDR2</b>        |            |          |       |   |
| M2                 | MD15       | I/O      | 8 mA  | DDR2 Data bit #15   |
| J1                 | MD14       | I/O      | 8 mA  | DDR2 Data bit #14   |
| L2                 | MD13       | I/O      | 8 mA  | DDR2 Data bit #13   |
| K1                 | MD12       | I/O      | 8 mA  | DDR2 Data bit #12   |
| K2                 | MD11       | I/O      | 8 mA  | DDR2 Data bit #11   |

| Pin | Name   | Type   | Driv. | Description          |
|-----|--------|--------|-------|----------------------|
| L1  | MD10   | I/O    | 8 mA  | DDR2 Data bit #10    |
| J2  | MD9    | I/O    | 8 mA  | DDR2 Data bit #9     |
| M1  | MD8    | I/O    | 8 mA  | DDR2 Data bit #8     |
| U1  | MD7    | I/O    | 8 mA  | DDR2 Data bit #7     |
| T2  | MD6    | I/O    | 8 mA  | DDR2 Data bit #6     |
| R1  | MD5    | I/O    | 8 mA  | DDR2 Data bit #5     |
| T3  | MD4    | I/O    | 8 mA  | DDR2 Data bit #4     |
| U3  | MD3    | I/O    | 8 mA  | DDR2 Data bit #3     |
| R2  | MD2    | I/O    | 8 mA  | DDR2 Data bit #2     |
| U2  | MD1    | I/O    | 8 mA  | DDR2 Data bit #1     |
| T1  | MD0    | I/O    | 8 mA  | DDR2 Data bit #0     |
| N5  | MA13   | O      | 8 mA  | DDR2 Address bit #13 |
| P5  | MA12   | O      | 8 mA  | DDR2 Address bit #12 |
| R3  | MA11   | O      | 8 mA  | DDR2 Address bit #11 |
| U5  | MA10   | O      | 8 mA  | DDR2 Address bit #10 |
| R4  | MA9    | O      | 8 mA  | DDR2 Address bit #9  |
| P4  | MA8    | O      | 8 mA  | DDR2 Address bit #8  |
| P6  | MA7    | O      | 8 mA  | DDR2 Address bit #7  |
| P3  | MA6    | O      | 8 mA  | DDR2 Address bit #6  |
| R5  | MA5    | O      | 8 mA  | DDR2 Address bit #5  |
| N3  | MA4    | O      | 8 mA  | DDR2 Address bit #4  |
| R6  | MA3    | O      | 8 mA  | DDR2 Address bit #3  |
| M4  | MA2    | O      | 8 mA  | DDR2 Address bit #2  |
| T5  | MA1    | O      | 8 mA  | DDR2 Address bit #1  |
| L4  | MA0    | O      | 8 mA  | DDR2 Address bit #0  |
| R7  | MBA2   | O      | 8 mA  | DDR2 MBA #2          |
| T6  | MBA1   | O      | 8 mA  | DDR2 MBA #1          |
| U6  | MBA0   | O      | 8 mA  | DDR2 MBA #0          |
| L3  | MRAS_N | O      | 8 mA  | DDR2 MRAS_N          |
| M3  | MCAS_N | O      | 8 mA  | DDR2 MCAS_N          |
| T7  | MWE_N  | O      | 8 mA  | DDR2 MWE_N           |
| P1  | MCK_P  | O      | 8 mA  | DDR2 MCK_P           |
| P2  | MCK_N  | O      | 8 mA  | DDR2 MCK_N           |
| N2  | MDQM1  | O      | 8 mA  | DDR2 MDM#1           |
| U4  | MDQM0  | O      | 8 mA  | DDR2 MDM#0           |
| K3  | MCS_N  | O      | 8 mA  | DDR2 MCS_N           |
| N1  | MDQS1  | I/O    | 8 mA  | DDR2 MDQS#1          |
| T4  | MDQS0  | I/O    | 8 mA  | DDR2 MDQS#0          |
| U7  | MCKE   | O, IPD | 8 mA  | DDR2 MCKE            |
| J3  | ODT    | O      | 8 mA  | DDR2 ODT             |

**PMU**

| Pin                                   | Name        | Type     | Driv. | Description   |
|---------------------------------------|-------------|----------|-------|---|
| A13                                   | FB          | A        |       | This pin is part of the error amplifier and provides the reference voltage which the sampled output voltage is compared to. A difference between these two voltages indicates an error in the output voltage. |
| C14                                   | COMP        | A        |       | This pin provides the error amplifier output which compensates for errors in the output voltage identified using the FB pin.  |
| A15                                   | UGATE       | A        |       | Gate drive for external upper MOSFET (Ipeak<200 mA; Iavg<20 mA)   |
| B14                                   | LGATE       | A        |       | Gate drive for external lower MOSFET (Ipeak<200 mA; Iavg<20 mA)   |
| A14                                   | DCDC_V33D   | P        |       | 3.3 V power supply only for gate driver of SW (Ipeak<200 mA; Iavg<20 mA)  |
| B16                                   | DCDC_V33A   | P        |       | 3.3 V analog power (Ipeak<200 mA; Iavg<10 mA)   |
| B17                                   | EXT_LDO_DIG | A        |       | Connect to Base terminal of external BJT (Iavg<20 mA)   |
| A17                                   | VFB_DIG     | A        |       | 1.2 V output feedback   |
| B15                                   | NC          | A        |       | NC  |
| A16                                   | VFB_DDR     | A        |       | DDR output feedback   |
| <b>PCIe*</b>                          |             |          |       |   |
| D10                                   | PERST_N     | I/O, IPU | 4 mA  | PCIe reset.   |
| A10                                   | PCIE_TXN    | A        |       | PCIe0 differential transmit TX -  |
| B10                                   | PCIE_TXP    | A        |       | PCIe0 differential transmit TX+   |
| B9                                    | PCIE_RXN    | A        |       | PCIe0 differential receive RX -   |
| A9                                    | PCIE_RXP    | A        |       | PCIe0 differential receive RX +   |
| C10                                   | PCIE_REXT   | A        |       | PCIe0 Reference resistor connection (12K Ohm +/- 1 %)   |
| <b>PCIe Reference Clock Generator</b> |             |          |       |   |
| A11                                   | APCK_RFCKOP | A        |       | External reference clock output (positive)  |
| B11                                   | APCK_RFCKON | A        |       | External reference clock output (negative)  |
| E10                                   | PCIE_V33A   | P        |       | PCIe 3.3 V analog power   |
| C11                                   | PCIE_RFCKP  | A        |       | Device reference clock input (positive)   |
| D11                                   | PCIE_RFCKN  | A        |       | Device reference clock input (negative)   |
| <b>PLL</b>                            |             |          |       |   |
| E9, D12                               | APCK_V12A   | P        |       | 1.2 V analog power supply for CPLL/PPLL   |
| A7                                    | BBPLL_V12A  | P        |       | 1.2 V analog power supply to BB PLL   |
| B6                                    |             |          |       | NC  |
| <b>Power</b>                          |             |          |       |   |
| D9, G5, M10, N10                      | SOC_IO_V33D | P        |       | 3.3 V digital I/O power supply  |
| E7, E8, L13, M9, N9, K13              | SOC_CO_V12D | P        |       | 1.2 V digital core power supply   |



| Pin  | Name                    | Type | Driv. | Description  |
|--|-------------------------|------|-------|--|
| L5   | DDR_IO_VREF             | P    |       | 0.9 V/1.25 V/GND reference voltage power supply for DDR2/DDR1/SDR    |
| H5, N6, J5, K5, P7                                       | DDR_IO_V18D/DDR_IO_V25D | P    |       | 1.8 V/2.5 V/3.3 V level shifter power supply for DDR2/DDR1/SDR       |
| M5, N4   | DDR_IOC_V12D            | P    |       | 1.2 V I/O core power supply for DDR and SDR                          |
| N12, N13   | EPHY_V33A               | P    |       | 3.3 V power supply for EPHY  |
| L14, L15   | EPHY_V12A               | P    |       | 1.2 V power supply for EPHY  |
| F13, G13   | GE_IO_V33D              | P    |       | 3.3 V power supply for RGMII   |
| M13  | EPHY_PLL_V12A           | P    |       | 1.2 V power supply for EPHY PLL                                      |
| <b>RF</b>  |                         |      |       |  |
| A1   | RF0_OUTP                | I/O  |       | 2.4 GHz TX0 PA output (positive)<br>2.4 GHz RX0 LNA input (positive) |
| B2   | RF0_OUTN                | I/O  |       | 2.4 GHz TX0 PA output (negative)<br>2.4 GHz RX0 LNA input (negative) |
| B1   | RF0_PA1_V33A            | P    |       | 3.3 V Supply for RF channel0   |
| A2   | RF0_PA2_V33N            | P    |       | 3.3 V Supply for RF channel0   |
| A3   | RF0_IN                  | I    |       | 2.4 GHz RX0 input (aux LNA0 input)                                   |
| B3   | RF0_VX_LDO              | P    |       | 1.2 V to 3.3 V supply for RF0  |
| D1   | RF1_OUTP                | I/O  |       | 2.4 GHz TX1 PA output (positive)<br>2.4 GHz RX1 LNA input (positive) |
| E1   | RF1_OUTN                | I/O  |       | 2.4 GHz TX1 PA output (negative)<br>2.4 GHz RX1 LNA input (negative) |
| E3   | RF1_PA1_V33A            | P    |       | 3.3 V Supply for RF channel1   |
| E2   | RF1_PA2_V33N            | P    |       | 3.3 V Supply for RF channel1   |
| C1   | RF1_IN                  | I    |       | 2.4 GHz RX1 input (aux LNA1 input)                                   |
| D3   | RF1_VX_LDO              | P    |       | 1.2 V to 3.3 V supply for RF1  |
| D4   | BG_V33A                 | P    |       | 3.3 V supply for band gap reference                                  |
| A4   | BG_EXTR                 | I/O  |       | External reference resistor (24 kΩ)                                  |
| B4   | PLL_VC_CAP              | I/O  |       | PLL external loop filter   |
| C4   | GND                     | G    |       | Ground ball  |
| C5   | ADC_VX_LDO              | P    |       | 1.3 V to 3.3 V Supply for ADC  |
| A5   | XTAL_XI                 | I    |       | Crystal oscillator input   |
| A6   | XTAL_XO                 | O    |       | Crystal oscillator output  |
| B5   | XTAL_V12A               | O    |       | Crystal LDO output   |
| A1, B2, D1, E1 will be output only when external PA/LNA. |                         |      |       |  |
| <b>Ground</b>  |                         |      |       |  |



| Pin   | Name | Type | Driv. | Description |
|---|------|------|-------|-------------|
| C2, D2, F2, K4,<br>F6 to F12,<br>G6 to G12,<br>H6 to H12,<br>J6 to J12,<br>K6 to K12,<br>L6 to L12,<br>M6 to M8,<br>M11, M12, N11 | GND  | G    |       | Ground ball |

**Total: 265 balls**

NOTE:

1. Pin types marked with an \* indicate that they are available only in the TFBGA package.
2. Ball mapping for these pins is shown in the DDR2 Ball Map table in section 2.3.1. For information on DDR1 ball mapping, see section 2.3.2.
3. Ball mapping for these pins is shown in the DDR2 Ball Map table in section 2.3.1. For information on DDR1 ball mapping, see section 2.3.2.

#### 2.4 Pin Descriptions (DRQFN)

| Pins              | Name             | Type     | Driv. | Description                               |
|-------------------|------------------|----------|-------|---|
| <b>WLAN LED</b>   |                  |          |       |   |
| 81                | WLED_N           | O, IPU   | 4 mA  | WLAN Activity LED                         |
| <b>UART Lite</b>  |                  |          |       |   |
| 37                | RXD2             | I, IPU   | 4 mA  | UART Lite RXD                             |
| 113               | TXD2             | O, IPU   | 4 mA  | UART Lite TXD                             |
| <b>SPI</b>        |                  |          |       |   |
| 137               | SPI_MISO         | I/O, IPD | 4 mA  | Master input/Slave output                 |
| 63                | SPI_MOSI         | I/O, IPD | 4 mA  | Master output/Slave input                 |
| 65                | SPI_WP           | O, IPD   | 4 mA  | GPO function                              |
| 138               | SPI_HOLD         | O, IPD   | 4 mA  | GPO function                              |
| 136               | SPI_CLK          | O, IPD   | 4 mA  | SPI clock                                 |
| 64                | SPI_CS0          | O, IPU   | 4 mA  | SPI chip select0                          |
| 62                | SPI_CS1          | O, IPU   | 4 mA  | SPI chip select1                          |
| <b>I2C</b>        |                  |          |       |   |
| 111               | I2C_SCLK         | I/O, IPU | 4 mA  | I2C Clock                                 |
| 36                | I2C_SD           | O, IPU   | 4 mA  | I2C Data                                  |
| <b>GPIO</b>       |                  |          |       |   |
| 139               | GPIO0            | O, IPD   | 8 mA  | GPO0 (output only)                        |
| <b>5-Port PHY</b> |                  |          |       |   |
| 82                | EPHY_LED0_N_JTDO | O, IPD   | 4 mA  | 10/100 PHY Port #0 activity LED, JTAG_TDO |
| 8                 | EPHY_LED1_N_JTDI | I/O, IPD | 4 mA  | 10/100 PHY Port #1 activity LED, JTAG_TDI |

| Pins           | Name                | Type     | Driv. | Description   |
|----------------|---------------------|----------|-------|---|
| 83             | EPHY_LED2_N_JTMS    | I/O, IPD | 4 mA  | 10/100 PHY Port #2 activity LED, JTAG_TMS                             |
| 7              | EPHY_LED3_N_JTCLK   | I/O, IPD | 4 mA  | 10/100 PHY Port #3 activity LED, JTAG_CLK                             |
| 9              | EPHY_LED4_N_JTRST_N | I/O, IPU | 4 mA  | 10/100 PHY Port #4 activity LED, JTAG_TRST_N                          |
| 43             | EPHY_RES_VBG        | A        |       | Connect to an external resistor to provide accurate bias current      |
| 115            | MDI_RN_P0           | I        |       | 10/100 PHY Port #0 RXN  |
| 38             | MDI_RP_P0           | I        |       | 10/100 PHY Port #0 RXP  |
| 116            | MDI_TN_P0           | O        |       | 10/100 PHY Port #0 TXN  |
| 39             | MDI_TP_P0           | O        |       | 10/100 PHY Port #0 TXP  |
| 42             | MDI_RN_P1           | I        |       | 10/100 PHY Port #1 RXN  |
| 118            | MDI_RP_P1           | I        |       | 10/100 PHY Port #1 RXP  |
| 41             | MDI_TN_P1           | O        |       | 10/100 PHY Port #1 TXN  |
| 40             | MDI_TP_P1           | O        |       | 10/100 PHY Port #1 TXP  |
| 121            | MDI_RN_P2           | I        |       | 10/100 PHY Port #2 RXN  |
| 44             | MDI_RP_P2           | I        |       | 10/100 PHY Port #2 RXP  |
| 46             | MDI_TN_P2           | O        |       | 10/100 PHY Port #2 TXN  |
| 45             | MDI_TP_P2           | O        |       | 10/100 PHY Port #2 TXP  |
| 125            | MDI_RN_P3           | I        |       | 10/100 PHY Port #3 RXN  |
| 48             | MDI_RP_P3           | I        |       | 10/100 PHY Port #3 RXP  |
| 124            | MDI_TN_P3           | O        |       | 10/100 PHY Port #3 TXN  |
| 47             | MDI_TP_P3           | O        |       | 10/100 PHY Port #3 TXP  |
| 126            | MDI_RN_P4           | I        |       | 10/100 PHY Port #4 RXN  |
| 49             | MDI_RP_P4           | I        |       | 10/100 PHY Port #4 RXP  |
| 127            | MDI_TN_P4           | O        |       | 10/100 PHY Port #4 TXN  |
| 50             | MDI_TP_P4           | O        |       | 10/100 PHY Port #4 TXP  |
| <b>Misc.</b>   |                     |          |       |   |
| 66             | PORST_N             | I, IPU   | 4 mA  | Power on reset  |
| 141            | PA_PE_G0            | O, IPD   | 16 mA | 0 V to 3.3 V control for external PA0                                 |
| 68             | PA_PE_G1            | O, IPD   | 16 mA | 0 V to 3.3 V control for external PA1                                 |
| 142            | ANT_TRN             | O, IPD   | 8 mA  | Positive signal for antenna T/R switch                                |
| 69             | ANT_TRNB            | O, IPD   | 8 mA  | Negative signal for antenna T/R switch                                |
| 67             | WDT_RST_N           | O, IPU   | 4 mA  | Watchdog Reset  |
| <b>USB PHY</b> |                     |          |       |   |
| 129            | UPHY0_V33A          | P        |       | 3.3 V USB PHY analog power supply                                     |
| 128            | UPHY0_V12D          | P        |       | 1.2 V USB PHY digital power supply                                    |
| 130            | UPHY0_VRES          | I/O      |       | Connect to an external 8.2 kΩ resistor for band-gap reference circuit |

| Pins            | Name       | Type | Driv. | Description               |
|-----------------|------------|------|-------|---------------------------|
| 53              | UPHY0_PADM | I/O  |       | USB Port0 data pin Data-  |
| 52              | UPHY0_PADP | I/O  |       | USB Port0 data pin Data+  |
| <b>DDR1/SDR</b> |            |      |       |                           |
| 85              | MD15       | I/O  | 8 mA  | SDRAM/DDR Data bit #15    |
| 11              | MD14       | I/O  | 8 mA  | SDRAM/DDR Data bit #14    |
| 86              | MD13       | I/O  | 8 mA  | SDRAM/DDR Data bit #13    |
| 12              | MD12       | I/O  | 8 mA  | SDRAM/DDR Data bit #12    |
| 87              | MD11       | I/O  | 8 mA  | SDRAM/DDR Data bit #11    |
| 13              | MD10       | I/O  | 8 mA  | SDRAM/DDR Data bit #10    |
| 88              | MD9        | I/O  | 8 mA  | SDRAM/DDR Data bit #9     |
| 14              | MD8        | I/O  | 8 mA  | SDRAM/DDR Data bit #8     |
| 27              | MD7        | I/O  | 8 mA  | SDRAM/DDR Data bit #7     |
| 102             | MD6        | I/O  | 8 mA  | SDRAM/DDR Data bit #6     |
| 26              | MD5        | I/O  | 8 mA  | SDRAM/DDR Data bit #5     |
| 101             | MD4        | I/O  | 8 mA  | SDRAM/DDR Data bit #4     |
| 100             | MD3        | I/O  | 8 mA  | SDRAM/DDR Data bit #3     |
| 24              | MD2        | I/O  | 8 mA  | SDRAM/DDR Data bit #2     |
| 99              | MD1        | I/O  | 8 mA  | SDRAM/DDR Data bit #1     |
| 23              | MD0        | I/O  | 8 mA  | SDRAM/DDR Data bit #0     |
| 97              | MA12       | O    | 8 mA  | SDRAM/DDR Address bit #12 |
| 21              | MA11       | O    | 8 mA  | SDRAM/DDR Address bit #11 |
| 31              | MA10       | O    | 8 mA  | SDRAM/DDR Address bit #10 |
| 96              | MA9        | O    | 8 mA  | SDRAM/DDR Address bit #9  |
| 20              | MA8        | O    | 8 mA  | SDRAM/DDR Address bit #8  |
| 19              | MA7        | O    | 8 mA  | SDRAM/DDR Address bit #7  |
| 94              | MA6        | O    | 8 mA  | SDRAM/DDR Address bit #6  |
| 92              | MA5        | O    | 8 mA  | SDRAM/DDR Address bit #5  |
| 17              | MA4        | O    | 8 mA  | SDRAM/DDR Address bit #4  |
| 104             | MA3        | O    | 8 mA  | SDRAM/DDR Address bit #3  |
| 105             | MA2        | O    | 8 mA  | SDRAM/DDR Address bit #2  |
| 30              | MA1        | O    | 8 mA  | SDRAM/DDR Address bit #1  |
| 106             | MA0        | O    | 8 mA  | SDRAM/DDR Address bit #0  |
| 107             | MBA1       | O    | 8 mA  | SDRAM/DDR MBA #1          |
| 32              | MBA0       | O    | 8 mA  | SDRAM/DDR MBA #0          |
| 33              | MRAS_N     | O    | 8 mA  | SDRAM/DDR MRAS_N          |
| 109             | MCAS_N     | O    | 8 mA  | SDRAM/DDR MCAS_N          |
| 34              | MWE_N      | O    | 8 mA  | SDRAM/DDR MWE_N           |
| 16              | MCK_P      | O    | 8 mA  | SDRAM MCK/DDR MCK_P       |
| 90              | MCK_N      | O    | 8 mA  | DDR MCK_N                 |

| Pins            | Name         | Type   | Driv. | Description   |
|-----------------|--------------|--------|-------|---|
| 15              | MDQM1        | O      | 8 mA  | SDRAM MDQM#1/DDR MDM#1  |
| 28              | MDQM0        | O      | 8 mA  | SDRAM MDQM#0/DDR MDM#0  |
| 108             | MCS_N        | O      | 8 mA  | SDRAM/DDR MCS_N   |
| 89              | MDQS1        | I/O    | 8 mA  | DDR MDQS#1  |
| 103             | MDQS0        | I/O    | 8 mA  | DDR MDQS#0  |
| 22              | MCKE         | O, IPD | 8 mA  | DDR MCKE  |
| 98              | ODT          | O      | 8 mA  | DDR2 ODT  |
| <b>PMU</b>      |              |        |       |   |
| 58              | FB           | A      |       | This pin is part of the error amplifier and provides the reference voltage which the sampled output voltage is compared to. A difference between these two voltages indicates an error in the output voltage. |
| 132             | COMP         | A      |       | This pin provides the error amplifier output which compensates for errors in the output voltage identified using the FB pin.  |
| 59              | UGATE        | A      |       | Gate drive for external upper MOSFET (Ipeak<200 mA; Iavg<20 mA)   |
| 133             | LGATE        | A      |       | Gate drive for external lower MOSFET (Ipeak<200mA; Iavg<20mA)   |
| 60              | DCDC_V33D    | P      |       | 3.3 V power supply only for gate driver of SW (Ipeak<200 mA; Iavg<20 mA)  |
| 56              | DCDC_V33A    | P      |       | 3.3 V analog power (Ipeak<200 mA; Iavg<10 mA)   |
| 54              | EXT_LDO_DIG  | A      |       | Connects to the base terminal of external BJT (Iavg<20 mA)  |
| 55              | VFB_DIG      | A      |       | 1.2 V output feedback   |
| 131             | NC           | A      |       | NC  |
| 57              | VFB_DDR      | A      |       | DDR output feedback   |
| <b>PLL</b>      |              |        |       |   |
| 61              | APCK_V33A    | P      |       | 3.3 V analog power supply for CPLL/PPLL   |
| 135             | APCK_V12A    | P      |       | 1.2 V analog power supply for CPLL/PPLL   |
| 143             | BBPLL_V12A   | P      |       | 1.2 V analog power supply to BB PLL   |
| 70              |              |        |       | NC  |
| <b>Power</b>    |              |        |       |   |
| 134, 6, 112     | SOC_IO_V33D  | P      |       | 3.3 V digital I/O power supply  |
| 84, 35, 140, 51 | SOC_CO_V12D  | P      |       | 1.2 V digital core power supply   |
| 91, 110         | DDR_VREF     | P      |       | 0.9 V/1.25 V/GND reference voltage power supply for DDR2/DDR1/SDR   |
| 10, 93, 95, 29  | VDD18/ VDD25 | P      |       | 1.8 V/2.5 V/3.3 V level shifter power supply for DDR2/DDR1/SDR  |

| Pins                   | Name         | Type | Driv. | Description  |
|------------------------|--------------|------|-------|--|
| 18, 25                 | DDR_IOC_V12D | P    |       | 1.2 V I/O core power supply for DDR and SDR                          |
| 122, 119, 117          | EPHY_V33A    | P    |       | 3.3 V power supply for EPHY  |
| 123, 114               | EPHY_V12A    | P    |       | 1.2 V power supply for EPHY  |
| <b>RF</b>              |              |      |       |  |
| 75                     | RF0_OUTP     | I/O  |       | 2.4 GHz TX0 PA output (positive)<br>2.4 GHz RX0 LNA input (positive) |
| 76                     | RF0_OUTN     | I/O  |       | 2.4 GHz TX0 PA output (negative)<br>2.4 GHz RX0 LNA input (negative) |
| 2                      | RF0_PA1_V33A | P    |       | 3.3 V Supply for RF channel0   |
| 1                      | RF0_PA2_V33N | P    |       | 3.3 V Supply for RF channel0   |
| 148                    | RF0_VX_LDO   | P    |       | 1.2 V to 3.3 V Supply for RF0  |
| 4                      | RF1_OUTP     | I/O  |       | 2.4 GHz TX1 PA output (positive)<br>2.4 GHz RX1 LNA input (positive) |
| 5                      | RF1_OUTN     | I/O  |       | 2.4 GHz TX1 PA output (negative)<br>2.4 GHz RX1 LNA input (negative) |
| 80                     | RF1_PA1_V33A | P    |       | 3.3 V Supply for RF channel1   |
| 79                     | RF1_PA2_V33N | P    |       | 3.3 V Supply for RF channel1   |
| 3                      | RF1_VX_LDO   | P    |       | 1.2 V to 3.3 V Supply for RF1  |
| 147                    | BG_V33A      | P    |       | 3.3 V supply for band gap reference                                  |
| 74                     | BG_EXTR      | I/O  |       | External reference resistor (24 kΩ)                                  |
| 73                     | PLL_VC_CAP   | I/O  |       | PLL external loop filter   |
| 146                    | PLL_VX_LDO   | P    |       | 3.3 V Supply for PLL (Xtal)  |
| 144                    | ADC_VX_LDO   | P    |       | 1.3 V to 3.3 V Supply for ADC  |
| 145                    | XTAL_XI      | I    |       | Crystal oscillator input   |
| 71                     | XTAL_XO      | O    |       | Crystal oscillator output  |
| 72                     | XTAL_V12A    | O    |       | Crystal LDO output   |
| 77, 78                 | NC           |      |       | NC   |
| <b>Ground</b>          |              |      |       |  |
| EPAD                   | GND          | G    |       | Ground pin   |
| <b>Total: 148 pins</b> |              |      |       |  |

**NOTE:**

IPD : Internal pull-down  
 IPU : Internal pull-up  
 I : Input  
 O : Output  
 IO : Bi-directional  
 P : Power

G : Ground  
NC : Not connected

## 2.5 Pin Sharing Schemes

Some pins are shared with GPIO to provide maximum flexibility for system designers. The MT7620 provides up to 73 GPIO pins. Users can configure SYSCFG and GPIOMODE registers in the System Control block to specify the pin function, or they can use the registers specified below. For more information, see the Programmer's Guide. Unless specified explicitly, all the GPIO pins are in input mode after reset.

### 2.5.1 GPIO pin share scheme

| I/O Pad Group   | Normal Mode         | GPIO Mode |
|-----------------|---------------------|-----------|
| WLED_N          | WLAN_LED_N          | GPO#72    |
| RGMII2          | GE2_RXCLK           | GPIO#71   |
|                 | GE2_RXDV            | GPIO#70   |
|                 | GE2_RXD3            | GPIO#69   |
|                 | GE2_RXD2            | GPIO#68   |
|                 | GE2_RXD1            | GPIO#67   |
|                 | GE2_RXD0            | GPIO#66   |
|                 | GE2_TXCLK           | GPIO#65   |
|                 | GE2_TXEN            | GPIO#64   |
|                 | GE2_TXD3            | GPIO#63   |
|                 | GE2_TXD2            | GPIO#62   |
|                 | GE2_TXD1            | GPIO#61   |
|                 | GE2_TXD0            | GPIO#60   |
| NAND            | ND_D7               | GPIO#59   |
|                 | ND_D6               | GPIO#58   |
|                 | ND_D5               | GPIO#57   |
|                 | ND_D4               | GPIO#56   |
|                 | ND_D3               | GPIO#55   |
|                 | ND_D2               | GPIO#54   |
|                 | ND_D1               | GPIO#53   |
|                 | ND_D0               | GPIO#52   |
|                 | ND_ALE              | GPIO#51   |
|                 | ND_CLE              | GPIO#50   |
|                 | ND_RB_N             | GPIO#49   |
|                 | ND_WP               | GPIO#48   |
|                 | ND_RE_N             | GPIO#47   |
|                 | ND_WE_N             | GPIO#46   |
| SW_PHY_LED/JTAG | ND_CS_N             | GPIO#45   |
|                 | EPHY_LED4_N_JTRST_N | GPIO#44   |
|                 | EPHY_LED3_N_JTCLK   | GPIO#43   |
|                 | EPHY_LED2_N_JTMS    | GPIO#42   |
|                 | EPHY_LED1_N_JTDI    | GPIO#41   |

| I/O Pad Group | Normal Mode      | GPIO Mode |
|---------------|------------------|-----------|
|               | EPHY_LED0_N_JTDO | GPIO#40   |
| SPI           | SPI_WP           | GPO#39    |
|               | SPI_HOLD         | GPO#38    |
|               | SPI_CS1          | GPIO#37   |
| PERST_N       | PERST_N          | GPIO#36   |
| RGMII1        | GE1_RXCLK        | GPIO#35   |
|               | GE1_RXDV         | GPIO#34   |
|               | GE1_RXD3         | GPIO#33   |
|               | GE1_RXD2         | GPIO#32   |
|               | GE1_RXD1         | GPIO#31   |
|               | GE1_RXD0         | GPIO#30   |
|               | GE1_TXCLK        | GPIO#29   |
|               | GE1_TXEN         | GPIO#28   |
|               | GE1_TXD3         | GPIO#27   |
|               | GE1_TXD2         | GPIO#26   |
|               | GE1_TXD1         | GPIO#25   |
|               | GE1_TXD0         | GPIO#24   |
|               | MDC              | GPIO#23   |
|               | MDIO             | GPIO#22   |
|               | PA_PE_G1         | GPIO#21   |
| PA_PE         | PA_PE_G0         | GPIO#20   |
|               | ANT_TRN          | GPO#19    |
|               | ANT_TRNB         | GPO#18    |
| WDT_RST       | WDT_RST_N        | GPIO#17   |
| UARTL         | RXD2             | GPIO#16   |
|               | TXD2             | GPO#15    |
| UARTF         | RIN              | GPIO#14   |
|               | DSR_N            | GPIO#13   |
|               | DCD_N            | GPIO#12   |
|               | DTR_N            | GPIO#11   |
|               | RXD              | GPIO#10   |
|               | CTS_N            | GPIO#9    |
|               | TXD              | GPIO#8    |
|               | RTS_N            | GPIO#7    |
|               | SPI_MISO         | GPIO#6    |
|               | SPI_MOSI         | GPO#5     |
| SPI           | SPI_CLK          | GPO#4     |
|               | SPI_CS0          | GPIO#3    |
|               | I2C_SCLK         | GPIO#2    |
| I2C/SUTIF     |                  |           |



| I/O Pad Group | Normal Mode | GPIO Mode |
|---------------|-------------|-----------|
|               | I2C_SD      | GPIO#1    |
| GPIO          | GPO0        | GPO#0     |

### 2.5.2 UARTF pin share scheme

Controlled by the UARTF\_SHARE\_MODE register.

| Pin Name | 3'b000<br>UARTF | 3'b001<br>PCM,<br>UARTF | 3'b010<br>PCM,<br>I2S | 3'b011<br>I2S<br>UARTF | 3'b100<br>PCM,<br>GPIO | 3'b101<br>GPIO,<br>UARTF | 3'b110<br>GPIO<br>I2S | 3'b111<br>GPIO |
|----------|-----------------|-------------------------|-----------------------|------------------------|------------------------|--------------------------|-----------------------|----------------|
| RIN      | RIN             | PCMDTX                  | PCMDTX                | RXD                    | PCMDTX                 | GPIO#14                  | GPIO#14               | GPIO#14        |
| DSR_N    | DSR_N           | PCMDRX                  | PCMDRX                | CTS_N                  | PCMDRX                 | GPIO#13                  | GPIO#13               | GPIO#13        |
| DCD_N    | DCD_N           | PCMCLK                  | PCMCLK                | TXD                    | PCMCLK                 | GPIO#12                  | GPIO#12               | GPIO#12        |
| DTR_N    | DTR_N           | PCMFS                   | PCMFS                 | RTS_N                  | PCMFS                  | GPIO#11                  | GPIO#11               | GPIO#11        |
| RXD      | RXD             | RXD                     | I2SSDI                | I2SSDI                 | GPIO#10                | RXD                      | I2SSDI                | GPIO#10        |
| CTS_N    | CTS_N           | CTS_N                   | I2SSDO                | I2SSDO                 | GPIO#9                 | CTS_N                    | I2SSDO                | GPIO#9         |
| TXD      | TXD             | TXD                     | I2SWS                 | I2SWS                  | GPIO#8                 | TXD                      | I2SWS                 | GPIO#8         |
| RTS_N    | RTS_N           | RTS_N                   | I2SCLK                | I2SCLK                 | GPIO#7                 | RTS_N                    | I2SCLK                | GPIO#7         |

NOTE: This scheme applies only to the TFBGA package.

### 2.5.3 RGMII pin share schemes

Controlled by the RGMII1\_GPIO\_MODE register.

| Pin Name       | 1'b0 RGMII1    | 1'b1 GPIO     |
|----------------|----------------|---------------|
| GE1_RXCLK      | GE1_RXCLK      | GPIO#35       |
| GE1_RXDV       | GE1_RXDV       | GPIO#34       |
| GE1_RXD 0 to 3 | GE1_RXD 0 to 3 | GPIO#33 to 30 |
| GE1_TXCLK      | GE1_TXCLK      | GPIO#29       |
| GE1_TXDV       | GE1_TXDV       | GPIO#28       |
| GE1_TXD0 to 3  | GE1_TXD0 to 3  | GPIO#27 to 24 |

NOTE: This scheme applies only to the TFBGA package.

Controlled by the RGMII2\_GPIO\_MODE register.

| Pin Name      | 1'b0 RGMII2   | 1'b1 GPIO     |
|---------------|---------------|---------------|
| GE2_RXCLK     | GE2_RXCLK     | GPIO#71       |
| GE2_RXDV      | GE2_RXDV      | GPIO#70       |
| GE2_RXD0 to 3 | GE2_RXD0 to 3 | GPIO#69 to 66 |
| GE2_TXCLK     | GE2_TXCLK     | GPIO#65       |
| GE2_TXDV      | GE2_TXDV      | GPIO#64       |
| GE2_TXD0 to 3 | GE2_TXD0 to 3 | GPIO#63 to 60 |

NOTE: This scheme applies only to the TFBGA package.

### 2.5.4 WDT\_RST\_MODE pin share scheme

Controlled by the WDT\_RST\_MODE register.

| Pin Name  | 2'b00     | 2'b01       | 2'b1x   |
|-----------|-----------|-------------|---------|
| WDT_RST_N | WDT_RST_N | REFCLK0_OUT | GPIO#17 |

### 2.5.5 PERST\_N pin share scheme

Controlled by the PERST\_GPIO\_MODE register.

| Pin Name | 2'b00   | 2'b01       | 2'b1x   |
|----------|---------|-------------|---------|
| PERST_N  | PERST_N | REFCLK0_OUT | GPIO#36 |

NOTE: This scheme applies only to the TFBGA package.

### 2.5.6 MDC/MDIO pin share scheme:

Controlled by the MDIO\_GPIO\_MODE register.

| Pin Name | 2'b00 | 2'b01       | 2'b1x    |
|----------|-------|-------------|----------|
| MDC      | MDC   | REFCLK0_OUT | GPIO #23 |
| MDIO     | MDIO  | REFCLK1_OUT | GPIO #24 |

### 2.5.7 EPHY\_LED pin share scheme

Controlled by the EPHY\_BT\_GPIO\_MODE register.

| Pin Name            | EPHY_LED_GPIO_MODE =1'b0         |                              | EPHY_LED_GPIO_MODE=1'b1 |
|---------------------|----------------------------------|------------------------------|-------------------------|
|                     | EPHY_LED BS<br>(dbg_jtag_mode=0) | JTAG BS<br>(dbg_jtag_mode=1) |                         |
| EPHY_LED4_N_JTRST_N | EPHY_LED4_N                      | JTAG_RST_N                   | GPIO#44                 |
| EPHY_LED3_N_JTCLK   | EPHY_LED3_N                      | JTAG_CLK                     | GPIO#43                 |
| EPHY_LED2_N_JTMS    | EPHY_LED2_N                      | JTAG_TMS                     | GPIO#42                 |
| EPHY_LED1_N_JTDI    | EPHY_LED1_N                      | JTAG_TDI                     | GPIO#41                 |
| EPHY_LED0_N_JTDO    | EPHY_LED0_N                      | JTAG_TDO                     | GPIO#40                 |

### 2.5.8 SPI pin share scheme

Controlled by SPI\_GPIO\_MODE & SPI\_REFCLK\_MODE registers.

| Pin Name | SPI_GPIO_MODE=0   |                   | SPI_GPIO_MODE=1 |
|----------|-------------------|-------------------|-----------------|
|          | SPI_REFCLK_MODE=0 | SPI_REFCLK_MODE=1 |                 |
| SPI_WP   | GPO#39            | GPO#39            | GPO#39          |
| SPI_HOLD | GPO#38            | GPO#38            | GPO#38          |
| SPI_CS1  | SPI_CS1           | REFCLK0_OUT       | GPIO#37         |
| SPI_MISO | SPI_MISO          | SPI_MISO          | GPIO#6          |
| SPI_MOSI | SPI_MOSI          | SPI_MOSI          | GPO#5           |
| SPI_CLK  | SPI_CLK           | SPI_CLK           | GPO#4           |
| SPI_CS0  | SPI_CS0           | SPI_CS0           | GPIO#3          |

### 2.5.9 ND/SD pin share scheme

Controlled by the ND\_SD\_GPIO\_MODE register.

| Pin Name | 2'b00 NAND | 2'b01 SD + BT + GPIO | 2'b1x GPIO*15 |
|----------|------------|----------------------|---------------|
| ND_D7    | ND_D7      | BT_ANT               | GPIO#59       |
| ND_D6    | ND_D6      | BT_WACT              | GPIO#58       |
| ND_D5    | ND_D5      | BT_AUX               | GPIO#57       |
| ND_D4    | ND_D4      | BT_STAT              | GPIO#56       |
| ND_D3    | ND_D3      | SD_D3                | GPIO#55       |
| ND_D2    | ND_D2      | SD_D2                | GPIO#54       |
| ND_D1    | ND_D1      | SD_D1                | GPIO#53       |
| ND_D0    | ND_D0      | SD_D0                | GPIO#52       |
| ND_ALE   | ND_ALE     | SD_CMD               | GPIO#51       |
| ND_CLE   | ND_CLE     | SD_CARD_DETECT       | GPIO#50       |
| ND_RB_N  | ND_RB_N    | SD_CLK               | GPIO#49       |
| ND_WP    | ND_WP      | SD_WP                | GPIO#48       |
| ND_RE_N  | ND_RE_N    | BT_ACT               | GPIO#47       |
| ND_WE_N  | ND_WE_N    | NA                   | GPIO#46       |
| ND_CS_N  | ND_CS_N    | NA                   | GPIO#45       |

NOTE :

1. All given GPIO are 4 mA drive capable.

#### 2.5.9.1 Pin share function description

| Pin Share Name | I/O | Pin Share Function description   |
|----------------|-----|--|
| PCMDTX         | O   | PCM Data Transmit<br>DATA signal sent from the PCM host to the external codec.   |
| PCMDRX         | I   | PCM Data Receive<br>DATA signal sent from the external codec to the PCM host.  |
| PCMCLK         | I/O | PCM Clock<br>The clock signal can be generated by the PCM host (Output direction), or provided by an external clock (input direction). The clock frequency should match the slot configuration of the PCM host.<br>e.g.<br>4 slots, PCM clock out/in should be 256 kHz.<br>8 slots, PCM clock out/in should be 512 kHz.<br>16 slots, PCM clock out/in should be 1.024 MHz.<br>32 slots, PCM clock out/in should be 2.048 MHz.<br>64 slots, PCM clock out/in should be 4.096 MHz.<br>128 slots, PCM clock out/in should be 8.192 MHz. |
| PCMFS          | I/O | PCM SYNC signal.<br>In our design, the direction of this signal is independent of the direction of PCMCLK. Its direction and mode is configurable.   |
| I2SSDI         | I   | I <sup>2</sup> S Data input  |
| I2SSDO         | O   | I <sup>2</sup> S Data output   |
| I2SWS          | I/O | I <sup>2</sup> S Channel Selection (or Word selection)<br>In master mode the pin data direction is set to output, in slave mode it is set to input.  |
| I2SCLK         | I/O | I <sup>2</sup> S clock<br>In master mode the pin data direction is set to output, in slave mode it is set to input.  |
| WDT_RST_N      | I/O | Watchdog timeout reset   |
| ND_D7          | I/O | Nand flash control data bit7   |
| ND_D6          | I/O | Nand flash control data bit6   |
| ND_D5          | I/O | Nand flash control data bit5   |
| ND_D4          | I/O | Nand flash control data bit4   |
| ND_ALE         | I/O | Nand flash Address Latch Enable  |
| ND_CLE         | I/O | Nand flash Command Latch Enable  |

### 2.5.10 xMII PHY/MAC Pin Mapping

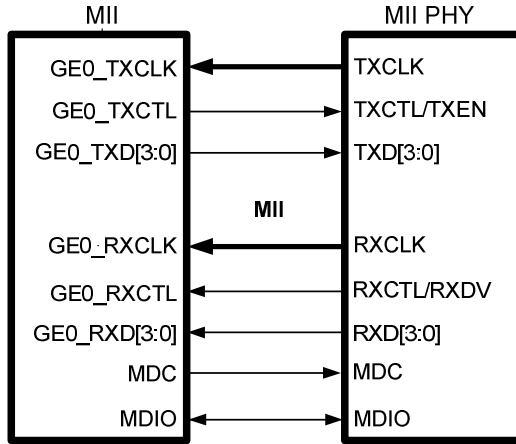


Figure 2-3 MII → MII PHY

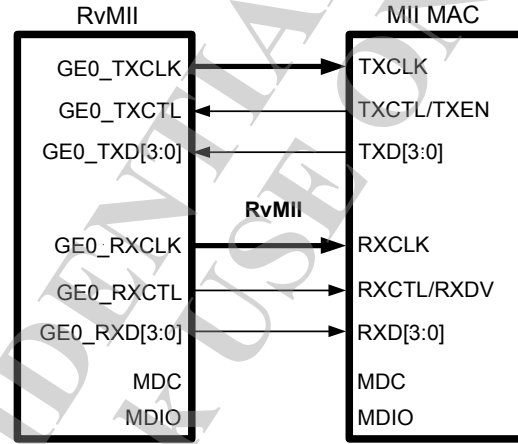


Figure 2-4 RvMII → MII MAC

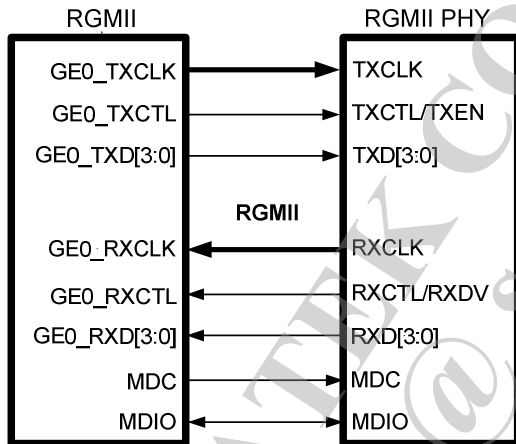


Figure 2-5 RGMII → RGMII PHY

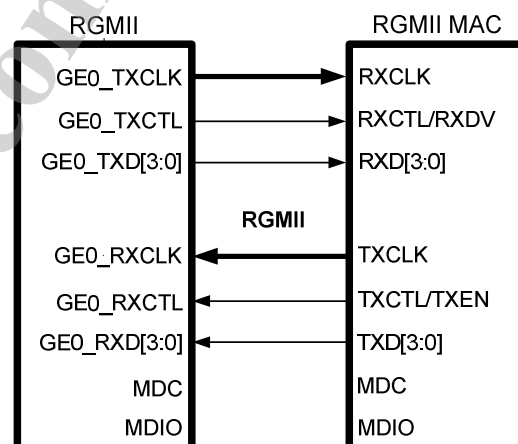


Figure 2-6 RGMII → RGMII MAC

## 2.6 Bootstrapping Pins Description

| Pin Name                                | Boot Strapping Signal Name | Description  |
|---|----------------------------|--|
| WLED_N                                  | DRAM_FROM_EE               | For non-scan mode:<br>(Validate at iNIC mode (chip mode 2 to 9) and NAND flash (chip mode 1 and 12))<br>0: DRAM/PLL configuration from EEPROM<br>1: DRAM configuration from Auto Detect  |
| ANT_TRN                                 | DBG_JTAG_MODE              | 0: EPHY_LED<br>1: JTAG MODE  |
| ANT_TRNB                                | XTAL_FREQ_SEL              | 0: 20 MHz<br>1: 40 MHz   |
| {SPI_WP,<br>SPI_HOLD}                   | DRAM_TYPE                  | 1: DDR1 (CPU/3) TSOP Package<br>2: DDR2 (CPU/3) FBGA Package<br>3: SDRAM (CPU/5) (LVTTL 3.3 V) TSOP Package  |
| {SPI_MOSI<br>SPI_CLK,<br>TXD2<br>GPIO0} | CHIP_MODE[3:0]             | A vector to set chip function/test/debug modes.<br>In non-test/debug operation,<br>1: Normal mode (boot from ROM+NAND flash 4 cycle address/2 KB page size)<br>2: Normal mode (boot from SPI 3-Byte Addr)<br>3: Normal mode (boot from SPI 4-Byte Addr)<br>4: iNIC RGMII (port 5) mode(boot from ROM)<br>5: iNIC MII (port 5) mode(boot from ROM)<br>6: iNIC RVMII (port 5) mode(boot from ROM)<br>7: iNIC PHY (port 0) mode(boot from ROM)<br>8: iNIC USB mode(boot from ROM)<br>9: iNIC PCIe mode(boot from ROM)<br>10: Normal mode (boot from ROM+NAND flash 4 cycle address/512 B page size)<br>11: Normal mode (boot from ROM+NAND flash 5 cycle address/2 KB page size)<br>12: Normal mode (boot from ROM+NAND flash 3 cycle address/512 B page size)<br>13: Debug mode<br>14: Scan mode<br>15: Test mode(CPU will be halted in this mode) |

NOTE: SDR/DDR1/DDR2 DRAM cell used is defined by register.

### 3. Maximum Ratings and Operating Conditions

#### 3.3 Absolute Maximum Ratings

|                               |                          |
|-------------------------------|--------------------------|
| I/O Supply Voltage            | 3.6 V                    |
| Input, Output, or I/O Voltage | GND -0.3 V to Vcc +0.3 V |

Table 3-1 Absolute Maximum Ratings

#### 3.4 Maximum Temperatures

|  |        |
|--|--------|
| Maximum Junction Temperature (Plastic Package) | 125 °C |
| Maximum Lead Temperature (Soldering 10 s)      | 260 °C |

Table 3-2 Maximum Temperatures

#### 3.5 Operating Conditions

|                           |               |
|---------------------------|---------------|
| Core Supply Voltage       | 1.27 V +/- 5% |
| Ambient Temperature Range | -20 to 55 °C  |
| I/O Supply Voltage        | 3.3 V +/- 10% |

Table 3-3 Operating Conditions

#### 3.6 Thermal Characteristics

Thermal characteristics without an external heat sink in still air conditions.

MT7620N:

|  |            |
|--|------------|
| Thermal Resistance $\theta_{JA}$ (°C /W) for JEDEC 2L system PCB | 20.14 °C/W |
| Thermal Resistance $\theta_{JA}$ (°C /W) for JEDEC 4L system PCB | 17.19 °C/W |
| Thermal Resistance $\theta_{JC}$ (°C /W) for JEDEC 2L system PCB | 7.29 °C/W  |
| Thermal Resistance $\theta_{JC}$ (°C /W) for JEDEC 4L system PCB | 6.14 °C/W  |
| Thermal Resistance $\psi_{Jt}$ (°C /W) for JEDEC 2L system PCB   | 2.02 °C/W  |
| Thermal Resistance $\psi_{Jt}$ (°C /W) for JEDEC 4L system PCB   | 1.84 °C/W  |

MT7620A:

|  |            |
|--|------------|
| Thermal Resistance $\theta_{JA}$ (°C /W) for JEDEC 2L system PCB | 26.67 °C/W |
| Thermal Resistance $\theta_{JA}$ (°C /W) for JEDEC 4L system PCB | 24.9 °C/W  |
| Thermal Resistance $\theta_{JC}$ (°C /W) for JEDEC 2L system PCB | 9.89 °C/W  |
| Thermal Resistance $\theta_{JC}$ (°C /W) for JEDEC 4L system PCB | 9.75 °C/W  |
| Thermal Resistance $\psi_{Jt}$ (°C /W) for JEDEC 2L system PCB   | 4.31 °C/W  |
| Thermal Resistance $\psi_{Jt}$ (°C /W) for JEDEC 4L system PCB   | 4.19 °C/W  |

Table 3-4 Thermal Characteristics



### 3.7 Storage Conditions

The calculated shelf life in a sealed bag is 12 months if stored between 0 °C and 40 °C at less than 90% relative humidity (RH). After the bag is opened, devices that are subjected to solder reflow or other high temperature processes must be handled in the following manner:

- Mounted within 168 hours of factory conditions, i.e. < 30 °C at 60% RH.
- Storage humidity needs to maintained at < 10% RH.
- Baking is necessary if the customer exposes the component to air for over 168 hrs, baking conditions: 125 °C for 8 hrs.

### 3.8 External Xtal Specification

|                  |                 |
|------------------|-----------------|
| Frequency        | 20 MHz/ 40 Mhz  |
| Frequency offset | +/-20 ppm       |
| VIH/VIL          | Vcc-0.3 V/0.3 V |
| Duty cycle       | 45% to 55%      |

*Table 3-5 External Xtal Specifications*

### 3.9 DC Electrical Characteristics

| Parameters                 | Sym   | Conditions | Min  | Typ  | Max  | Unit |
|----------------------------|-------|------------|------|------|------|------|
| 3.3 V Supply Voltage       | Vcc33 |            | 3.0  | 3.3  | 3.6  | V    |
| _VX supply Voltage         | Vcc15 |            | 1.3  | 1.5  | 3.3  | V    |
| RGMII IO Supply Voltage    | Vdd25 |            | 2.25 | 2.5  | 2.7  | V    |
|                            | Vdd33 |            | 3.0  | 3.3  | 3.6  | V    |
| 1.27 V Supply Voltage      | Vcc12 |            | 1.20 | 1.27 | 1.33 | V    |
| 3.3 V Current Consumption  | Icc33 |            |      | 218  | 436  | mA   |
| 1.5 V Current Consumption  | Icc15 |            |      | 147  | 173  | mA   |
| 1.27 V Current Consumption | Icc12 |            |      | 380  | 540  | mA   |
| DDR2 Current               | Icc18 |            |      | 95   | 253  | mA   |

*Table 3-6 DC Electrical Characteristics*

| Vdd=2.5V  | Min   | Typ  | Max   |
|-----------|-------|------|-------|
| Vdd       | 2.25V | 2.5V | 2.75V |
| VIH       | 1.7V  |      |       |
| VIL       |       |      | 0.7V  |
| VOH       | 1.7V  |      |       |
| VOL       |       |      | 0.7V  |
| IOL (4mA) | 5.5   | 9.0  | 12.9  |
| (8mA)     | 11.1  | 18.1 | 26.2  |
| (12mA)    | 16.7  | 27.3 | 39.4  |

|           |      |      |      |
|-----------|------|------|------|
| (16mA)    | 22.3 | 36.5 | 52.7 |
| IOH (4mA) | 4.7  | 9.4  | 16.5 |
| (8mA)     | 9.5  | 18.8 | 33.0 |
| (12mA)    | 14.2 | 28.2 | 49.4 |
| (16mA)    | 18.9 | 37.6 | 65.9 |

Table 3-7 Vdd 2.5V Electrical Characteristics

| Vdd=3.3V  | Min  | Typ  | Max  |
|-----------|------|------|------|
| Vdd       | 3.0V | 3.3V | 3.6V |
| VIH       | 2.0V |      |      |
| VIL       |      |      | 0.8V |
| VOH       | 2.4V |      |      |
| VOL       |      |      | 0.4V |
| IOL (4mA) | 4.8  | 7.1  | 9.4  |
| (8mA)     | 9.8  | 14.4 | 19.1 |
| (12mA)    | 14.8 | 21.8 | 28.8 |
| (16mA)    | 19.7 | 29.1 | 38.5 |
| IOH (4mA) | 7.0  | 13.4 | 22.7 |
| (8mA)     | 13.9 | 26.8 | 45.2 |
| (12mA)    | 20.8 | 40.1 | 67.8 |
| (16mA)    | 27.8 | 53.5 | 90.3 |

Table 3-8 Vdd 3.3V Electrical Characteristics

### 3.10 AC Electrical Characteristics

#### 3.10.1 SDRAM Interface

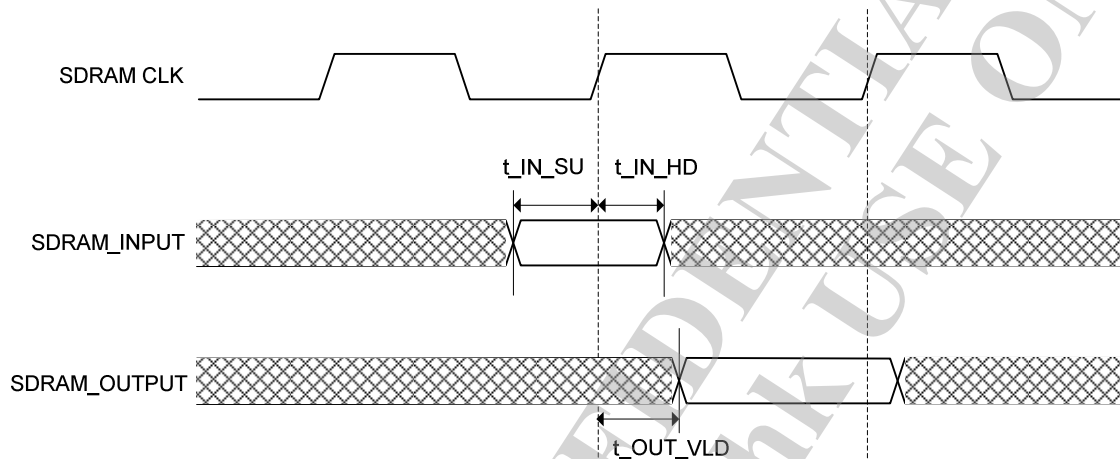


Figure 3-1 SDRAM Interface

| Symbol         | Description   | Min | Max | Unit | Remark            |
|----------------|---|-----|-----|------|-------------------|
| $t_{IN\_SU}$   | Setup time for Input signals (e.g. MD*)                       | 1.5 | -   | ns   |                   |
| $t_{IN\_HD}$   | Hold time for input signals                                   | 1.7 | -   | ns   |                   |
| $t_{OUT\_VLD}$ | SDRAM_CLK to output signals (MA*, MD*, SDRAM_RAS_N,...) valid | 0.8 | 5   | ns   | output load: 8 pF |

Table 3-9 SDRAM Interface Diagram Key

### 3.10.2 DDR2 SDRAM Interface

The DDR2 SDRAM interface complies with 200 MHz timing requirements for standard DDR2 SDRAM. The interface drivers are SSTL\_18 drivers matching the EIA/JEDEC standard JESD8-15A.

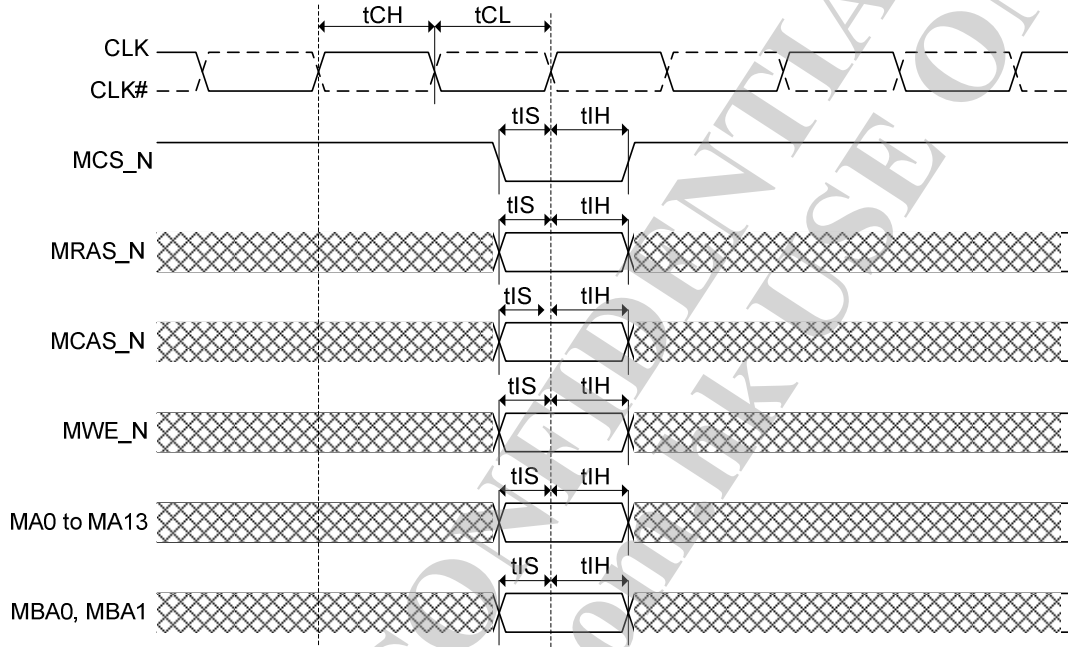


Figure 3-2 DDR2 SDRAM Command

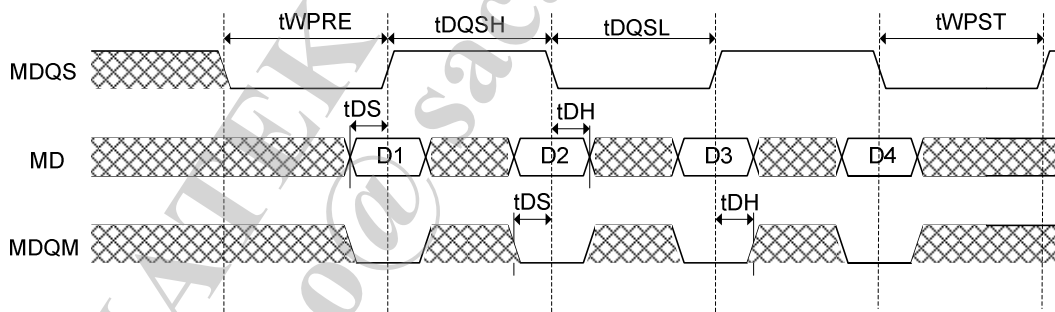


Figure 3-3 DDR2 SDRAM Write data

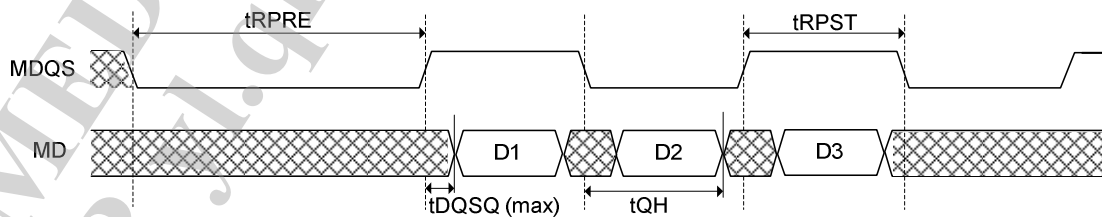


Figure 3-4 DDR2 SDRAM Read data

| Symbol   | Description                               | Min          | Max  | Unit     | Remark |
|----------|---|--------------|------|----------|--------|
| tCK(avg) | Clock cycle time                          | 5            | -    | ns       |        |
| tAC      | DQ output access time from SDRAM CLK      | -0.6         | 0.6  | ns       |        |
| tDQSCK   | DQS output access time from SDRAM CLK     | -0.5         | 0.5  | ns       |        |
| tCH      | SDRAM CLK high pulse width                | 0.48         | 0.52 | tCK(avg) |        |
| tCL      | SDRAM CLK low pulse width                 | 0.48         | 0.52 | tCK(avg) |        |
| tHP      | SDRAM CLK half period                     | Min(tCH,tCL) | -    | ns       |        |
| tIS      | Address and control input setup time      | 0.75         | -    | ns       |        |
| tIH      | Address and control input hold time       | 0.75         | -    | ns       |        |
| tDQSQ    | Data skew of DQS and associated DQ        | -            | 0.4  | ns       |        |
| tQH      | DQ/DQS output hold time from DQS          | tHP-0.5      | -    | ns       |        |
| tRPRE    | DQS read preamble                         | 0.9          | 1.1  | tCK      |        |
| tRPST    | DQS read postamble                        | 0.4          | 0.6  | tCK      |        |
| tDQSS    | DQS rising edge to CK rising edge         | -0.25        | 0.25 | tCK      |        |
| tDQSH    | DQS input-high pulse width                | 0.35         | -    | tCK      |        |
| tDQSL    | DQS input-low pulse width                 | 0.35         | -    | tCK      |        |
| tDSS     | DQS falling edge to SDRAM CLK setup time  | 0.2          | -    | tCK      |        |
| tDSH     | DQS falling edge hold time from SDRAM CLK | 0.2          | -    | tCK      |        |
| tWPRE    | DQS write preamble                        | 0.35         | -    | tCK      |        |
| tWPST    | DQS write postamble                       | 0.4          | 0.6  | tCK      |        |
| tDS      | DQ and DQM input setup time               | *0.4         | -    | ns       |        |
| tDH      | DQ and DQM input hold time                | *0.4         | -    | ns       |        |

Table 3-10 DDR2 SDRAM Interface Diagram Key

NOTE: Depends on slew rate of DQS and DQ/DQM for single ended DQS.

### 3.10.3 RGMII Interface

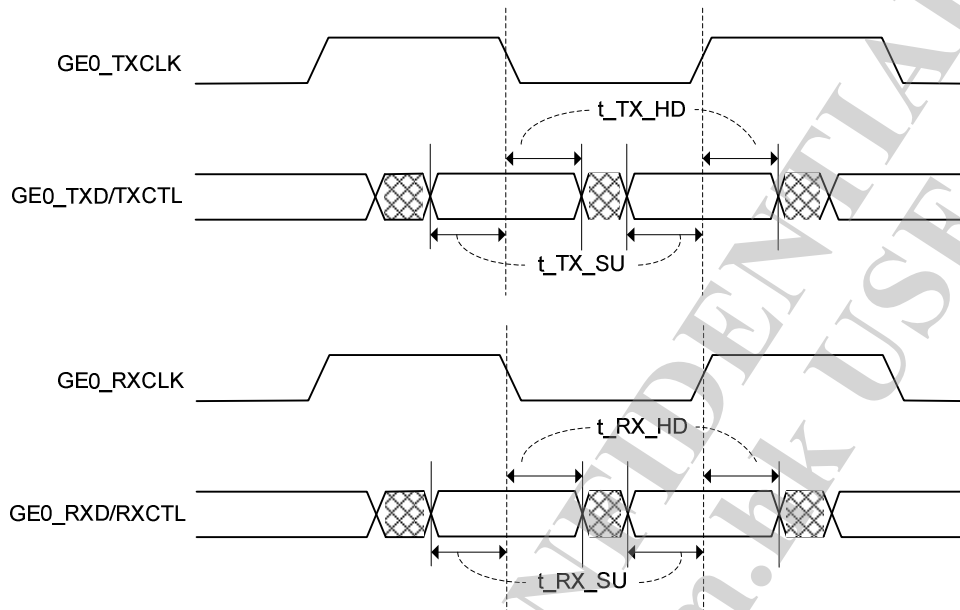


Figure 3-5 RGMII Interface

| Symbol  | Description  | Min | Max | Unit | Remark            |
|---------|--|-----|-----|------|-------------------|
| t_TX_SU | Setup time for output signals<br>(e.g. GE0_TXD*, GE0_TXEN) | 1.2 | -   | ns   | output load: 5 pF |
| t_TX_HD | Hold time for output signals                               | 1.2 | -   | ns   | output load: 5 pF |
| t_RX_SU | Setup time for input signals<br>(e.g. GE0_RXD*, GE0_RXDV)  | 1.0 | -   | ns   |                   |
| t_RX_HD | Hold time for input signals                                | 1.0 | -   | ns   |                   |

Table 3-11 RGMII Interface Diagram Key

### 3.10.4 MII Interface (25 Mhz)

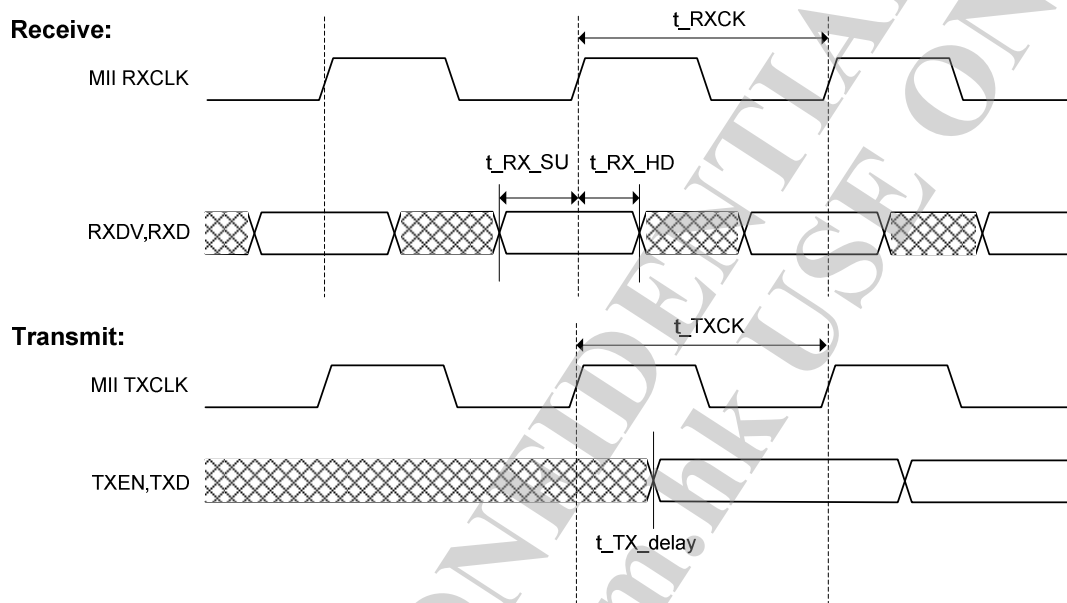


Figure 3-6 MII Interface

(For 25 Mhz TXCLK & RXCLK)

| Symbol     | Description   | Min | Max | Unit | Remark            |
|------------|---|-----|-----|------|-------------------|
| t_TX_delay | Delay to output signals<br>(e.g. GEO_TXD*, GEO_TXEN)      | 6   | 22  | ns   | output load: 5 pF |
| t_RX_SU    | Setup time for input signals<br>(e.g. GEO_RXD*, GEO_RXDV) | 10  | -   | ns   |                   |
| t_RX_HD    | Hold time for input signals                               | 5   | -   | ns   |                   |

Table 3-12 MII Interface Diagram Key

### 3.10.5 RvMII Interface (PHY Mode MII Timing) (25 Mhz)

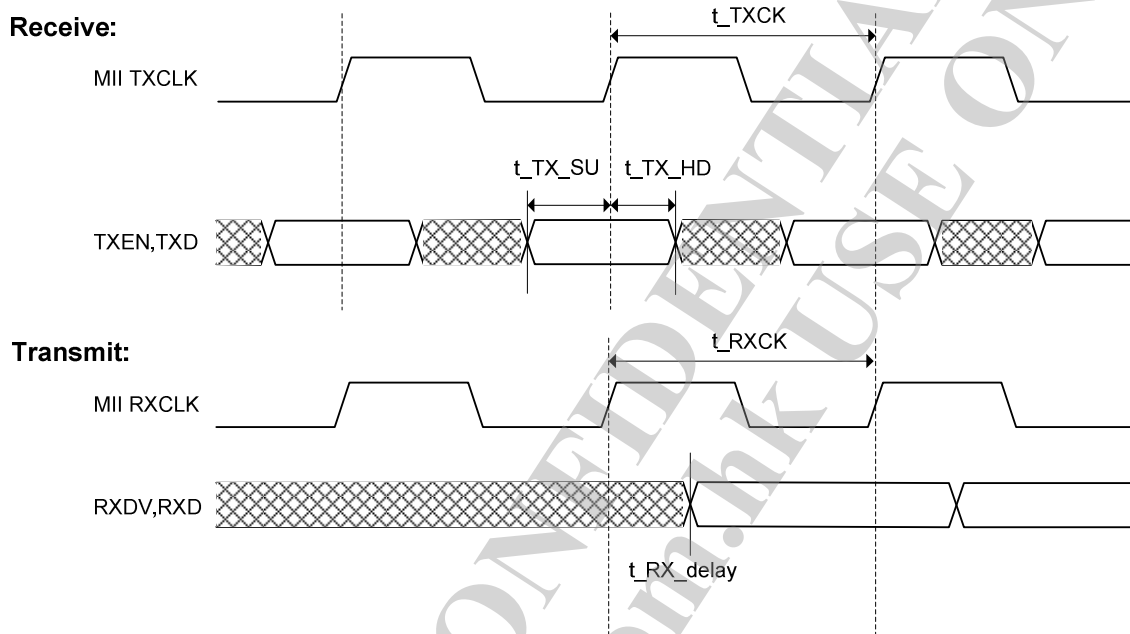


Figure 3-7 RvMII Interface

(For 25 Mhz TXCLK & RXCLK)

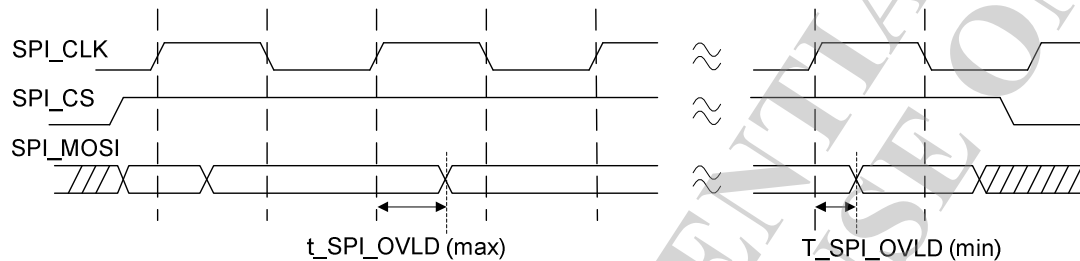
| Symbol     | Description   | Min | Max | Unit | Remark            |
|------------|---|-----|-----|------|-------------------|
| t_RX_delay | Delays to output signals<br>(e.g. GEO_TXD*, GEO_TXEN)     | 5   | 25  | ns   | output load: 5 pF |
| t_TX_SU    | Setup time for input signals<br>(e.g. GEO_RXD*, GEO_RXDV) | 15  | -   | ns   |                   |
| t_TX_HD    | Hold time for input signals                               | 6   | -   | ns   |                   |

Table 3-13 RvMII Interface Diagram Key

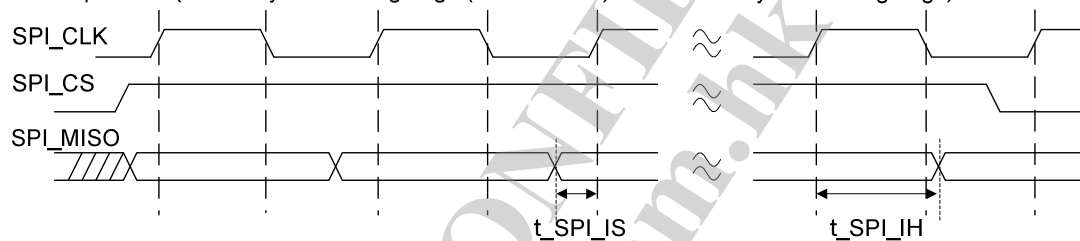


### 3.10.6 SPI Interface

Write operation (driven by clock rising edge)



Read operation (Driven by clock rising edge (slave-device) and latched by clock rising edge)



NOTE: 1) SPI\_CLK is a gated clock.  
2) SPI\_CS is controlled by software

Figure 3-8 SPI Interface

| Symbol          | Description                 | Min  | Max | Unit | Remark            |
|-----------------|-----------------------------|------|-----|------|-------------------|
| $t_{SPI\_IS}$   | Setup time for SPI input    | 6.0  | -   | ns   |                   |
| $t_{SPI\_IH}$   | Hold time for SPI input     | -1.0 | -   | ns   |                   |
| $t_{SPI\_OVLD}$ | SPI_CLK to SPI output valid | -2.0 | 3.0 | ns   | output load: 5 pF |

Table 3-14 SPI Interface Diagram Key

### 3.10.7 I<sup>2</sup>S Interface

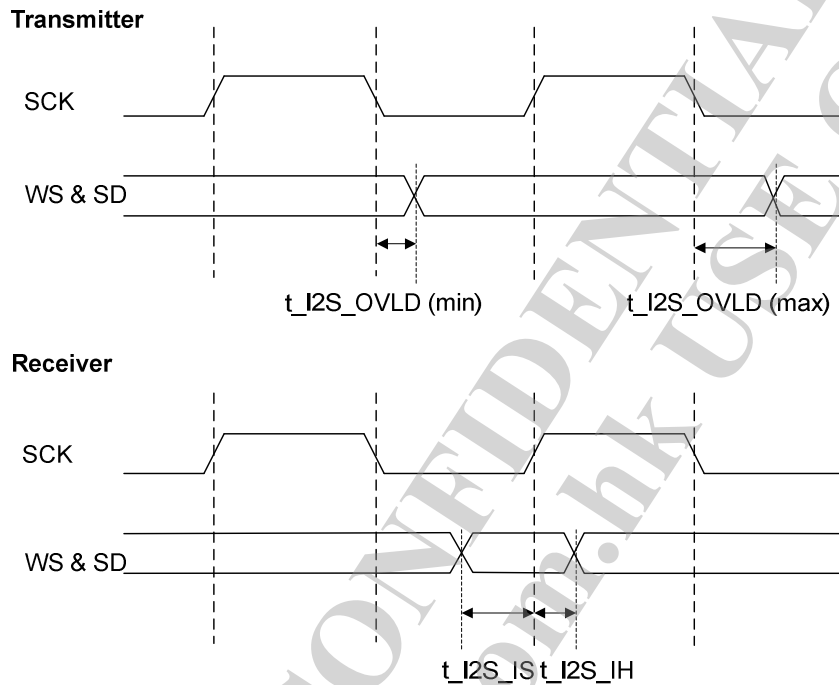


Figure 3-9 I2S Interface

| Symbol     | Description                             | Min | Max  | Unit | Remark            |
|------------|---|-----|------|------|-------------------|
| t_I2S_IS   | Setup time for I2S input (data & WS)    | 3.5 | -    | ns   |                   |
| t_I2S_IH   | Hold time for I2S input (data & WS)     | 0.5 | -    | ns   |                   |
| t_I2S_OVLD | I2S_CLK to I2S output (data & WS) valid | 2.5 | 10.0 | ns   | output load: 5 pF |

Table 3-15 I2S Interface Diagram Key

### 3.10.8 PCM Interface

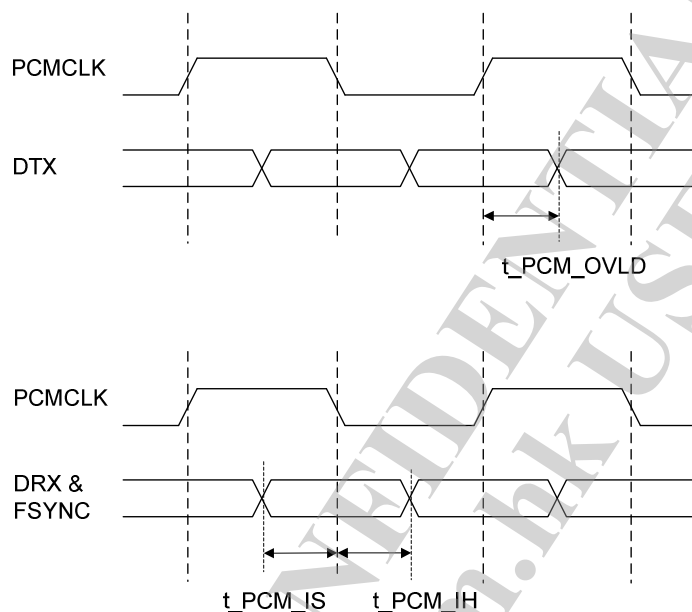


Figure 3-10 PCM Interface

| Symbol          | Description                              | Min  | Max  | Unit | Remark            |
|-----------------|--|------|------|------|-------------------|
| $t_{PCM\_IS}$   | Setup time for PCM input to PCM_CLK fall | 3.0  | -    | ns   |                   |
| $t_{PCM\_IH}$   | Hold time for PCM input to PCM_CLK fall  | 1.0  | -    | ns   |                   |
| $t_{PCM\_OVLD}$ | PCM_CLK rise to PCM output valid         | 10.0 | 35.0 | ns   | output load: 5 pF |

Table 3-16 PCM Interface Diagram Key

### 3.10.9 Power On Sequence

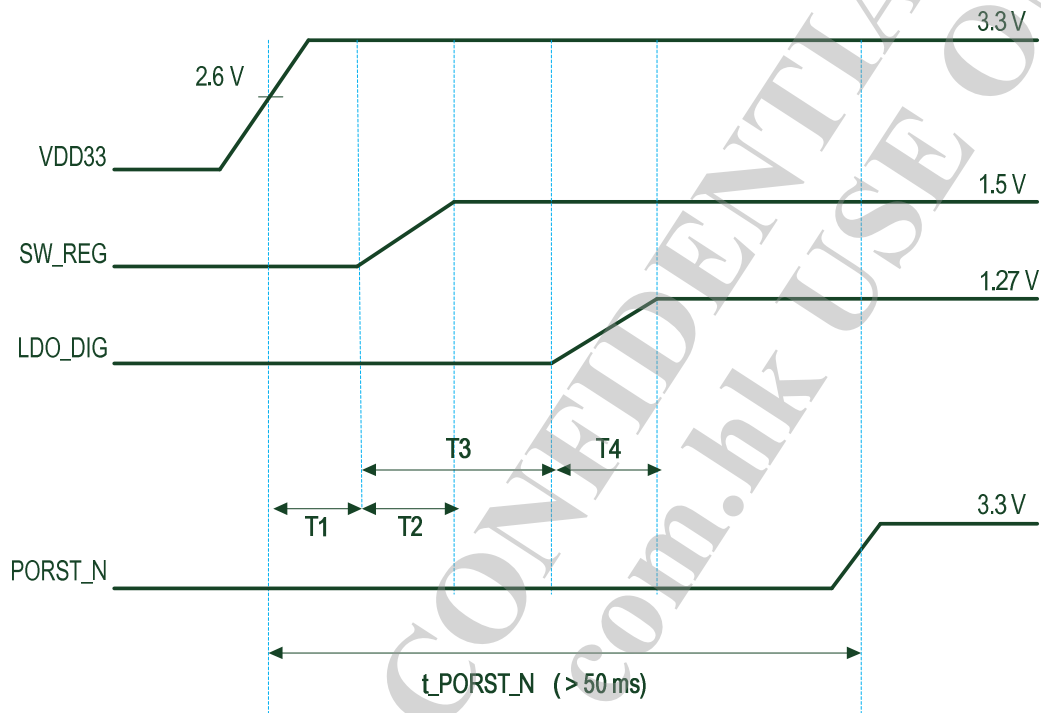


Figure 3-11 Power ON Sequence

| Symbol    | Description                                       | Min*(1) | Max*(2) | Unit | Remark |
|-----------|---|---------|---------|------|--------|
| T1        | POR delay   | 800     | >0      | us   |        |
| T2        | Soft start  | 850     | >0      | us   |        |
| T3        | Soft start done                                   | 1.4     | >0      | ms   |        |
| T4        | LDO_DIG soft start                                | 650     | >0      | us   |        |
| t_PORST_N | Time between I/O power on to PORST_N de-assertion | 50      | 50      | ms   |        |

Min(\*1) : Internal PMU sequence, Min(\*2): External power providing sequence

Table 3-17 Power ON Sequence Diagram Key

### 3.11 Package Physical Dimensions

#### 3.11.1 TFBGA (11 mm x 11 mm) 265 balls

##### 3.11.1.1 TFBGA Top View

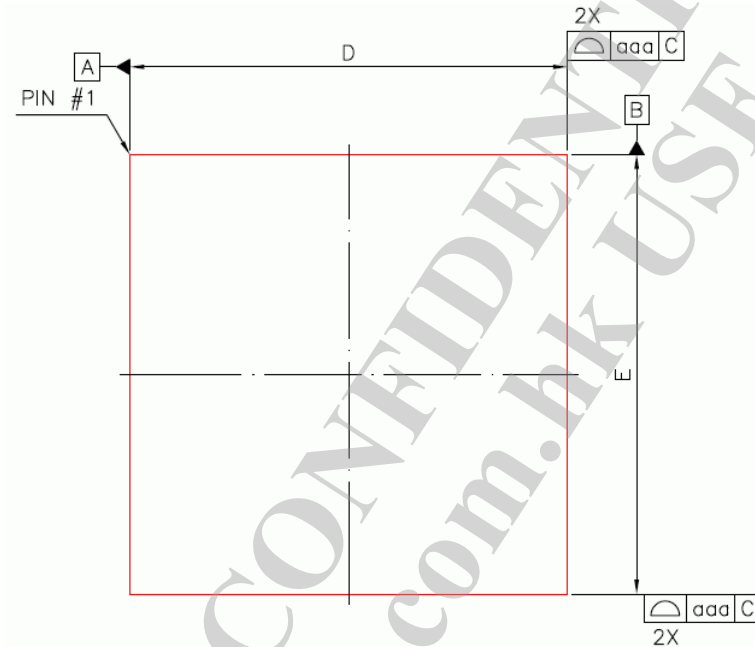


Figure 3-12 TFBGA Top View

##### 3.11.1.2 TFBGA Side View



Figure 3-13 TFBGA Side View

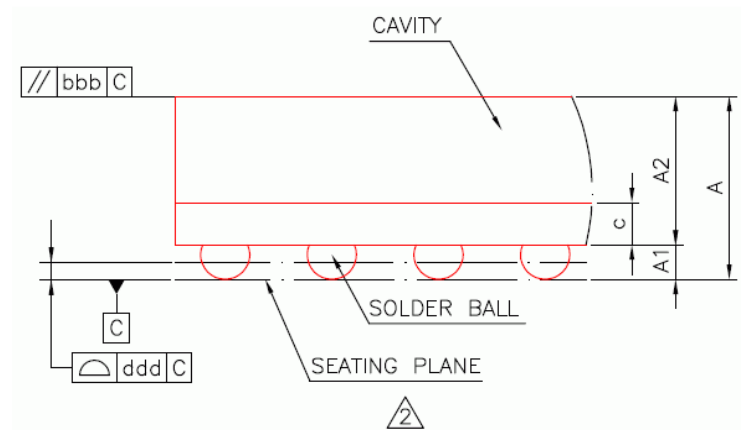


Figure 3-14 TFBGA "A" Expanded

##### 3.11.1.3 TFBGA "A" Expanded

### 3.11.1.4 TFBGA Bottom View

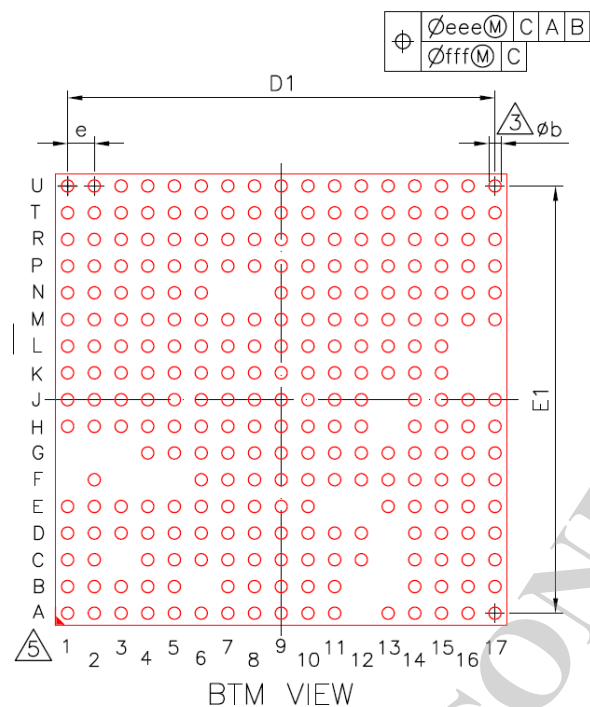


Figure 3-15 TFBGA Bottom View

### 3.11.1.5 TFBGA "B" Expanded

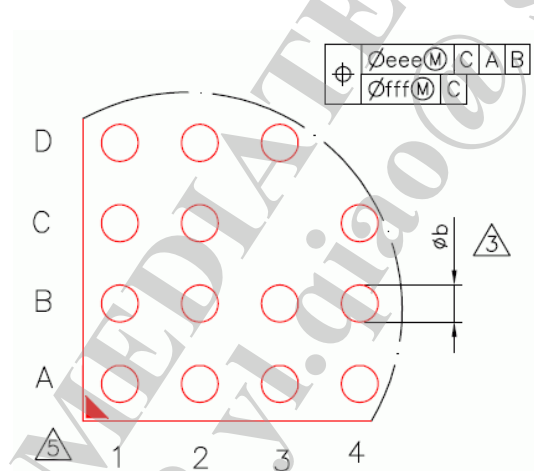


Figure 3-16 TFBGA "B" Expanded

### 3.11.1.6 Package Diagram Key

| Sym-<br>bol | Dimensions<br>(mm) |       |       | Dimensions (inches) |       |       |
|-------------|--------------------|-------|-------|---------------------|-------|-------|
|             | Min.               | Nom.  | Max.  | Min.                | Nom.  | Max.  |
| A           | ---                | ---   | 1.20  | ---                 | ---   | 0.047 |
| A1          | 0.16               | 0.21  | 0.26  | 0.006               | 0.008 | 0.010 |
| A2          | 0.86               | 0.91  | 0.96  | 0.034               | 0.036 | 0.038 |
| c           | 0.22               | 0.26  | 0.30  | 0.009               | 0.010 | 0.012 |
| D           | 10.90              | 11.00 | 11.10 | 0.429               | 0.433 | 0.437 |
| E           | 10.90              | 11.00 | 11.10 | 0.429               | 0.433 | 0.437 |
| D1          | ---                | 10.40 | ---   | ---                 | 0.409 | ---   |
| E1          | ---                | 10.40 | ---   | ---                 | 0.409 | ---   |
| e           | ---                | 0.65  | ---   | ---                 | 0.026 | ---   |
| b           | 0.25               | 0.30  | 0.35  | 0.010               | 0.012 | 0.014 |
| aaa         | 0.15               |       |       | 0.006               |       |       |
| bbb         | 0.10               |       |       | 0.004               |       |       |
| ddd         | 0.08               |       |       | 0.003               |       |       |
| eee         | 0.15               |       |       | 0.006               |       |       |
| fff         | 0.08               |       |       | 0.003               |       |       |
| MD/ME       | 17/17              |       |       | 17/17               |       |       |

#### NOTE:

- Controlling dimensions are in millimeters.
- Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
- Dimension b is measured at the maximum solder ball diameter, parallel to primary datum C.
- Special characteristics C class: bbb, ddd.
- The pattern of pin 1 fiducial is for reference only.

### 3.11.2 DR-QFN (12 mm x 12 mm) 148LD

#### 3.11.2.1 DR-QFN Top View

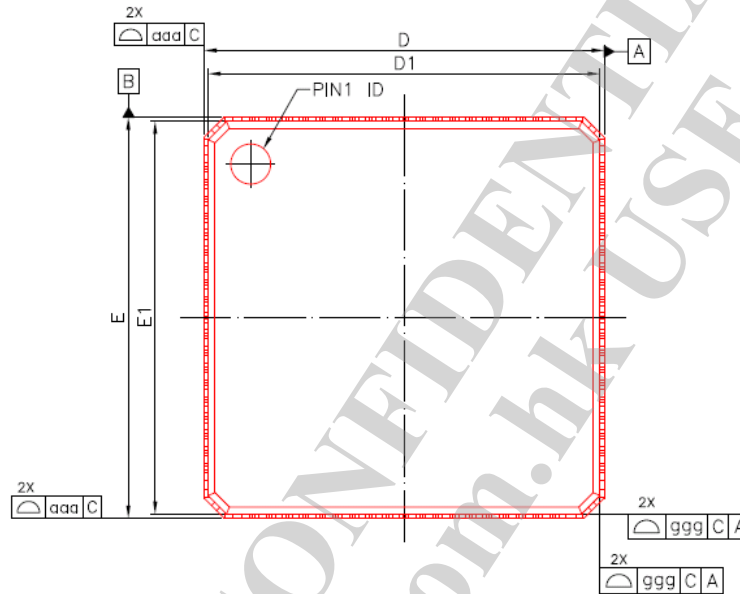


Figure 3-17 DR-QFN Top View

#### 3.11.2.2 DR-QFN Side View



Figure 3-18 DR-QFN Side View

#### 3.11.2.3 DR-QFN "B" Expanded

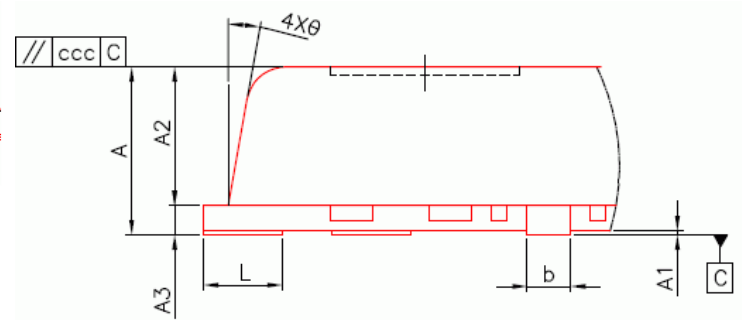


Figure 3-19 DR-QFN "B" Expanded

### 3.11.2.4 DR-QFN Bottom View

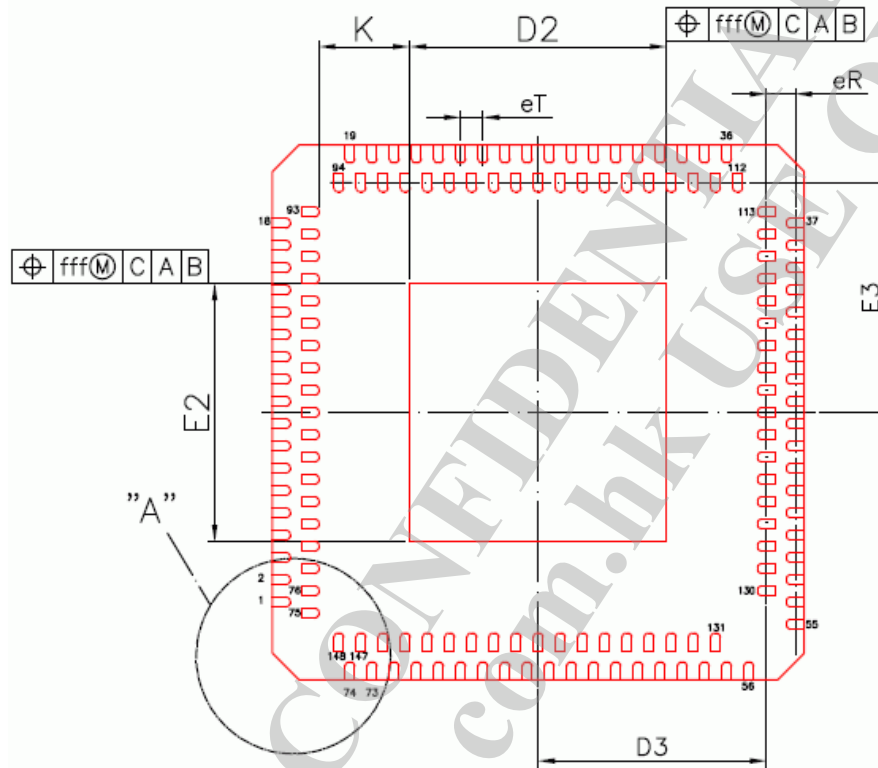


Figure 3-20 DR-QFN Bottom View

### 3.11.2.5 DR-QFN "A" Expanded

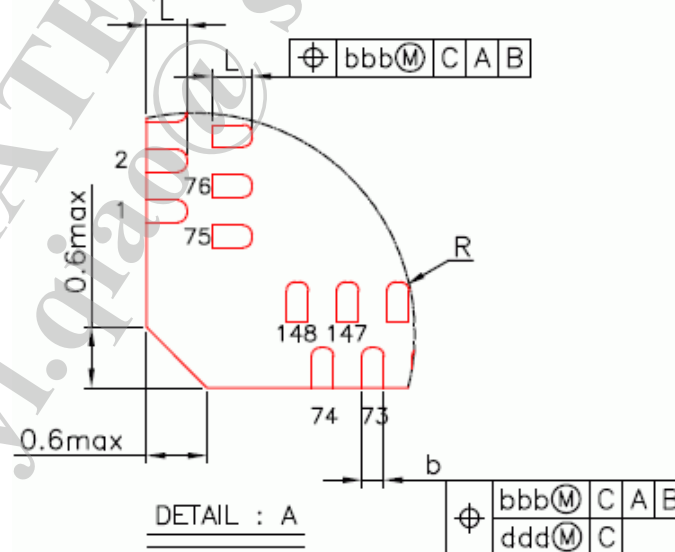


Figure 3-21 DR-QFN "A" Expanded



### 3.11.2.6 Package Diagram Key

| Sym-<br>bol | Dimensions (mm) |       |       | Dimensions (inches) |        |       |
|-------------|-----------------|-------|-------|---------------------|--------|-------|
|             | Min.            | Nom.  | Max.  | Min.                | Nom.   | Max.  |
| A           | 0.80            | 0.85  | 0.90  | 0.031               | 0.033  | 0.035 |
| A1          | 0.00            | 0.02  | 0.05  | 0.000               | 0.0008 | 0.002 |
| A2          | 0.65            | 0.70  | 0.75  | 0.026               | 0.028  | 0.030 |
| A3          | 0.15 REF        |       |       | 0.006 REF           |        |       |
| b           | 0.18            | 0.22  | 0.30  | 0.007               | 0.009  | 0.012 |
| D/E         | 11.90           | 12.00 | 12.10 | 0.469               | 0.472  | 0.476 |
| D1/E1       | 11.75 BSC       |       |       | 0.463 BSC           |        |       |
| D3/E3       | 5.15 BSC        |       |       | 0.203 BSC           |        |       |
| eT          | 0.50 BSC        |       |       | 0.020 BSC           |        |       |
| eR          | 0.65 BSC        |       |       | 0.026 BSC           |        |       |
| L           | 0.30            | 0.40  | 0.50  | 0.012               | 0.016  | 0.020 |
| θ           | 5°              | ---   | 15°   | 5°                  | ---    | 15°   |
| K           | 0.20            | ---   | ---   | 0.008               | ---    | ---   |
| R           | 0.09            | ---   | ---   | 0.004               | ---    | ---   |
| aaa         | 0.10            |       |       | 0.004               |        |       |
| bbb         | 0.10            |       |       | 0.004               |        |       |
| ccc         | 0.10            |       |       | 0.004               |        |       |
| ddd         | 0.05            |       |       | 0.002               |        |       |
| eee         | 0.08            |       |       | 0.003               |        |       |
| fff         | 0.10            |       |       | 0.004               |        |       |
| ggg         | 0.20            |       |       | 0.008               |        |       |

**NOTE:**

1. Controlling dimensions are in millimeters.
2. Reference document: JEDEC MO-267

| Exposed Pad Size |            |      |      |                |       |       |
|------------------|------------|------|------|----------------|-------|-------|
| L/F              | D2/E2 (mm) |      |      | D2/E2 (inches) |       |       |
|                  | Min.       | Nom. | Max. | Min.           | Nom.  | Max.  |
|                  | 5.65       | 5.80 | 5.95 | 0.222          | 0.228 | 0.234 |

| Internal Pad Size |      |      |      |          |       |       |
|-------------------|------|------|------|----------|-------|-------|
| L/F               | (mm) |      |      | (inches) |       |       |
|                   | Min. | Nom. | Max. | Min.     | Nom.  | Max.  |
|                   | 5.85 | 6.00 | 6.15 | 0.230    | 0.236 | 0.242 |

### 3.11.3 MT7620 N/A marking



YYWW: Date code  
LLLLLLLLLL : Lot number  
“.” : Pin #1 dot

Figure 3-22 MT7620N top marking



YYWW: Date code  
LLLLLLLLLL : Lot number  
“.” : Pin #1 dot

Figure 3-23 MT7620A top marking

### 3.11.4 Reflow profile guideline

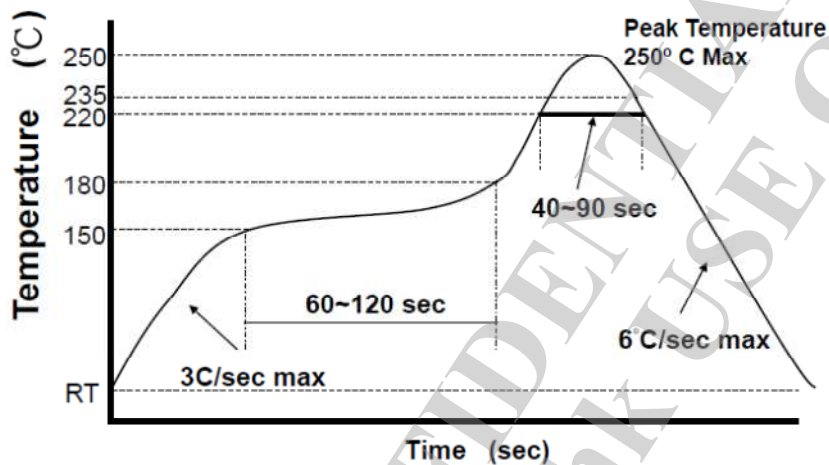


Figure 3-24 Reflow profile for MT7620

Notes;

1. Reflow profile guideline is designed for SnAgCu lead-free solder paste.
2. Reflow temperature is defined at the solder ball of package/or the lead of package.
3. MTK would recommend customer following the solder paste vendor's guideline to design a profile appropriate your line and products.
4. Appropriate N<sub>2</sub> atmosphere is recommended since it would widen the process window and mitigate the risk for having solder open issues.

## 4. Abbreviations

| Abbrev. | Description  | Abbrev.           | Description   |
|---------|--|-------------------|---|
| AC      | Access Category  | CLK               | Clock   |
| ACK     | Acknowledge/ Acknowledgement   | CPU               | Central Processing Unit                             |
| ACPR    | Adjacent Channel Power Ratio   | CRC               | Cyclic Redundancy Check                             |
| AD/DA   | Analog to Digital/Digital to Analog converter                                | CSR               | Control Status Register                             |
| ADC     | Analog-to-Digital Converter  | CTS               | Clear to Send                                       |
| AES     | Advanced Encryption Standard   | CW                | Contention Window                                   |
| AGC     | Auto Gain Control  | CW <sub>max</sub> | Maximum Contention Window                           |
| AIFS    | Arbitration Inter-Frame Space  | CW <sub>min</sub> | Minimum Contention Window                           |
| AIFSN   | Arbitration Inter-Frame Spacing Number                                       | DAC               | Digital-To-Analog Converter                         |
| ALC     | Asynchronous Layered Coding  | DCF               | Distributed Coordination Function                   |
| A-MPDU  | Aggregate MAC Protocol Data Unit   | DDONE             | DMA Done  |
| A-MSDU  | Aggregation of MAC Service Data Units  | DDR               | Double Data Rate                                    |
| AP      | Access Point   | DFT               | Discrete Fourier Transform                          |
| ASIC    | Application-Specific Integrated Circuit                                      | DIFS              | DCF Inter-Frame Space                               |
| ASME    | American Society of Mechanical Engineers                                     | DMA               | Direct Memory Access                                |
| ASYNCR  | Asynchronous   | DSP               | Digital Signal Processor                            |
| BA      | Block Acknowledgement  | DW                | DWORD   |
| BAC     | Block Acknowledgement Control  | EAP               | Expert Antenna Processor                            |
| BAR     | Base Address Register  | EDCA              | Enhanced Distributed Channel Access                 |
| BBP     | Baseband Processor   | EECS              | EEPROM chip select                                  |
| BGSEL   | Band Gap Select  | EEDI              | EEPROM data input                                   |
| BIST    | Built-In Self-Test   | EEDO              | EEPROM data output                                  |
| BSC     | Basic Spacing between Centers  | EEPROM            | Electrically Erasable Programmable Read-Only Memory |
| BJT     |  | eFUSE             | electrical Fuse                                     |
| BSSID   | Basic Service Set Identifier   | EESK              | EEPROM source clock                                 |
| BW      | Bandwidth  | EIFS              | Extended Inter-Frame Space                          |
| CCA     | Clear Channel Assessment   | EIV               | Extend Initialization Vector                        |
| CCK     | Complementary Code Keying  | EVM               | Error Vector Magnitude                              |
| CCMP    | Counter Mode with Cipher Block Chaining Message Authentication Code Protocol | FDS               | Frequency Domain Spreading                          |
| CCX     | Cisco Compatible Extensions  | FEM               | Front-End Module                                    |
| CF-END  | Control Frame End  | FEQ               | Frequency Equalization                              |
| CF-ACK  | Control Frame Acknowledgement  | FIFO              | First In First Out                                  |
|         |  | FSM               | Finite-State Machine                                |
|         |  | GF                | Green Field   |
|         |  | GND               | Ground  |
|         |  | GP                | General Purpose                                     |

| Abbrev.          | Description                                |
|------------------|--|
| GPO              | General Purpose Output                     |
| GPIO             | General Purpose Input/Output               |
| HCCA             | HCF Controlled Channel Access              |
| HCF              | Hybrid Coordination Function               |
| HT               | High Throughput                            |
| HTC              | High Throughput Control                    |
| ICV              | Integrity Check Value                      |
| IFS              | Inter-Frame Space                          |
| iNIC             | Intelligent Network Interface Card         |
| IV               | Initialization Vector                      |
| I <sup>2</sup> C | Inter-Integrated Circuit                   |
| I <sup>2</sup> S | Integrated Inter-Chip Sound                |
| I/O              | Input/Output                               |
| IPI              | Idle Power Indicator                       |
| IQ               | In phase/Quadrature phase                  |
| JEDEC            | Joint Electron Devices Engineering Council |
| JTAG             | Joint Test Action Group                    |
| kbps             | kilo (1000) bits per second                |
| KB               | Kilo (1024) Bytes                          |
| LDO              | Low-Dropout Regulator                      |
| LDODIG           | LDO for DIGital part output voltage        |
| LED              | Light-Emitting Diode                       |
| LNA              | Low Noise Amplifier                        |
| LO               | Local Oscillator                           |
| L-SIG            | Legacy Signal Field                        |
| MAC              | Medium Access Control                      |
| MCU              | Microcontroller Unit                       |
| MCS              | Modulation and Coding Scheme               |
| MDC              | Management Data Clock                      |
| MDIO             | Management Data Input/Output               |
| MEM              | Memory                                     |
| MFB              | MCS Feedback                               |
| MFS              | MFB Sequence                               |
| MIC              | Message Integrity Code                     |
| MIMO             | Multiple-Input Multiple-Output             |
| MLNA             | Monolithic Low Noise Amplifier             |
| MM               | Mixed Mode                                 |

| Abbrev. | Description                                       |
|---------|---|
| MOSFET  | Metal Oxide Semiconductor Field Effect Transistor |
| MPDU    | MAC Protocol Data Units                           |
| MSB     | Most Significant Bit                              |
| NAV     | Network Allocation Vector                         |
| NAS     | Network-Attached Server                           |
| NAT     | Network Address Translation                       |
| NDP     | Null Data Packet                                  |
| NVM     | Non-Volatile Memory                               |
| ODT     | On-die Termination                                |
| Oen     | Output Enable                                     |
| OFDM    | Orthogonal Frequency-Division Multiplexing        |
| OSC     | Open Sound Control                                |
| PA      | Power Amplifier                                   |
| PAPE    | Provider Authentication Policy Extension          |
| PBC     | Push Button Configuration                         |
| PBF     | Packet Buffer                                     |
| PCB     | Printed Circuit Board                             |
| PCF     | Point Coordination Function                       |
| PCM     | Pulse-Code Modulation                             |
| PHY     | Physical Layer                                    |
| PIFS    | PCF Interframe Space                              |
| PLCP    | Physical Layer Convergence Protocol               |
| PLL     | Phase-Locked Loop                                 |
| PME     | Physical Medium Entities                          |
| PMU     | Power Management Unit                             |
| PN      | Packet Number                                     |
| PROM    | Programmable Read-Only Memory                     |
| PSDU    | Physical layer Service Data Unit                  |
| PSI     | Power supply Strength Indication                  |
| PSM     | Power Save Mode                                   |
| PTN     | Packet Transport Network                          |
| QoS     | Quality of Service                                |
| RDG     | Reverse Direction Grant                           |
| RAM     | Random Access Memory                              |
| RF      | Radio Frequency                                   |
| RGMII   | Reduced Gigabit Media Independent Interface       |

| Abbrev. | Description                                     |
|---------|---|
| RH      | Relative Humidity                               |
| RoHS    | Restriction on Hazardous Substances             |
| ROM     | Read-Only Memory                                |
| RSSI    | Received Signal Strength Indication (Indicator) |
| RTS     | Request to Send                                 |
| RvMII   | Reverse Media Independent Interface             |
| Rx      | Receive   |
| RXD     | Received Data                                   |
| RXINFO  | Receive Information                             |
| RXWI    | Receive Wireless Information                    |
| S       | Stream  |
| SDXC    | Secure Digital eXtended Capacity                |
| SDIO    | Secure Digital Input Output                     |
| SDRAM   | Synchronous Dynamic Random Access Memory        |
| SEC     | Security  |
| SGI     | Short Guard Interval                            |
| SIFS    | Short Inter-Frame Space                         |
| SoC     | System-on-a-Chip                                |
| SPI     | Serial Peripheral Interface                     |
| SRAM    | Static Random Access Memory                     |
| SSCG    | Spread Spectrum Clock Generator                 |
| STBC    | Space-Time Block Code                           |
| SW      | Switch Regulator                                |
| TA      | Transmitter Address                             |
| TBTT    | Target Beacon Transmission Time                 |
| TDLS    | Tunnel Direct Link Setup                        |

| Abbrev. | Description                                    |
|---------|--|
| TKIP    | Temporal Key Integrity Protocol                |
| TRSW    | Tx/Rx Switch                                   |
| TSF     | Timing Synchronization Function                |
| TSSI    | Transmit Signal Strength Indication            |
| Tx      | Transmit                                       |
| TxBF    | Transmit Beamforming                           |
| TXD     | Transmitted Data                               |
| TXDAC   | Transmit Digital-Analog Converter              |
| TXINFO  | Transmit Information                           |
| TXOP    | Opportunity to Transmit                        |
| TXWI    | Tx Wireless Information                        |
| UART    | Universal Asynchronous Rx/ Tx                  |
| USB     | Universal Serial Bus                           |
| UTIF    | Universal Test Interface                       |
| VGA     | Variable Gain Amplifier                        |
| VCO     | Voltage Controlled Amplifier                   |
| VIH     | High Level Input Voltage                       |
| VIL     | Low Level Input Voltage                        |
| VoIP    | Voice over IP                                  |
| WCID    | Wireless Client Identification                 |
| WEP     | Wired Equivalent                               |
| WI      | Wireless Information                           |
| WIV     | Wireless Information Valid                     |
| WMM     | Wi-Fi Multimedia                               |
| WPA     | Wi-Fi Protected Access                         |
| WPDMA   | Wireless Polarization Division Multiple Access |
| WS      | Word Select                                    |

## 5. Revision History

| Rev | Date       | Description                      |
|-----|------------|----------------------------------|
| 1.0 | 2012/07/09 | Initial Release                  |
| 1.1 | 2012/07/18 | Update SPI_WP/SPI_HOLD GPO table |
| 1.2 | 2012/08/20 | Fix DRQFN internal pad size typo |
| 1.3 | 2012/09/12 | Add IR reflow guideline          |

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