JK Flip Flop Design Code

```
module JKFF(
   output reg Q,
   output reg Qbar,
   input J,
   input K,
   input RST,
   input CLK
   );
   initial Q=0;
   always@(posedge CLK)
      if(RST==1)
         begin
            Q<=0;
            Qbar<=1;
         end
      else
         begin
            case({J,K})
               2'b00: begin Q<=Q; Qbar<=Qbar; end
               2'b01: begin Q<=0; Qbar<=1; end
               2'b10: begin Q<=1; Qbar<=0; end
               2'b11: begin Q<=~Q; Qbar<=~Qbar; end
            endcase
          end
endmodule
```

6 Mod Counter Design Code

```
module COUNTERMOD6(
   output Qa,
   output Qb,
   output Qc,
   input CLK,
   input RST
   );

   wire J1,J2,J3,BLANK1,BLANK2;
   JKFF F1(Qa,BLANK1,1,1,RST,CLK);
   JKFF F2(Qb,BLANK2,J1,Qa,RST,CLK);
   JKFF F3(Qc,J3,J2,Qa,RST,CLK);
   and A0(J1,Qa,J3);
   and A1(J2,Qb,Qa);
endmodule
```

6 Mod Counter TestBench Code

```
module COUNTER_TEST();
   wire Qa,Qb,Qc;
   reg CLK,RST;
   COUNTERMOD6 C1(Qa,Qb,Qc,CLK,RST);
   always #10 CLK=~CLK;
   initial begin
            RST=1;CLK=0;#20;
            RST=0;#20;
            #600
            $finish;
         end
endmodule
```