Lab 8. FSM의 기초

Prelab

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4. 가

Up/Down Counter

State Encoding

S0 : CS = [0, 0, 0] -> OUT = [0, 0, 0]

S1 : CS = [0, 0, 1] -> OUT = [0, 0, 1]

S2 : CS = [0, 1, 0] -> OUT = [0, 1, 0]

S3 : CS = [1, 0, 1] -> OUT = [1, 0, 1]

State Transition Table

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| CS[2] | CS[1] | CS[0] | IN | NS[2] | NS[1] | NS[0] |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 |

Output Table

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| NS[2] | NS[1] | NS[0] | OUT[2] | OUT[1] | OUT[0] |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 |

NS[2] = CS[1]’ CS[0]’ IN’ + CS[1] IN

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| CS[2] CS[1]  CS[0] IN | 00 | 01 | 11 | 10 |
| 00 | 1 | 0 | X | X |
| 01 | 0 | 1 | X | X |
| 11 | 0 | X | X | 0 |
| 10 | 0 | X | X | 0 |

NS[1] = CS[2]’ CS[0] IN + CS[2] CS[0] IN’

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| CS[2] CS[1]  CS[0] IN | 00 | 01 | 11 | 10 |
| 00 | 0 | 0 | X | X |
| 01 | 0 | 0 | X | X |
| 11 | 1 | X | X | 0 |
| 10 | 0 | X | X | 1 |

NS[0] = CS[0]’

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| CS[2] CS[1]  CS[0] IN | 00 | 01 | 11 | 10 |
| 00 | 1 | 1 | X | X |
| 01 | 1 | 1 | X | X |
| 11 | 0 | X | X | 0 |
| 10 | 0 | X | X | 0 |

Schematic Diagram

Diagram

Description automatically generated

4. 나

String Pattern Recognizer

State Encoding (Explanation of states)

S0 : CS = [0, 0, 0] -> OUT = [0] (Initial State)

S1 : CS = [0, 0, 1] -> OUT = [0] (When 1 ‘1’ is detected)

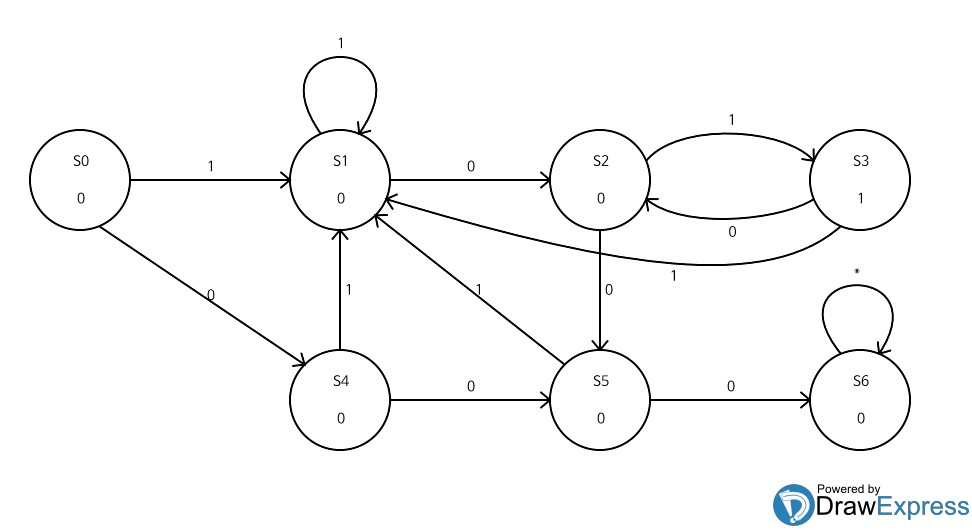
S2 : CS = [0, 1, 0] -> OUT = [0] (When a ‘10’ is detected)

S3 : CS = [0, 1, 1] -> OUT = [1] (When a ‘101’ is detected)

S4 : CS = [1, 0 ,0] -> OUT = [0] (When 1 ‘0’ is detected, but not in ‘10’ sequence)

S5 : CS = [1, 0, 1] -> OUT = [0] (When 2 ‘0’s are detected)

S6 : CS = [1, 1, 0] -> OUT = [0] (When 3 ‘0’s are detected, terminal state)



reset

State Transition Table

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| CS[2] | CS[1] | CS[0] | IN | NS[2] | NS[1] | NS[0] |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 |

Output Table

|  |  |  |  |
| --- | --- | --- | --- |
| CS[2] | CS[1] | CS[0] | OUT |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

NS[2] = CS[2] CS[1] + CS[0]’ IN’ + CS[2] IN’

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| CS[2] CS[1]  CS[0] IN | 00 | 01 | 11 | 10 |
| 00 | 1 | 1 | 1 | 1 |
| 01 | 0 | 0 | 1 | 0 |
| 11 | 0 | 0 | X | 0 |
| 10 | 0 | 0 | X | 1 |

NS[1] = CS[0] IN’ + CS[2] CS[1] + CS[1] CS[0]’ IN

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| CS[2] CS[1]  CS[0] IN | 00 | 01 | 11 | 10 |
| 00 | 0 | 0 | 1 | 0 |
| 01 | 0 | 1 | 1 | 0 |
| 11 | 0 | 0 | X | 0 |
| 10 | 1 | 1 | X | 1 |

NS[0] = IN + CS[1] CS[0]’ + CS[2] CS[0]’

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| CS[2] CS[1]  CS[0] IN | 00 | 01 | 11 | 10 |
| 00 | 0 | 1 | 1 | 1 |
| 01 | 1 | 1 | 1 | 1 |
| 11 | 1 | 1 | X | 1 |
| 10 | 0 | 0 | X | 0 |

OUT = CS[1] CS[0]

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| CS[2] CS[1]  CS[0] | 00 | 01 | 11 | 10 |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | X | 0 |

Schematic Diagram

Diagram, schematic

Description automatically generated