Lab 9. Traffic Light Controller의 구현을 통한 Verilog 실습

Prelab

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Traffic Light Controller

State Encoding (Explanation of states)

S0 : CS = [0, 0, 0] -> OUT = [0, 0, 1, 0, 1, 0, 0] (Initial State – Highway Green)

S1 : CS = [0, 0, 1] -> OUT = [0, 1, 0, 0, 1, 0, 0] (Highway Green -> Yellow, when FS=1 and HS=0)

S2 : CS = [0, 1, 0] -> OUT = [0, 0, 0, 1, 1, 0, 0] (Highway Left)

S3 : CS = [0, 1, 1] -> OUT = [1, 0, 0, 0, 0, 0, 1] (Farm Road Left)

S4 : CS = [1, 0 ,0] -> OUT = [1, 0, 0, 0, 0, 1, 0] (Farm Road Left -> Yellow)

S5 : CS = [1, 0, 1] -> OUT = [0, 1, 0, 0, 1, 0, 0] (Highway Left -> Yellow, when FS=0)

S6 : CS = [1, 1, 0] -> OUT = [0, 1, 0, 0, 1, 0, 0] (Highway Green -> Yellow, when HS=1)

S7 : CS = [1, 1, 1] -> OUT = [0, 1, 0, 0, 1, 0, 0] (Highway Left -> Yellow, when FS=1)

State Diagram

Diagram

Description automatically generated

State Transition Table

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| CS[2] | CS[1] | CS[0] | HS | FS | NS[2] | NS[1] | NS[0] |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | X | 1 | 1 | 0 |
| 0 | 0 | 1 | X | X | 0 | 1 | 1 |
| 0 | 1 | 0 | X | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | X | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | X | X | 1 | 0 | 0 |
| 1 | 0 | 0 | X | X | 0 | 0 | 0 |
| 1 | 0 | 1 | X | X | 0 | 0 | 0 |
| 1 | 1 | 0 | X | X | 0 | 1 | 0 |
| 1 | 1 | 1 | X | X | 0 | 1 | 1 |

Output Table

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| CS[2] | CS[1] | CS[0] | OUT[6] | OUT[5] | OUT[4] | OUT[3] | OUT[2] | OUT[1] | OUT[0] |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |

NS[2] = CS[2]’ CS[1]’ CS[0]’ HS + CS[2]’ CS[1] CS[0]’ FS + CS[2]’ CS[1] CS[0]’ FS’ + CS[2]’ CS[1] CS[0]

= CS[2]’ CS[1]’ CS[0]’ HS + CS[2]’ CS[1] CS[0]’ + CS[2]’ CS[1] CS[0]

= CS[2]’ CS[1]’ CS[0]’ HS + CS[2]’ CS[1]

NS[1] = CS[2]’ CS[1]’ CS[0]’ HS + CS[2]’ CS[1]’ CS[0] + CS[2]’ CS[1] CS[0]’ FS + CS[2] CS[1] CS[0]’ + CS[2] CS[1] CS[0]

= CS[2]’ CS[1]’ CS[0]’ HS + CS[2]’ CS[1] CS[0]’ FS + CS[2]’ CS[1]’ CS[0] + CS[2] CS[1]

NS[0] = CS[2]’ CS[1]’ CS[0]’ HS’ FS + CS[2]’ CS[1]’ CS[0] + CS[2]’ CS[1] CS[0]’ FS + CS[2]’ CS[1] CS[0]’ FS’ + CS[2] CS[1] CS[0]

= CS[2]’ CS[1]’ CS[0]’ HS’ FS + CS[0] (CS[2]’ CS[1]’ + CS[2] CS[1]) + CS[2]’ CS[1] CS[0]’

= CS[2] CS[1]’ CS[0]’ HS’ FS + CS[0] (CS[1] ◉ CS[2]) + CS[2]’ CS[1] CS[0]’

OUT[6] = CS[2]’ CS[1] CS[0] + CS[2] CS[1]’ CS[0]’

OUT[5] = CS[2]’ CS[1]’ CS[0] + CS[2] CS[1]’ CS[0] + CS[2] CS[1] CS[0]’ + CS[2] CS[1] CS[0]

= CS[1]’ CS[0] + CS[2] CS[1]

OUT[4] = CS[2]’ CS[1]’ CS[0]’

OUT[3] = CS[2]’ CS[1] CS[0]’

OUT[2] = CS[2]’ CS[1]’ CS[0]’ + CS[2]’ CS[1]’ CS[0] + CS[2]’ CS[1] CS[0]’ + CS[2] CS[1]’ CS[0] + CS[2] CS[1] CS[0]’ + CS[2] CS[1] CS[0]

= CS[2]’ CS[1]’ + CS[1] CS[0]’ + CS[2] CS[0]

OUT[1] = CS[2] CS[1]’ CS[0]’

OUT[0] = CS[2]’ CS[1] CS[0]

Schematic

Diagram, schematic

Description automatically generated