Course Outline – Computer Architecture

This outline provides an overview of the course and assignments by week. Please remember to check the calendar for specific due dates.

Each course module runs for a period of seven (7) days, i.e., one week. Due dates for readings and other assignments are referred to by the day of the module week in which they are due. For example, if a reading assignment is to be completed by Day 3 and the module started on Monday, then the reading assignment should be completed by Wednesday or the 3rd day of the module.

Module	Dates	Topics	Assignments
Module 1	Mon 01/22/24–Sun 01/28/24	Module 1 Introduction to Computer Architecture	Discussion Forum: MIPS Programming, Get Tools In place Homework: MIPS Assembly Language
Module 2	Mon 01/29/24–Sun 02/04/24	Module 2 Digital Logic Design, Introduction to System Verilog, Verilog and VHDL	Discussion Forum: Lab1 and Lab2, Examination of MIPS Processor, Some Digital Simulation. Hardware debugging via simulation. Homework; Examples of Verilog Code
Module 3	Mon 02/05/24–Sun 02/11/24	Module 3 Computer Arithmetic – Fixed Point	Discussion Forum: Verilog of computer Arithmetic, Simulation of Algorithms Project Ideas Discussion, IC Labs Homework – Fixed Point Computer Arithmetic
Module 4	Mon 02/12/24–Sun 02/18/24	Module 4 Computer Arithmetic – Floating Point	Discussion Forum: Simulation of Floating Point Algorithms, IC Labs Homework, Floating Point Computer Arithmetic
Module 5	Mon 02/19/24–Sun 02/25/24	Module 5 The Processor (CPU and Control Unit) – Single Cycle Processor	Discussion Forum, Examination of execution of instruction Simulations, Interrupt and Exception Experiments, IC Labs, Homework: Processor chapter
Module 6	Mon 02/26/24–Sun 03/03/24	Module 6 The Processor (CPU and Control Unit) – MultiCycle Processor	Discussion Forum: Examination of execution of Instruction Simulation, IC Labs, Homework: Processor Chapter (Possibly from Harris) Project Proposals Due
Module 7	Mon 03/04/24–Sun 03/10/24	Module 7 Pipeline Processing - Hazard Detection	Discussion Forum: Examination of Execution of Instruction Simulation, Adding Instructions to MIPS Design, IC Labs, Homework: Pipeline Processing
Module 8	Mon 03/11/24–Sun 03/24/24	Module 8 Instruction Level Parallelism, FPU Pipeline	Discussion Forum, Examination of Execution of Instruction Simulation, Adding

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			Instructions to MIPS designs (IC Labs), Examination of pipeline in Li Design, Homework: From Text
Module 9	Mon 03/25/24–Sun 03/31/24	Module 9 Memory Subsystems - Cache	Discussion Forum: Examination of Memory Subsystem in Veriog Code, Cache and TLB in Li Pipeline, Homework: From Text, Status Reports/Revision of Proposals due
Module 10	Mon 04/01/24–Sun 04/07/24	Module 10 Memory Subsystems – Virtual Memory	Discussion Forum: Cache Benchmarking. (IC Labs) Homework: From Text
Module 11	Mon 04/08/24–Sun 04/14/24	Module 11 Computer I/O Subsystems	Discussion Forum: I/O Labs (IC Labs) Last Homework Assignment – From Text
Module 12	Mon 04/15/24–Sun 04/21/24	Module 12 Parallel Processing	Discussion Forum: Dual Processor Simulation (Li Design) – Parallel Processing State of the Art Commercial Hardware)
Module 13	Mon 04/22/24–Sun 04/28/24	Module 13 Computer Networks, Clusters and Multiprocessing	Discussion Forum: Cluster Design – (Thought Experiment) Sign up for Presentation Time
Module 14	Mon 04/29/24–Tues 05/07/24	Module 14 Projects Presentations	The presentations will be recorded and then posted on TEAMS, typically 5 students per TEAM. Each student will be expected to provide questions to 5 presentations. Each presentation will be 30 minutes In addition you are expected to ask at least one question of an different TEAM.