Scott Strathman
Assignment 2

1.)

A	B	C	F	G
0	0	0	0	1
0	0	1	1	0
0	1	0	0	1
0	1	1	1	0
1	0	0	0	0
1	0	1	1	0
1	1	0	1	1
1	1	1	1	0

→ Verilog code, test bench, and simulation output picture included in zip file