Module 2: Problem Set A2

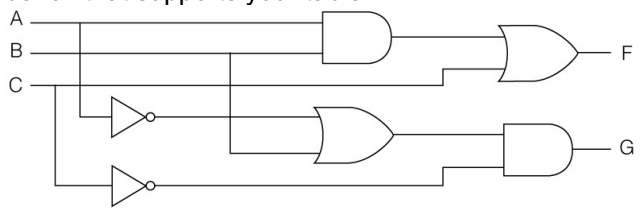
Overview

Summary

This problem set covers Chapter 2 and 3 of the Harris text and uses Vivado with Verilog. These are digital circuit problems that may be trivial review if you have design background. While the problems deal with digital design and can be done by hand, you might find it faster to employ a program like Vivado. Some of the problems may be formulated using a schematic approach or a Verilog Implementation.

Problem Set (Maximum Points 100):

1. Given the following logic circuit, construct a truth table that describes it's behavior. Note, you should solve this by converting to Verilog and running on Vivado. Submit Verilog code and test bench that supports your table.



2. A long list of test benches have been identified from the Li Archive:

    1. encoder8ep_tb.v
    2. mux2x1_dataflow1_tb.v
    3. mux2x1_dataflow2_tb.v
    4. shift_tb.v
    5. d_flip_flop.v
    6. fadder_tb.v
    7. jkff_tb.v
    8. mux2x1_3s_tb.v
    9. shift_mux_tb.v
    10. alu_tb.v
    11. regfile_tb.v
    12. d_ff_tb.v
    13. counter_6_tb.v (Note, this is a subject of a later problem, do not do this one for problem 2)
    14. decoder3e_tb.v
    15. mux2x1_gate_tb.v
    16. add1_tb.v
    17. cla32_tb.v
    18. addsub4_tb.v
    19. time_counter_verilog_tb.v

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Please select 4 of the models to demonstrate (capture waveform via snapshot or PDF) Note, some of these are more interesting than others. I would like you to summarize what each test bench and DUT (Device Under Test) does. These problems were assigned also as a discussion topic. I am included a few of the designs here.

3 Problem A.30 The following K-map is formed incorrectly. Show the reduced equation that is produced by the incorrect map, and then form the K-map correctly, and derive the reduced equation from the correct map. Note that both K-maps will produce functionally correct equations, but only the properly formed K-map will produce a minimized two-level equation.

D \ ABC	000	001	011	010	110	111	101	100
0	1			1	1			1
1	1			1	1			1

4 Counter_6_tb.v is a state machine design. Please analyze this circuit, generate waveforms, and draw the state table. Use Vivado to draw a schematic of the simulation (Hint, run RTL Analysis)

5 Analyze the FSM shown below. Write the state transition and output tables and sketch the state transition diagram. Describe in words what the FSM does. (Note, you could solve this by turning it into a Verilog problem, or you can do it by hand.