The Stampede Architecture: A tool that proved Einstein's General Theory of Relativity (May 2017)

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***Abstract*— This paper discusses a deep understanding of the core architecture behind the Stampede super computer. We explore how the inner workings of the 17th fastest and most robust cluster in the world harnesses processing power to help discover some of the most groundbreaking theories of our time. Through an obscure single simulation on Rochester Institute of Technology's NewHorizons supercomputer, the Stampede was able to reposition its resources to pin point the collision of two blackholes in space. The predictions made about the collision of blackholes based on Einstein's General Theory of Relativity were brought to life after the NewHorizons and Stampede supercomputers leveraged its processing prowess to track the path of the two blackholes and follow them after their collision.**

***Index Terms*— Computational and artificial intelligence, Supercomputers, computer architecture, computer applications, computers, computer performance**

I. Introduction

Supercomputing has become an invaluable asset assisting researchers of all sciences since the creation of Atlas at the University of Manchester in 1962 [1]. Ever since Atlas first designed the relationship between supercomputers and university research projects has been symbiotic. Supercomputers benefit researchers far more than general-purpose computers due to their ability to run simultaneous processes on large sets of data at impeccable speeds. Supercomputers accomplish this by being designed as computer clusters. That is, tightly connected nodes (each with one or multiple processors and some local memory) acting on one shared memory resources. This makes supercomputers extremely adept to handle large-scale simulations with research applications.

One such supercomputer is NewHorizons supercomputer at the Center of Computational Relativity and Gravitation at Rochester Institute of Technology. NewHorizons helped RIT's LIGO researchers to prove the existence of gravitational waves, a hotly debated topic since Albert Einstein proposed their existence in 1916 [2]. NewHorizons, which is a Linux based 736-core computational cluster with a 200 TB storage pool, initially uncovered evidence of gravitational waves but was not powerful enough to conclude the research on its own [3]. The research was then moved over to the Texas Advanced Computing Center at University of Texas Austin where the supercomputer Stampede took over research. Stampede, which NewHorizons architecture was based on, was a more powerful and capable computer that could be used to complete the research. Stampede, which has 522,080 compute nodes and a 14PB storage system, was more capable of handling the four-dimensional computations necessary to prove the existence of gravitational waves [4].

II. Einstein's General Theory of Relativity: Algorithmic Background

Einstein's General Theory of relativity says that what we imagine as force of gravity comes from the curvature of space and time. What this means is that everything in space is relative. It has been long predicted that when two blackholes collide, they continue to form one large blackhole. That prediction was based on the theory of relativity. However, until recently there was no evidence of this happening. Once researchers at LIGO and RIT's CCRG tracked this, the jury is now out. Here we discuss some of the algorithms implemented on the supercomputer that made this discovery possible.

A. The Main Equation

One of the main equations implemented to make the tracking simulations successful was one of the Einstein Field Equations (EFE). The EFE in written form is described in Eq. 1.

$$R_{\mu\nu} - \frac{1}{2} R\, g_{\mu\nu} + \Lambda\, g_{\mu\nu} = \frac{8\pi G}{c^4} T_{\mu\nu} \qquad (1)$$

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The equation is written as a tensor equation which relates to a set of 4x4 symmetric tensors. Initially, this equation was established in 4-dimensions by Einstein, however, scientists have now been able to establish this as n-dimensions. Despite the relatively straight forward appearance of this equation, the equations were formed based off rather complicated theories and understandings relative to time and energy.

B. Simulations and Tests

Using the formula described above along with other data structures, various simulations and tests were run to be able to track the location of the blackholes. Using a software established at the Louisiana State University called Cactus, a lot of trained models were established. Firstly, the Berger-

Fig. 1. Berger-Oliger Time Stepping Algorithm.

Oliger time stepping algorithm was used to help position distance and time to be able to find a proper location of anything emitting gravitational waves. As described in Fig. 1, the Breg-Oliger time stepping delays are shown in the fine grid system. On the left is the time stepping algorithm described and on the right is the fine boundary conditions that are determined via interpolation. The interpolation was implemented in both space and time.

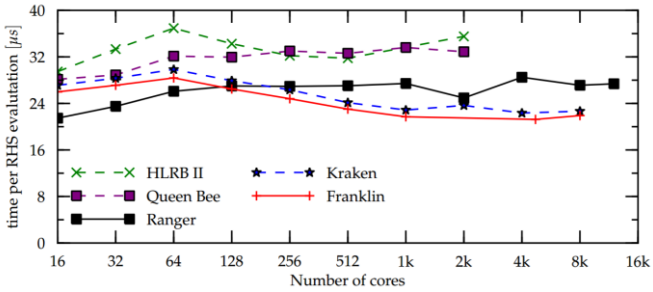


Fig. 2. Results from various testing metrics that proved excellent scalability for the Stampede implementation with an increased number of cores.

Based on the number of cores, a test was run to evaluate the performance of the different cores at different rates. The scale was evaluated to show the required grids per point where smaller numbers are generally defined as better. This shows that the cactus program along with the actual simulations are highly scalable.

C. Coordinate Systems

While running tests and different simulations, there was a huge debate about which coordinate systems were appropriate to be used for testing purposes. Fig. 3. describes appropriately one of the coordinate systems implemented. The first coordinate system implemented involved a TwoPunctures coordinate system for BH-NS binary initial data. This implementation was designed to mimic the traditional Cartesian coordinates while using two different spectrum views to allow greater precision and accuracy when assessing data.

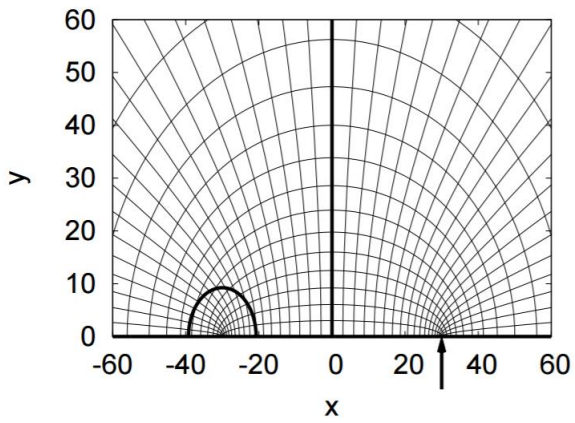


Fig. 3. Scalar tests using Cartesian coordinate system.

The Einstein Toolkit which has a compiled list of various formulas that were implemented when coming up with the simulations. The next vital coordinate system implemented was the Lorene-based binary platform. This coordinate system was four-dimensional and was evaluated respectively. Lorene uses a multigrid approach to solve very thin equations for

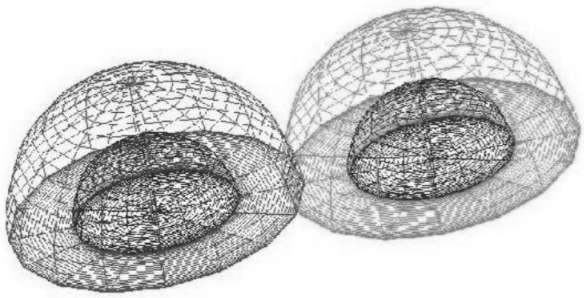


Fig. 4. Lorene multi-domain coordinate system allowing for plotting outside of the regular domain constraints.

binary initial configurations which accounts for all the spatial values being read from the sensors in space. The multi-domain coordinate system is described in the Fig. 4.

As shown specifically in the Lorene multi-domain coordinate system around every object is a set of nested spherical subdomains which extend through space. Within each sphere, there are more angled nested sub-domains which allow for the scientific analysis to span across *n* domains. Conclusively, the scientific studies shown here showcase the idea that the Stampede mechanism comprehensively computed various simulations that span across *n* domains eventually leading to the detection of gravitational waves and proving one of the greatest theories of this century.

III. Contributions of the NewHorizons Architecture

The NewHorizons supercomputer, while not among the most powerful in the world is among the most impactful in the world. In a brief period of existence, the NewHorizons supercomputer has accomplished the unthinkable. It helped track a blackhole that ended up colliding with another blackhole which in turn formed a single blackhole. This discovery goes on to prove what we have been speculating and theorizing about for over

100 years. Einstein first came up with the General Theory of Relativity which implies that blackholes exist and that they emit gravitational waves. Claims were also made that when blackholes collide, they join to form a single, larger blackhole. With the help of NewHorizons simulation tracker, one blackhole was spotted colliding with another blackhole which led to proving Einstein's theory.

A. *Introduction to NewHorizons*

NewHorizons is a Linux-based specialized cluster largely dedicated to federally funded research in numerical relativity computational relativistic astrophysics. It was initially put together in 2007 and has been subsequently updated to match growing needs [3]. The main unit is housed in the Center for Computational Relativity and Gravitation at the Rochester Institute of Technology in Rochester, NY. The cluster is funded by various National Science Foundation awards. Since interdisciplinary research increased, the need for computing power has also increased. Therefore, a new NSF MRI Award was granted to fulfill the respective needs [5].

B. *NewHorizons Technical Specifications*

The NewHorizons computing cluster consists of a comprehensive 736 cores using both AMD and Intel 64-bit 'daily use' CPUs. In addition, it has 2.9TB of RAM and 200TB pipelined storage pool. These specifications allow for mass computation and simulation operations, some of which led to the Einstein discovery [3].

IV. The Stampede Architecture

The National Science Foundation funded the TACC's Stampede system. The cluster was put together in January of 2012. The Stampede cluster includes a whopping 6400+ nodes powered by Intel Xeon E5 Sandy Bridge processors using the newest Many Integrated Core (MIC) architecture. In 2016, there was an update to the Stampede cluster to incorporate Intel's Knights Landing (KNL) system. This upgrade paves the way for Stampede 2 which boasts 508 additional Intel Xeon Phi coprocessors [6].

The Stampede KNL cluster is mostly independent and has a comprehensive Sandy Bridge sub system. It is important to note that the KNL upgrade allows new nodes to the system. The KNL cluster also includes the OmniPath network, which allows for the ability to run Centos 6 and Centos 7 simultaneously to allow interconnections between the Sandy Bridge cluster and the KNL cluster. Interestingly, some of the older modules from the initially declared cluster seamlessly translated over to the new cluster.

Robust networking capabilities allow for users to SSH into either cluster and transition between clusters seamlessly. These ease of access modules allow for hundreds and thousands of simulations to be run simultaneously from different corners of the world making this supercomputer one of the most versatile in the world.

A. *Technical Specifications*

The Stampede supercomputer is heavily technical. With a lot of moving parts, this supercomputer is positioned as a high-risk high-reward computing giant. The Stampede is based on Intel's prominent Many Integrated Core architecture with a comprehensive 462,462 cores. It also boasts 6400 nodes with 205TB of memory and 15.6PB of storage [7].

B. *Architectural Overview*

The unique architecture here is the KNL cluster. The cores are divided up into pairs where each pair takes up a single tile on the actual hardware. Each node of the 6400 accommodates

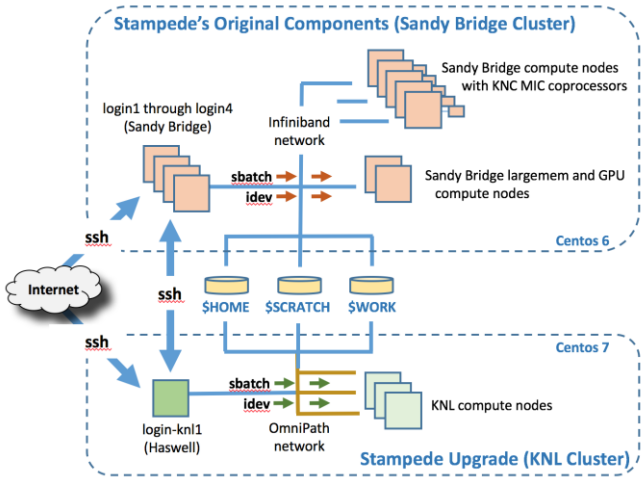


Fig. 3. Stampede's Original Components. An overview of how the Sandy Bridge Cluster allows researchers from all over the world to remotely access the system. Its flexibility allows resources to be shared between different project simultaneously based on what is available and what is demanded.

68 cores giving us 34 active tiles per node. The active tiles are connected by mesh interconnects. The memory is broken up into 8 major memory controllers, 4 for DDR4 RAM and 4 for MCDRAM.

The structure is broken up into 4 quadrants with 2 memory controllers in each quadrant. Each core on every tile has its own local L1 cache with 32KB data and 32KB instruction [8]. There are two 512-bit vector units that are pretty much identical except one of them can execute legacy vector instructions. Each core also runs up to 4 hardware threads. When selecting different cluster modes, L2 and L3 cache are also available for access.

C. *Memory Modes*

Memory modes are extremely valuable in any cluster so memory can be appropriately allocated to optimize various performance metrics within the system. The memory modes also determine whether the MCDRAM operates as RAM, direct-mapped L3 cache or as a mix of both.

There are 3 major memory modes that the abstraction layer can select from. The first is cache mode. In cache mode, MCDRAM is configured as L3 cache and the operating system transparently accesses MCDRAM to move data from memory. Additionally, the user has full access to the 96GB offered by the DDR4 RAM. The next mode is flat mode. In flat mode, DDR4 and MCDRAM act as two distinct Non-Uniform Memory Access (NUMA) nodes. Therefore, in this mode the user could allocate which memory to select when allocating memory. The user gets full access to 112GB of RAM, 96GB from DDR4 and

16GB from MCDRAM [9]. As a rule of thumb, the abstraction

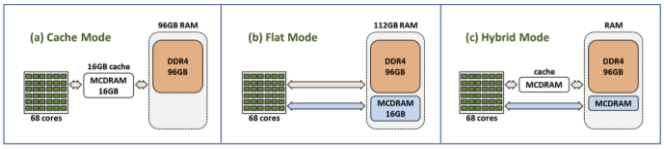


Fig. 4. The different memory modes present within Stampede. The different modes allow the user to have a different amount of control on how the memory is stored.

layer does memory allocation
in DDR4 so to use MCDRAM in this mode, the user must specify it while allocating memory. The last mode is hybrid mode. In hybrid mode, MCDRAM is configured so that part of it acts like L3 cache while the rest serves as regular RAM. Unfortunately, this mode is not actually supported on the Stampede cluster. In addition to all the memory modes, Stampede also supports 3 cluster modes.

D. Cluster Modes

A supercomputer cluster can be configured in several ways. Usually, two to three most optimal ways are selected so the most optimal modes are available for as many users as possible. Through the L1 and L2 cache access provided by the memory modes, time can be reduced to access data. However, to safely share memory, mechanisms to ensure and enhance a coherent transition of data exists [10]. To have a cache coherent system means that all cores have a consistent view of the data and with multi-core processors this goal becomes increasingly difficult.

While the details for KNLs cluster modes are proprietary, the general idea was published for educational purposes. Essentially, each tile tracks a given range of memory addresses. The tile tracks the addresses on behalf of the core so there is a

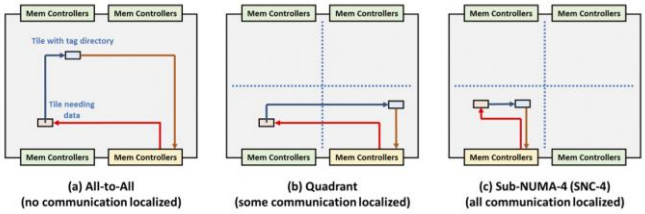


Fig. 5. Stampede's original components in the Sandy Bridge configuration compared to Stampede's upgrade in the KNL cluster. Both can be accessed in the same way using ssh and an internet connection.

map that serves as a tag directory for each address to tile. There is tile-to-tile and tile-to-memory communication as per the coherence principle. If a core manipulates or modifies data, it communicates with the map to update the data on their respective tile.

Additionally, when cores need data from memory, the tiles do the communication on behalf of the cores and prepare the data for usage [10]. There are several ways to accomplish those goals. This cluster selects three major ways as showcased in fig. 5. The first cluster mode is All-to-All. What this means is simply that this mode provides the most flexibility and is relatively general. It is intended to work with all kinds of hardware and has higher latency thus lower optimization. To use an analogy, imagine this as the Java programming language where there is an abstraction layer that accommodates all the memory allocation, reducing development time but also reducing optimization. The second mode is called Quadrant mode. Most engineers and Intel recommends this mode as well. In this mode, communication between memory nodes is localized without using explicit memory management from the user. What the abstraction layer does is it groups tiles into virtual quadrants, requiring each quadrant to manage its own memory. This reduces the number of hops from tile to memory

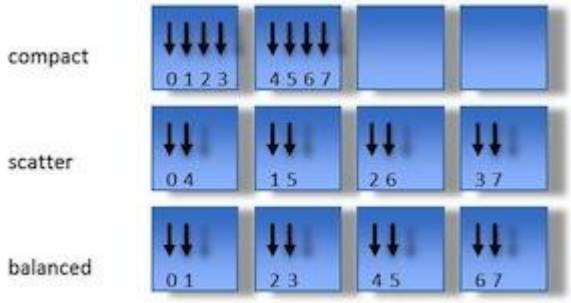


Fig. 6. This figure describes the parallel architecture counting system to Stampede's. This counting mechanism was established in Intel's system as the stock counting mechanism for clusters.

which leads to the reduction of latency and congestion on the interconnects. Lastly, the Sub-NUMA 4 (SNC4) mode is accessible. SNC4 divides the chip into 4 NUMA modes so it works like a four-socket processor. This mode requires manual memory management from the user. While there is a lot of control in this mode and it increases memory optimization, it also increases development time a great amount. This mode is not recommended for quick implementations.

The Stampede has slowly deviated from Intel's standard MIC mode and implemented these three modes to increase the usability of the supercomputer. The cache-quadrant model seems to be a very popular choice among engineers and is also the most efficient for a lot of the workflows. While there are significant performance differences across the different modes, it really comes down to what the need of a certain project or simulation is at any given time. The best decision is made based on numerous factors such as time, simulation quality, result precision and so forth.

E. Memory Management

Memory management can be the most useful but also the most tedious portion of computing. Fortunately, Stampede has cluster modes where all the memory management is automated but also has a mode that allows users full control to manage memory. By design, any application can run in any cluster mode. However, there are always instances where little amounts of custom memory management greatly impact performance. Stampede's team has determined certain best practices and litmus tests to see if custom memory management is worthwhile. Firstly, it's not a clever idea to run all 272 hardware threads at the same time.
The safe testing metric lies between 64-68 threads at any given time. The next metric when testing performance while comparing KNL to traditional processors is to do a node-to-node analysis instead of a core-to-core analysis. Since KNL runs at lower frequencies than traditional processors, the fixed

```
numactl       --membind=0   ./a.out   # launch a.out (non-MPI); use DDR (default)
ibrun numactl --membind=0   ./a.out   # launch a.out (MPI-based); use DDR (default)
numactl       --membind=1   ./a.out   # use only MCDRAM
numactl       --preferred=1 ./a.out   # use MCDRAM if possible; else DDR
numactl       --hardware              # show numactl settings
numactl       --help                  # list available numactl options
```

Fig. 7. The differing memory controllers present in Stampede. Each one allows the user to have a different amount of control over where memory is stored.

number of tasks per thread runs slower on KNL. Therefore, testing core vs core performance does not provide an accurate measure of the KNL's capabilities. Next, there are general expectation guidelines set by Stampede engineers as to what you would expect when running certain applications [11].
From a hardware perspective, Stampede's single KNL mode provides 6x performance compared to dual socket SandyBridge nodes. Of course, this is under the assumption that the peripheral modules are running at the best of their abilities and that all memory is well optimized [11]. Conclusively, while memory management is a vital part of implementing applications on Stampede, the Stampede infrastructure is well developed to the extent that using one of its automated modes should provide impressive results.

V. Improvements in Supercomputing Since Stampede

A. Improvements to Stampede

Ever since the TACC began production of Stampede on January 7th, 2013 there has been leaps of progress in computing and supercomputing technology. The organization Top500 compiles a biannual report on the Top500 most powerful supercomputers. From looking at the list since Stampede was first included in June 2013 it's evident that supercomputing technology is increasing at an exponential rate. When Stampede was first added to the Top500 list it debuted as the seventh most powerful supercomputer in the world [6]. As of the most recent list in November 2016 Stampede dropped to the seventeenth spot. Over the last four years ten supercomputers more powerful than stampede were added to the list. This is also because Stampede was improved in 2016 by adding additional compute nodes built around second generation of Intel Xeon Phi processors. These processors are much more powerful than the first generation Xeon Phi processors original in Stampede. Had this upgrade been listed separately to Stampede on the Top500 list it would have placed at #117. This truly shows the increase in supercomputing despite these improvements in Stampede it has still drop ten spots in the rankings over a period of four years.

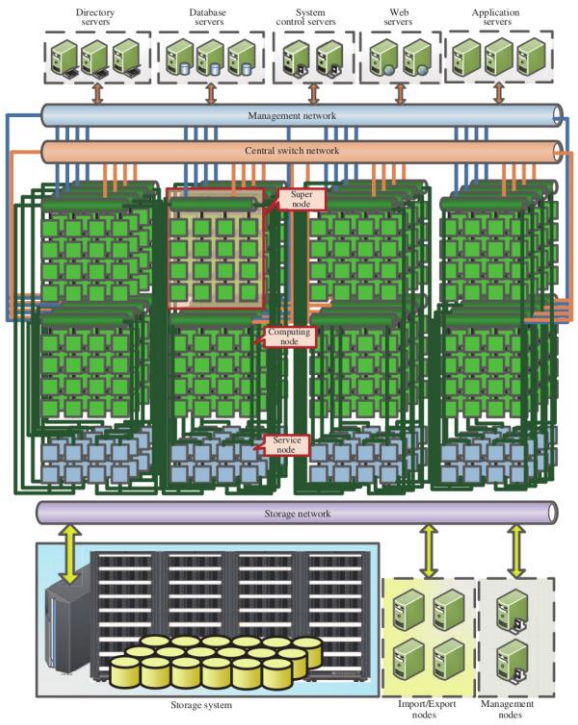
B. Improvements at TACC

In addition to Stampede the TACC boasts a total of twenty supercomputing clusters. Since Stampede the TACC has built two noteworthy supercomputers. The Lonestar 5 [12] and the Stampede 2 [13]. On January 12th 2016 the University of Austin announced their second petaflop system, Lone Star 5, was completed. It was developed to be shared amongst researchers at fourteen Universities of Texas. Although state of the art Lonestar 5 is not nearly as powerful Stampede. Lonestar 5 only has a total of 30,048 cores compared to Stampede's 462,462 cores [15]. The real improvement over Stampede is that Lonestar 5 exclusively uses the second generation Intel Xeon Phi processors that had to be added to Stampede after intial built. The Lonestar 5 does boast a 5 TB state of the art DataDirect storage system. At its highest rating it reached #78 on the Top500 list in a prescreening in November 2015. As of November 2016 Stampede 5 has dropped to the #109 spot on the Top500 list, once again showing the impressive improvements in supercomputing in just the last year.

The true advancement the TACC computing systems, Stampede 2, is debuting in the summer of 2017. The system will not be replacing Stampede but instead will be working alongside Stampede [16]. Exact specifications of the system are not known at this time however it is known that the system will employ Intel "Knights Landing" Xeon Phi processors each of which have 72 cores and three teraflops per processor. As of right now it's estimated that Stampede 2 will be using 6,000 such chips [17]. In addition to this Stampede 2 will double memory, storage capacity, and system bandwidth of its predecessor. Using this technology and Intel's new Omni-Path interconnect to connect the nodes. The Omni-Path system will allow for 100 GBps of inter-server bandwidth, which is a huge upgrade over Stampede's 52 GBps of inter-server bandwidth. The overall project is estimated to cost $30 million. Stampede 2 promises to be a huge upgrade over Stampede and is sure to place in the top ten of the Top500 list.

C. Supercomputing in the U.S. and P.R.C.

In terms of the top supercomputing technology in the world the United States and the People's Republic of China lead the way. As of the most recent Top500 list, which was compiled in November 2016, the US and China each have a total of 171 systems in the top 500. This essentially means that each country have almost one-third of the total supercomputers in the world. By comparison Germany, the third place leader, only has a total of 32 systems on the list. The driving force between the American and Chinese domination in supercomputing technology comes from public funding. The two nations appear locked in a Cold War space race of sorts in supercomputing at the moment. The practical application in both university research and military prowess pushes each country to outdo each other year after year. Since Stampede's debut and fall from the number seven spot the Chinese have taken the number one and two spots on the Top500 list. Currently the top supercomputer in the world is Sunway TaihuLight in the National Supercomputing Center in Wuxi, China [18]. Not much is known about the system due to restrictions in the Chinese press and the Chinese being apprehensive of sharing their supercomputing technology with the Western world. There are some aspects, which are known, for instance the system uses the Sunway SW26010 Architecture [19].



As seen in Fig. 8., the general Sunway architecture uses a series of super nodes, computing nodes, and service nodes connected to interact with storage systems and a plethora of servers. Although exact details of Chinese supercomputers are not known it can be inferred that they are not far off from their Western counterparts.

What is known of the Sunway architecture and Sunway TaihuLight is simply a broad overview. Sunway TaihuLight has 10,649,600 CPU cores. The high number of cores is achieved by using 40,960 SW26010 manycore 64-bit RISC processors. Each one of these processors contains 265 processor cores as well as some system management cores. The benefit of these SW26010 processors over their Western counterparts is the increased ability of parallel processing due to the large number of independent processor cores. In addition to this the processing cores each have 64KB of scratch pad memory instead of a traditional cache hierarchy. The scratchpad memory is essentially a local RAM for the processor. Thus reducing the amount of time needed to access RAM for temporary calculations.

The most widely kept secrets about TaihuLight is its software. Almost nothing is known about its custom operating system, Sunway RaiseOS 2.0.5, other than it's based off of Linux. What is known is that it uses its own customized version of OpenACC 2.0. Developed by Cray, OpenACC, is a programming standard written in C, C++, and Fortran. The software is a high-speed algorithm to simplify parallel computing among manycore architectures. With its abundance of processing cores, TaihuLight makes great use of algorithm helping to increase parallelism.

As of right now no new systems capable of supplanting Sunway TaihuLight are planned to be unveiled by the June 2017 Top500 list. Advancement is happening though. Its estimated that the title of world fastest computer will belong to Summit at the Oak Ridge National Laboratory in Oak Ridge, Tennessee [20]. Although not nearly as powerful as TaihuLight, or any of the most powerful computers, the system will the first of its kind in node-level parallelism [21]. The technology used in Summit will surely be used and built upon in future supercomputers. This year will also be the first time India, an emerging global superpower, will be added to the list [22]. Their new system, Param, will be a 4,500 core system propelling India onto the global stage of supercomputing. In addition to this India's National Super Computing Mission aims to build 80 supercomputers in the next seven years. As the technology behind the America and China's dominance becomes more widely known and available it can be expected that more advanced nations will join the list.

VI. Conclusion

Supercomputing is an asset to researchers of all sciences. What makes a supercomputer so adept for research is their ability to run simultaneous processes on large sets of data at impeccable speeds. Supercomputers accomplish this by interconnecting computing cores which each contain processors and local memory. Each on of these cores act simultaneously on one shared memory resource. This make supercomputers extremely adept to handle large scale simulations with research applications. One application is relativity and gravitation research, for which Rochester Institute of Technology's Center of Computational Relativity developed the NewHorizons supercomputer.

The cluster was designed based off the existing Sandy Bridge cluster design and the Texas Advanced Computing Center at University of Texas Austin's Stampede supercomputer. Using these two clusters researchers have been able to prove the existence of gravitational waves which is being referred to as one of the greatest scientific discoveries of the last century. This is just one of the many applications Stampede and comparable supercomputers are currently working on.

With the advancements of supercomputing over the last 50 years, particularly in the United States of America and the People's Republic of China, the applications and possibilities of supercomputing seem limitless. The worlds most powerful Supercomputer, Sunway TaihuLight, is currently shattering expectations of what supercomputers are capable of. Competition between the two nations is driving supercomputing advancement at an exponentially speed.

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John J. Judge was born in Pearl River, NY, in 1996. He graduated from Pearl River High School with honors in June of 2014. He is currently in his third year of study at the Kate Gleason College of Engineering at Rochester Institute of Technology in Rochester, NY. He plans on graduating in May of 2019 with a Bachelors of Science in Computer Engineering. In this time he is also pursuing a minor in Economics

He is working for Architecture Technology Corporation in Ithaca, NY from May 2017 to January of 2018. He will be working on both low-level I/O applications as well as software design. His qualifications include hardware design as well as low-level design protocol. In his personal time he devotes himself to projects that include digital system design as well as instruction set architectures that can run on the projects. These projects include an 8-bit MIPS personal computer and microcontroller programming.

Suhail Prasathong was born in Bangkok, Thailand in 1995. He is pursuing a B.S. degree in Computer Engineering at the Kate Gleason College of Engineering from the Rochester Institute of Technology, Rochester, 2013-2018. Throughout his experience at RIT, he has worked towards achieving a comprehensive understanding of algorithms, data structures, lower and higher level programming, computer architectures, digital signals and so forth. Prasathong's main field of interest is Machine Learning where he intends to pursue a senior design capstone project that uses machine learning models to recognize objects and translate them to different languages. His expertise in higher and lower level programming provides him a good platform to pursue projects in the machine learning space.

In his time at RIT, Mr. Prasathong has acquired 3 co-op opportunities at Kodak Alaris, PayPal Inc. and Deutsche Bank's machine learning team respectively. Through the co-op program at Rochester Institute of Technology, Mr. Pasathong has had the opportunity to apply the skills acquired through academics. Taking full advantage of the program, Mr. Prasathong was able to leverage his academic learning complemented with industry experience to his advantage.