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OF ITU

G.726

Appendix II
Test Vectors
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SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Digital transmission systems – Terminal equipments – Coding of analogue signals by methods other than PCM

Description of the digital test sequences for the verification of the G.726 40, 32, 24 and 16 kbit/s ADPCM algorithm

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DESCRIPTION OF THE DIGITAL TEST SEQUENCES FOR THE VERIFICATION OF THE G.726 40, 32, 24 AND 16 KBIT/S ADPCM ALGORITHM

1 Introduction

This guide describes the test sequences (vectors) for the ADPCM algorithms of Recommendation G.726 at the four fixed bit rates (16 kbit/s, 24 kbit/s, 32 kbit/s, 40 kbit/s) for both A-law and μ-law. It reproduces mainly the text of the CCITT collective letter No. 11/XV, dated 21/03/1991, the only amendments corresponding to the grouping on two 3½" disks of the files which were previously on four 5¼" disks.

The tests are arranged in two separate diskettes, one for the μ-law and one for the A-law. For each law, the diskette contains the reset test vectors and the homing test vectors. The diskettes are of the 3½ MS-DOS format[1]. Within each diskette, the files are distributed in subdirectories that correspond to individual bit rates for the homing and reset case. A READ.ME file lists the contents of each diskette.

2 General description

The verification testing procedure consists in applying an input sequence to an ADPCM implementation and verifying that the output sequence is the same sequence in the output file for the same test conditions (PCM coding law, type of input, initial state of the implementation).

There are three types of input sequences. The first type consists of various sinusoidal PCM inputs that are representative of the signals expected in normal operation. These are called "normal inputs". A second group of input sequences is the set of "overload inputs" that contain PCM signals of very large amplitudes. The third group is the set of ADPCM sequences that can exercise the algorithm in a manner that is not possible with any PCM input sequence. They test the arithmetic and algorithmic performance of the ADPCM decoder by driving it to states that are unreachable by PCM signals under normal conditions. For example, these states may result from errors on the transmission line. These intermediate sequences will be denoted as "I-inputs".

The values (or samples) contained in a test file are given in ASCII hexadecimal representation with two hexadecimal characters per 8-bit value. In files with 5-bit ADPCM values, the three most significant bits are set to 0. Files containing 4-bit ADPCM values have the four most significant bits or each value set to 0. Files that contain 3-bit ADPCM values have the five most significant bits of each word set to 0. For files containing 2-bit ADPCM values, the six most significant bits are set to 0. All PCM A-law inputs are in the format specified by Table 1a/G.711, i.e. the even bits are inverted.

Each line in any file contains up to 32 values (or 64 characters) and ends with a line feed character. Two more hexadecimal characters representing the result of a checksum computation over the entire file are appended to each file. This checksum is the remainder of the division of 255 of the sum of all sample values (two hexadecimal characters comprise a sample value) in the file.

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[1] It has been noted that these diskettes do not always copy correctly using DISKCOPY due to the interaction of DISKCOPY with certain character sequences found in the test sequences. Either files should be copied individually using COPY, or XCOPY should be used instead of DISKCOPY.

3 Test configurations

Test sequences are derived for the two configurations shown in Figures 1 and 2, respectively. The configuration of Figure 1 is the arrangement with the encoder transmitting to the decoder for error-free operation. The configuration of Figure 2 allows for input ADPCM words that would not normally emanate from an encoder and a PCM input word. The word formats of the various sequences are detailed in Table 1.

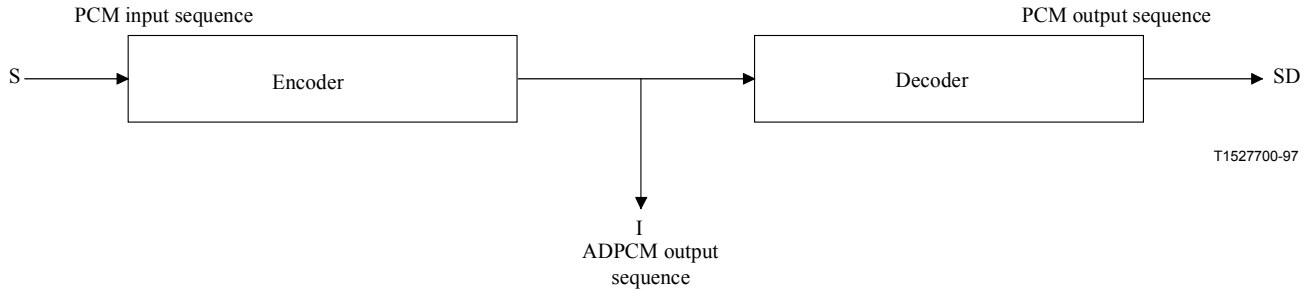

Figure 1 – Encoder and decoder configuration

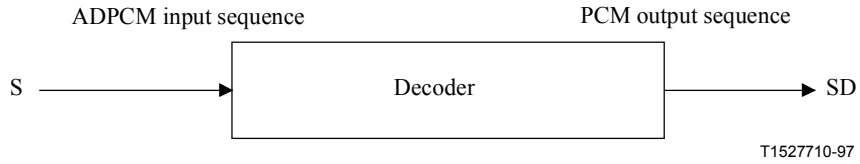

Figure 2 – Decoder only configuration

Table 1 – Word format of test sequences

Name	Description	Word format
S	PCM input word	Identical to that of SP described in the sub-block COMPRESS of the synchronous coding adjuster (4.2.8/G.726).
I	ADPCM word	As specified in the sub-block RECONST of the inverse adaptive quantizer (4.2.3/G.726).
SD	PCM output word	Identical to that of SP described in the sub-block COMPRESS (4.2.8/G.726).

4 Test combinations

The initial state of the implementation may be either the reset state of the algorithm defined in Table 2 or a well-defined initial state that follows the application of an initialization (or homing) sequence. Accordingly, there are two types of test sequences, reset sequences and homing sequences.

Table 2 – State values at reset

Variable	Value
A_1, A_2	0
B_1, ..., B_6	0
DQ_1, ..., DQ_6	32
PK_1, PK_2	0
SR_1, SR_2	32
TD	0
YL	34 816
YU	544

The homing sequences are based on the initial states that follow the application of an initialization (homing) sequence. These initialization sequences are described in further detail in 6.4.

For each initial state, both PCM laws (A-law and μ-law) are considered. To allow for the interoperation of both PCM laws, four possible input/output combinations must be considered as shown in Table 3.

Table 3 – Input/output combinations

Input	Output
A-law	A-law
μ-law	μ-law
A-law	μ-law
μ-law	A-law

5 Test organization

Tables 4 to 7 contain the names of files containing various reset/homing sequences for the following cases:

1) μ-law;
2) A-law;
3) $\mu \rightarrow$ A; and
4) A $\rightarrow \mu$.

Files whose names start with an "R" contain reset sequences while the names of files for the homing sequences start with an "H". The suffix ".I" is reserved for the intermediate ADPCM encoder response to a PCM input. Files with the suffix ".O" are the output PCM files.

Table 4 – Reset and homing sequences for μ-law

Algorithm	Normal			I-input		Overload		
	Input (PCM)	Intermediate (ADPCM)	Output (PCM)	Input (ADPCM)	Output (PCM)	Input (PCM)	Intermediate (ADPCM)	Output (PCM)
16F	NRM.M	RN16FM.I HN16FM.I	RN16FM.O HN16FM.O	I16	RI16FM.O HI16FM.O	OVR.M	RV16FM.I HV16FM.I	RV16FM.O HV16FM.O

24F	NRM.M	RN24FM.I HN24FM.I	RN24FM.O HN24FM.O	I24	RI24FM.O HI24FM.O	OVR.M	RV24FM.I HV24FM.I	RV24FM.O HV24FM.O
32F	NRM.M	RN32FM.I HN32FM.I	RN32FM.O HN32FM.O	I32	RI32FM.O HI32FM.O	OVR.M	RV32FM.I HV32FM.I	RV32FM.O HV32FM.O
40F	NRM.M	RN40FM.I HN40FM.I	RN40FM.O HN40FM.O	I40	RI40FM.O HI40FM.O	OVR.M	RV40FM.I HV40FM.I	RV40FM.O HV40FM.O

Table 5 – Reset and homing sequences for A-law

Algorithm	Normal			I-input		Overload		
	Input (PCM)	Intermediate (ADPCM)	Output (PCM)	Input (ADPCM)	Output (PCM)	Input (PCM)	Intermediate (ADPCM)	Output (PCM)
16F	NRM.A	RN16FA.I HN16FA.I	RN16FA.O HN16FA.O	I16	RI16FA.O HI16FA.O	OVR.A	RV16FA.I HV16FA.I	RV16FA.O HV16FA.O
24F	NRM.A	RN24FA.I HN24FA.I	RN24FA.O HN24FA.O	I24	RI24FA.O HI24FA.O	OVR.A	RV24FA.I HV24FA.I	RV24FA.O HV24FA.O
32F	NRM.A	RN32FA.I HN32FA.I	RN32FA.O HN32FA.O	I32	RI32FA.O HI32FA.O	OVR.A	RV32FA.I HV32FA.I	RV32FA.O HV32FA.O
40F	NRM.A	RN40FA.I HN40FA.I	RN40FA.O HN40FA.O	I40	RI40FA.O HI40FA.O	OVR.A	RV40FA.I HV40FA.I	RV40FA.O HV40FA.O

Table 6 – Reset and homing cross sequences for μ → A

Algorithm	Normal			Overload		
	Input (PCM)	Intermediate (ADPCM)	Output (PCM)	Input (PCM)	Intermediate (ADPCM)	Output (PCM)
16F	NRM.M	RN16FM.I HN16FM.I	RN16FC.O HN16FC.O	OVR.M	RV16FM.I HV16FM.I	RV16FC.O HV16FC.O
24F	NRM.M	RN24FM.I HN24FM.I	RN24FC.O HN24FC.O	OVR.M	RV24FM.I HV24FM.I	RV24FC.O HV24FC.O
32F	NRM.M	RN32FM.I HN32FM.I	RN32FC.O HN32FC.O	OVR.M	RV32FM.I HV32FM.I	RV32FC.O HV32FC.O
40F	NRM.M	RN40FM.I HN40FM.I	RN40FC.O HN40FC.O	OVR.M	RV40FM.I HV40FM.I	RV40FC.O HV40FC.O

Table 7 – Reset and homing cross sequences for A → μ

Algorithm	Normal			Overload		
	Input (PCM)	Intermediate (ADPCM)	Output (PCM)	Input (PCM)	Intermediate (ADPCM)	Output (PCM)
16F	NRM.A	RN16FA.I HN16FA.I	RN16FX.O HN16FX.O	OVR.A	RV16FA.I HV16FA.I	RV16FX.O HV16FX.O
24F	NRM.A	RN24FA.I HN24FA.I	RN24FX.O HN24FX.O	OVR.A	RV24FA.I HV24FA.I	RV24FX.O HV24FX.O
32F	NRM.A	RN32FA.I HN32FA.I	RN32FX.O HN32FX.O	OVR.A	RV32FA.I HV32FA.I	RV32FX.O HV32FX.O
40F	NRM.A	RN40FA.I HN40FA.I	RN40FX.O HN40FX.O	OVR.A	RV40FA.I HV40FA.I	RV40FX.O HV40FX.O

5.1 Reset test sequences

The test sequences that are available when the initial state of the algorithm in the reset state are:

1) μ-law (A-law) PCM encoder input sequences for normal operation: NRM.M and NRM.A.
2) ADPCM encoder output sequences corresponding to the input in 1) and for the various rates: RN16FM.I, RN16FA.I, RN24FM.I, RN24FA.I, RN32FM.I, RN32FA.I, RN40FM.I and RN40FA.I.
3) μ-law (A-law) PCM decoder output sequences corresponding to the ADPCM input in 2): RN16FM.O, RN16FA.O, RN24FM.O, RN24FA.O, RN32FM.O, RN32FA.O, RN40FM.O and RN40FA.O.
4) ADPCM intermediate sequences that are applied to the decoder: I16., I24, I32 and I40.
5) μ-law (A-law PCM) output sequence corresponding to the I-input ADPCM decoder input in 4): RI16FM.O, RI16FA.O, RI24FM.O, RI24FA.O, RI32FM.O, RI32FA.O, RI40FM.O and RI40FA.O.
6) μ-law (A-law) PCM encoder input sequence for overload conditions: OVR.M and OVR.A.
7) ADPCM encoder output sequence in response to the input in 6): RV16FM.I, RV16FA.I, RV24FM.I, RV24FA.I, RV32FM.I, RV32FA.I, RV40FM.I and RV40FA.I.
8) μ-law (A-law) PCM output sequence corresponding to the ADPCM encoder output in 7): RV16FM.O, RV16FA.O, RV24FM.O, RV24FA.O, RV32FM.O, RV32FA.O, RV40FM.O and RV40FA.O.
9) The $\mu \rightarrow A$ and $A \rightarrow \mu$ cross test sequences for the normal and overload cases: RN16FC.O, RV16FC.O, RN24FC.O, RV24FC.O, RN32FC.O, RV32FC.O, RN40FC.O, RV40FC.O, RN16FX.O, RV16FX.O, RN24FX.O, RV24FX.O, RN32FX.O, RV32FX.O, RN40FX.O and RV40FX.O.

5.2 Homing test sequences

The test sequences in this are:

1) Initialization (homing) sequence to drive the implementation to a known initial state: PCM_INIT.M for the μ-law and PCM_INIT.A for the A-law.
2) μ-law (A-law) PCM encoder input sequence for normal operation starting from this normal state: NRM.M and NRM.A.
3) ADPCM encoder output sequence corresponding to the input in 2): HN16FM.I, HN16FA.I, HN24FM.I, HN24FA.I, HN32FM.I, HN32FA.I, HN40FM.I and HN40FA.I.
4) μ-law (A-law) PCM decoder output sequence corresponding to the ADPCM encoder output in 3): HN16FM.O, HN16FA.O, HN24FM.O, HN24FA.O, HN32FM.O, HN32FA.O, HN40FM.O and HN40FA.O.
5) ADPCM initialization sequence for I-input operation: I_INI_16.M, I_INI_24.M, I_INI_32.M, and I_INI_40.M for μ-law; I_INI_16.A, I_INI_24.A, I_INI_32.A and I_INI_40.A for A-law.
6) μ-law (A-law PCM) output sequence corresponding to the I-input ADPCM decoder input in 5): HI16FM.O, HI16FA.O, HI24FM.O, HI24FA.O, HI32FM.O, HI32FA.O, HI40FM.O and HI40FA.O.
7) μ-law (A-law) PCM encoder input sequence for overload conditions: OVR.M and OVR.A.
8) ADPCM encoder output sequence corresponding to the input in 7): HV16FM.O, HV16FA.O, HV24FM.O, HV24FA.O, HV32FM.O, HV32FA.O, HV40FM.O and HV40FA.O.

9) μ-law (A-law) PCM output sequence corresponding to the ADPCM sequence in 8): HV16FM.O, HV16FA.O, HV24FM.O, HV24FA.O, HV32FM.O, HV32FA.O, HV40FM.O and HV40FA.O.

10) The μ → A and A → μ cross test sequences for the normal and overload cases: HN16FC.O, HV16FC.O, HN24FC.O, HV24FC.O, HN32FC.O, HV32FC.O, HN40FC.O, HV40FC.O, HN16FX.O, HV16FX.O, HN24FX.O, HV24FX.O, HN32FX.O, HV32FX.O, HN40FX.O, and HV40FX.O.

6 Description of the input sequences

6.1 PCM normal input

The PCM normal input sequences consist of 16 384 values that represent narrow-band and broadband signal sequences as detailed in Table 8. NRM.M is the PCM normal μ-law input sequence while NRM.A is the corresponding A-law input sequence.

Table 8 – Sequence of PCM test signal

Signal	Length
3504 Hz tone	1 024
2054 Hz tone	1 024
1504 Hz tone	1 024
504 Hz tone	1 024
254 Hz tone	1 024
1254 Hz tone	1 024
2254 Hz tone	1 024
3254 Hz tone	1 024
4000 Hz tone	512
DC, positive, low level	512
DC, value of zero	512
DC, negative, low level	512
4800 bit/s differential phase shift keyed voice-band data switched carrier	3 072
4800 bit/s differential phase shift keyed voice-band data continuous carrier (with asynchronous switched carrier secondary channel)	3 072
Total length of sequence	16 384

6.2 PCM overload input

The PCM overload input sequences have 2048 values from three high level (> +1 dBm0) single frequency tones at 404, 1004 and 3204 Hz arranged in various combinations and for differing intervals. The sequence is generated digitally without analogue filtering but with the +3 dBm0 overload point enforced. OVR.M is the PCM overload μ-law input sequence while OVR.A is the corresponding A-law sequence. Both sequences contain 2048 samples.

6.3 ADPCM input

The ADPCM input sequence is a combination of a sign bit sequence and a sequence of 2-, 3- or 4-bit magnitudes respectively for operation at 16, 24, 32 and 40 kbit/s. These input sequences are denoted as I16, I24, I32 and I40 respectively. The sign bit sequence consists of eight subsequences, each of length 2048 as follows:

1) + + + + + + + + ...

2) + + + + − − − − + + + + − − − − ...

3) − − + − − + − − + ...

4) + + − − + + − − ...

5) + + − − − + + − − − ...

6) − − − − − + − + − − − − − + − + ...

7) − − + − + − − + − + ...

8) + − + − + − ...

The magnitude sequence for 32 kbit/s consists of 27 concatenated subsequences of various lengths as detailed in Table 9 (the values are shown in decimal integer form).

Table 9 – Sequence of I-input value magnitudes for 32 kbit/s

Repetitive pattern	Length
00000	1 024
Alternating sixteen 0s sixteen 1s	512
11111	512
Alternating sixteen 1s sixteen 2s	512
22222	512
Alternating sixteen 2s sixteen 3s	256
33333	1 024
Alternating sixteen 3s sixteen 4s	512
44444	512
Alternating sixteen 4s sixteen 5s	512
55555	512
Alternating sixteen 5s sixteen 6s	256
66666	1 024
Alternating sixteen 6s sixteen 7s	256
77777	1 024
66666	1 024
55555	1 024
Alternating sixteen 5s sixteen 4s	512
Alternating sixteen 4s sixteen 3s	512
33333	512
22222	1 024
Alternating sixteen 2s sixteen 1s	512
Alternating sixteen 1s sixteen 0s	512
00000	1 024
Alternating sixteen 5s sixteen 7s	256
Alternating sixteen 2s sixteen 7s	256
Alternating sixteen 1s sixteen 6s	256
Total length of sequence	16 384

Table 10 contains the magnitude sequence for 40 kbit/s which is obtained from the one for 32 kbit/s through a left shift of one bit position.

Table 10 – Sequence of I-input value magnitudes for 40 kbit/s

Repetitive pattern	Length
00000	1 024
Alternating sixteen 0s sixteen 2s	512
22222	512
Alternating sixteen 2s sixteen 4s	512
44444	512
Alternating sixteen 4s sixteen 6s	256
66666	1 024
Alternating sixteen 6s sixteen 8s	512
88888	512
Alternating sixteen 8s sixteen 10s	512
1010101010	512
Alternating sixteen 10s sixteen 12s	256
1212121212	1 024
Alternating sixteen 12s sixteen 14s	256
1414141414	1 024
1212121212	1 024
1010101010.....	1 024
Alternating sixteen 10s sixteen 8s	512
Alternating sixteen 8s sixteen 6s	512
66666	512
44444	1 024
Alternating sixteen 4s sixteen 2s	512
Alternating sixteen 2s sixteen 0s	512
00000	1 024
Alternating sixteen 10s sixteen 14s	256
Alternating sixteen 4s sixteen 14s	256
Alternating sixteen 2s sixteen 12s	256
Total length of sequence	16 384

Similarly, the magnitude sequence for 24 kbit/s is derived from its counterpart at 32 kbit/s through a right shift of one bit position. Table 11 contains the resulting sequence of values.

Table 11 – Sequence of I-input value magnitudes for 24 kbit/s

Repetitive pattern	Length
00000	2 048
Alternating sixteen 0s sixteen 1s	512
11111	1 792
Alternating sixteen 1s sixteen 2s	512
22222	1 536
Alternating sixteen 2s sixteen 3s	256
33333	3 328
22222	1 536
Alternating sixteen 2s sixteen 1s	512
11111	1 536
Alternating sixteen 1s sixteen 0s	512
00000	1 536
Alternating sixteen 2s sixteen 3s	256
Alternating sixteen 1s sixteen 3s	256
Alternating sixteen 0s sixteen 3s	256
Total length of sequence	16 384

Finally, the magnitude sequence for 16 kbit/s is derived from the sequence at 32 kbit/s by shifting to the right for two bit positions. Table 12 displays the corresponding sequence of values.

Table 12 – Sequence of I value magnitudes for 16 kbit/s

Repetitive pattern	Length
00000	4 352
Alternating sixteen 0s sixteen 1s	512
11111	6 656
Alternating sixteen 1s sixteen 0s	512
00000	3 584
11111	256
Alternating sixteen 0s sixteen 1s	512
Total length of sequence	16 384

6.4 Initialization sequences

6.4.1 PCM initialization sequences

The PCM initialization sequences for both A-law and μ-law are those described in [2]. They consist of 3496 samples. For a μ-law encoder in normal operation for the homing case, the input becomes (PCM_INIT.M + NRM.M) while for an A-law encoder the input becomes (PCM_INIT.A + NRM.A). Therefore, when they are put to precede the normal inputs, the length of the combined input sequence increases to 19 880 samples. Similarly, when they are combined with the overload inputs, the combined sequences contain 5544 samples. In each case, the relevant intermediate ADPCM sequence and PCM output from the ADPCM decoder is extracted by skipping the first 3496 samples.

6.4.2 μ-law ADPCM initialization

The μ-law ADPCM initialization sequence is obtained by applying the μ-law PCM initialization sequence to an μ-law → ADPCM coder at the given rate. These resulting initialization sequences are I_INI_16.M, I_INI_24.M, I_INI_32.M and I_INI_40.M for operation at 16, 24, 32 and 40 kbit/s respectively. They are prepended to the corresponding input sequence as follows: to the I16 for 16 kbit/s, I24 for 24 kbit/s, I32 for 32 kbit/s and I40 for 40 kbit/s. Thus, the length of the combined sequence increases to 19 880 samples. To check the ADPCM decoder operation the combined sequence is applied to a decoder and the PCM outputs corresponding to the i-inputs are obtained by skipping the first 3496 samples. These 3496 samples represent the μ-law PCM initialization sequences coded by the ADPCM coder and then decoded by the ADPCM decoder at the given rate.

To test the cross-coding operation (μ → A), the ADPCM initialization sequence for A-law decoding is prepended to the output of the ADPCM encoder at the respective rate. For example, at 32 kbit/s and for μ-law PCM input and A-law PCM output, the combined sequence is I_INI_32.A + HN32FM.I for normal operation and I_INI_32.A + HV32FM.I for overload operation. Thus, the length of the combined sequence increases to 19 880 samples for normal operation and to 5544 samples for overload operation. The combined sequence is used to exercise the ADPCM decoder. After skipping the first 3496 samples, the relevant output PCM sequence, HN32FC.O or HV32FC.O, is extracted. The same can be done at the other rates.

6.4.3 A-law ADPCM initialization

The A-law ADPCM initialization sequence is obtained by applying the A-law PCM initialization sequence to an A-law → ADPCM coder at the given rate. These resulting initialization sequences are I_INI_16.M, I_INI_24.M, I_INI_32.M and I_INI_40.M for operation at 16, 24, 32 and 40 kbit/s respectively. They are prepended to the corresponding input sequence as follows: to the I16 for 16 kbit/s, I24 for 24 kbit/s, I32 for 32 kbit/s and I40 for 40 kbit/s. Thus, the length of the combined sequence increases to 19 880 samples. To check the ADPCM decoder operation the combined sequence is applied to a decoder and the PCM outputs corresponding to the i-inputs are obtained by skipping the first 3496 samples. These 3496 samples represent the A-law PCM initialization sequences coded by the ADPCM coder and then decoded by the ADPCM decoder at the given rate.

To test the cross-coding operation (A → μ), the ADPCM initialization sequence for μ-law decoding is prepended to the output of the ADPCM encoder at the respective rate. For example, at 40 kbit/s and for A-law PCM input and μ-law PCM output, the combined sequence is I_INI_40.M + HN40FA.I for normal operation and I_INI_40.M + HV40FA.I for overload operation. Thus, the length of the combined sequence increases to 19 880 samples for normal operation and to 5544 samples for overload operation. The combined sequence is used to exercise the ADPCM decoder. After skipping the first 3496 samples, the relevant output PCM sequence, HN32FX.O or HV32FX.O, is extracted. The same can be done at the other rates.

7 Commonality of test sequences

Many test conditions share the same sequences; Table 13 summarizes this commonality. A table entry gives the total number of sequences for a specific test case. The superscript identifies entries that share the same test sequences. For example, the 8 ADPCM sequences in the normal case of the μ-law are pairwise identical to the corresponding ADPCM sequences in the normal tests of the conversion from μ-law to A-law.

Table 13 – Number and commonality of test sequences

Test	μ-law	A-law

sequences	Input (PCM)	ADPCM	Output (PCM)	Input (PCM)	ADPCM	Output (PCM)
Normal	1^{1}	8^{2}	8	1^{4}	8^{8}	8
I-input	N/A	4^{5}	8	N/A	4^{5}	8
Overload	1^{6}	8^{7}	8	1^{8}	8^{9}	8
Test sequences	**μ-law → A-law**			**A-law → μ-law**		
	Input (μ-PCM)	**ADPCM**	**Output (A-PCM)**	**Input (A-PCM)**	**ADPCM**	**Output (μ-PCM)**
Normal	1^{1}	8^{2}	8	1^{3}	8^{8}	8
Overload	1^{6}	8^{7}	8	1^{8}	8^{9}	8

8 Note to the user

The digital sequences are chosen to exercise the major arithmetic components and give a reasonable level of confidence of the compliance of an implementation with this Recommendation. It should be noted that all states cannot be covered with such a limited number of sequences. Suggestions for increasing the coverage and/or reports of problems encountered during the usage of the test sequences should be addressed to the ITU-T.

References

[1] CCITT Recommendation G.726 (1990), *40, 32, 24, 16 kbit/s Adaptive Differential Pulse Code Modulation (ADPCM)*.

[2] BANERJEE (S.), BERTOCCI (G.): Testing implementations of the 32 kbit/s CCITT and ANSI ADPCM algorithm, *Proc. ICC 1987,* Vol. 3, 1487-1490, 10 June 1987.

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G.191 (11.96)	Software Tools Library 96 (STL-96) and STL-96 Manual
G.722 Appendix II (03.87)	Digital test sequences for the verification of the G.722 64 kbit/s SB-ADPCM 7 kHz codec
G.723.1 Annex A (11.96)	C reference code, test signals and test sequences for the fixed point 5.3 and 6.3 kbit/s dual rate speech coder and for the silence compression scheme, version 5.1
G.723.1 Annex B (11.96)	C reference code and test signals for the floating point 5.3 and 6.3 kbit/s dual rate speech coder, version 5.1F
G.723.1 Annex C (11.96)	C reference code and test signals for the scalable channel codec, version 3.1
G.726 Appendix II (03.96)	Digital test sequences for the verification of the G.726 40, 32, 24 and 16 kbit/s ADPCM algorithm
G.727 Appendix I (03.96)	Digital test sequences for the verification of the G.727 5-, 4-, 3- and 2-bit/sample embedded ADPCM algorithm
G.728 Appendix I (06.95)	Programs and test sequences for implementation verification of the algorithm of the G.728 16 kbit/s LD-CELP speech coder
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P.501 (08.96)	Test signals for use in telephonometry
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