Power Supply:

电源名称	输出电压	最大供电能力	预计谁在用
AXP209 DCDC2 CPUVDD	1.25V	1600mA	CPU
AXP209 DCDC3 INT_VDD1V2	1.2V	1200mA	CORE
AXP209 LCD1 RTCVDD	1.3V	30mA	RTC
AXP209 LDO2 AVCC	3V	200mA	AVCC
AXP209 LDO3 CSI-IOVDD	2.8V	400mA	CSI0-IO
AXP209 LDO4 CSI-AVDD	2.8V	200mA	CSI1-IO
AP1231-2.5 LDO VCC_2V5	2.5V	300mA	TV-IN / MAC /RGB
SY8008 DCDC DRAM-VCC	1.5V	1200mA	DRAM
SY8008 DCDC VCC-3V	3V	1200mA	板上其它所有外设
RTC BACKUP BAT VBACKUP	3V	5mA	RTC
外部电源总输入 VDD_5V	5V	1000mA	整个板子
外部电池输入	4.2V	1200mA	整个板子
对外输出总电源 IPSOUT	5V/4.2V	1200mA	整个板子
AP1231-2.5 LDO GMAC_2V5	2.5	300mA	1000M网卡芯片

AllWinner Technology Co.,Ltd

Title: A20_PAD_STD

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Date: Saturday, June 14, 2014 | Sheet 1 of 18

PIO ASSIGNMENT

Pin Group	Pin Name	Define	Function
PA(18)	PA0	GPIO-OUT	
	PA1	GPIO-OUT	
	PA2	GPIO-OUT	
	PA3	GPIO-OUT	
	PA4	ETXD3	
	PA5	ETXD2	
	PA6	ETXD1	
	PA7	ETXD0	
	PA8	ERXCK	
	PA9	ERXERR	
	PA10	ERXDV	
	PA11	EMDC	
	PA12	EMDIO	
	PA13	ETXEN	
	PA14	ETXCK	
	PA15	ECRS	
	PA16	ECOL	
	PA17	GPIO_OUT	
PB(24)	PB0	TWI0_SCK	PMU
	PB1	TWI0_SDA	
	PB2	PWM0	PWM
	PB3	GPIO_OUT	MT-C
	PB4	IR0_RX	IR
	PB5	GPIO_OUT	BT-RST
	PB6	I2S_BCLK	BT-PCM-CLK
	PB7	I2S_LRCK	BT-PCM-SYNC
	PB8	I2S_DO0	BT-PCM-OUT
	PB9	GPIO_OUT	USB0-DRV
	PB10	GPIO_OUT	
	PB11	GPIO_OUT	
	PB12	I2S_DI	BT-PCM-IN
	PB13	GPIO_OUT	TP-WAKEUP
	PB14	JTAG_MS0	JTAG
	PB15	JTAG_CK0	
	PB16	JTAG_DO0	
	PB17	JTAG_DI0	
	PB18	TWI1_SCK	TWI1
	PB19	TWI1_SDA	
	PB20	TWI2_SCK	TWI2
	PB21	TWI2_SDA	
	PB22	UART0_TX	UART (DBUG)
	PB23	UART0_RX	

Pin Group	Pin Name	Define	Function
PC(25)	PC0	NWE#	NAND
	PC1	NALE	
	PC2	NCLE	
	PC3	NCE1	
	PC4	NCE0	
	PC5	NRE#	
	PC6	NRB0	
	PC7	NRB1	
	PC8	NDQ0	
	PC9	NDQ1	
	PC10	NDQ2	
	PC11	NDQ3	
	PC12	NDQ4	
	PC13	NDQ5	
	PC14	NDQ6	
	PC15	NDQ7	
	PC16	NWP	
	PC17	NCE2	
	PC18	NCE3	
	PC19	GPIO_OUT	
	PC20	GPIO_OUT	
	PC21	GPIO_OUT	
	PC22	GPIO_OUT	
	PC23	GPIO_OUT	
	PC24	NDQS	
PD(28)	PD0	LCD0_D0	LCD
	PD1	LCD0_D1	
	PD2	LCD0_D2	
	PD3	LCD0_D3	
	PD4	LCD0_D4	
	PD5	LCD0_D5	
	PD6	LCD0_D6	
	PD7	LCD0_D7	
	PD8	LCD0_D8	
	PD9	LCD0_D9	
	PD10	LCD0_D10	
	PD11	LCD0_D11	
	PD12	LCD0_D12	
	PD13	LCD0_D13	
	PD14	LCD0_D14	
	PD15	LCD0_D15	
	PD16	LCD0_D16	
	PD17	LCD0_D17	

Pin Group	Pin Name	Define	Function
PD(28)	PD18	LCD0_D18	LCD
	PD19	LCD0_D19	
	PD20	LCD0_D20	
	PD21	LCD0_D21	
	PD22	LCD0_D22	
	PD23	LCD0_D23	
	PD24	LCD0_CLK	
	PD25	LCD0_DE	
	PD26	LCD0_HSYNC	
	PD27	LCD0_VSYNC	
PE(12)	PE0	CSI0_PCLK	CSI0
	PE1	CSI0_MCLK	
	PE2	CSI0_HSYNC	
	PE3	CSI0_VSYNC	
	PE4	CSI0_D0	
	PE5	CSI0_D1	
	PE6	CSI0_D2	
	PE7	CSI0_D3	
	PE8	CSI0_D4	
	PE9	CSI0_D5	
	PE10	CSI0_D6	
	PE11	CSI0_D7	
PF(6)	PF0	SDC0_D1	SDC0
	PF1	SDC0_D0	
	PF2	SDC0_CLK	
	PF3	SDC0_CMD	
	PF4	SDC0_D3	
	PF5	SDC0_D2	
PG(12)	PG0	CSI1_PCLK	CSI1
	PG1	CSI1_MLCK	
	PG2	CSI1_HSYNC	
	PG3	CSI1_VSYNC	
	PG4	CSI1_D0	
	PG5	CSI1_D1	
	PG6	CSI1_D2	
	PG7	CSI1_D3	
	PG8	CSI1_D4	
	PG9	CSI1_D5	
	PG10	CSI1_D6	
	PG11	CSI1_D7	

Pin Group	Pin Name	Define	Function
PH(28)	PH0	EINT0	USB-ICTRL
	PH1	GPIO_IN	SD0-DET
	PH2	GPIO_IN	
	PH3	GPIO_OUT	USB2-DRV
	PH4	GPIO_IN	USB0-IDDET
	PH5	GPIO_IN	USB0-VBUSDET
	PH6	GPIO_OUT	USB1-DRV
	PH7	GPIO_OUT	LCD-BL-EN
	PH8	GPIO_OUT	LCD-PWR
	PH9	GPIO_OUT	WIFI-SHDN
	PH10	GPIO_IN	WIFI-HOST-WAKE
	PH11	GPIO_OUT	
	PH12	GPIO_OUT	
	PH13	GPIO_OUT	CAM-R-RESET#
	PH14	GPIO_OUT	CAM-F-RESET#
	PH15	GPIO_OUT	PA-SHDN#
	PH16	GPIO_OUT	CAM-PWR-EN
	PH17	GPIO_OUT	CAM-F-PWR-EN
	PH18	EINT18	CAM-R-STBY-EN
	PH19	EINT19	CAM-F-STBY-EN
	PH20	EINT20	
	PH21	EINT21	TP-INT
	PH22	SDC1_CMD	
	PH23	SDC1_CLK	
	PH24	SDC1_D0	
	PH25	SDC1_D1	
	PH26	SDC1_D2	
	PH27	SDC1_D3	
PI(22)	PI0	GPIO	
	PI1	GPIO	
	PI2	GPIO	
	PI3	PWM1	
	PI4	SDC3_CMD	WIFI
	PI5	SDC3_CLK	
	PI6	SDC3_D0	
	PI7	SDC3_D1	
	PI8	SDC3_D2	
	PI9	SDC3_D3	
	PI10	SPI0_CS0	
	PI11	GPIO_OUT	
	PI12	SPI0_MOSI	CLK-32K
	PI13	SPI0_MISO	
	PI14	GPIO_OUT	

Pin Group	Pin Name	Define	Function
PI(22)	PI15	GPIO_OUT	
	PI16	UART2_RTS	
	PI17	UART2_CTS	
	PI18	UART2_TX	
	PI19	UART2_RX	
	PI20	GPIO_OUT	
	PI21	GPIO_OUT	

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Title: A20_PAD_STD

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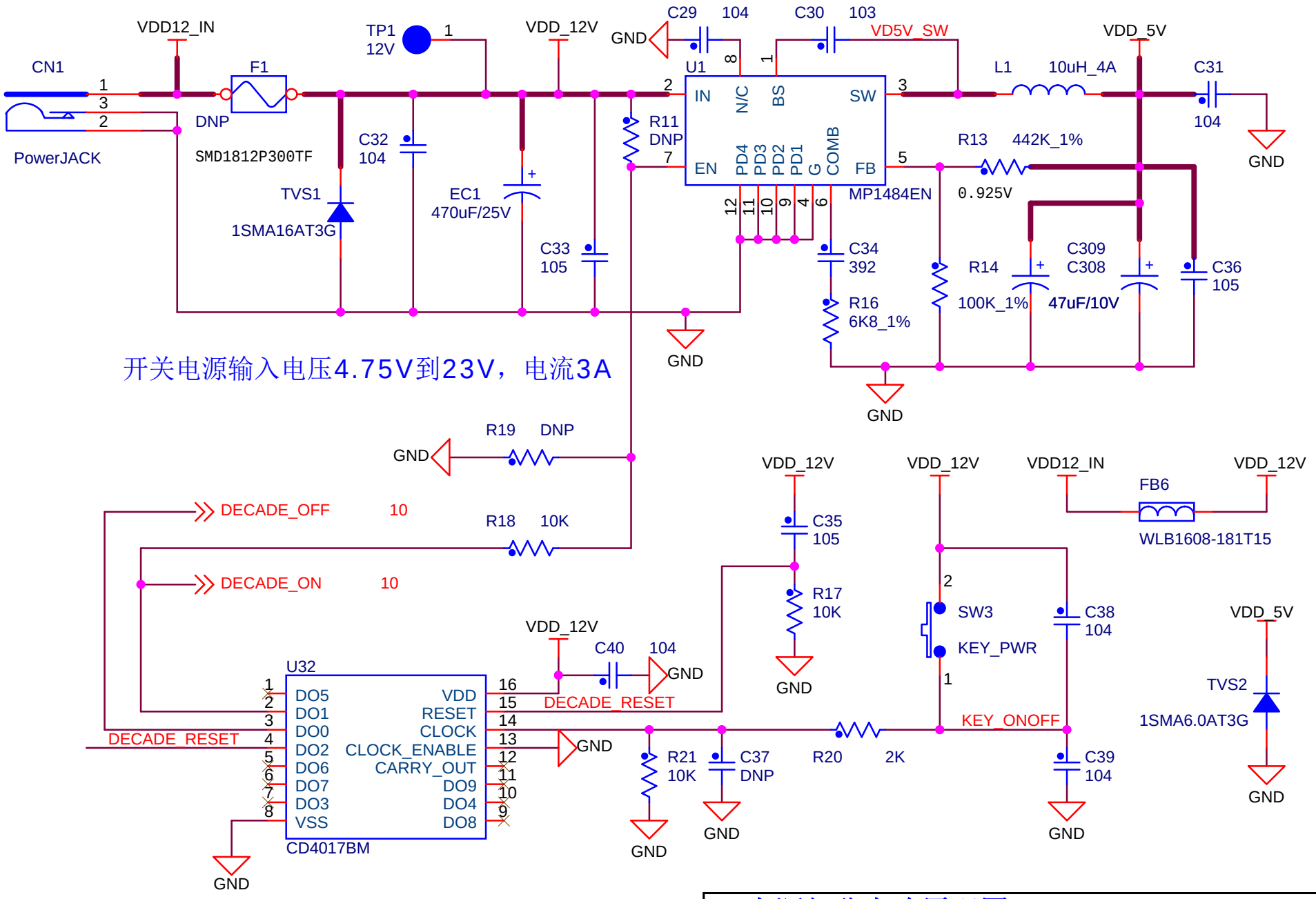


Title: 电源部分电路原理图		
Size	OrgName: RAINTI	Rev
Custom	Designer: 龚俊 Mender: GongJun	1.0
Date: Saturday, June 14, 2014	Sheet 3 of 18	

备注：
对于电感尺寸有轻薄要求的，推荐使用乾坤的PSE250201B-2R2MS,其体积为2.6x2.1平方毫米，饱和电流为1.8A,直流阻抗为85毫欧。

POWER LINE:Width>=80mil

POWER LINE:Width>=40mil

CSI-IOVDD =2.8V
CSI-AVDD =2.8V

靠近LDO3IN放置

靠近VIN1放置

DCDC3网络为反馈网络，lay板时走细线即可。

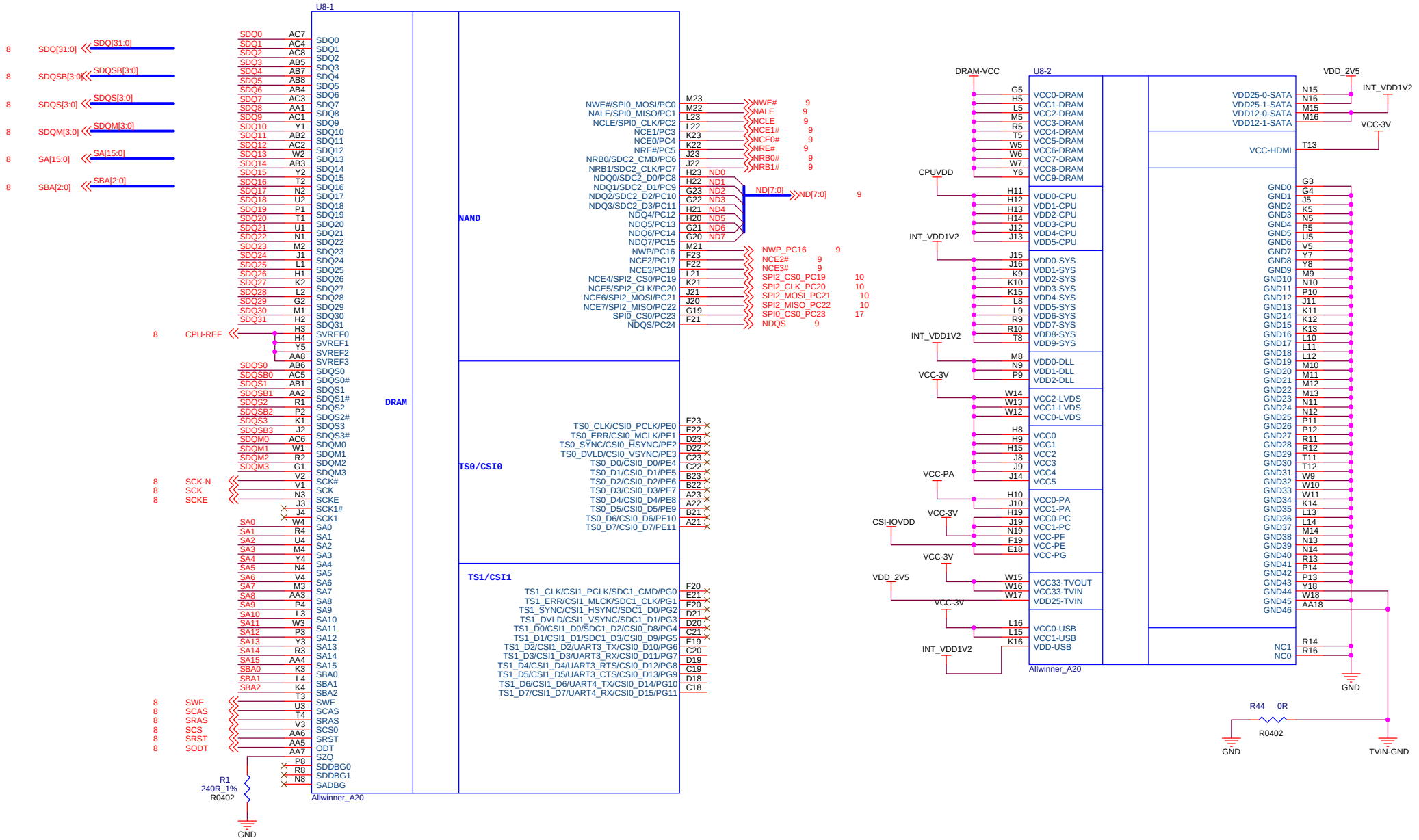
DCDC2网络为反馈网络，lay板时走细线即可。

所选用的二极管在环境温度75摄氏度时反向漏电要小于 5uA。

$$Vout = 0.6*(1+R1/R2)$$

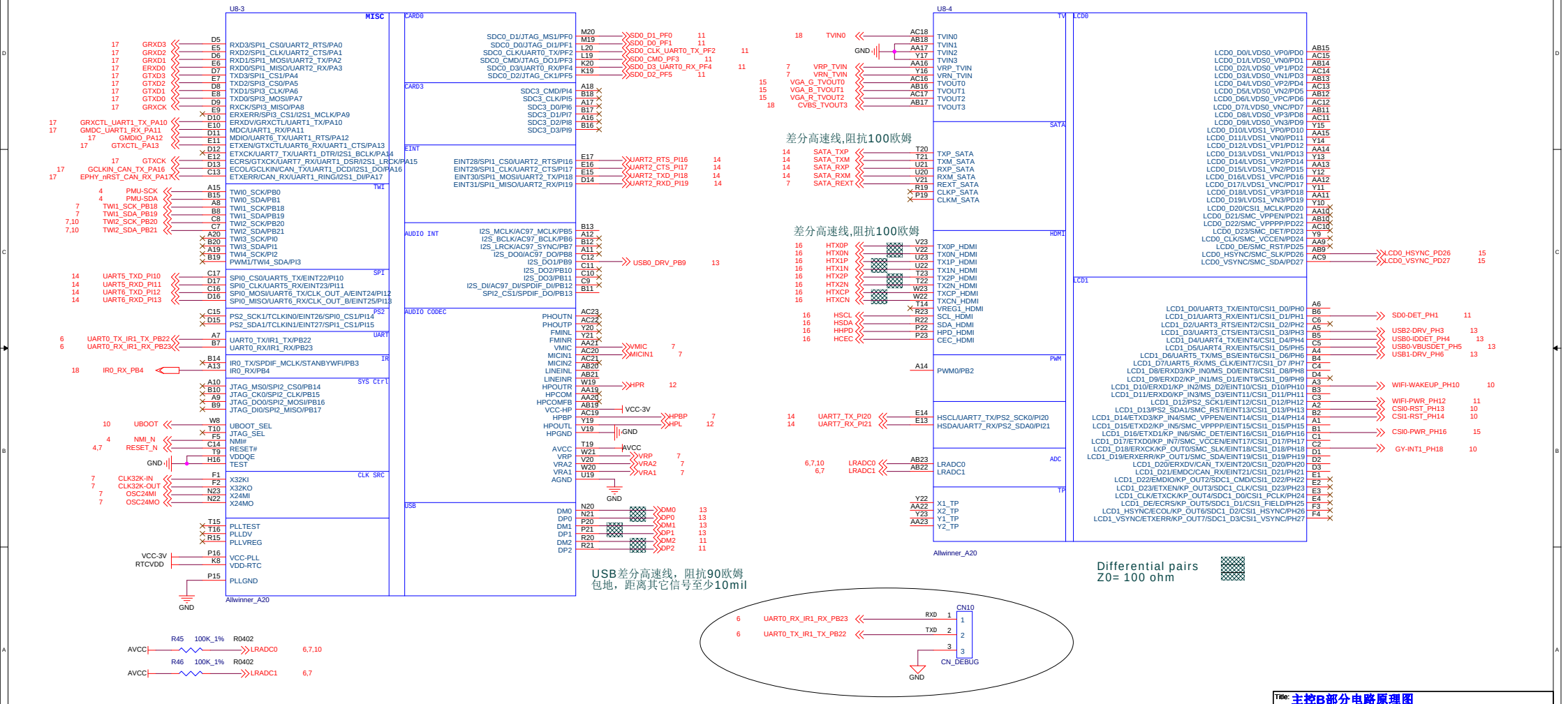
Title:	PMU电源管理电路原理图
Size	
OrgName:	RAINTI
Rev	1.0
Designer:	龚俊
Mender:	GongJun
Date:	Saturday, June 14, 2014
Sheet	4 of 18

CPU1



Title: 主控A部分电路原理图			
Size: A3	OrgName: RAINTI		Rev: 1.0
	Designer: 龚俊	Mender: GongJun	
Date: Saturday, June 14, 2014	Sheet 5 of 18		

CPU2

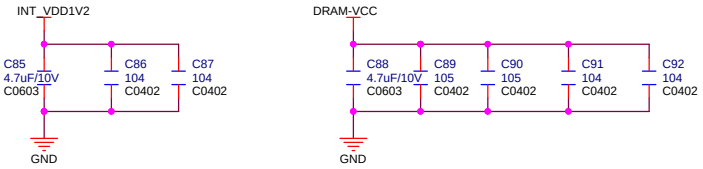


Title: 主控B部分电路原理图

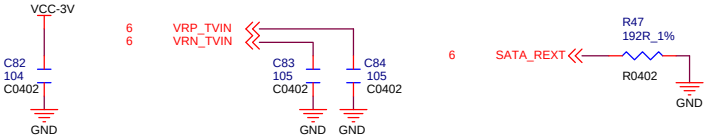
Size	OrgName: RAINTI	Rev
CustDesigner: 裘俊	Mender: GongJun	1.0
Date: Saturday, June 14, 2014	Sheet 6 of 18	

BESIDE CPU

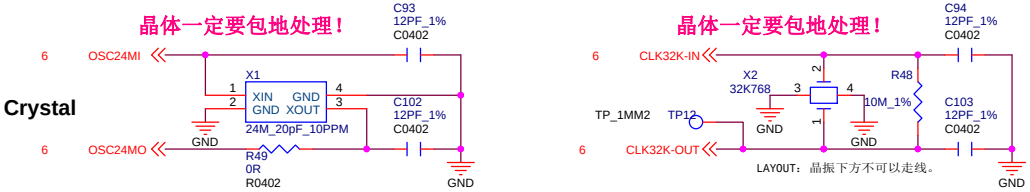
DRAM



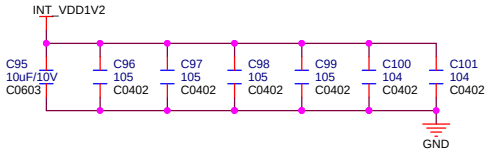
PLL



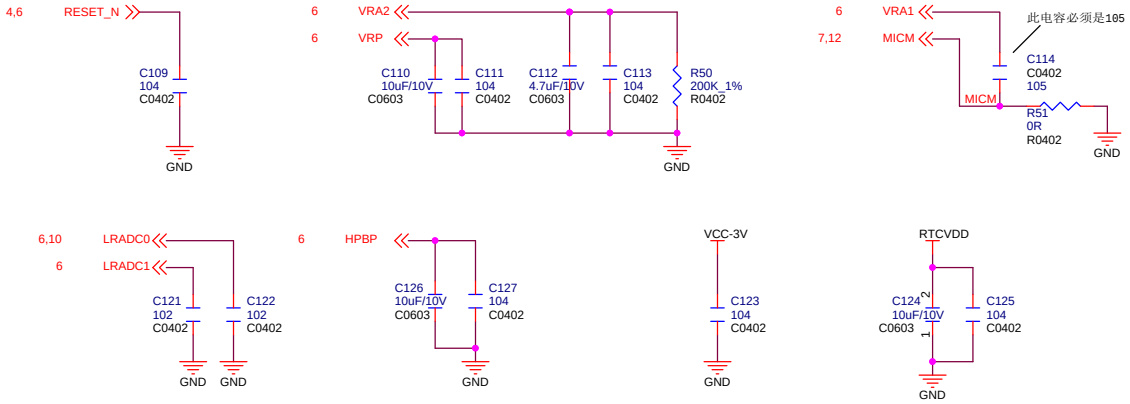
Crystal



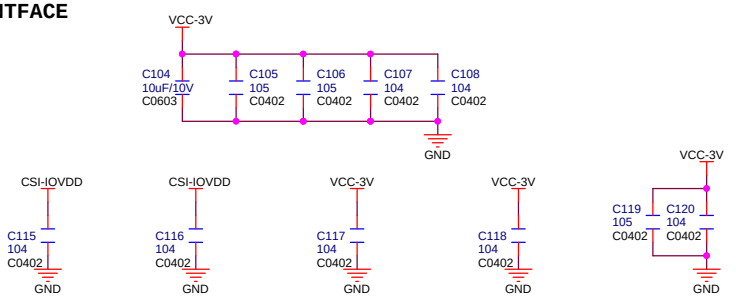
CORE



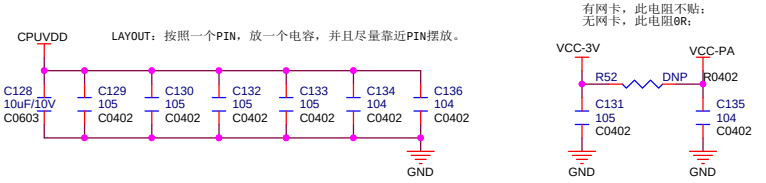
AUDIO&SYS&TP



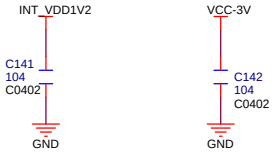
PIO-INTFACE



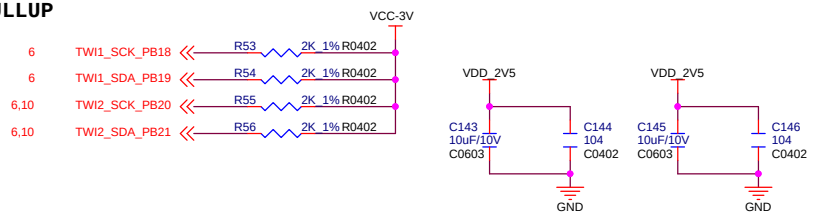
CPU&TV



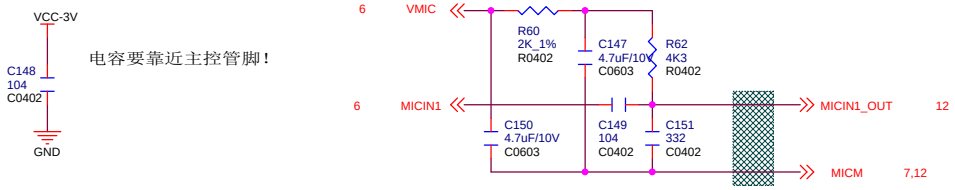
USB



TWI-PULLUP



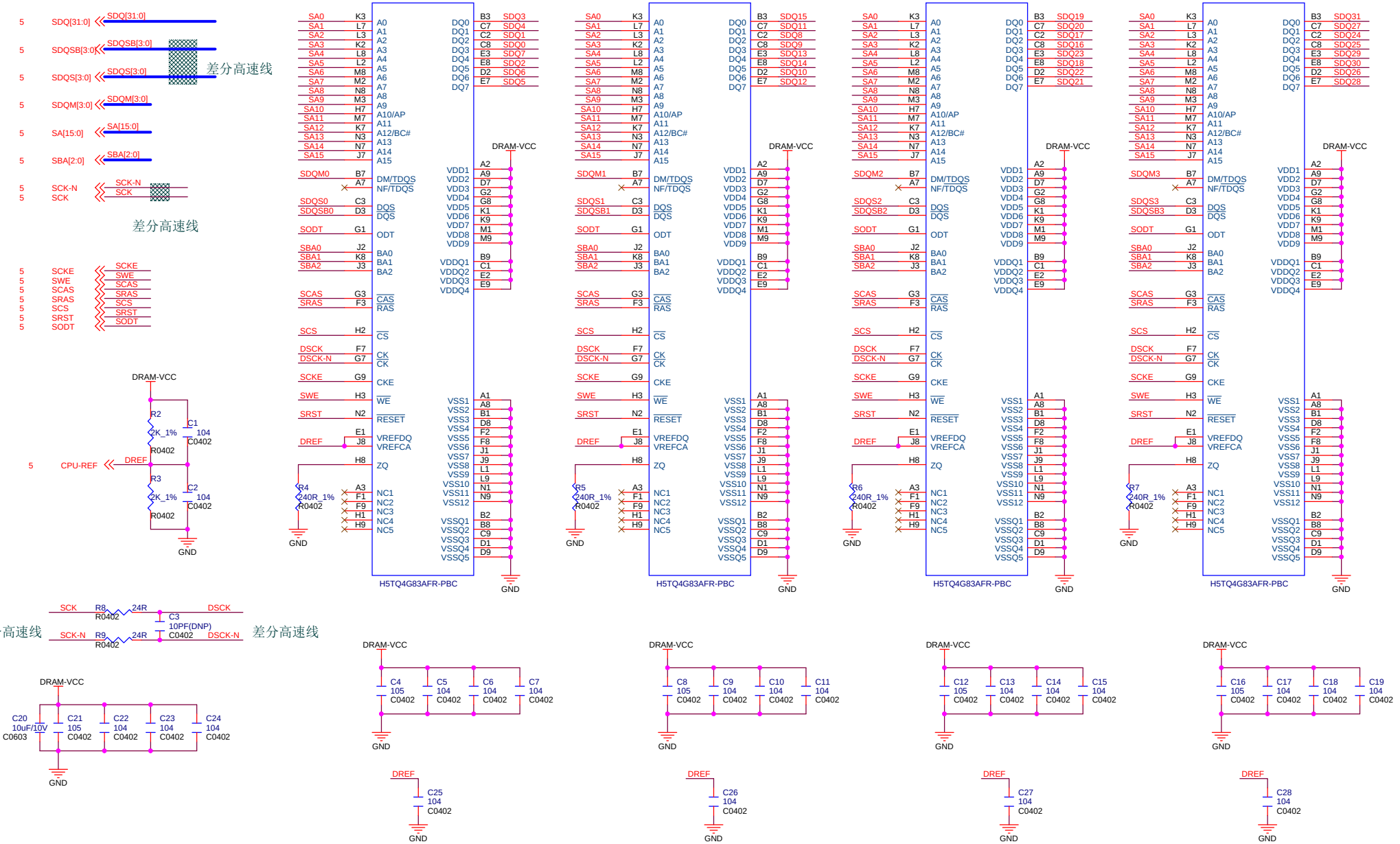
HDMI



Title: 主控周边部分电路原理图		
Size: A3	OrgName: RAINTI	Rev: 1.0
	Designer: 龚俊	Mender: GongJun
Date: Saturday, June 14, 2014	Sheet 7 of 18	

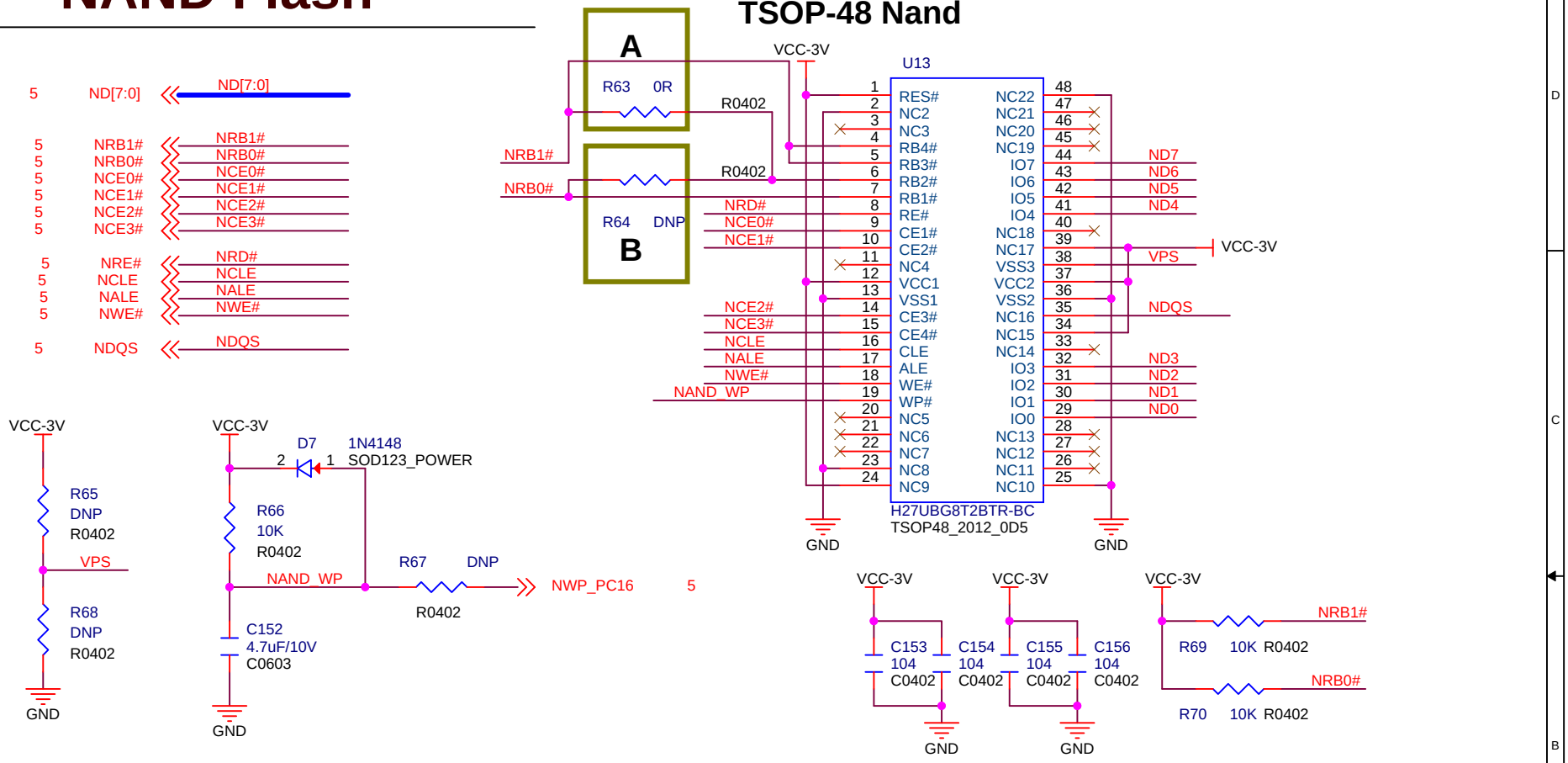
DDR3-8BITX4

Please copy DRAM PCB template and follow PCB layout guide. The circuit is only for single-side PCB layout.

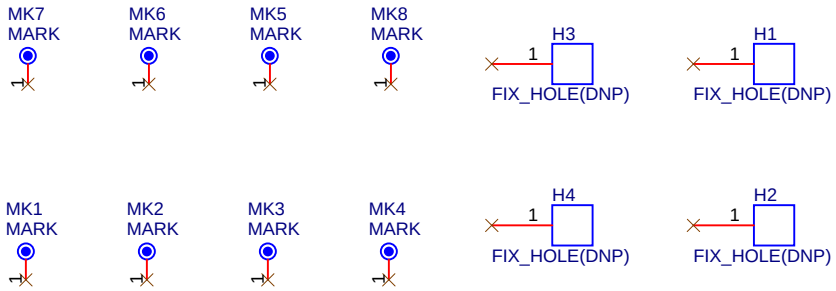


Title: DDR3内存电路原理图			
Size: A3	OrgName: RAINTI		Rev: 1.0
	Designer: 龚俊	Mender: GongJun	
Date: Saturday, June 14, 2014	Sheet 8 of 18		

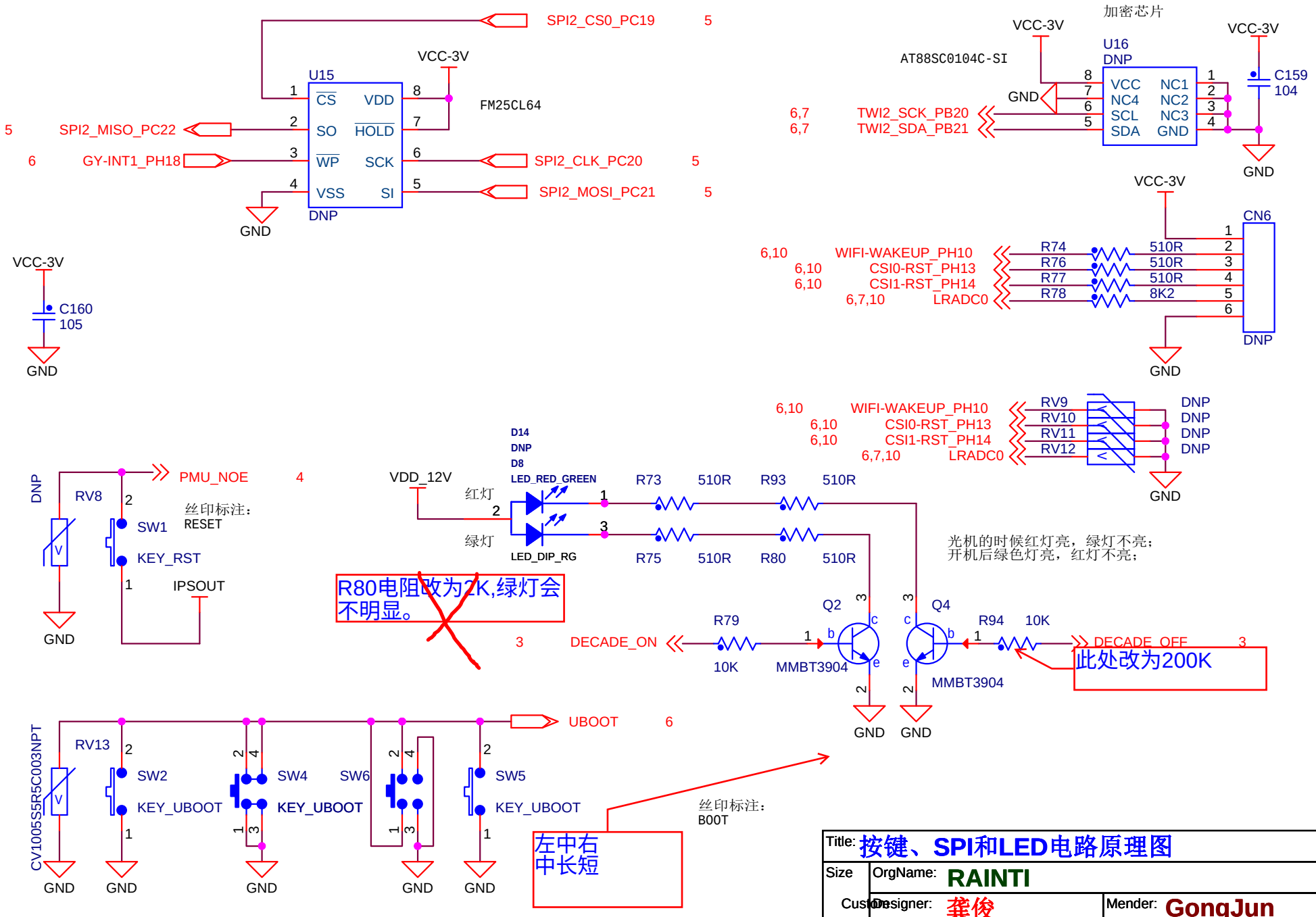
NAND Flash



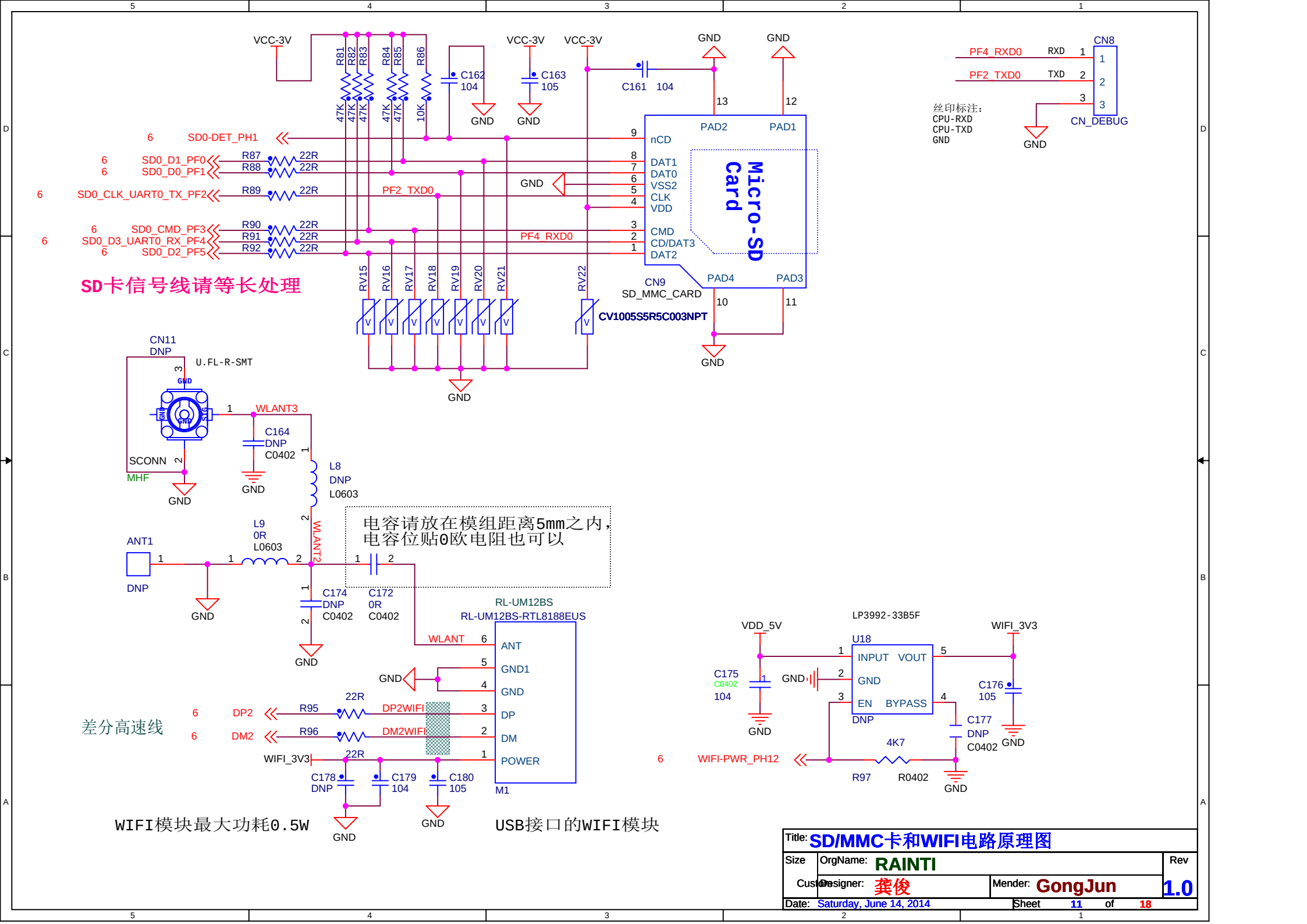
(1) 接1片单片选Nand 时，电阻A，B全断开
(2) 接1片双片选Nand 时，连接电阻A， 断开电阻B
(3) 接1片四片选Nand 时，连接电阻B， 断开电阻A
(4) 接2片单片选或接2片双片选Nand 时，
连接电阻A， 断开电阻B



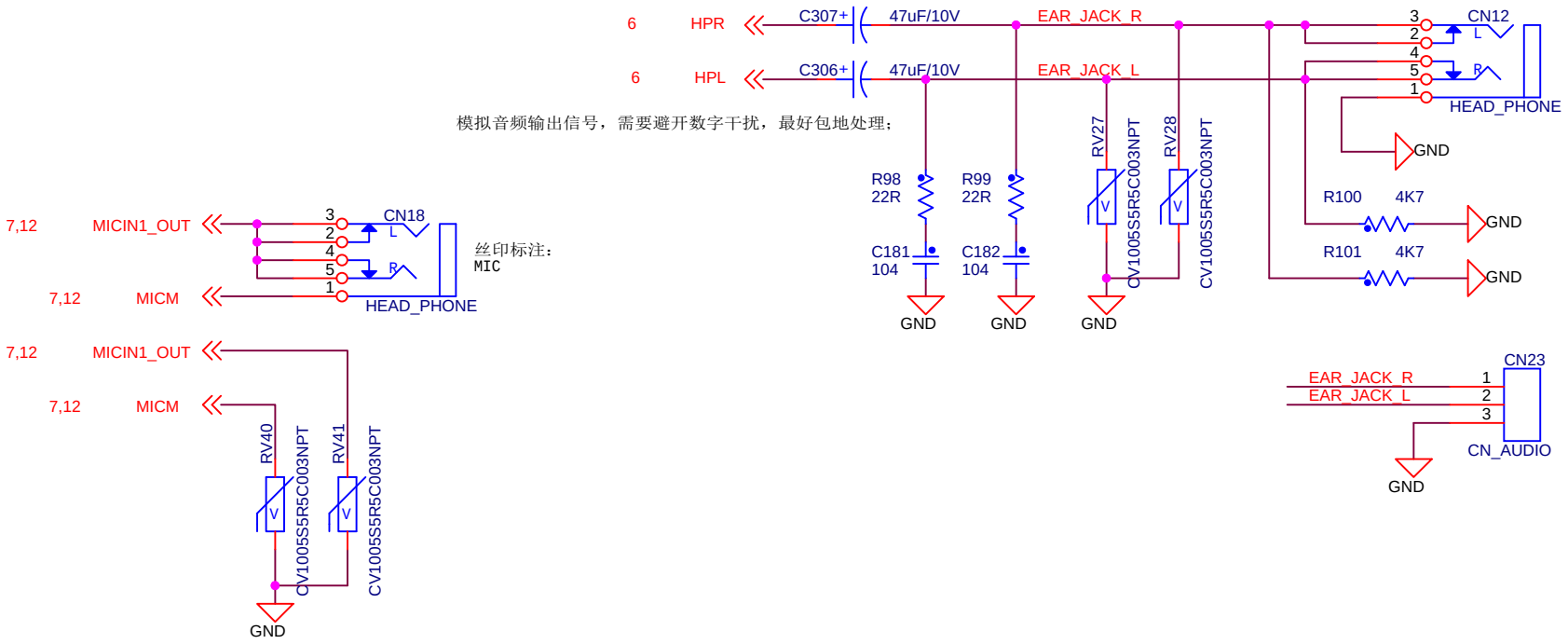
Title: NAND Flash电路原理图		
Size	OrgName: RAINTI	Rev
Custom	Designer: 龚俊 Mender: GongJun	1.0
Date: Saturday, June 14, 2014	Sheet 9 of 18	



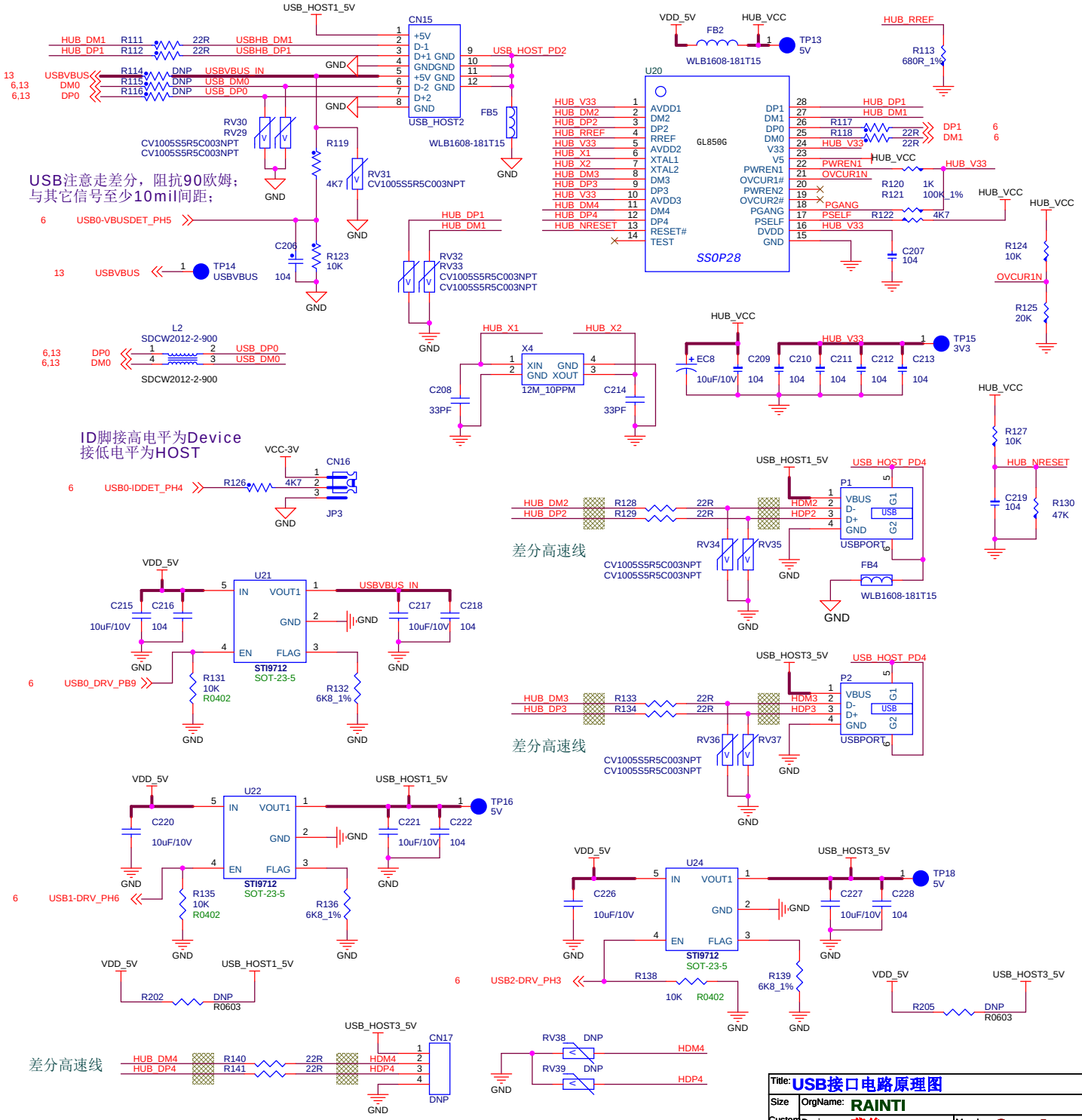
Title: 按键、SPI和LED电路原理图		
Size	OrgName: RAINTI	Rev
CustomDesigner: 龚俊	Mender: GongJun	1.0
Date: Saturday, June 14, 2014	Sheet 10 of 18	

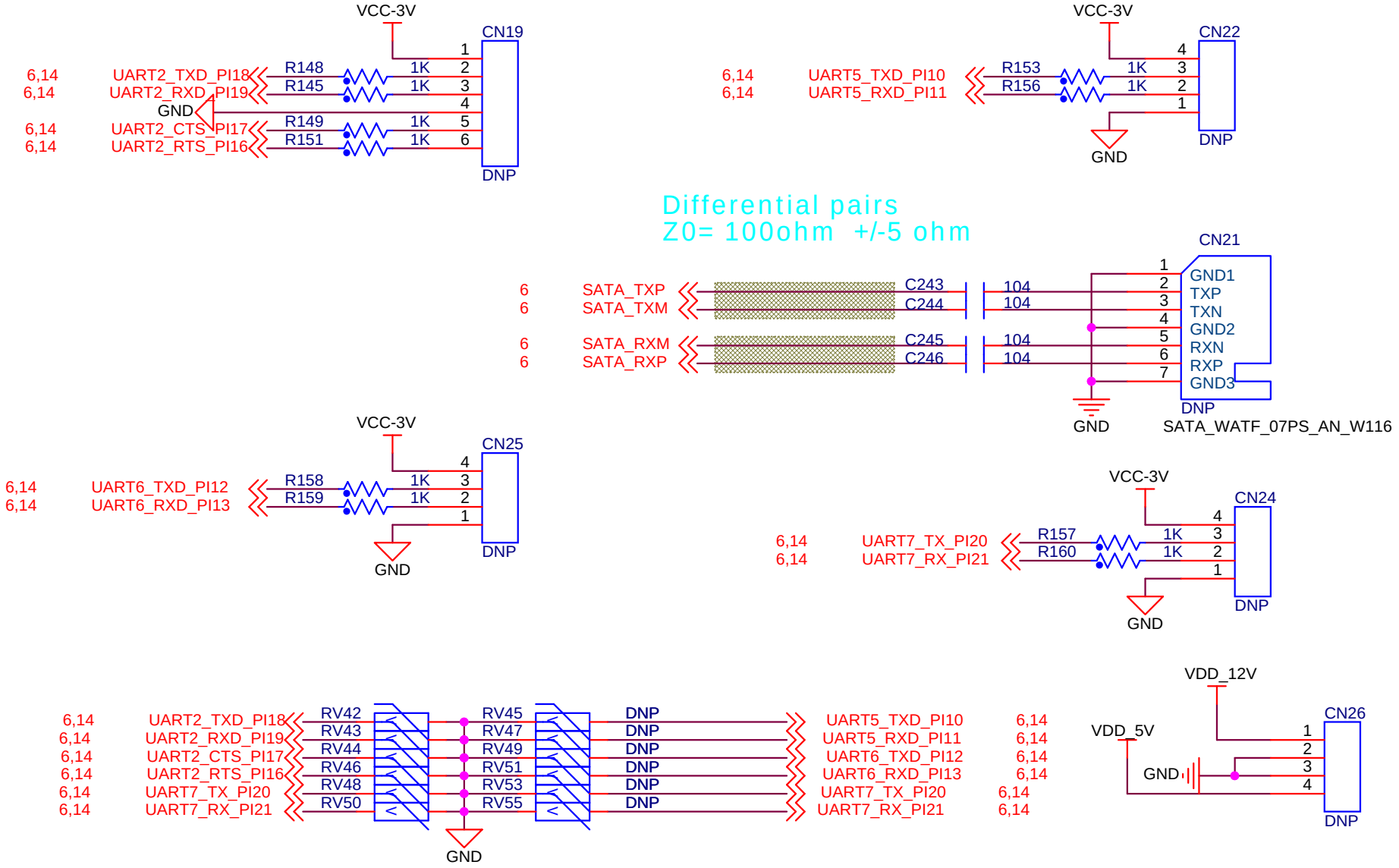


Title:	SD/MMC卡和WIFI电路原理图		
Size	OrgName: RAINTI		Rev
Custom	Designer: 龚俊	Mender: GongJun	1.0
Date: Saturday, June 14, 2014		Sheet 11 of 18	

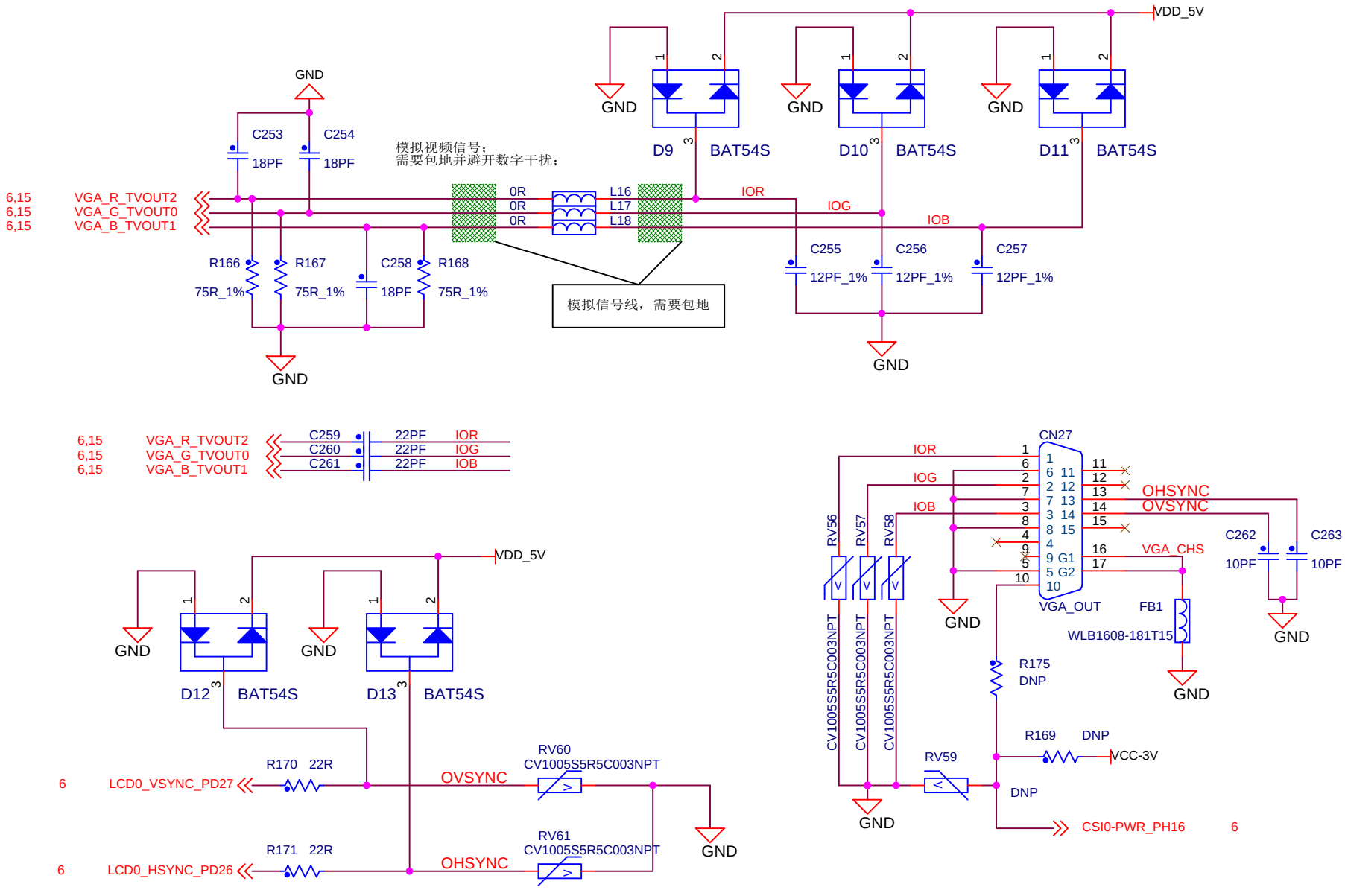


Title: 音频放大接口电路原理图			
Size	OrgName: RAINTI		Rev
Custom	Designer: 龚俊	Mender: GongJun	1.0
Date: Saturday, June 14, 2014	Sheet 12 of 18		


USB_HOST1_5V
CN15
HUB_DM1
HUB_DP1
R111 22R USBHB_DM1
R112 22R USBHB_DP1
USB_HOST_PD2
USBVBUS
DM0
DP0
R114 DNP USBVBUS_IN
R115 DNP USB_DM0
R116 DNP USB_DP0
GND
USB_HOST2
FB5
WLB1608-181T15
RV30
RV29
CV1005S5R5C003NPT
CV1005S5R5C003NPT
R119
4K7
RV31
CV1005S5R5C003NPT
USB注意走差分，阻抗90欧姆；
与其它信号至少10mil间距；
USB0-VBUSDET_PH5
C206
104
R123
10K
TP14
USBVBUS
HUB_DP1
HUB_DM1
RV32
RV33
CV1005S5R5C003NPT
CV1005S5R5C003NPT
L2
SDCW2012-2-900
USB_DP0
USB_DM0
SDCW2012-2-900
HUB_X1
HUB_X2
X4
XIN GND
GND XOUT
12M_10PPM
C208
33PF
C214
33PF
ID脚接高电平为Device
接低电平为HOST
VCC-3V
CN16
USB0-IDDET_PH4
R126
4K7
JP3
VDD_5V
U21
C215
C216
10uF/10V
104
IN
VOUT1
GND
EN
FLAG
STI9712
SOT-23-5
USBVBUS_IN
C217
C218
10uF/10V
104
USB0_DRV_PB9
R131
10K
R0402
R132
6K8_1%
VDD_5V
U22
C220
10uF/10V
USB_HOST1_5V
TP16
5V
C221
C222
10uF/10V
104
USB1-DRV_PH6
R135
10K
R0402
R136
6K8_1%
VDD_5V
USB_HOST1_5V
R202
DNP
R0603
差分高速线
USB_HOST3_5V
CN17
HUB_DM4
HUB_DP4
R140
R141
22R
HDM4
HDP4
DNP
RV38
DNP
RV39
DNP
HDM4
HDP4
VDD_5V
FB2
HUB_VCC
TP13
5V
WLB1608-181T15
U20
AVDD1
DM2
DP2
RREF
AVDD2
XTAL1
XTAL2
DM3
DP3
AVDD3
DM4
DP4
RESET#
TEST
GL850G
SS0P28
DP1
DM1
DP0
DM0
V33
V5
PWREN1
OVCUR1#
PWREN2
OVCUR2#
PGANG
PSELF
DVDD
GND
HUB_RREF
R113
680R_1%
HUB_V33
HUB_DP1
HUB_DM1
R117
R118
22R
22R
DP1
DM1
HUB_V33
HUB_VCC
PWREN1
OVCUR1N
R120
1K
R121
100K_1%
HUB_VCC
PGANG
PSELF
R122
4K7
HUB_V33
C207
104
HUB_VCC
R124
10K
OVCUR1N
R125
20K
HUB_VCC
EC8
10uF/10V
C209
C210
C211
C212
C213
104
HUB_V33
TP15
3V3
HUB_VCC
R127
10K
HUB_NRESET
C219
104
R130
47K
差分高速线
USB_HOST1_5V
USB_HOST_PD4
P1
VBUS
D-
D+
GND
USB
HDM2
HDP2
G1
G2
USBPORT
HUB_DM2
HUB_DP2
R128
R129
22R
22R
RV34
RV35
CV1005S5R5C003NPT
CV1005S5R5C003NPT
FB4
WLB1608-181T15
GND
差分高速线
USB_HOST3_5V
USB_HOST_PD4
P2
HUB_DM3
HUB_DP3
R133
R134
22R
22R
RV36
RV37
CV1005S5R5C003NPT
CV1005S5R5C003NPT
VDD_5V
U24
C226
10uF/10V
USB_HOST3_5V
TP18
5V
C227
C228
10uF/10V
104
USB2-DRV_PH3
R138
10K
R0402
R139
6K8_1%
VDD_5V
USB_HOST3_5V
R205
DNP
R0603
Title: USB接口电路原理图
Size
Custom
OrgName: RAINTI
Rev
Designer: 龚俊
Mender: GongJun
1.0
Date: Saturday, June 14, 2014
Sheet 13 of 18



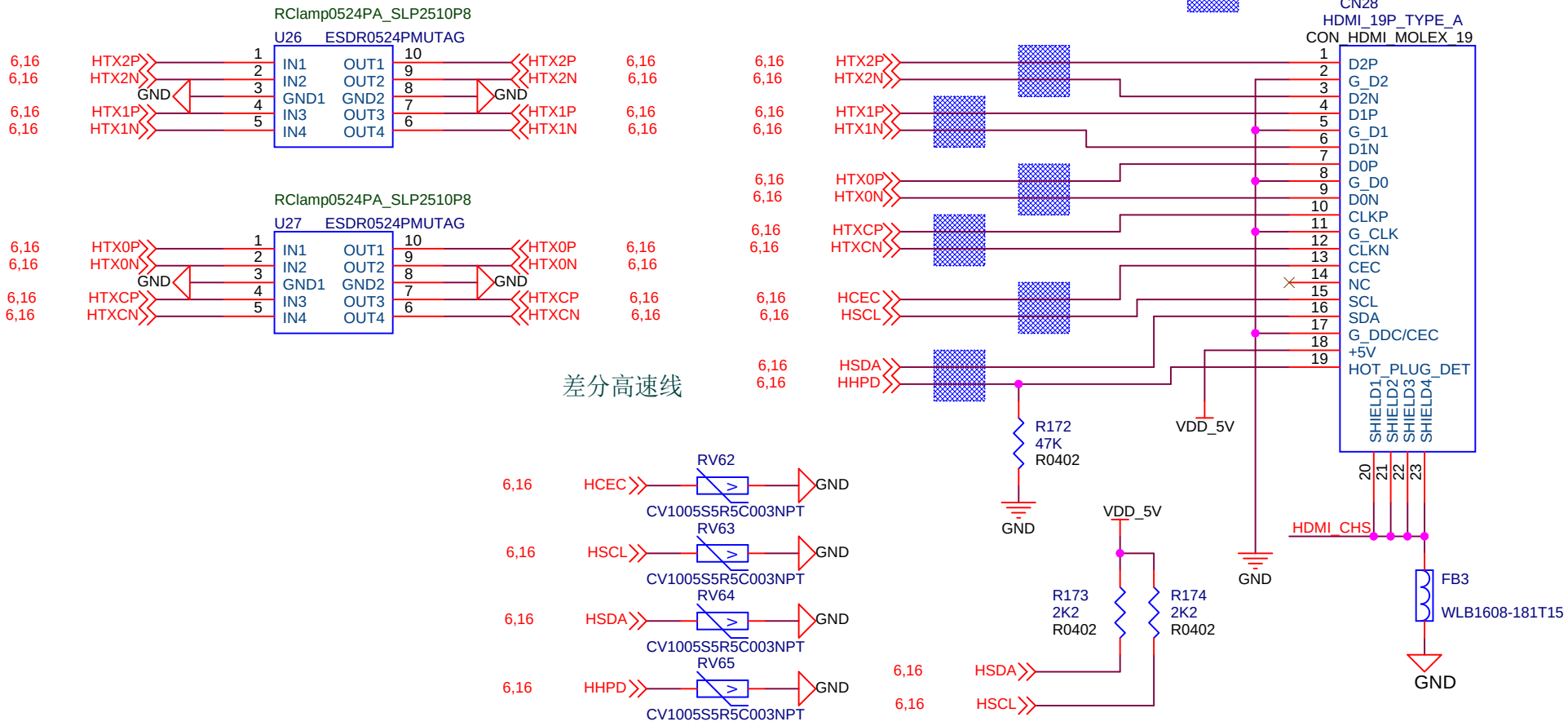
Title: **UART接口电路原理图**		
Size: Custom	OrgName: **RAINTI**	Rev: **1.0**
	Designer: **龚俊**	Mender: **GongJun**
Date: Saturday, June 14, 2014	Sheet **14** of **18**	



Title: VGA接口电路原理图			
Size: A4	OrgName: RAINTI		Rev: 1.0
	Designer: 龚俊	Mender: GongJun	
Date: Saturday, June 14, 2014		Sheet 15 of 18	

HDMI高速信号，需要走差分和控制阻抗，并包地处理；

Differential pairs
Z0= 100 ohm



Title: HDMI和LVDS接口电路原理图			
Size: Custom	OrgName: RAINTI		Rev: 1.0
	Designer: 龚俊	Mender: GongJun	
Date: Saturday, June 14, 2014		Sheet 16 of 18	

GMAC

10/100/1000 RGMII Ethernet PHY

晶体一定要包地处理！

GMAC-RGMII

If you use the GMAC-RGMII interface,
Please use the Gigabit Ethernet PHY.

VCC-PA不能接到其它电源网络上，GMAC供电为2.5V。

Note 1: The Trace length between La and PHY's Pin48 must be within 0.5 cm. CJ(22uF) and CK(0.1uF) to La must be within 0.5cm.

PHYAD0=1: LED0 Low Active
PHYAD1=0: LED1 High Active
RXDLY=1: LED2 Low Active
CD, CE, CF reserve for EMI.

Place filter network close to CLK125. Reserved for EMI

Place filter network close to RX_CLK. Reserved for EMI

VCC-2V5 > 55mA

VCC-3V>200mA

Note 2: The Trace length from CA(22uF),CB(0.1uF) to Pin 44,45(VDDREG) must bewithin 0.5 cm. The trace width from AVDD33 to Pin 44,45 should>40mils.

Differential pairs
线宽W=4.5mil
线距C=8mil
阻抗Z0= 100 ohm
差分高速线

PHY Address=001(RTL8211E)

Pull down for 2.5V RGMII(RTL8211D/8211E)

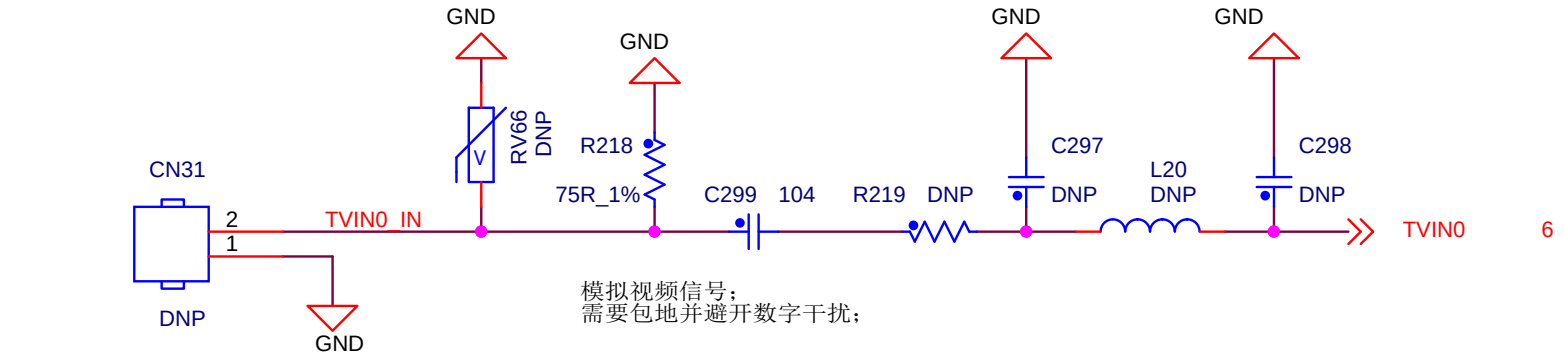
Config for all capability

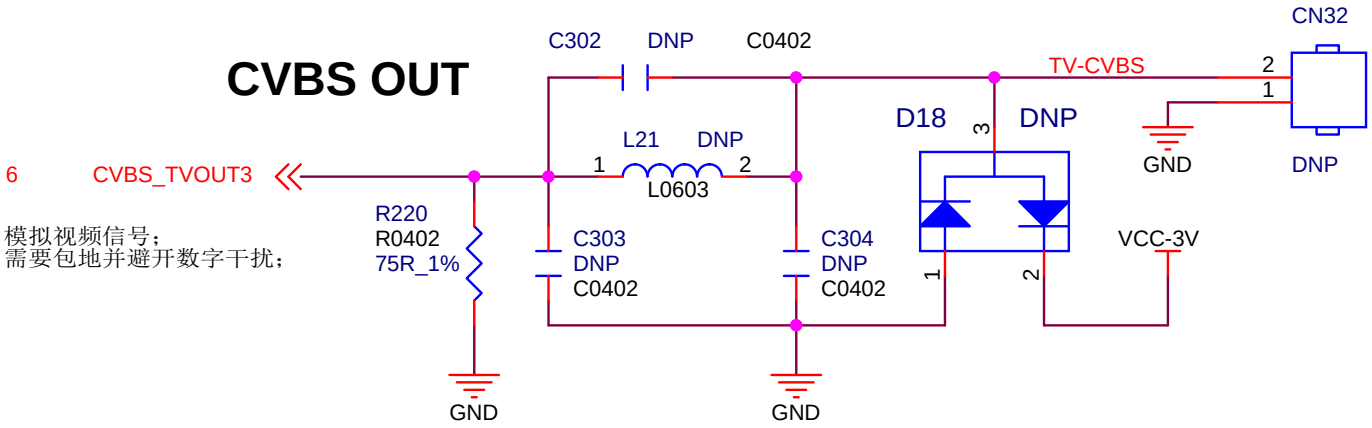
Add TX/RX Delay

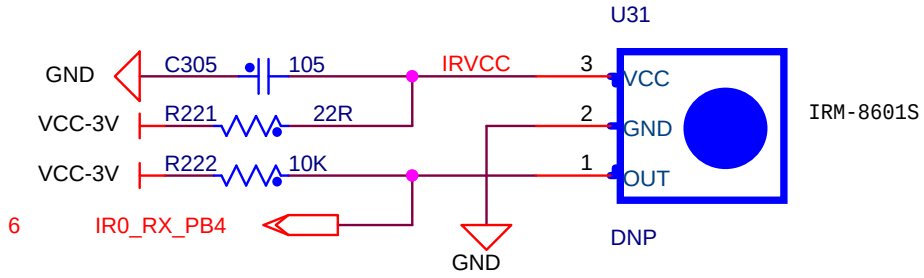
GRXCTL	RXCTL-AD2
GRXD0	RXD0-SELRGV
GRXD1	RXD1-TXDLY
GRXD2	RXD2-AN0
GRXD3	RXD3-AN1

GTXCTL	TXCTL
GTXD0	TXD0
GTXD1	TXD1
GTXD2	TXD2
GTXD3	TXD3

Title:	1000M以太网接口电路原理图	
Size: A3	OrgName: RAINTI	Rev: 1.0
	Designer: 龚俊	Mender: GongJun
Date: Saturday, June 14, 2014	Sheet 17 of 18	







Title: TVIN、CVBS和IR接口电路原理图			
Size	OrgName: RAINTI		Rev
Custom	Designer: 龚俊	Mender: GongJun	1.0
Date: Saturday, June 14, 2014	Sheet 18 of 18		