AXM88180-EVB-RTL8211E-1 SMDK2440 Demo Board Schematic Index

Note:

1.Please refer to AX88180 Gigabit Ethernet Controller Application Design Note for more AX88180 PCB layout design notes.

2.Please deliver us your AX88180 schematic and PCB layout files for further review.

3.Please refer to Appendix A3 of the latest AX88180 datasheet (v1.09 or later) for more details of AX88180 System Power Up Reference Clock Design Considerations.

4.Please contact RealTek's support guys to get the latest RTL8211E reference schematic, PCB Layout Guide and further suggestions before making your PCB board.

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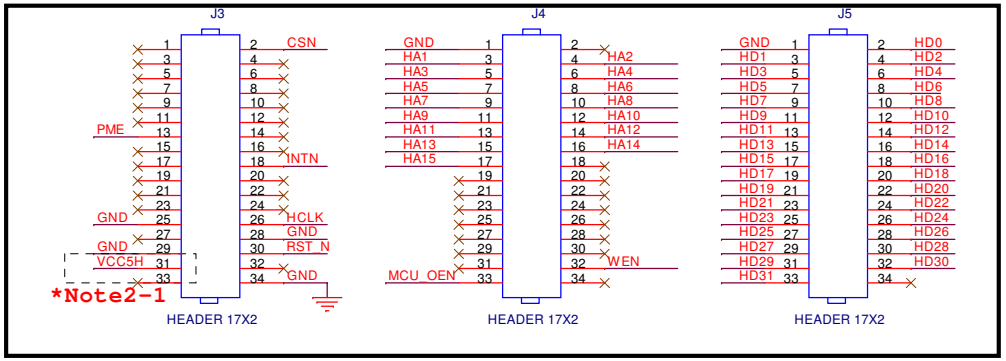
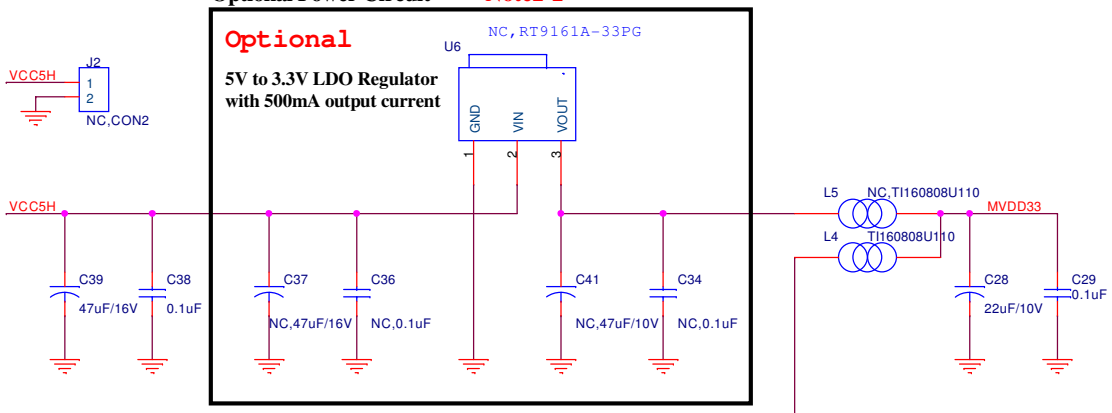
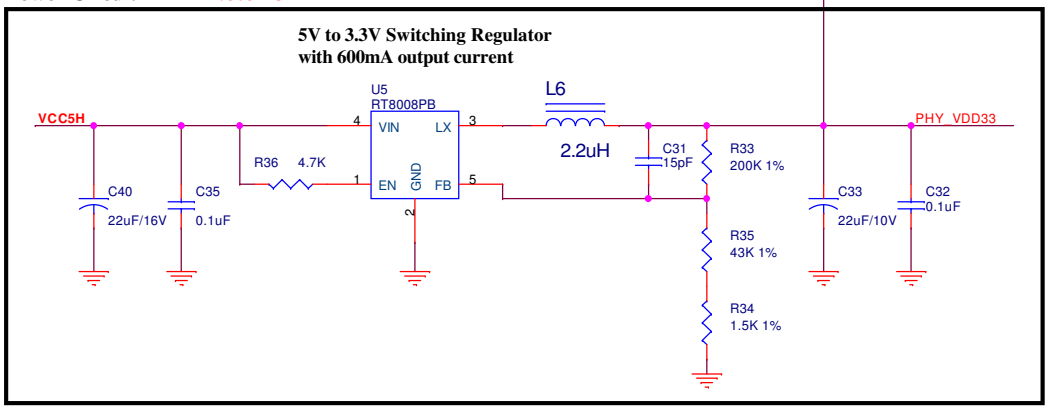
S3C2440 Host Interface Connectors



Optional Power Circuit *Note2-2



Power Circuit *Note2-3



***Note2-1:**
The VCC5H should be kept the trace wider than 200mil. The 5V power trace as short as possible with Regulator input pin and kept the trace over than 100mils as possible.

***Note2-2:**
This power circuit is optional to provide separate 3.3V power sources for AX88180 and RTL8211E. The C37, C36, C41 and C34 as close to Regulator (U6) VIN/VOUT pins for good power efficiency and please kept the trace over than 50mils as possible.

***Note2-3:**
The C40, C35 as close to Regulator (U5) VIN pin for good power regulation and kept the 5V trace wider than 100 mils. The L6, C33 and C32 as close to U5's LX pin for good power swiching.

HD0 HD1 HD2 HD3 HD4 HD5 HD6 HD7 HD8 HD9 HD10 HD11 HD12 HD13 HD14 HD15 3
HD16 HD17 HD18 HD19 HD20 HD21 HD22 HD23 HD24 HD25 HD26 HD27 HD28 HD29 HD30 HD31 3
HA1 HA2 HA3 HA4 HA5 HA6 HA7 HA8 HA9 HA10 HA11 HA12 HA13 HA14 HA15 3
CSN MCU_OEN WEN 3
HCLK 3
RST_N 3,4
INTN PME 3,4
MVDD33 3
PHY_VDD33 4
GND 3,4

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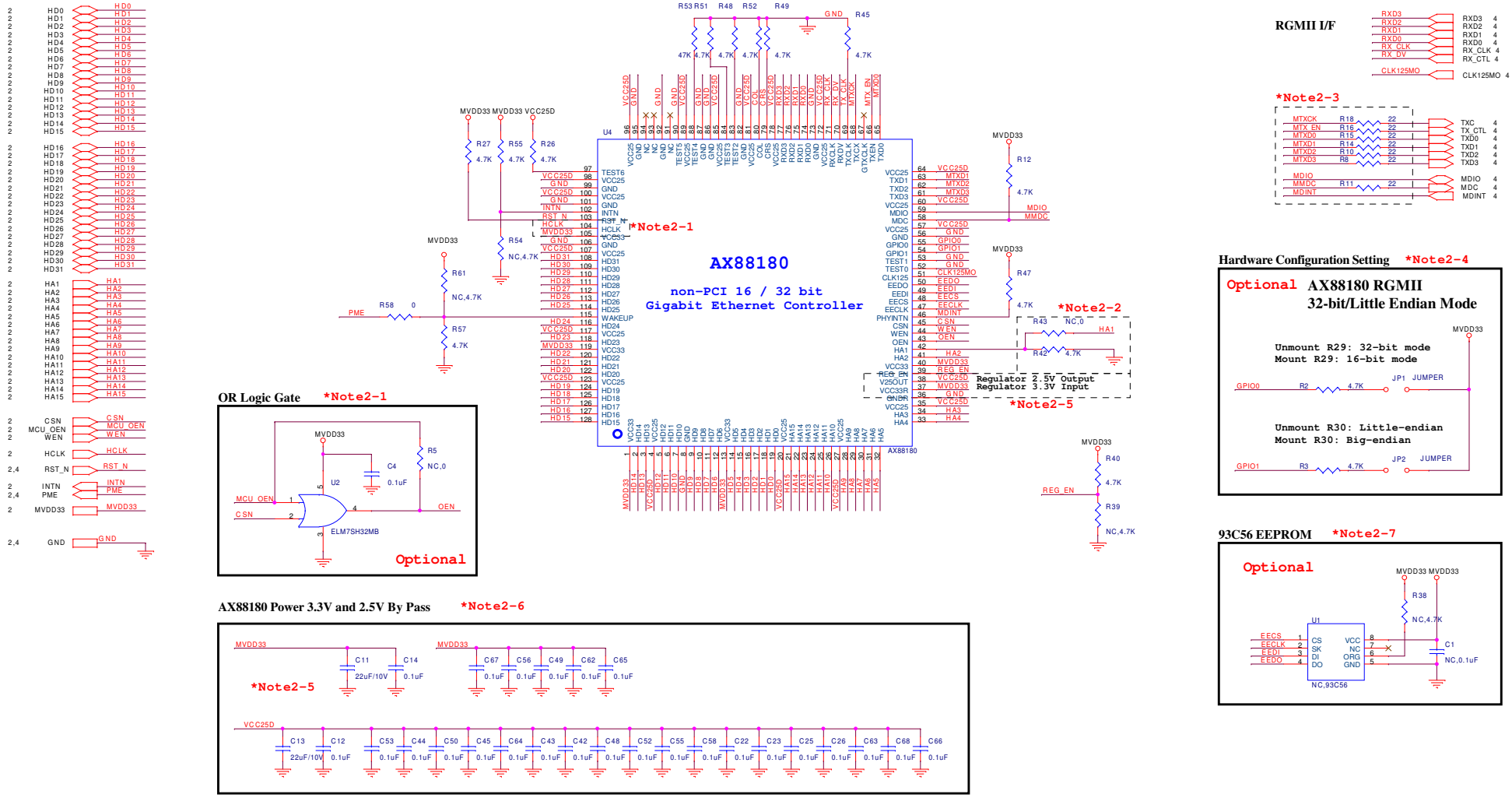

***Note2-1**
The OR logic gate circuit is necessary if the MCU couldn't synchronously provide the host interface clock signals to AX88180 HCLK while powering ON the system. Please refer to Appendix A3 of the latest AX88180 datasheet (v1.09 or later) for more details.
If you need to by-pass the OR gate circuit, please remove U2, C4 and mount R5 with 0 ohm resistor.

***Note2-2**
The HA1 pin should be connected to GND when the MCU is set to the double-word boundary mode on AX88180 32-bit mode applications.
For AX88180 16-bit mode applications, the HA1 pin should be connected to a proper MCU address pin.
Please refer to Appendix A2 of AX88180 datasheet for more details.

***Note2-3**
These 22 Ohm terminal resistors should be as close to AX88180's RGMII interface pins.

***Note2-4**
The AX88180 GPIO 0/GPIO 1 signals are pulled down by hardware default.

***Note2-5**
The VCC33R signal should be wider than 40mils on regulator input trace and C11,C14 as close to VCC33R for good power regulation.
The VCC25OUT signal should be wider than 20mils and C13,C12 as close to VCC25OUT for good power regulation.

***Note2-6**
Every by-pass capacitors should be as close to each power pin to reduce high freqency power noises.

***Note2-7:**
The AX88180 supports 16-bit mode 93C56 EEPROM. The EEPROM is optional if the MAC address can be stored on the Flash memory of your embedded system.

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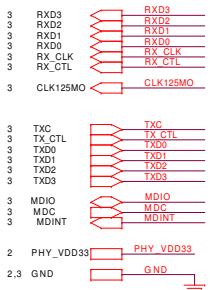
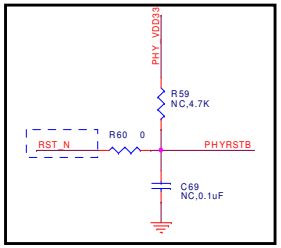
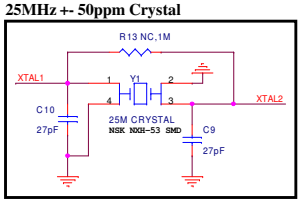


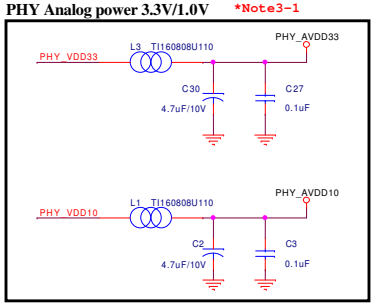
PHY Reset Circuit



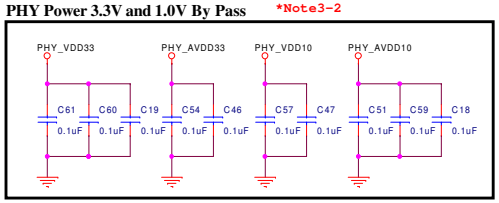
25MHz +- 50ppm Crystal

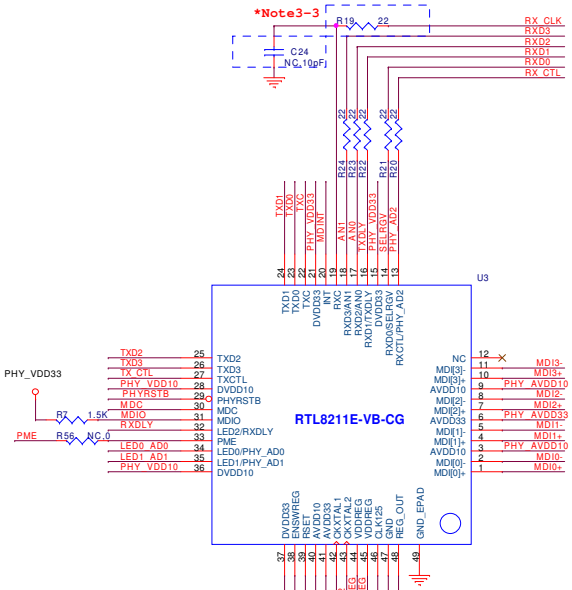


PHY Analog power 3.3V/1.0V *Note3-1

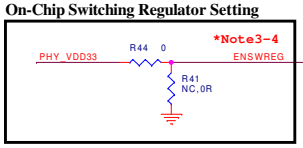


PHY Power 3.3V and 1.0V By Pass *Note3-2

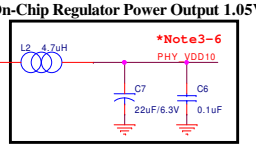




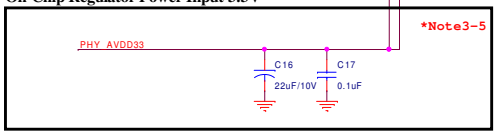
On-Chip Switching Regulator Setting



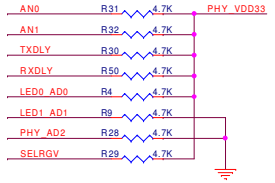
On-Chip Regulator Power Output 1.05V



On-Chip Regulator Power Input 3.3V

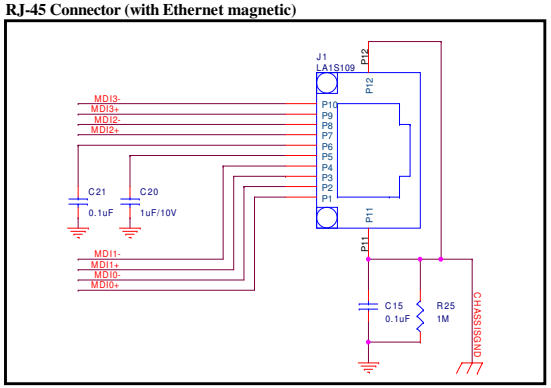


RTL8211E PHY Hardware Configuration

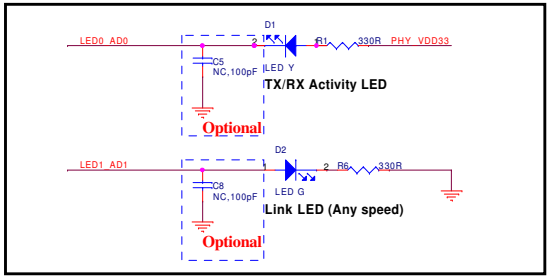


	AN0 Pull High	AN1 Pull High	Enable all Nway capabilities
	TXDLY Pull High	RXDLY Pull High	Delay TXCLK/RXCLK 2ns
AD2 Pull Low	AD1 Pull Low	AD0 Pull High	PHY Address=001 (0x01)
		SELREG Pull High	Pull Up for 3.3V GMII/RGMII

RJ-45 Connector (with Ethernet magnetic)



Ethernet LED Circuit *Note3-7



***Note3-1**
The C30, C27, C2 and C3 should be close to L3 and L1 as possible for reduce power noise.

***Note3-2**
Those 0.1uF by-pass capacitors should be as close to every power input pins as possible.

***Note3-3**
The R19 and C24 are reserved for EMI, please close to PHY as possible.

***Note3-4**
1. Enable On-chip Switch Regulator: (Default)
   Connect ENSWREG to PHY_VDD33 (i.e. Mount R44and unmount R41)
2. Disable On-chip Switch Regulator:
   Connect ENSWREG to GND (i.e. Mount R41 and unmount R44)

***Note3-5**
The 3.3V power input VDDREG trace should be wider than 100mils (Keep floating while disabling on-chip switching regulator)
The capacitors C16 and C17 as close to the VDDREG pin (within 200mils) for good power effeciency.
C16 must be a ceramic (X5R) capacitor
C17 is recommended to be ceramic capacitor

***Note3-6**
L2 (4.7uH) should be as close to RTL8211E REG_OUT pin (within 200mils).
The 1.05V power output REG_OUT trace should be wider than 60 mils.
The C7 and C6 capacitors as close to L2 if possible. (Keep floating while disabling on-chip switching regulator)
C7 must be a ceramic (X5R) capacitor
C6 is recommended to be ceramic capacitor

***Note3-7**
The Ethernet LED circuit is a reference circuit while the PHY Address was set to 01h. (i.e. LED0_AD0 was pulled high and LED1_AD1 was pulled low)
Please refer to Realtek's GigaPHY reference circuit for more details if necessary.
The C5 and C8 are reserved for EMI that should be close to LED0_AD0 and LED1_AD1 pins.

***Note:**
1. The RTL8211E GigaPHY reference circuits are for customers' reference purpose.
Please contact Realtek's support guys to get the latest RTL8211E reference schematic and Layout Guide before making your PCB board.

2. Please exactly follow up Realtek's RTL8211E Layout Guide to layout RTL8211E 3.3V to 1.05V On-chip Switching Regulator and Ethernet magnetic circuits; otherwise,the RTL8211E might not work normally. Please refer to Realtek's layout guide for more details.

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Revision History

Revision	Date	Comment
V1.00	2011/09/07	Initial release.

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