REV	Description	DATE	BY
A4A	Initial production Release.	11/19/2012	GC
A5	On the initial production release the processors were to be found incorrect as supplied by TI. Parts while marked AM3359 were actually AM3352. This revision uses the correct parts.	1/2/2013	GC
A5A	1. Deleted R29-R44 from the LCD lines. 2. Added 47pf capacitors C156-C173 to LCD data lines to ground. 3. Changed schematic revision to A5A. 4. Changed a few footprints after PCB update for above changes. 5. Added access point for the battery function of the TPS65217C. 6. Added Ferrite beads in series with LED power and 5V power rail of the USB host connector. Required to pass FCC/CE testing due to noise emissions on that pin. 7. Added power button to enable sleep, wakeup, power down and power up features on the system. 8. Added Modification to add 100K ohm resistor to ground to prvent crosstalk when serial cable is not plugged in.	2/8/2013	GC
A5B	1. Added 100K pulldown on J1 pin 4 to prvent crosstalk when serial cable is not connected into PCB layout.	4/1/2013	

PAGE NO.	SCHEMATIC PAGE
1	COVER PAGE
2	POWER MANAGEMENT
3	PROCESSOR 1 OF 3, JTAG HEADER
4	PROCESSOR 2 OF 3, UAB PORTS
5	PROCESSOR 3 OF 3
6	LED, CONFIGURATION AND BUTTON
7	DDR3 MEMORY
8	eMMC FLASH
9	10/100 ETHERNET
10	HDMI FRAMER
11	EXP CONN, uSD

NOTE: PCB Revision for this board is Rev B4.

This schematic is *NOT SUPPORTED* and DOES NOT constitute a reference design. Only “community” support is allowed via resources at BeagleBoard.org/discuss.

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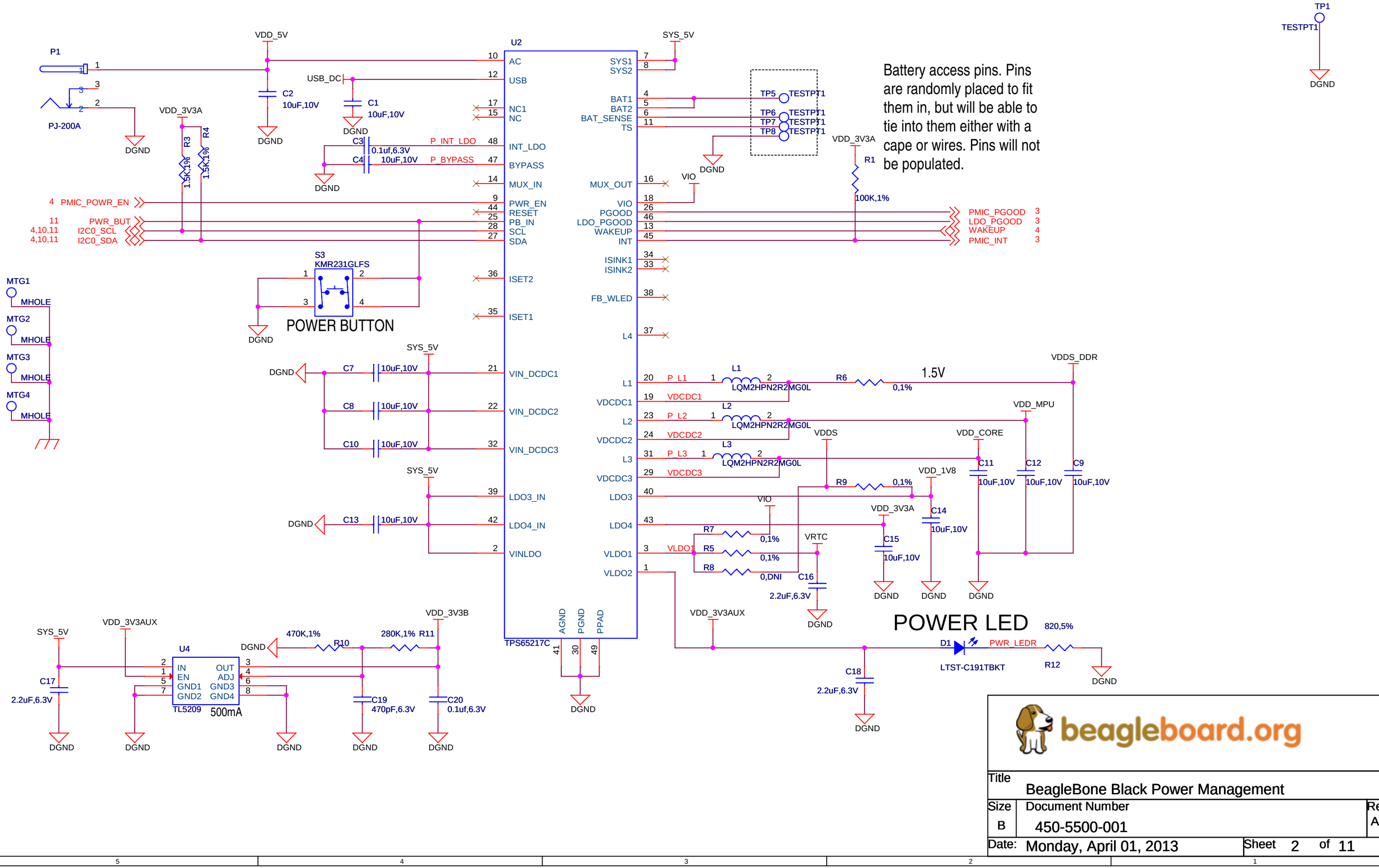
Title	BeagleBone Black Cover Page	
Size: B	Document Number: 450-5500-001	Rev: A5B
Date: Monday, April 01, 2013	Sheet 1 of 11	



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Title	BeagleBone Black Power Management	
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SubArctic AM335x

15mm x 15mm
Package

U5A
XAM3359AZCZ100

Clocks

C21 18pF,50V
C22 18pF,50V
Y1 32.768kHz MC-306
Y2 24MHz
R17 1M,1%
C25 18pF,50V
C26 18pF,50V
GND_OSC0

OSC0_IN V10
OSC0_OUT U11
GND_OSC0 V11
OSC1_IN A6
OSC1_OUT A4
GND_OSC1 A5

Power / Reset

3.3V
S1 KMR231GLFS
RESET
R14 10K,1%
C24 1uF,10V
DGND
VDD_3V3A

2 LDO_PGOOD
2 PMIC_PGOOD

PORZn B15
NRESET_INOUT A10
1.8V RTC_PORZn B5
SYS_RESETn 9,11

DDR

7 DDR_A[15..0]
DDR_A0 F3
DDR_A1 H1
DDR_A2 E4
DDR_A3 C3
DDR_A4 C2
DDR_A5 B1
DDR_A6 D5
DDR_A7 E2
DDR_A8 D4
DDR_A9 C1
DDR_A10 F4
DDR_A11 F2
DDR_A12 E3
DDR_A13 H3
DDR_A14 H4
DDR_A15 D3

7 DDR_BA[2..0]
DDR_BA0 C4
DDR_BA1 E1
DDR_BA2 B3

7 DDR_D[15..0]
DDR_D0 M3
DDR_D1 M4
DDR_D2 N1
DDR_D3 N2
DDR_D4 N3
DDR_D5 N4
DDR_D6 P3
DDR_D7 P4
DDR_D8 J1
DDR_D9 K1
DDR_D10 K2
DDR_D11 K3
DDR_D12 K4
DDR_D13 L3
DDR_D14 L4
DDR_D15 M1

7 DDR_CLK D2
7 DDR_CLKn D1
7 DDR_CKE G3
7 DDR_CSn H2
7 DDR_CASn F1
7 DDR_RASn G4
7 DDR_WEn B2

7 DDR_DQM0 M2
7 DDR_DQS0 P1
7 DDR_DQSN0 P2
7 DDR_DQM1 J2
7 DDR_DQS1 L1
7 DDR_DQSN1 L2

7 DDR_ODT G1
7 DDR_RESETn G2
J3
DDR_VTP
J4
VREFSSTL
DDR_VREF
C28 0.1uf,6.3V
DDR_VTP
R22 49.9,1%
DGND

Boot / JTAG

NMI B18
EVENT_INTR0/TIMER4/CLKOUT1/SPI1_CS1/PR1PRU1R31_16/EMU2/GPIO0_19 A15
EVENT_INTR1/TCLKIN/CLKOUT2/TIMER7/PR1PRU0_PRUR31_16/EMU3/GPIO0_20 D14
PROC_A15 R18 33 XDMA_EVENT_INTR0
CLKOUT_SRC R19 0,1%
PMIC_INT 2
CLKOUT2 3,11
R20 0,1%
GPIO3_20 4

NTRST B10 JTAG_TRSTn
TMS C11 JTAG_TMS
TDI B11 JTAG_TDI
TCK A12 JTAG_TCK
TDO A11 JTAG_TDO
EMU0/GPIO3_7 C14 JTAG_EMU0
EMU1/GPIO3_8 B14 JTAG_EMU1

GPMC

GPMC_CLK/LCD_MEM_CLK/GPMC_WAIT1/MMC2_CLK/PRT1_MII1_TXEN/MCASP0_FSR/GPIO2_1 V12 GPIO2_1 11
GPMC_CSN0/GPIO1_29 V6 GPIO1_29 11
GPMC_CSN1/GPMC_CLK/MMC1_CLK/PRT1EDIO_DATA_IN6/PRT1_EDIO_DATA_OUT6/PR1_PRU1_PRU_R30_12/PR1_PRU1_PRU_R31_12/GPIO1_30 U9 MMC1_CLK 8,11
GPMC_CSN2/GPMC_BE1N/MMC1_CMD/PR1_EDIO_DATA_IN7/PR1_EDIO_DATA_OUT7/PR1_PRU1_PRU_R30_13/PR1_PRU1_PRU_R31_13/GPIO1_31 V9 MMC1_CMD 8,11
GPMC_CSN3/MMC2_CMD/PR1_MDIO_DATA/GPIO2_0 T13 H U5_T13
GPMC_WEN/TIMER6/GPIO2_4 U6 TIMER6 11
GPMC_OEN_REN/TIMER7/EMU4/GPIO2_3 T7 TIMER7 11
GPMC_ADVN_ALE/TIMER4/GPIO2_2 R7 TIMER4 11
GPMC_BE0N_CLE/TIMER5/GPIO2_5 T6 TIMER5 11
GPMC_BE1N/GMII2_COL/GPMC_CSN6/MMC2_DAT3/GPMC_DIR/PR1_MII1_RXLINK/MCASP0_ACLKR/GPIO1_28 U18 GPIO1_28 11
GPMC_WAIT0/GM112_CRS/GPMC_CSN4/RMII2_CRS_DV/MMC1_SDCD/PR1_MII1_RXDV/UART4_RXD/GPIO0_30 T17 UART4_RXD 11
GPMC_WPN/GMII2_RXERR/GPMC_CSN5/RMII2_RXERR/MMC2_SDCD/PR1_MDIO_MDCLK/UART4_TXD/GPIO0_31 U17 UART4_TXD 11

GPMC_AD0/MMC1_DAT0//////GPIO1_0 U7 MMC1_DAT0 8,11
GPMC_AD1/MMC1_DAT1//////GPIO1_1 V7 MMC1_DAT1 8,11
GPMC_AD2/MMC1_DAT2//////GPIO1_2 R8 MMC1_DAT2 8,11
GPMC_AD3/MMC1_DAT3//////GPIO1_3 T8 MMC1_DAT3 8,11
GPMC_AD4/MMC1_DAT4//////GPIO1_4 U8 MMC1_DAT4 8,11
GPMC_AD5/MMC1_DAT5//////GPIO1_5 V8 MMC1_DAT5 8,11
GPMC_AD6/MMC1_DAT6//////GPIO1_6 R9 MMC1_DAT6 8,11
GPMC_AD7/MMC1_DAT7//////GPIO1_7 T9 MMC1_DAT7 8,11
GPMC_AD8/LCD_DATA23/MMC1_DAT0/MMC2_DAT4/EHRPWM2A/PR1_MII_MT0_CLK//GPIO0_22 U10 EHRPWM2A 11
GPMC_AD9/LCD_DATA22/MMC1_DAT1/MMC2_DAT5/EHRPWM2B/PR1_MII0_CRS//GPIO0_23 T10 EHRPWM2B 11
GPMC_AD10/LCD_DATA21/MMC1_DAT2/MMC2_DAT6/EHRPWM2_TRIPZONE_INPUT/PR1_MII0_TXEN//GPIO0_26 T11 GPIO0_26 11
GPMC_AD11/LCD_DATA20/MMC1_DAT3/MMC2_DAT7/EHRPWM2_SYNCI_O/PR1_MII0_TXD3//GPIO0_27 U12 GPIO0_27 11
GPMC_AD12/LCD_DATA19/MMC1_DAT4/MMC2_DAT0/EQEP2A_IN/PR1_MII0_TXD2/PR1_PRU0_PRU_R30_14/GPIO1_12 T12 GPIO1_12 11
GPMC_AD13/LCD_DATA18/MMC1_DAT5/MMC2_DAT1/EQEP2B_IN/PR1_MII0_TXD1/PR1_PRU0_PRU_R30_15/GPIO1_13 R12 GPIO1_13 11
GPMC_AD14/LCD_DATA17/MMC1_DAT6/MMC2_DAT2/EQEP2_INDEX/PR1_MII0_TXD0/PR1_PRU0_PRU_R31_14/GPIO1_14 V13 GPIO1_14 11
GPMC_AD15/LCD_DATA16/MMC1_DAT7/MMC2_DAT3/EQEP2_STROBE/PR1_ECAP0_ECAP_CAPIN_APWM_O/PR1_PRU0_PRU_R31_15/GPIO1_15 U13 GPIO1_15 11

GPMC_A0/GMII2_TXEN/RGMII2_TCTL/RMII2_TXEN/GPMC_A16/PR1_MII_MT1_CLK/EHRPWM1_TRIPZONE_INPUT/GPIO1_16 R13 U5_R13
R160 0,1% GPIO1_16 11
GPMC_A1/GMII2_RXDV/RGMII2_RCTL/MMC2_DAT0/GPMC_A17/PR1_MII1_TXD3/EHRPWM1_SYNCI_O/GPIO1_17 V14 GPIO1_17 11
GPMC_A2/GMII2_TXD3/RGMII2_TD3/MMC2_DAT1/GPMC_A18/PR1_MII1_TXD2/EHRPWM1A/GPIO1_18 U14 EHRPWM1A 11
GPMC_A3/GMII2_TXD2/RGMII2_TD2/MMC2_DAT2/GPMC_A19/PR1_MII1_TXD1/EHRPWM1B/GPIO1_19 T14 EHRPWM1B 11
GPMC_A4/GMII2_TXD1/RGMII2_TD1/RMII2_TXD1/GPMC_A20/PR1_MII1_TXD0/EQEP1A_IN/GPIO1_20 R14
GPMC_A5/GMII2_TXD0/RGMII2_TD0/RMII2_TXD0/GPMC_A21/PR1_MII1_RXD3/EQEP1B_IN/GPIO1_21 V15 USR0 6
GPMC_A6/GMII2_TXCLK/RGMII2_TCLK/MMC2_DAT4/GPMC_A22/PR1_MII1_RXD2/EQEP1_INDEX/GPIO1_22 U15 USR1 6
GPMC_A7/GMII2_RXCLK/RGMII2_RCLK/MMC2_DAT5/GPMC_A23/PR1_MII1_RXD1/EQEP1_STROBE/GPIO1_23 T15 USR2 6
GPMC_A8/GMII2_RXD3/RGMII2_RD3/MMC2_DAT6/GPMC_A24/PR1_MII1_RXD0/MCASP0_ACLKX/GPIO1_24 V16 USR3 6
GPMC_A9/GMII2_RXD2/RGMII2_RD2/MMC2_DAT7/GPMC_A25/PR1_MII_MR1_CLK/MCASP0_FSX/GPIO1_25 U16 HDMI_INT 10
GPMC_A10/GMII2_RXD1/RGMII2_RD1/RMII2_RXD1/GPMC_A26/PR1_MII1_CRS/MCASP0_AXR0/GPIO1_26 T16 USB1_OCn 4
GPMC_A11/GMII2_RXD0/RGMII2_RD0/RMII2_RXD0/GPMC_A27/PR1_MII1_RXER/MCASP0_AXR1/GPIO1_27 V17 HDMICLK_DISn

MMC0_CLK/GPMC_A24/UART3_CTSN/UART2_RXD/DCAN1_TX/PR1_PRU0_PRU_R30_12/PR1_PRU0_PRU_R31_12/GPIO2_30 G17 MMC0_CLKO 11
MMC0_CMD/GPMC_A25/UART3_RTSN/UART2_TXD/DCAN1_RX/PR1_PRU0_PRU_R30_13/PR1_PRU0_PRU_R31_13/GPIO2_31 G18 MMC0_CMD 11
MMC0_DAT0/GPMC_A23/UART5_RTSN/UART3_TXD/UART1_RIN/PR1_PRU0_PRU_R30_11/PR1_PRU0_PRU_R31_11/GPIO2_29 G16 MMC0_DAT0 11
MMC0_DAT1/GPMC_A22/UART5_CTSN/UART3_RXD/UART1_DTRN/PR1_PRU0_PRU_R30_10/PR1_PRU0_PRU_R31_10/GPIO2_28 G15 MMC0_DAT1 11
MMC0_DAT2/GPMC_A21/UART4_RTSN/TIMER6/UART1_DSRN/PR1_PRU0_PRU_R30_9/PR1_PRU0_PRU_R31_9/GPIO2_27 F18 MMC0_DAT2 11
MMC0_DAT3/GPMC_A20/UART4_CTSN/TIMER5/UART1_DCDN/PR1_PRU0_PRU_R30_8/PR1_PRU0_PRU_R31_8/GPIO2_26 F17 MMC0_DAT3 11

U6 SN74AUC1G74

VDD_3V3A
U6 SN74AUC1G74
12M_LOOP
C27 0.1uf,6.3V
R21 33 12MHZ 10
DGND

CEC Clock for HDMI Framer
Run over ground plane.
Do not cross over plane
breaks.

Y4 24.576MHZ

VDD_3V3A
Y4 24.576MHZ
R167 33 GPIO3_21 6,10,11
C159 0.1uf,6.3V
DGND

External clock to the
McASP0 interface.
Oscillator can be disabled via SW
for power down modes or if
GPIO3_21 needs to be used.

U3 SN74LVC1G06DCK

VDD_3V3A
C158 0.1uf,6.3V
U3 SN74LVC1G06DCK
R162 0,1% eMMC_RSTn 8
DGND

CTI JTAG,DNI

VDD_3V3B
R23 4.75K,1%
P2 CTI JTAG,DNI
JTAG_TMS JTAG_TDI JTAG_TDO JTAG_TCK JTAG_EMU0 SYS_RESETn XDMA_EVENT_INTR0 MMC0_CD 4,11
JTAG_TRSTn JTAG_EMU1 CLKOUT2 3,11
R24 4.75K,1%
R25 4.75K,1%
C30 0.1uf,6.3V
C29 0.1uf,6.3V
DGND

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Title	BeagleBone Black Processor 1 of 3 and JTAG	
Size C	Document Number 450-5500-001	Rev A5B
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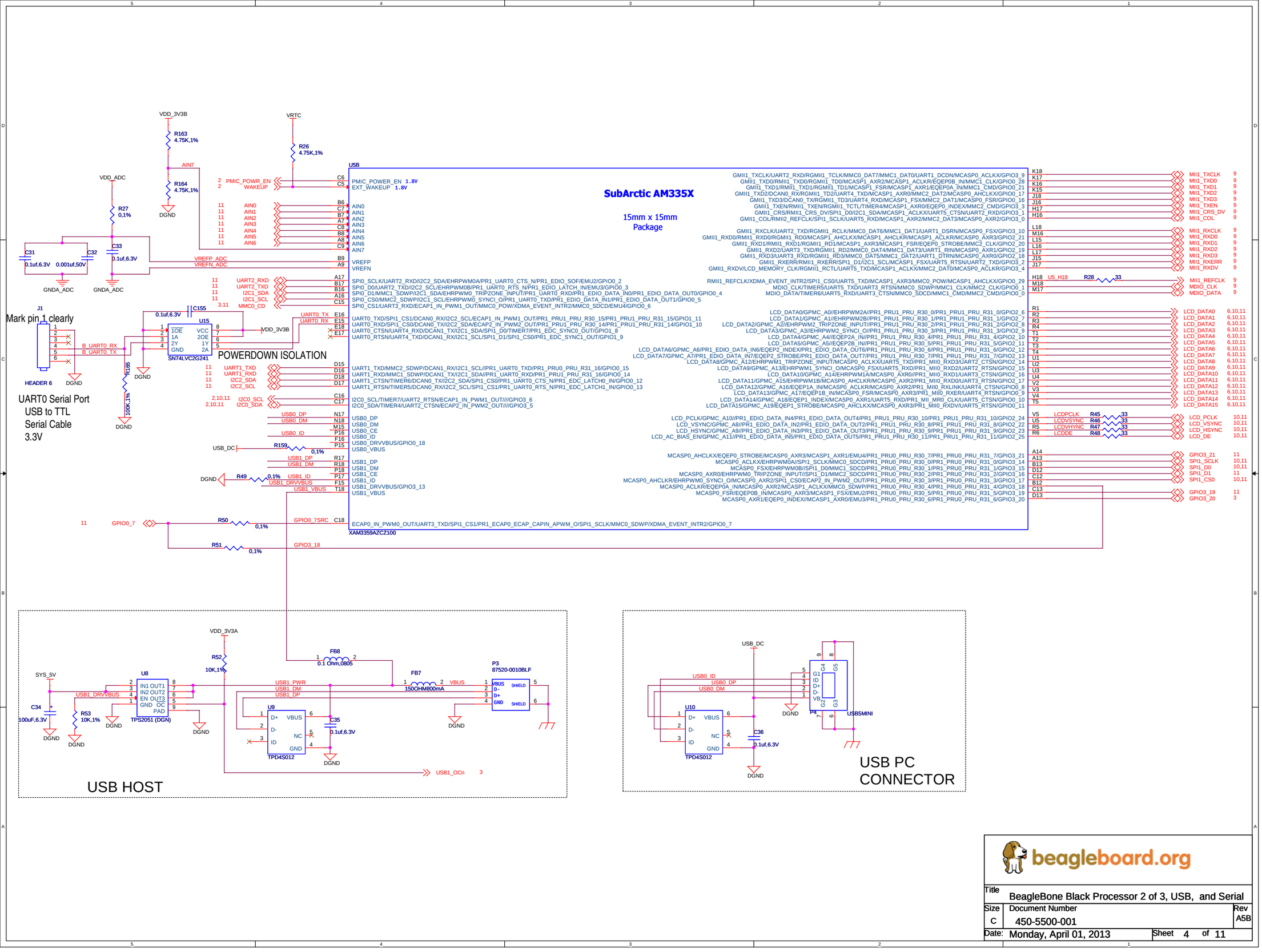
SubArctic AM335X
15mm x 15mm
Package
XAM3359AZCZ100
USB HOST
USB PC
CONNECTOR
POWERDOWN ISOLATION
UART0 Serial Port
USB to TTL
Serial Cable
3.3V
Mark pin 1 clearly
TPS2051 (DGN)
SN74LVC2G241
TPD4S012
USB5MINI
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Title
BeagleBone Black Processor 2 of 3, USB, and Serial
Size
C
Document Number
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A5B
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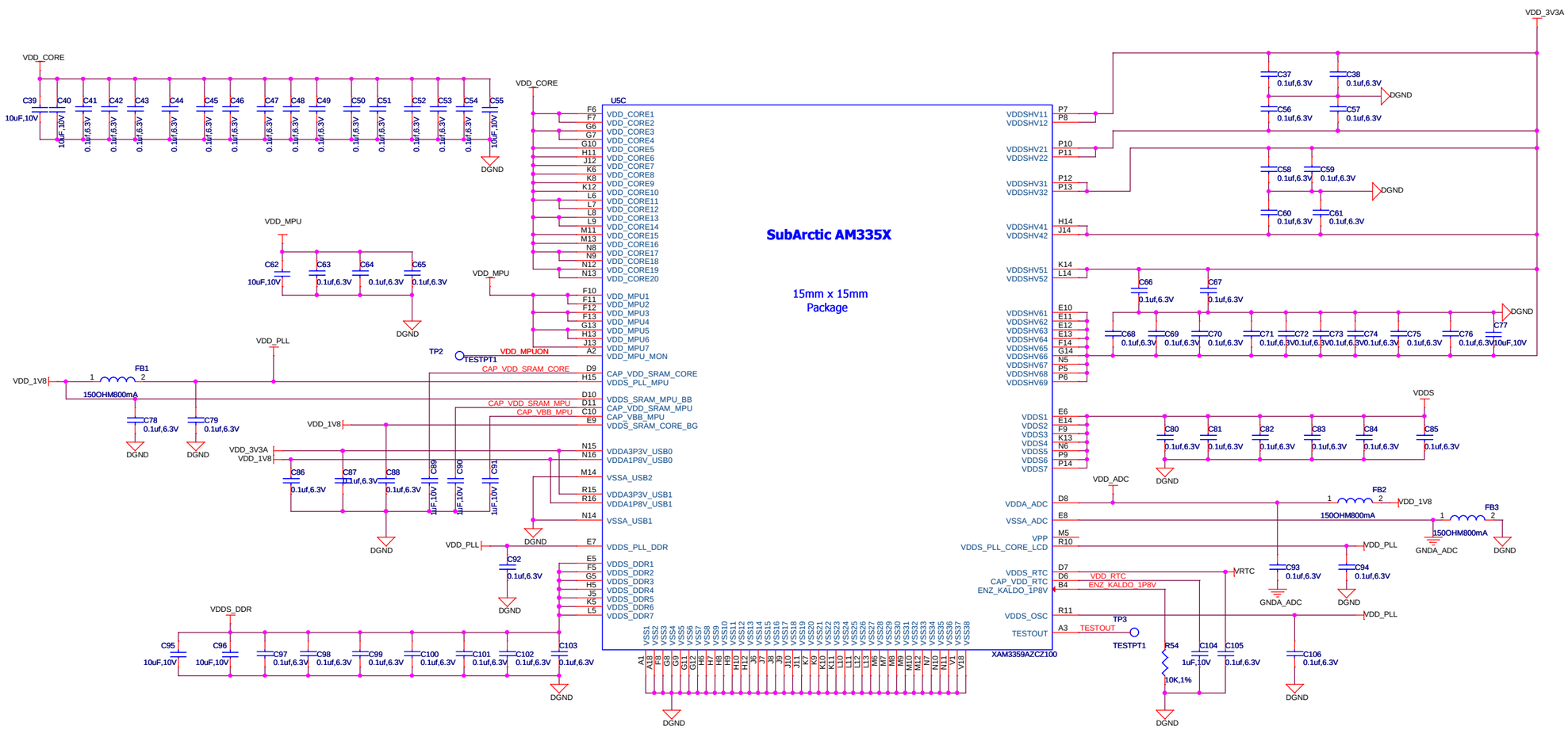
11



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Size C	Document Number 450-5500-001	Rev A5B
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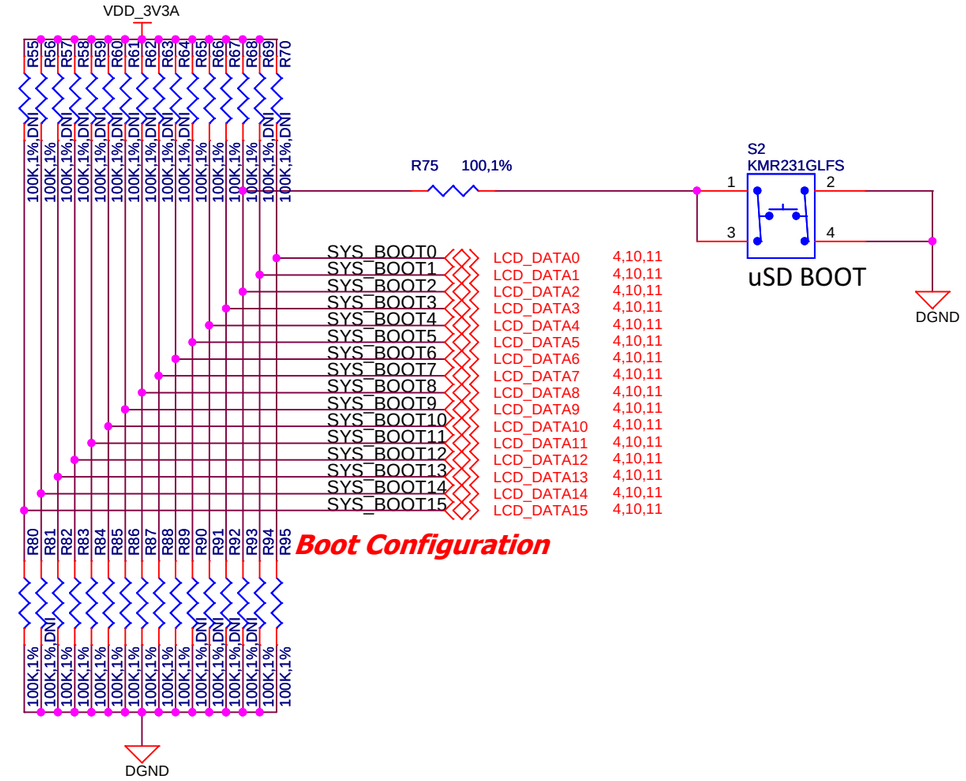

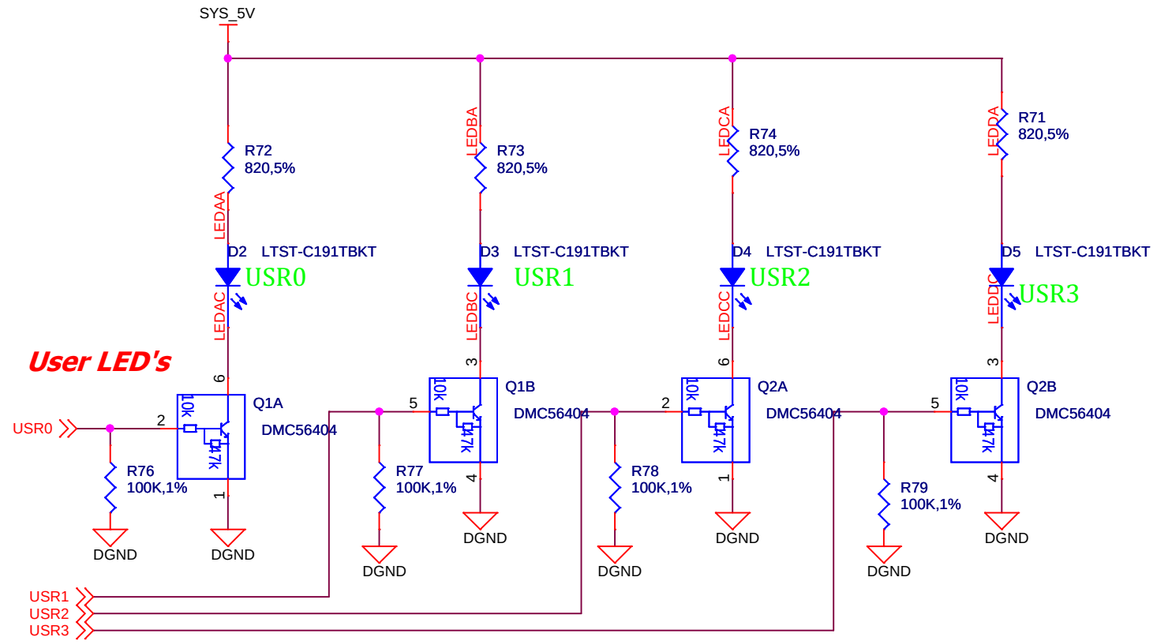

SYSBOOT[15:14]	SYSBOOT[13:12]	SYSBOOT[11:10]	SYSBOOT[9]	SYSBOOT[8]	SYSBOOT[7:6]	SYSBOOT[5]	SYSBOOT[4:0]	Boot Sequence			
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11100b	MMC1	MMC0	UART0	USB0[5]
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11000b	SPI0	MMC0	USB0[5]	UART0

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Title	BeagleBone Black LED, Configuration, and Reset	
Size: B	Document Number: 450-5500-001	Rev: A5B
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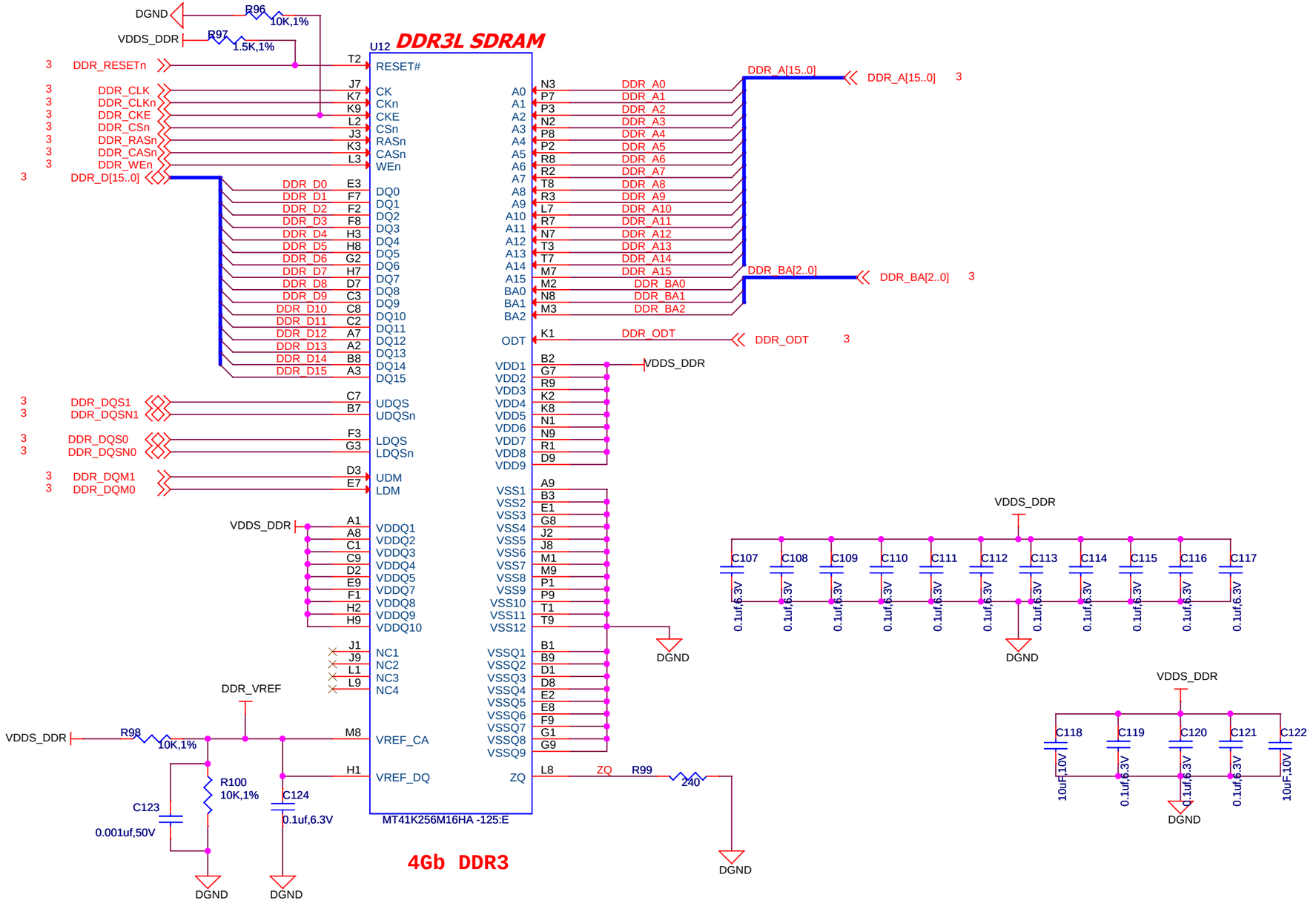

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Title	BeagleBone Black DDR3 Memory	
Size: B	Document Number: 450-5500-001	Rev: A5B
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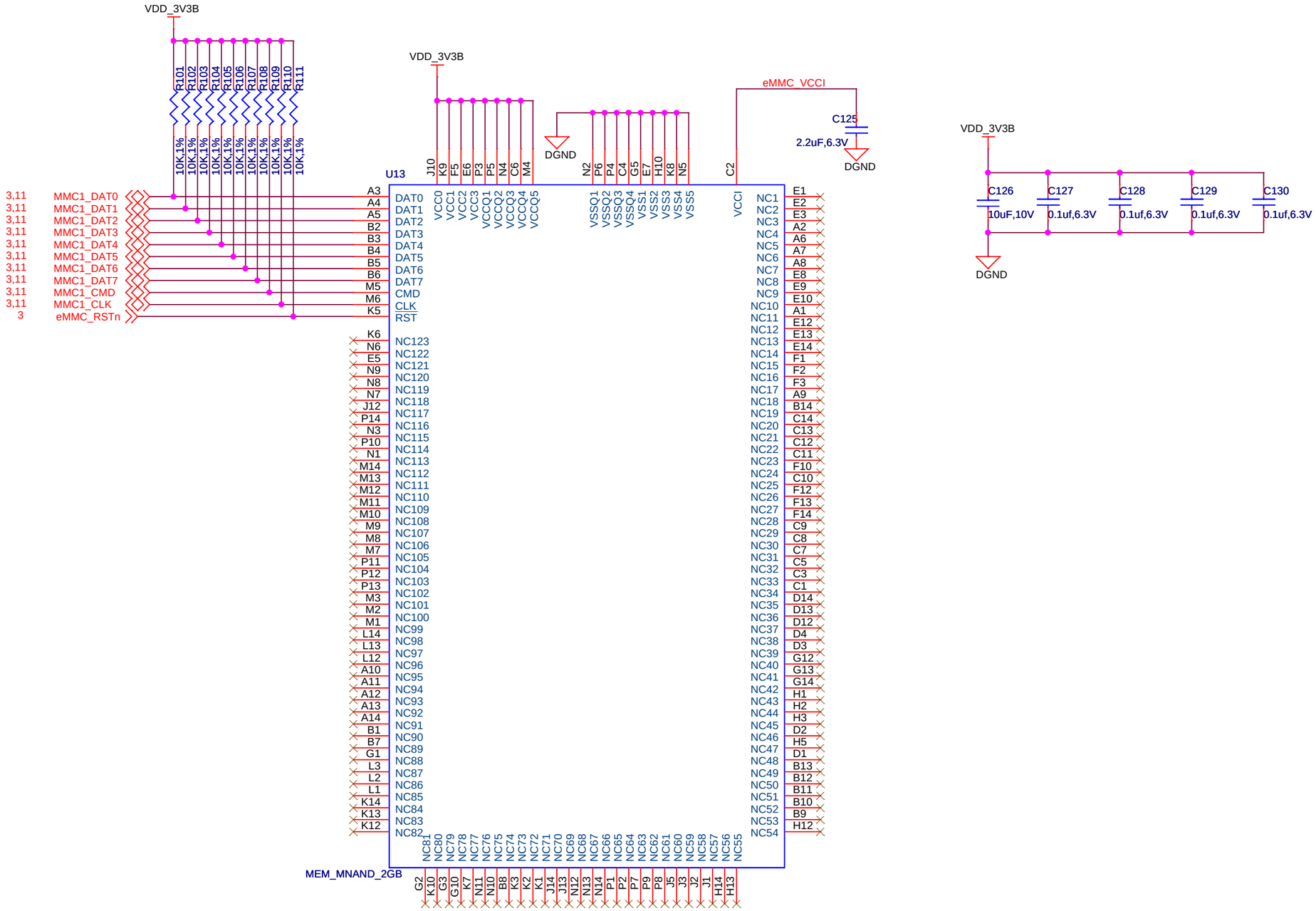

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Title	Beagle BoneBlack 2G eMMC	
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ETHERNET CONNECTOR

U14 LAN8710A

QFN32_5X5MM_EP3P3MM

Power / Clocks

VDD_3V3B, VDD_PHYA, DGND

C131 0.1uf,6.3V
C132 0.1uf,6.3V
C133 10uF,10V
C135 0.1uf,6.3V
C136 470pF,6.3V
C134 1uF,10V
150OHM800mA FB4
R119 1.5K,1%

MII1 MAC Interface

MII1_REFCLK	R124 10,1%,DNI		
MDIO_DATA		MDIO	16
MDIO_CLK		MDC	17
MII1_RXD3	R125 100,1%	RXD3/PHYAD2	8
MII1_RXD2	R126 100,1%	RXD2/RMIISEL	9
MII1_RXD1	R127 100,1%	RXD1/MODE1	10
MII1_RXD0	R128 100,1%	RXD0/MODE0	11
MII1_RXDV	R129 100,1%	RXDV	26
MII1_RXCLK	R131 100,1%	REFCLKO	7
MII1_RXERR	R133 100,1%	RXER/PHYAD0	13
MII1_TXCLK	R134 100,1%	TXCLK	20
MII1_TXEN		TXEN	21
MII1_TXD0		TXD0	22
MII1_TXD1		TXD1	23
MII1_TXD2		TXD2	24
MII1_TXD3		TXD3	25
MII1_COL	R138 100,1%	MODE2	15
MII1_CRS_DV	R139 100,1%	CRS	14
		COL/CRS_DV/MODE2	
		CRS	

Reset / Crystal

SYS_RESETn 3,11 — R140 0,1%,DNI — nRST 19

R141 1M,1%,DNI — PHY_XTAL1 — R142 0,1% — RCLKIN 5 — XTAL1/CLKIN

PHY_XTAL2 — XTAL2 4

R143 10,1%

Y3 25.000MHz XTAL150SMD_125X196 (PHYX, 2, 1)

C142 30pF,50V
C143 30pF,50V

RMII Data

TXP	29	TXP
TXN	28	TXN
RXP	31	RXP
RXN	30	RXN

C137 15pF,DNI
C138 15pF,DNI
C139 15pF,DNI
C140 15pF,DNI

R120 49.9,1%
R121 49.9,1%
R122 49.9,1%
R123 49.9,1%

LED / Misc

LED1/REGOFF	3	ACTIVE WHEN LINK PRESENT. BLINKS OFF DURING ACTIVITY.
LED2/nINTSEL	2	ACTIVE WHEN AT 100MB
nINT/TXER/TXD4	18	ETH_TXD4
RBIAS	32	RBIAS

R144 12.1K,1%
R145 10K,1%

GND_EP 33

Strap Resistors

REFCLKO — R115 10K,1%
RXD2/RMIISEL — R116 10K,1%
RXD3/PHYAD2 — R117 10K,1%
RXER/PHYAD0 — R118 10K,1%

MODE2 — R113 1.3K,1%
RXD1/MODE1 — R114 1.5K,1%
RXD0/MODE0 — R112 1.5K,1%

P9 RJ45

TCT	5		
TD+	3		
TD-	6		
RD+	1	NC	7
RD-	2		
RCT	4	GND	8
YELC	11	SHD1	13
YELA	12	SHD2	14
GRNC	10		
GRNA	9		

LPJ0011BBNL

R130 470,5% — YEL_C
R132 470,5% — GRN_C

R135 10K,1%

TCT_RCT — R137 0,1% — VDD_PHYA

C141 0.022uF,10V

R136 ESD_RING 1,0805

Title	BeagleBone Black Ethernet
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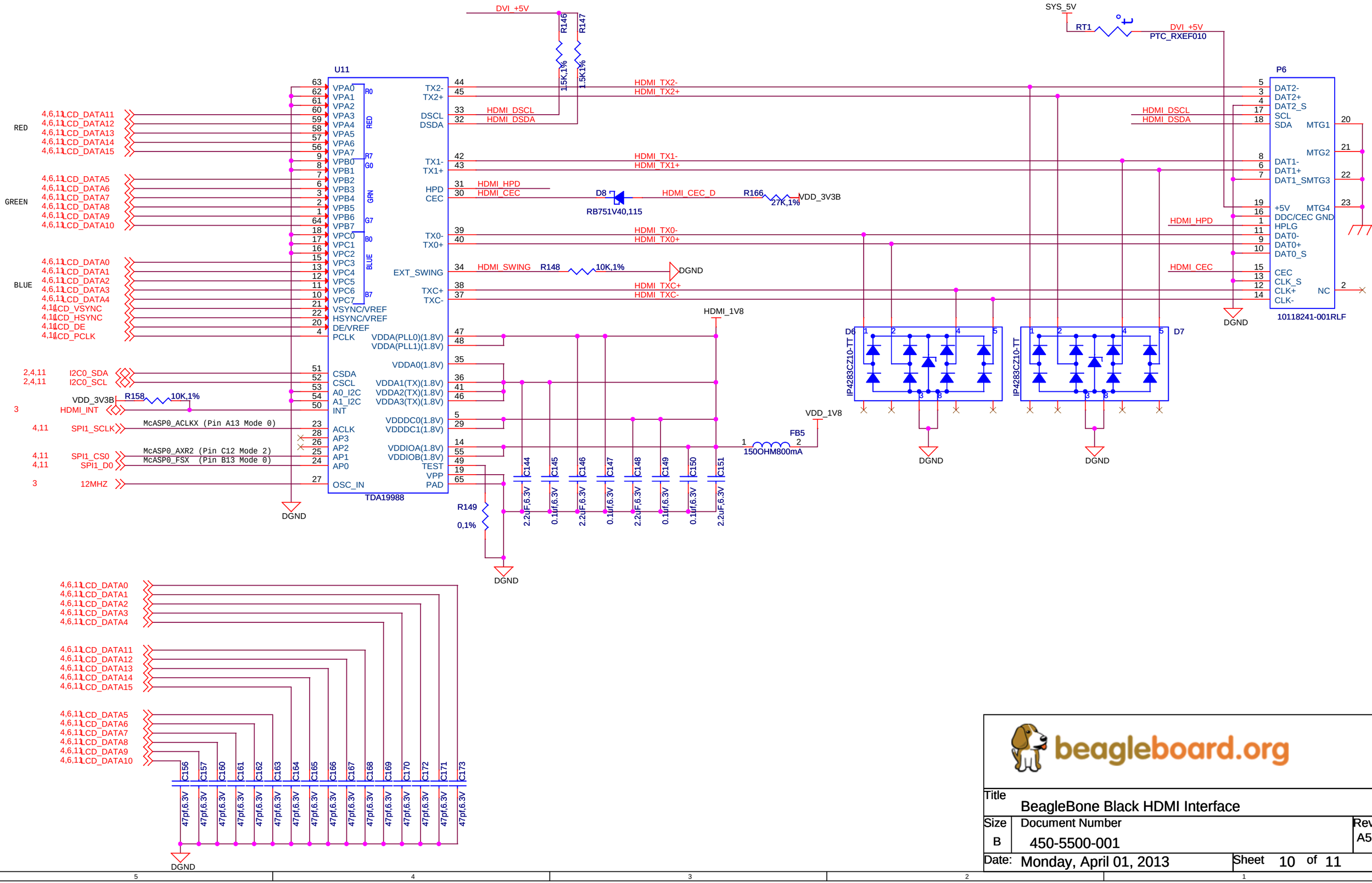

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Title	BeagleBone Black HDMI Interface	
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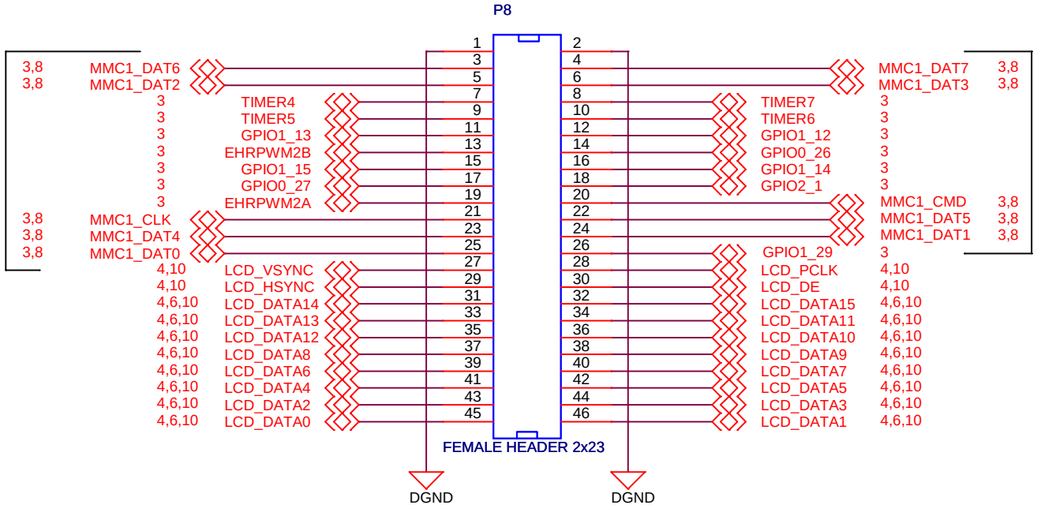
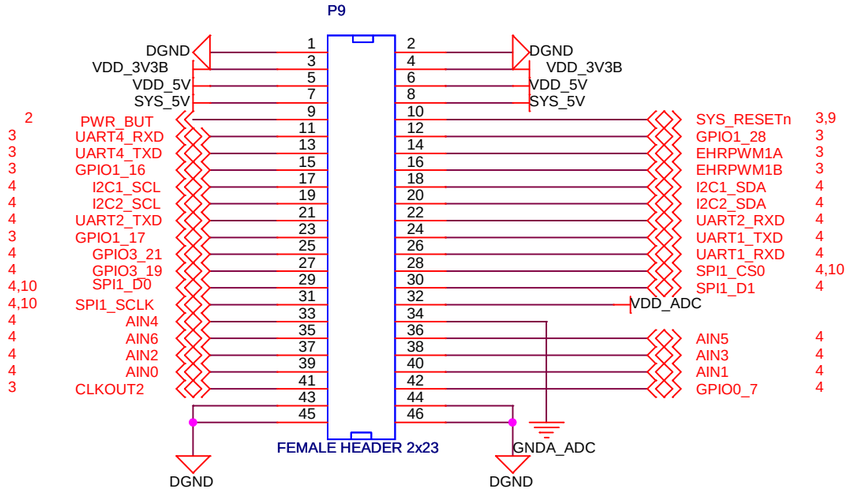
CAUTION: USED ON BOARD

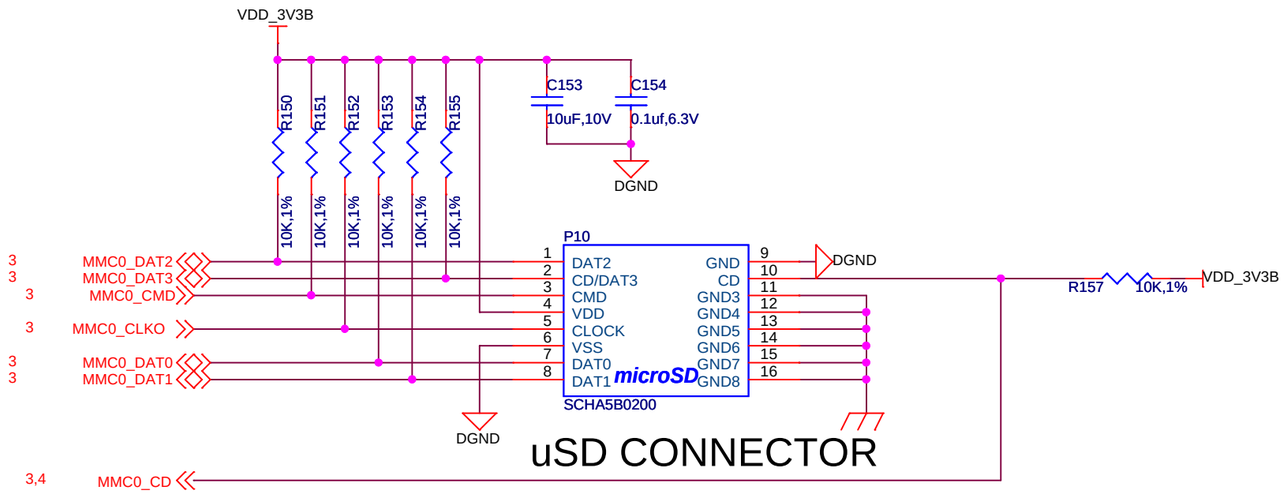


EXPANSION HEADER

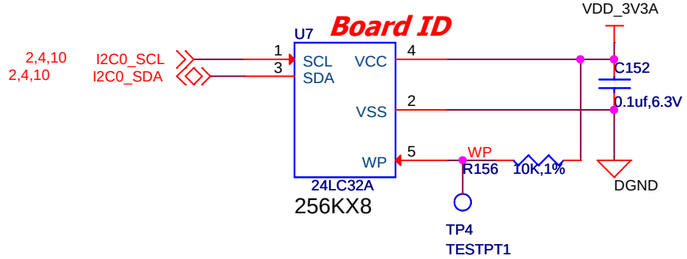
CAUTION: USED ON BOARD



EXPANSION HEADER



uSD CONNECTOR



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