RTL8723AS-CG

SINGLE-CHIP IEEE 802.11b/g/n 1T1R WLAN with Integrated Bluetooth 2.1/ 3.0/ 4.0 CONTROLLER With SDIO and HS-UART Mixed INTERFACE

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.6	2011/12/20	Preliminary release
0.7	2012/1/10	1. RF Interface Pin Description Modification for DPDT_SEL_P and DPDT_SEL_N
0.7r4	2012/1/11	1. Modify Pin Assignments Fig. 4 2. Add Power On Trap Pin Definition Table 3. modify pin 11 description

Table of Contents

List of Tables

List of Figures

1. General Description

The Realtek RTL8723AS is a highly integrated single-chip 802.11n Wireless LAN (WLAN) network SDIO interface (SDIO 1.1/ 2.0/ 3.0 compliant) controller and Bluetooth 2.1/ 3.0/ 4.0 HS-UART interface controller. It combines a WLAN MAC, a 1T1R capable WLAN baseband, BT Protocol Stack (LM, LL and LE), BT Baseband, modem, and WLAN/BT RF in a single chip. The RTL8723AS provides a complete solution for a high throughput performance integrated wireless LAN and Bluetooth device.

The RTL8723AS WLAN baseband implements Orthogonal Frequency Division Multiplexing (OFDM) with 1 transmit and 1 receive path and is compatible with the IEEE 802.11n specification. Features include one spatial stream transmission, short guard interval (GI) of 400ns, spatial spreading, and transmission over 20MHz and 40MHz bandwidth.

For legacy compatibility, Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK) and OFDM baseband processing are included to support all IEEE 802.11b and 802.11g data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability, are available, and CCK provides support for legacy data rates, with long or short preamble. The high-speed FFT/IFFT paths, combined with BPSK, QPSK, 16QAM, and 64QAM modulation of the individual subcarriers and rate compatible punctured convolutional coding with coding rate of 1/2, 2/3, 3/4, and 5/6, provide higher data rates of 54Mbps and 150Mbps for IEEE 802.11g and 802.11n OFDM respectively.

The RTL8723AS WLAN Controller builds in an enhanced signal detector, an adaptive frequency domain equalizer, and a soft-decision Viterbi decoder to alleviate severe multi-path effects and mutual interference in the reception of multiple streams. Robust interference detection and suppression are provided to protect against Bluetooth, cordless phone, and microwave oven interference.

Efficient IQ-imbalance, DC offset, phase noise, frequency offset, and timing offset compensations are provided for the radio frequency front-end. Selectable digital transmit and receive FIR filters are provided to meet transmit spectrum mask requirements and to reject adjacent channel interference, respectively.

The RTL8723AS WLAN Controller supports fast receiver Automatic Gain Control (AGC) with synchronous and asynchronous control loops among antennas, antenna diversity functions, and adaptive transmit power control function to obtain the better performance in the analog portions of the transceiver.

The RTL8723AS WLAN MAC supports 802.11e for multimedia applications, 802.11i for security, and 802.11n for enhanced MAC protocol efficiency. Using packet aggregation techniques such as A-MPDU with BA and A-MSDU, protocol efficiency is significantly improved. Power saving mechanisms such as Legacy Power Save, and U-APSD, reduce the power wasted during idle time, and compensates for the extra power required to transmit OFDM. The RTL8723AS provides simple legacy and 20MHz/40MHz co-existence mechanisms to ensure backward and network compatibility.

The RTL8723AS Bluetooth controller complies with Bluetooth core specifications v4.0 and supports dual mode (BR/EDR + AMP + Low Energy Controllers). It can compatible with previous versions, including v2.1 + EDR and v3.0 + HS. For BR/EDR, it supports scatternet topology and allows four active links in slave mode and seven active links in master mode. For Low Energy, it supports multiple states and allows eight active links in master mode. The links in BR/EDR and LE can be active simultaneously.

2. Features

General

- 68-pin QFN
- CMOS MAC, Baseband PHY, and RF in a single chip for IEEE 802.11b/g/n compatible WLAN
- Complete 802.11n solution for 2.4GHz band
- 72.2Mbps receive PHY rate and 72.2Mbps transmit PHY rate using 20MHz bandwidth
- 150Mbps receive PHY rate and 150Mbps transmit PHY rate using 40MHz bandwidth
- Compatible with 802.11n specification
- Backward compatible with 802.11b/g devices while operating in 802.11n mode
- Qualified Bluetooth v2.1 and v3.0 Systems
- Support for Bluetooth Low Energy
- Integrated class 1, class 2, and class 3 PA and modem in Bluetooth Controller

Host Interface

- Complies with SDIO 1.1/ 2.0/ 3.0 for WLAN with clock rate up to 100MHz
- GSPI interface for configurable endian for WLAN
- Complies with HS-UART with configurable baud rate for Bluetooth

Standards Supported

- IEEE 802.11b/g/n compatible WLAN
- IEEE 802.11e QoS Enhancement (WMM)
- 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services

WLAN MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate High-Throughput Block Acknowledgement (HT-BA)
- PHY-level spoofing to enhance legacy compatibility
- Power saving mechanism
- Channel management and co-existence
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth

WLAN PHY Features

- IEEE 802.11n OFDM
- One Transmit and one Receive path (1T1R)
- 20MHz and 40MHz bandwidth transmission
- Short Guard Interval (400ns)
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, and 64QAM modulation.
  Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- Maximum data rate 54Mbps in 802.11g and 150Mbps in 802.11n
- Switch diversity for DSSS/CCK

- Hardware antenna diversity in per packet base
- Selectable receiver FIR filters
- Programmable scaling in transmitter and receiver to trade quantization noise against increased probability of clipping
- Fast receiver Automatic Gain Control (AGC)
- On-chip ADC and DAC

BT Controller

- HS-UART interface for BT data transmission compliant with H4 and H5 specification
- PCM interface for audio data transmission via BT controller.
- Integrated MCU to execute Bluetooth protocol stack
- Support all packet types in basic rate and enhanced data rate
- Support SCO / eSCO link (allow one link for PCM interface and three links for HS-UART)
- Support 4 piconets in a scatternet
- Support Secure Simple Pairing
- Support Low Power Mode (Sniff / Sniff Sub-rating / Hold / Park)
- Enhanced BT/WIFI Coexistence Control to improve transmission quality in different profiles
- Bluetooth 4.0 Dual Mode support: Simultaneous LE and BR/EDR
- Support multiple states of Low Energy to increase the flexibility of application

Bluetooth Transceiver Features

- Fast AGC control to improve receiving dynamic range
- Support AFH to dynamically detect channel quality to improve transmission quality
- Integrated internal class 1, class 2, and class 3 PA
- Bluetooth 3.0+HS compliant
- Power Control / Enhanced Power Control Supported
- Bluetooth Low Energy supported
- Integrated 32K oscillator for power management

Peripheral Interfaces

- General Purpose Input/Output (8 pins)
- 4-wire EEPROM control interface (93C46)
- Three configurable LED pins

3. Application Diagram

3.1. Single-Band 11n (1x1) Solution with Integrated Bluetooth Controller with Dual Antenna

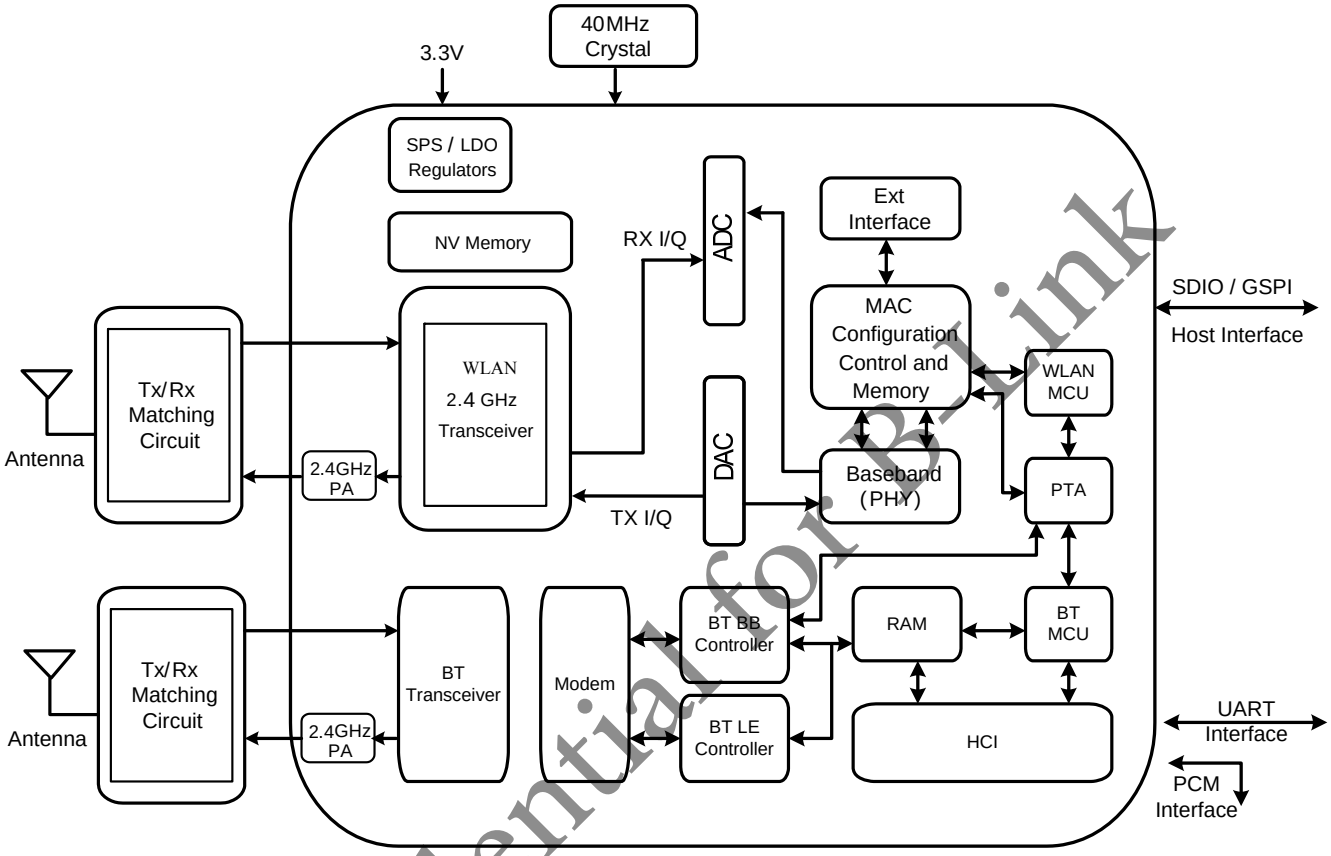


Figure 1. Single-Band 11n (1x1) and Integrated Bluetooth Controller Solution

3.2. Single-Band 11n (1x1) Solution (11n 1x1 MAC/BB/RF) with Antenna Diversity

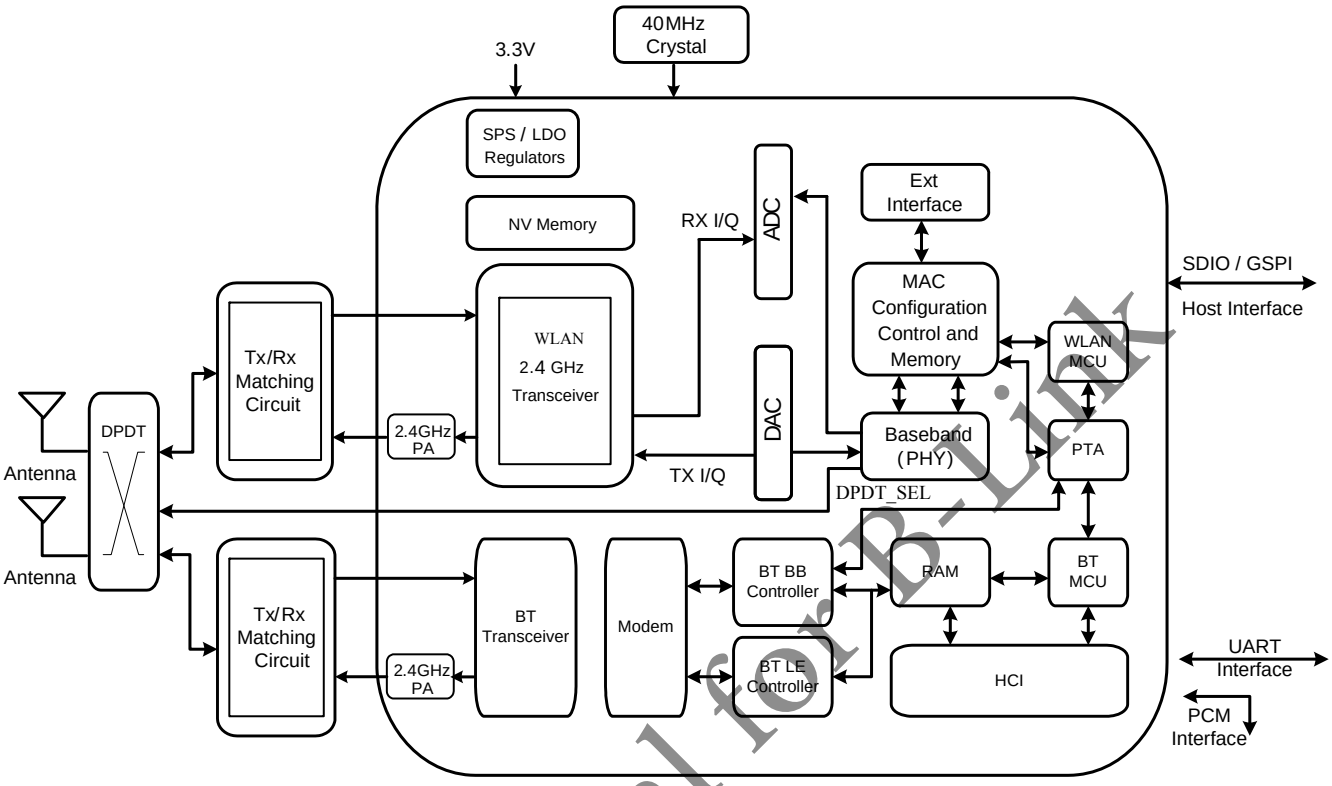


Figure 2. Single-Band 11n (1x1) Solution and Integrated Bluetooth Controller with Antenna Diversity

3.3. Single-Band 11n (1x1) Solution (11n 1x1 MAC/BB/RF) with Single Antenna

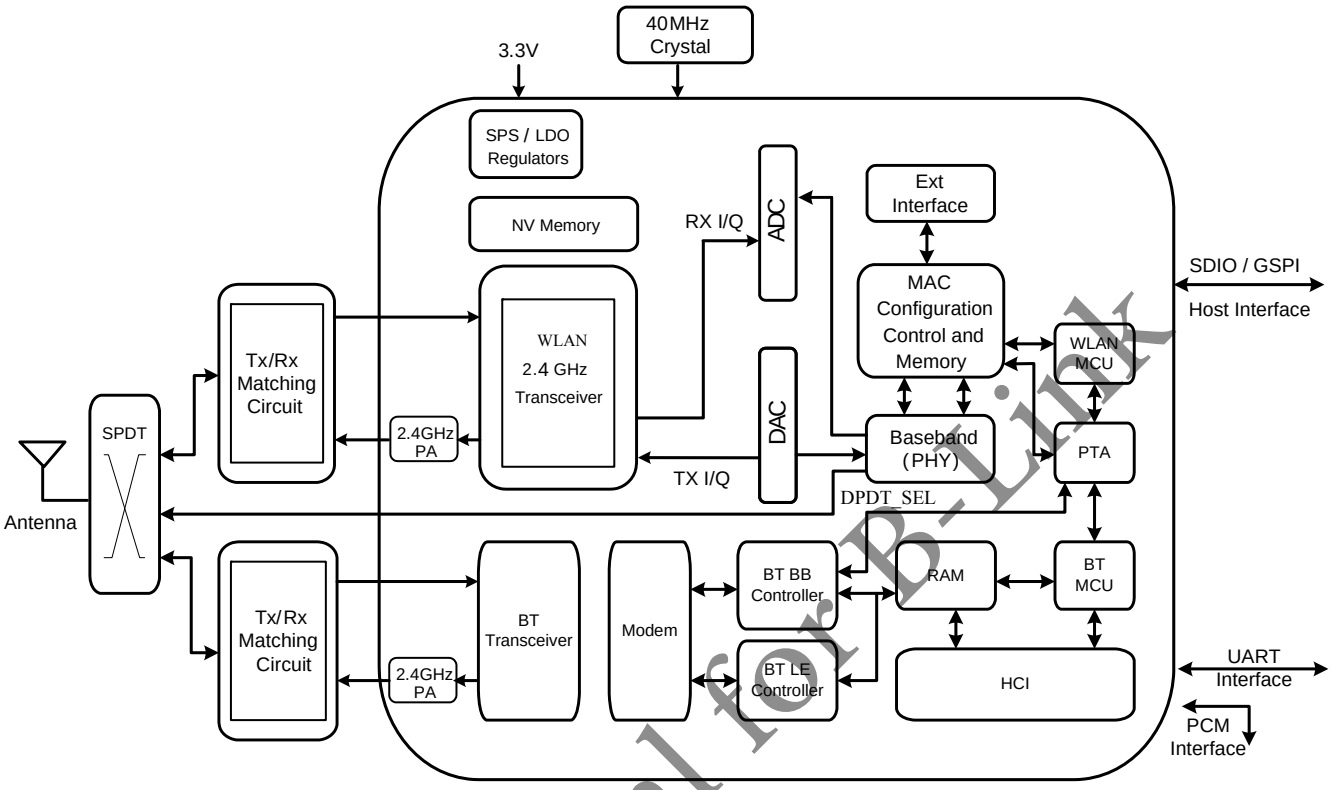


Figure 3. Single-Band 11n (1x1) Solution and Integrated Bluetooth Controller with single Antenna

4. Pin Assignments

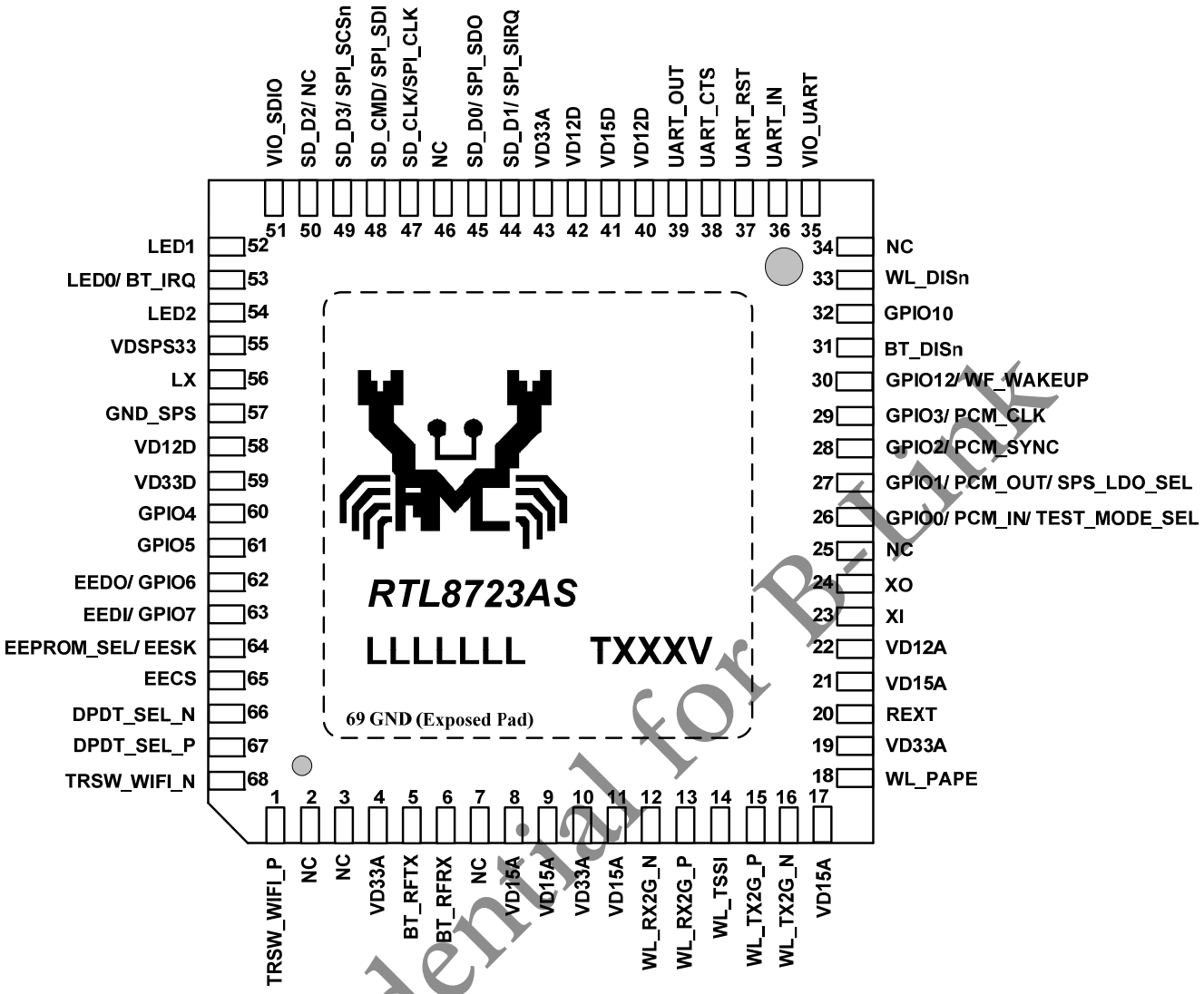


Figure 4. Pin Assignments

4.1. Package Identification

'Green' package is indicated by a 'G' in the location marked 'T' in Figure 4.

5. Pin Descriptions

The following signal type codes are used in the tables:

I: Input O: Output

T/S: Tri-State bi-directional input/output pin S/T/S: Sustained Tri-State

O/D: Open Drain P: Power pin

5.1. Power On Trap Pin

Table 1. SDIO Interface

Symbol	Type	Pin No	Description
TEST_MODE_SEL	I	26	Power On Value = "0": normal operation mode Power On Value = "1": Enter into test/ debug mode
SPS_LDO_SEL	I	27	Power On Value = "0": Internal switching regulator select Power On Value = "1": Internal LDO select
EEPROM_SEL		64	Power On Value = "0": Internal NV memory select Power On Value = "1": External EEPROM select

5.2. SDIO Interface

Table 2. SDIO Interface

Symbol	Type	Pin No	Description
SD_CLK	I	47	SDIO Clock Input
SD_CMD	I/O	48	SDIO Command Input
SD_D0	I/O	45	SDIO Data Line 0
SD_D1	I/O	44	SDIO Data Line 1
SD_D2	I/O	50	SDIO Data Line 2
SD_D3	I/O	49	SDIO Data Line 3

The SDIO interface selection can be referred to subsection 6.5.1, "SDIO Power on Sequence".The signal level section of SDIO interface selection can be referred to subsection 6.5.1, "SDIO/GSPI Signal Level".

5.3. GSPI Interface

Table 3. GSPI Interface

Symbol	Type	Pin No	Description
SPI_CLK	I	47	GSPI Clock Input
SPI_SDI	I	48	GSPI Data Input
SPI_SDO	O	45	GSPI Data Out
SPI_SIRQ	O	44	GSPI Interrupt
SPI_SCSn	I	49	GSPI Chip Select Bar

The GSPI interface pins are shared with SDIO interface. The GSPI interface selection can be referred to subsection 6.5.1, "GSPI Power on Sequence". The signal level section of SDIO interface selection can be referred to subsection 6.5.1, "SDIO/GSPI Signal Level".

5.4. HS-UART Transceiver Interface

Table 4. HS-UART Interface

Symbol	Type	Pin No	Description
UART_OUT	O	39	High-Speed UART Data Out
UART_CTS	O	38	High-Speed UART CTS
UART_RTS	O	37	High-Speed UART RTS
UART_IN	I	36	High-Speed UART Data In

The selection of signal level of UART interface can be referred to subsection 6.5.2. The characteristics and format of UART interface can be also referred in subsection 6.5.3

5.5. PCM Interface

Table 5. PCM Interface

Symbol	Type	Pin No	Description
PCM_IN	I	26	PCM Input
PCM_OUT	O	27	PCM Out
PCM_SYNC	O	28	PCM Sync
PCM_CLK	I/O	29	PCM Clock

The selection of signal level of PCM interface can be referred to subsection 6.5.3. The characteristics and format of PCM interface can be also referred in subsection 6.5.3.

5.6. Power Pins

Table 6. Power Pins

Symbol	Type	Pin No	Description
LX	P	56	Switching Regulator Output
VDSPS33	P	55	Switching Regulator Input Or Linear Regulator input from 3.3V to 1.5V
VD33A	P	4, 10, 19, 43	VDD 3.3V for Analog
VD33D	P	59	VDD3.3V for Digital
VIO_SDIO	P	51	VDD for SDIO Pin, the power supply is same as the signal level of SDIO bus (3.3V ~ 1.8V)
VIO_UART	P	35	VDD for UART Pin, the power supply is same as the signal level of UART bus (3.3V ~ 1.8V)
VD15A	P	8, 9, 11, 17, 21	VDD 1.5V for Analog
VD15D	P	41	VDD 1.5V for Digital
VD12A	P	22	Analog 1.2V Regulator Output
VD12D	P	40, 42, 58,	Digital 1.2V Regulator Output
GND_SPS	P	57	Switching Regulator Ground
RETX	P	20	24k (1%) Precision Resistor for Bandgap

5.7. RF Interface

Table 7. RF Interface

Symbol	Type	Pin No	Description
TRSW_WIFI_N	O	68	WLAN RF TX/RX Path Select negative control signal
TRSW_WIFI_P	O	1	WLAN RF TX/RX Path Select Positive control signal
WL_PAPE	O	18	2.4GHz Transmit Power Amplifier Power Enable 0
TSSI	I	14	WLAN PA TSSI control signal
WL_RX2G_N	I	12	RF RX Negative Signal
WL_RX2G_P	I	13	RF RX Positive Signal
WL_TX2G_N	O	16	RF TX Negative Signal
WL_TX2G_P	O	15	RF TX Positive Signal
BT_RFTX	O	5	Bluetooth RFTX signal
BT_RFRX	I	6	Bluetooth RFRX signal
DPDT_SEL_P	O	67	Antenna Control Positive Signal
DPDT_SEL_N	O	66	Antenna Control Negative Signal

5.8. LED Interface

Table 8. LED Interface

Symbol	Type	Pin No	Description
LED0	O	53	LED Pins (Active Low)
LED1	O	52	LED Pins (Active Low)
LED2 GPIO8	O IO	54	LED Pins (Active Low) Shared with GPIO8, can be selected by control register

5.9. Power Management Handshake Interface

Symbol	Type	Pin No	Description
WL_DISn	I	33	This Pin Can Externally Shutdown the RTL8723AS (no requirement for Extra Power Switch) when BT_DISn is pulled low This pin can also support the WLAN Radio-off function with host interface remaining connected.
BT_DISn	I	31	This Pin Can Externally Shutdown the RTL8723AS (no requirement for Extra Power Switch) when WL_DISn is pulled low This pin can also support the BT Radio-off function with host interface remaining connected.
WF_WAKEUP	O	30	This pin is for WIFI function to wakeup host when remote wake function is enabled. The Polarity can be defined by customer.
BT_WAKEUP_DEV	I	52	Host wakes up BT controller in Remote Wakeup Mode. This pin is shared with LED1 function.
BT_IRQ	O	53	BT controller wakes up host in Remote Wakeup Mode. This pin is shared with LED0 function

5.10. Clock and Other Pins

Table 9. Clock and Other Pins

Symbol	Type	Pin No	Description
XI	I	23	40MHz OSC Input Input of 40MHz Crystal Clock Reference
XO	O	24	Output of 40MHz Crystal Clock Reference
GPIO0	IO	26	Trap function: weak pull low to enable RTL8723 to enter normal operation mode. General Purpose Input/Output Pin
GPIO1	IO	27	Trap function: weak pull low to enable integrated switching regulator; weak pull high to enable integrated linear regulator . General Purpose Input/Output Pin
GPIO2	IO	28	General Purpose Input/Output Pin
GPIO3	IO	29	General Purpose Input/Output Pin
GPIO4	IO	60	General Purpose Input/Output Pin
GPIO5	IO	61	General Purpose Input/Output Pin
GPIO6/EEDO	IO	62	General Purpose Input/Output Pin or EEPROM Interface EEDO Signal
GPIO7/EEDI	IO	63	General Purpose Input/Output Pin or EEPROM Interface EEDI Signal
EEPROMSEL/EESK	I	64	Trap Function: Weakly pull high at power on to enable NV-memory debug. EESK for internal NV-memory debug
EECS	O	65	External NV-memory enable
GPIO8	IO	54	General Purpose Input/Output Pin
GPIO12	IO	30	General Purpose Input/Output Pin

6. Electrical and Thermal Characteristics

6.1. Temperature Limit Ratings

Table 10. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

6.2. Temperature Limit Ratings

Table 11. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

6.3. DC Characteristics

6.3.1. Power Supply Characteristics

Table 12. DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
VD33A, VD33D	3.3V I/O Supply Voltage	3.0	3.3	3.6	V
VD12A, VD12D	1.2V Core Supply Voltage	1.10	1.2	1.32	V
VD15A, VD15D	1.5V Supply Voltage	1.425	1.5	1.575	V
IDD33	3.3V Rating Current	-	-	600	mA

6.3.2. Digital IO Pin DC Characteristics

Table 13. 3.3V GPIO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	2.0	3.3	3.6	V
V_{IL}	Input low voltage	--	0	0.9	V
V_{OH}	Output high voltage	2.97	--	3.3	V
V_{OL}	Output low voltage	0	--	0.33	V

Table 14. 2.8V GPIO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	1.8	2.8	3.1	V
V_{IL}	Input low voltage	--	0	0.8	V
V_{OH}	Output high voltage	2.5	--	3.1	V
V_{OL}	Output low voltage	0	--	0.28	V

Table 15. 1.8V GPIO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	1.7	1.8	2.0	V
V_{IL}	Input low voltage	--	0	0.8	V
V_{OH}	Output high voltage	1.62	--	1.8	V
V_{OL}	Output low voltage	0	--	0.18	V

6.4. IO Characteristics

6.5. AC Characteristics

6.5.1. SDIO/GSPI Interface Characteristics

- **SDIO/GSPI Interface Timing**

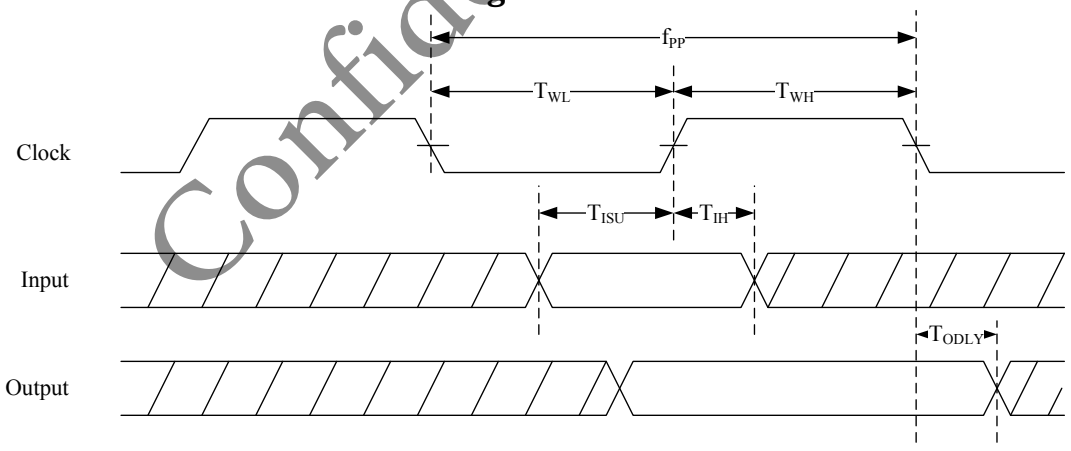


Figure 5. SDIO Interface Timing

Table 16. SDIO Interface Timing Parameters

NO	Parameter	Mode	MIN	MAX	Unit
f_{PP}	Clock frequency	Default	0	25	MHz
		HS	0	50	MHz
T_{WL}	Clock low time	DEF	10		ns
		HS	7		ns
T_{WH}	Clock high time	DEF	10		ns
		HS	7		
T_{ISU}	Input setup time	DEF	5		ns
		HS	6		
T_{IH}	Input hold time	DEF	5		ns
		HS	2		
T_{ODLY}	Output delay time	DEF		14	ns
		HS		14	

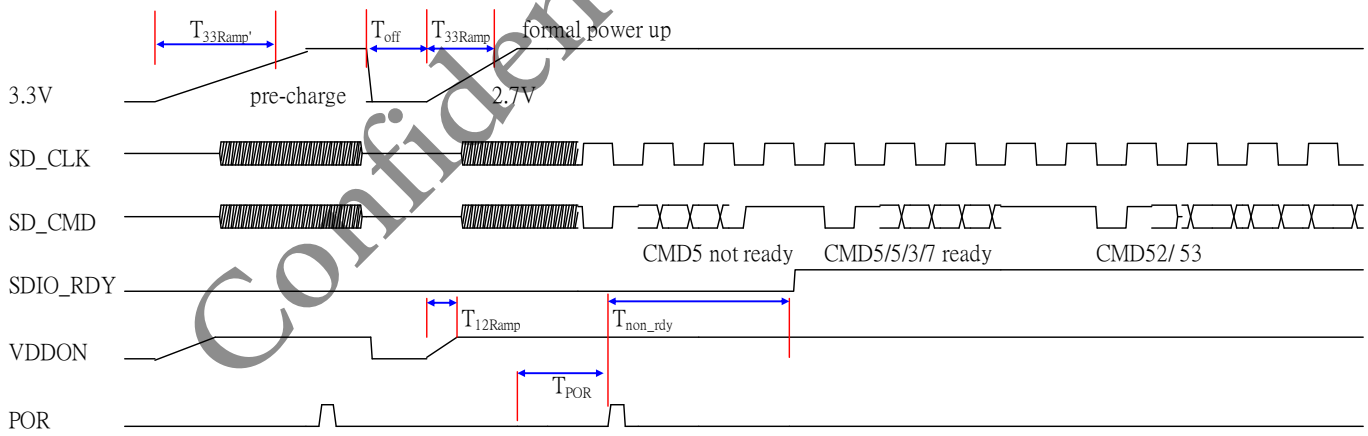
■ SDIO/ GSPI Interface Signal Level

The SDIO and GSPI signal level ranges from 1.8V to 3.3V. The host shall provide the power source with targeting power level to RTL8723AS SDIO and GSPI interface via VIO_UART pin (pin # 50).

The DC characteristics of typical signal level, 3.3V/ 2.8V/ 1.8V are shown in section 6.3.2.

■ SDIO Interface Power On Sequence

After power on, the SDIO interface is selected by RTL8723AS automatically when a valid SDIO command is received. To attain better SDIO host compatibility, the following power on sequence is recommended:



Variable definition:

T33ramp': The 3.3V power pre-charge ramp up duration before formal power up. It is recommended that a 3.3V power on and then power off sequence is executed by host controller before the formal power on

sequence. This procedure can eliminate the host card detection issue when power ramp up duration is too long or the system warm reboot failure issue.

Toff : The duration the 3.3V is cut off before formal power up.

T33ramp: The 3.3V main power ramp up duration

T12ramp: The internal 1.2V ramp up duration.

T_{POR}: The duration the power on reset releases and power management unit executes power on tasks. The power on reset will detect both 3.3V and 1.2V power ramp up and after a predetermined duration.

T_{non_rdy}: SDIO not ready duration, in this state, RTL8723AS may respond command without ready bit set. After ready bit set, host will initiate complete card detection procedure.

The power on flow description:

It is recommended that the card detection procedures are divided into two phases: a 3.3V power pre-charge phase and a formal power up phase.

For the 3.3V power pre-charge phase, the power ramp up duration is not limited. The 3.3V is then cut off and is turned on after T_{off} period. The ramp up time is specified by T_{33ramp} duration.

After main 3.3V ramp up and 1.2V ramp up, the power management unit will be enabled by power ready detection circuit, and enables SDIO block. Efuse is then autoloaded to SDIO circuits during T_{non_rdy} duration. After autoload done, the SDIO responds command with ready bit set. After CMD5/ 5/ 3/ 7 procedures, the card detection is then executed. After driver loaded, normal command 52 and 53 are then used.

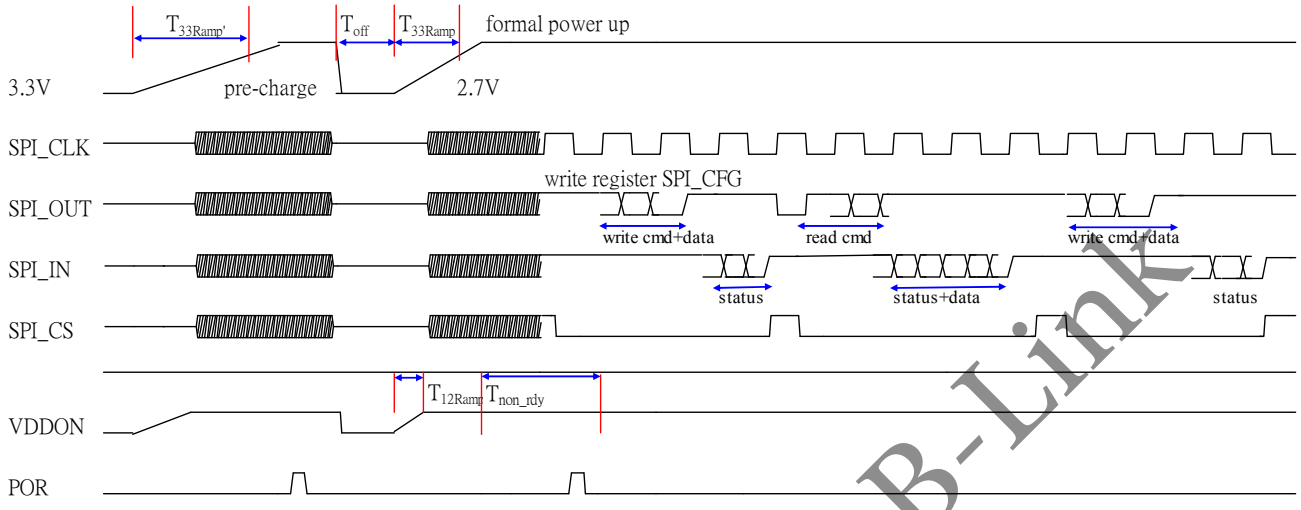
The typical timing spec is shown as follows:

Table 17. SDIO Interface Power On Timing Parameters

	Min	Typical	Max	Unit
T_{33ramp}'	--	--	No Limit	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.1	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
T_{por}	2	2	8	ms
$T_{non\text{-}rdy}$	1	2	10	ms

GSPI Interface Power On Sequence

The GSPI interface is enabled automatically when a valid GSPI command is first received. The recommended power on sequence is as follows:



Variable definition:

T_{33ramp}`: The 3.3V power pre-charge ramp up duration before formal power up. It is recommended that a 3.3V power on and then power off sequence is executed by host controller before the formal power on sequence. This procedure can avoid the host card detection issue when power ramp up duration is too long or the system warm reboot failure.

T_{off} : The duration the 3.3V is cut off before formal power up.

T_{33ramp}: The 3.3V main power ramp up duration

T_{12ramp}: The internal 1.2V ramp up duration.

T_{non_rdy}: The duration SPI device internal initialization. After T_{non_rdy}, SPI host can then send command to write SPI_CFG register. SPI_CFG register is to control SPI endian and word length.

The power on flow description:

It is recommended that the card detection procedures are divided into two phases: a 3.3V power pre-charge phase and a formal power up phase.

For the 3.3V power pre-charge phase, the power ramp up duration is not limited. The 3.3V is then cut off and is turned on after T_{off} period. The ramp up time is specified by T_{33ramp} duration.

After main 3.3V ramp up and 1.2V ramp up, the power management unit will be enabled by power ready detection circuit, and enables SPI block. Efuse is then autoloaded to SPI circuits, and the internal power circuits are configured during T_{non_rdy} duration.

The typical timing spec is shown as follows:

Table 18. SPI Interface Power On Timing Parameters

	Min	Typical	Max	Unit
T_{33ramp}'	--	--	No Limit	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.1	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
$T_{non-rdy}$	3	4	18	ms

6.5.2. UART Interface Characteristics

■ UART Feature

RTL8723AS UART interface is a standard 4-wire interface with RX, TX, CTS and RTS. The interface supports the Bluetooth 2.0 UART HCI H4 and H5 specification. The default baud rate is 115.2 kbaud. In order to support high and low speed baud rate, RTL8723AS provides multiple UART clock. Below shows the rates supported.

Table 19. UART Interface Power On Timing Parameter

Desired Baud Rate	Actual Baud Rate	Error (%)
300	300	0.00%
600	600	0.00%
900	900	0.00%
1200	1200	0.00%
1800	1800	0.00%
2400	2400	0.00%
3600	3601	0.03%
4800	4798	-0.04%
7200	7198	-0.03%
9600	9603	0.03%
14400	14395	-0.03%
19200	19182	-0.09%
28800	28846	0.16%
38400	38462	0.16%
56000	55970	-0.05%
57600	57692	0.16%
76800	76531	-0.35%
115200	115385	0.16%

Desired Baud Rate	Actual Baud Rate	Error (%)
128000	127119	-0.69%
153600	153061	-0.35%
230400	229167	-0.54%
460800	458333	-0.54%
500000	500000	0.00%
921600	916667	-0.54%
1000000	1000000	0.00%
1382400	1375000	-0.54%
1444444	1437500	-0.48%
1500000	1500000	0.00%
1843200	1833333	-0.54%
2000000	2000000	0.00%
2100000	2083333	-0.79%
2764800	2777778	0.47%
3000000	3000000	0.00%
3250000	3250000	0.00%
3692300	3703704	0.31%
3750000	3750000	0.00%
4000000	4000000	0.00%

■ UART Interface Timing

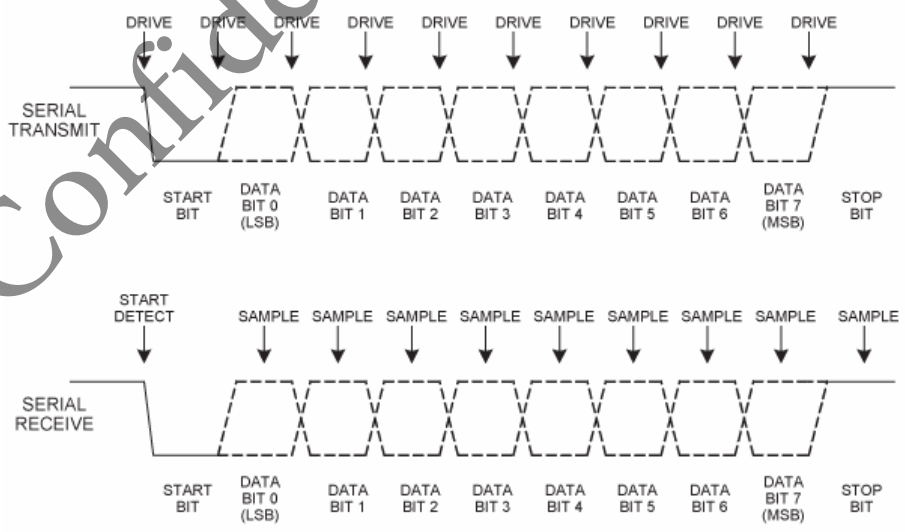


Figure 6. UART Interface waveform

■ UART Interface Signal Level

The UART signal level ranges from 1.8V to 3.3V. The host shall provide the power source with targeting power level to RTL8723AS UART interface via VIO_UART pin (pin # 38).

The DC characteristics of typical signal level, 3.3V/ 2.8V/ 1.8V are shown in section 6.3.2.

■ UART Interface Power On Sequence

The UART interface power on sequence is dependent on whether host flow control is supported. To attain better UART host compatibility, the following power on sequences are recommended for both conditions:

No support UART hardware flow control:

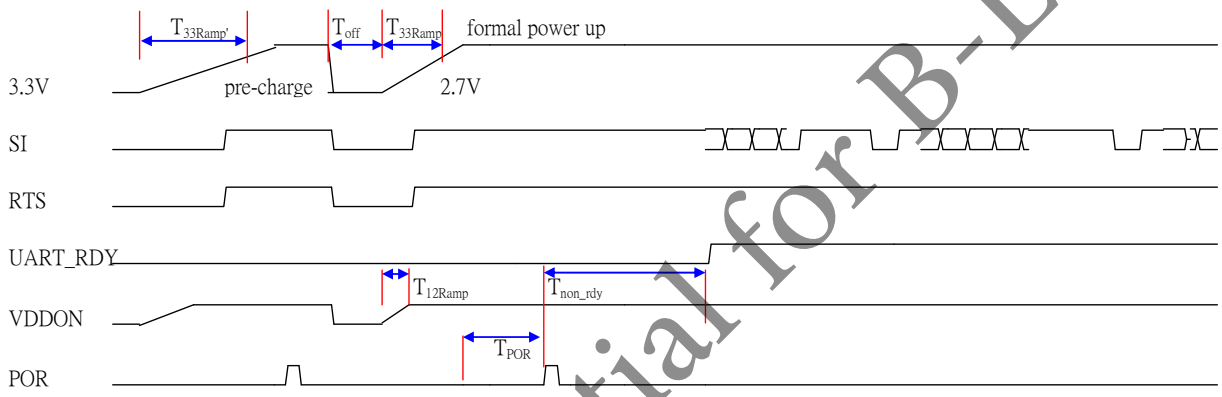


Figure 7. UART power on sequence without hardware flow control

Support UART hardware flow control:

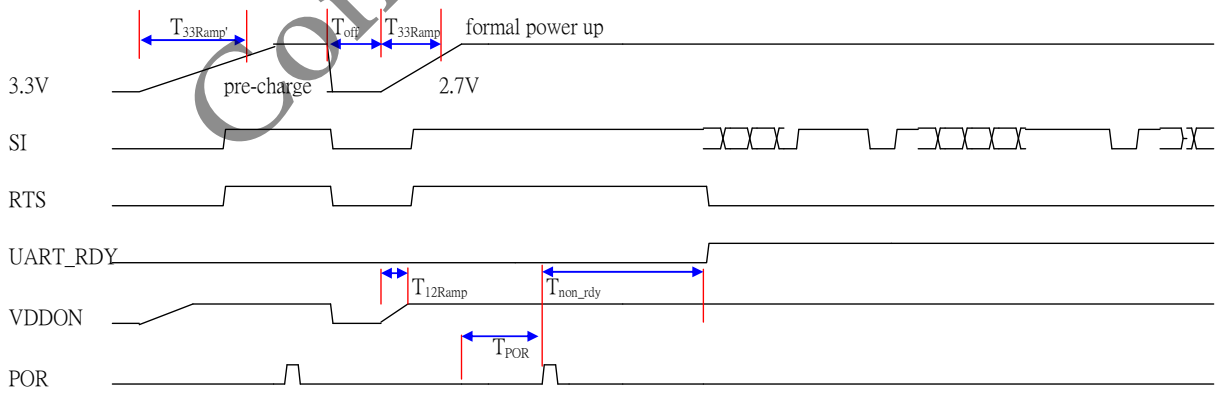


Figure 8. UART power on sequence with hardware flow control

Variable definition:

T_{33ramp}`: The 3.3V power pre-charge ramp up duration before formal power up. It is recommended that a 3.3V power on and then power off sequence is executed by host controller before the formal power on sequence. This procedure can eliminate the host card detection issue when power ramp up duration is too long or the system warm reboot failure issue.

T_{off} : The duration the 3.3V is cut off before formal power up.

T_{33ramp}: The 3.3V main power ramp up duration

T_{12ramp}: The internal 1.2V ramp up duration.

T_{POR}: The duration the power on reset releases and power management unit executes power on tasks. The power on reset will detect both 3.3V and 1.2V power ramp up and after a predetermined duration.

T_{non_rdy}: The duration UART not ready to respond command. During this state, RTL8723AS can't respond any command. After this duration, host can send any command.

The power on flow description:

It is recommended that the card detection procedures are divided into two phases: a 3.3V power pre-charge phase and a formal power up phase.

For the 3.3V power pre-charge phase, the power ramp up duration is not limited. The 3.3V is then cut off and is turned on after T_{off} period. The ramp up time is specified by T_{33ramp} duration.

After main 3.3V ramp up and 1.2V ramp up, the power management unit will be enabled by power ready detection circuit and enable BT block. BT firmware then initials all circuits included UART during T_{non_rdy} duration. After initial procedure done, the host can execute any procedure with UART interface. In addition to wait T_{non_rdy} time, if host can support UART hardware flow control, it can detect RTS signal and follow the formal UART flow control handshake.

The typical timing spec is shown as follows:

Table 20. UART Interface Power On Timing Parameters

	Min	Typical	Max	Unit
T_{33ramp}'	--	--	No Limit	Ms
T_{off}	250	500	1000	Ms
T_{33ramp}	0.1	0.5	2.5	Ms

T_{12ramp}	0.1	0.5	1.5	Ms
T_{por}	2	2	8	Ms
$T_{non-rdy}$	1	2	10	Ms

6.5.3. PCM Interface Characteristics

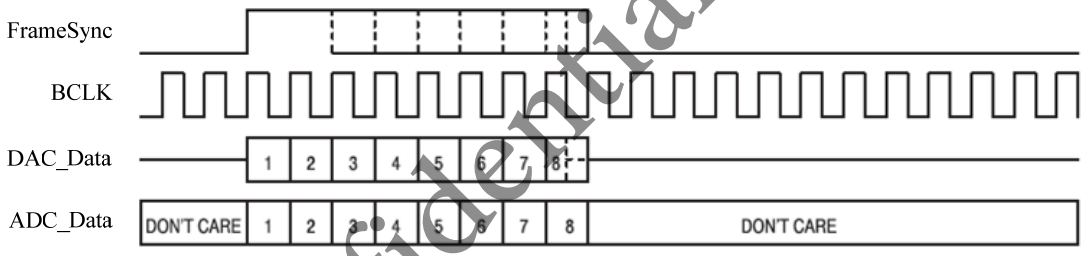
RTL8723 supports PCM digital audio interface used for transmitting digital audio/voice data to/from Audio Codec. There are features supported by RTL8723:

- Support both Master and Slave mode
- Programmable long/short Frame Sync
- Support 8-bit a-Law/u-Law and 13/16-bit linear PCM formats
- Support sign-extension and zero-padding for 8-bit and 13-bit samples
- Support padding of Audio Gain to 13-bit samples
- PCM Master clock output: 64, 128, 256 or 512kHz
- Support SCO/ESCO link

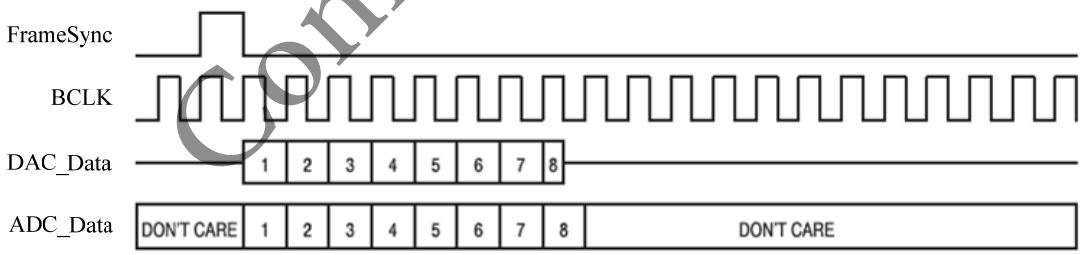
■ PCM Format

Frame Sync is the synchronizing function used to control the transfer of DAC_Data and ADC_Data. In common Audio Codec, Long Frame Sync indicates the start of ADC_Data at rising edge of FrameSync and Short Frame Sync indicates the start of ADC_Data at falling edge of FrameSync.

- Long Frame Sync



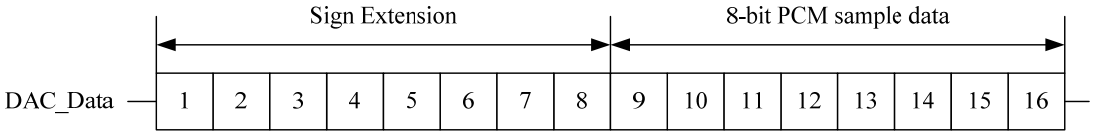
- Short Frame Sync



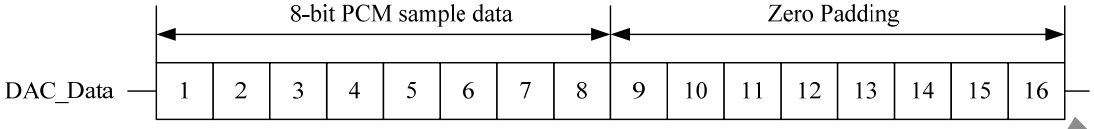
Sign-extension and zero-padding for 8-bit and 13-bit samples

For 16-bit linear PCM output format,, 3 or 8 unused bits maybe filled with sign extension, padding with zeros.

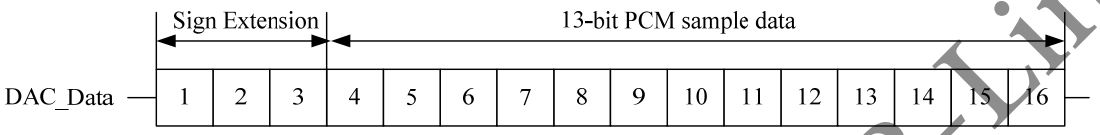
· 16-bit output data with 8-bit PCM sample data and Sign extension



· 16-bit output data with 8-bit PCM sample data and Zero padding

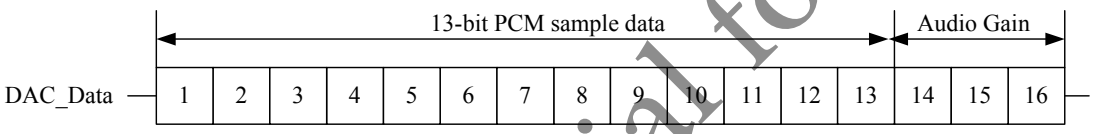


· 16-bit output data with 13-bit PCM sample data and Sign extension



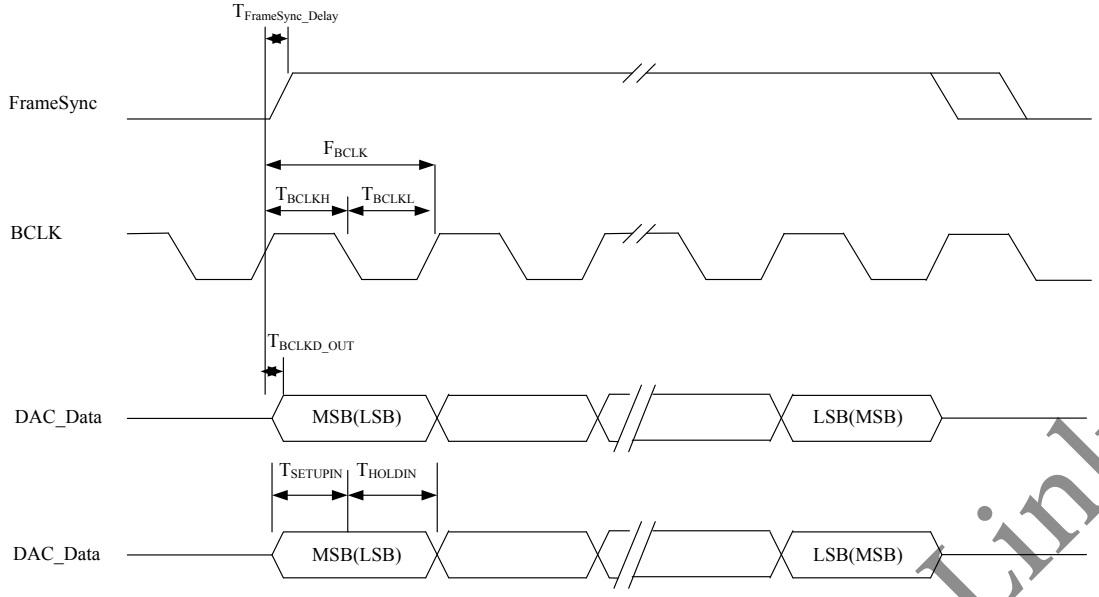
· For 16-bit linear PCM output format, 3-bit programmable audio gain value can be padded to 13-bit sample data

16-bit output data with 13-bit PCM sample data and Audio gain

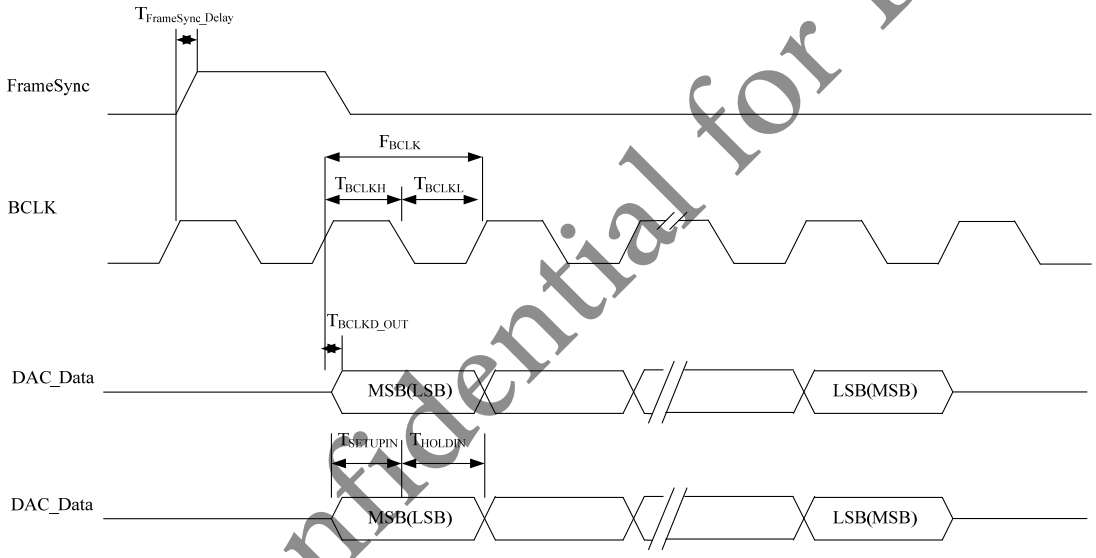


■ PCM Interface Timing

· PCM Interface(Long FrameSync)



· CM Interface(Short FrameSync)



· PCM Interface Clock Spec

Symbol	Description	Min.	Typ.	Max.	Unit
F_{BCLK}	Frequency of BCLK(Master)	64	-	512	kHz
$F_{FrameSync}$	Frequency of FrameSync(Master)		8		kHz
F_{BCLK}	Frequency of BCLK(Slave)	64	-	512	kHz

$F_{FrameSync}$	Frequency of FrameSync(Slave)		8		kHz
D	Data size	8	8	16	bits
N	Number of slots per frame	1	1	1	

· PCM Interface timing

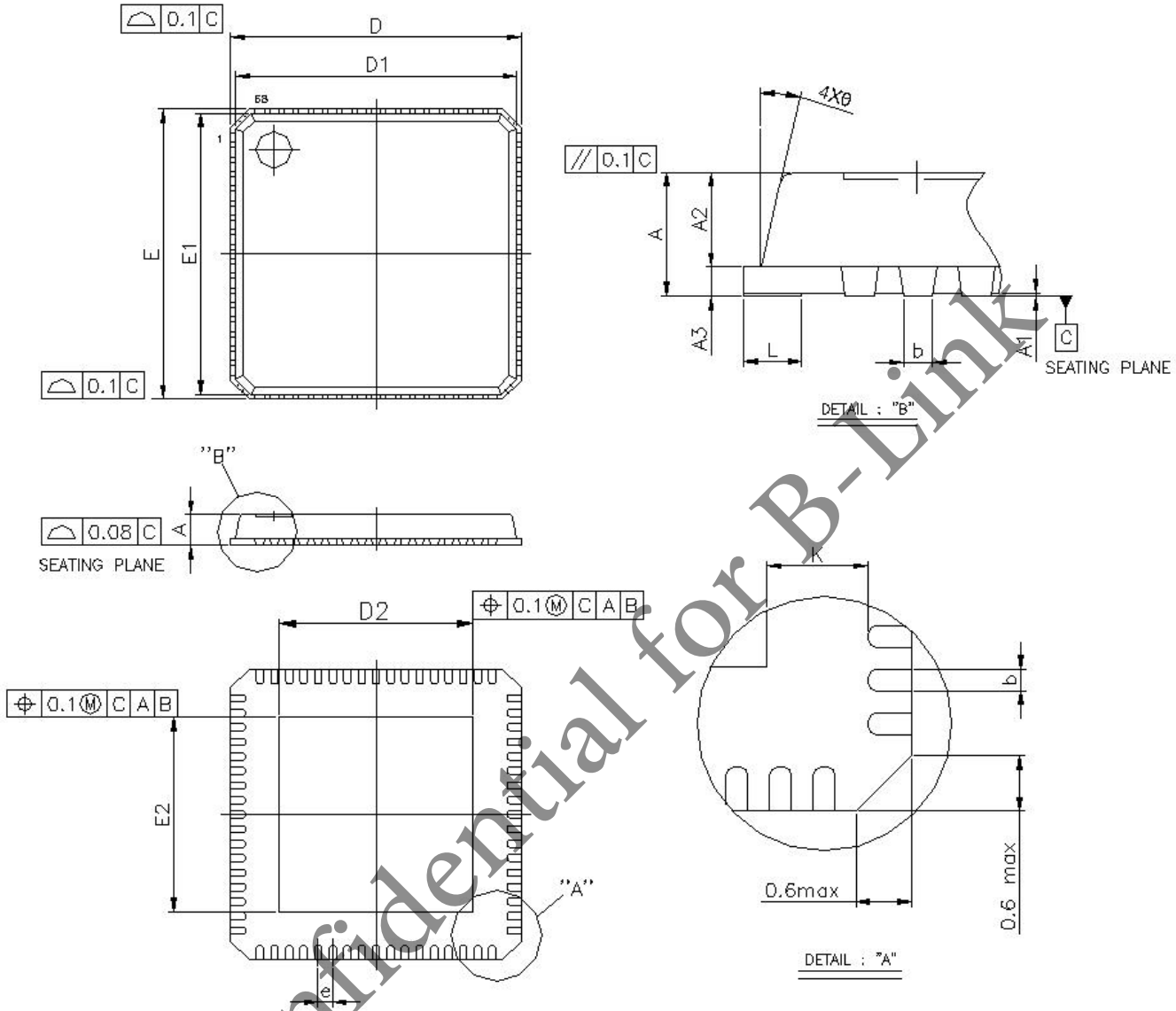
Symbol	Description	Min.	Typ.	Max.	Unit
T_{BCLKH}	High period of BCLK	980	-	-	ns
T_{BCLKL}	Low period of BCLK	970	-	-	ns
$T_{FrameSync\_Delay}$	Delay time from BCLK high to FrameSync high	-	-	75	ns
T_{BCLKD_OUT}	Delay time from BCLK high to valid DAC_Data	-	-	125	ns
$T_{SETUPIN}$	Set-up time for ADC_Data valid to BCLK low	10	-	-	ns
T_{HOLDIN}	Hold time for BCLK low to ADC_Data invalid	125	-	-	ns

■ PCM Interface Signal Level

The PCM signal level ranges from 1.8V to 3.3V. The host shall provide the power source with targeting power level to RTL8723AS PCM interface via VIO_UART pin (pin # 38).

The DC characteristics of typical signal level, 3.3V/ 2.8V/ 1.8V are shown in section 6.3.2.

7. Mechanical Dimensions



7.1. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_2	0.55	0.65	0.80	0.022	0.026	0.032
A_3		0.20REF			0.008REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E		8.00BSC			0.315BSC	
D_1/E_1		7.75BSC			0.305BSC	
D_2/E_2	5.25	5.5	5.75	0.206	0.216	0.226
e		0.40BSC			0.016BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0^o	-	14^o	0^o	-	14^o

Note1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note2: REFERENCE DOCUMENT: JEDEC MO-220.

8. Ordering Information

Table 21. Ordering Information

Part Number	Package	Status
RTL8723AS-CG	QFN-68, 'Green' Package	To Be Avaible

Note: See page 8 for package identification.

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II, Hsinchu Science Park,
Hsinchu 300, Taiwan, R.O.C.
Tel: 886-3-5780211 Fax: 886-3-5776047
www.realtek.com