THC63LVD823B

135MHz 51Bits LVDS Transmitter

General Description

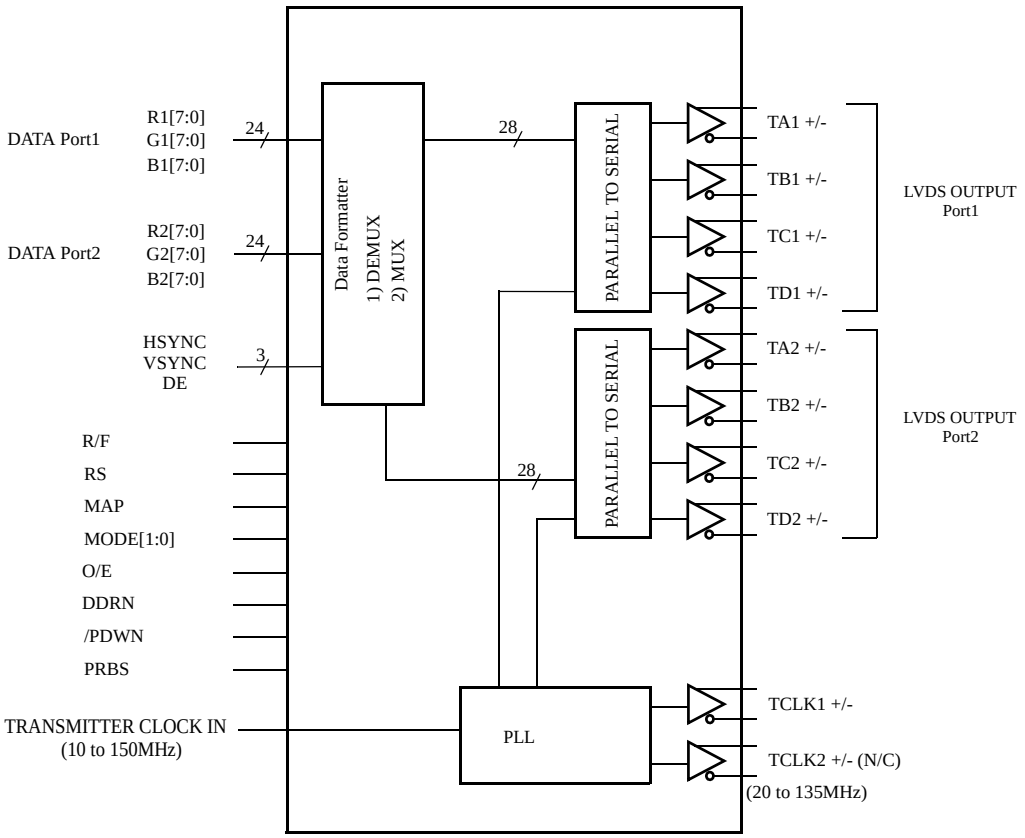
The THC63LVD823B transmitter is designed to support Single Link transmission between Host and Flat Panel Display and Dual Link transmission between Host and Flat Panel Display up to 1080p/QXGA resolutions.

The THC63LVD823B converts 51bits of CMOS/TTL data into LVDS (Low Voltage Differential Signaling) data stream. The transmitter can be programmed for rising edge or falling edge clocks through a dedicated pin. In Dual Link, the transmit clock frequency of 135MHz, 51bits of RGB data are transmitted at an effective rate of 945Mbps per LVDS channel.

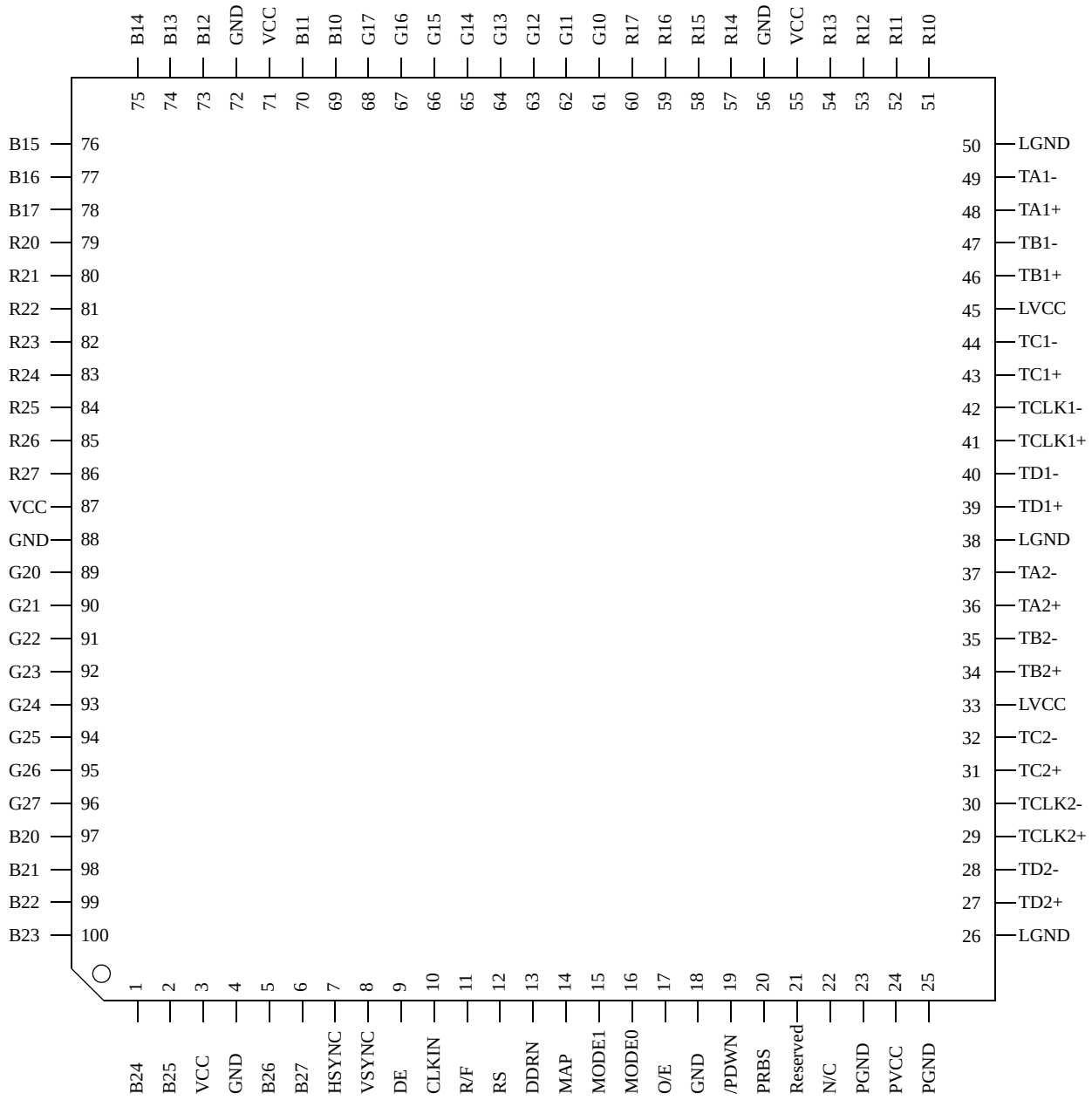
Features

- Wide dot clock range suited for TV Signal (480p-1080p), PC Signal (VGA-QXGA)
  TTL/CMOS Input: 10-150MHz
  LVDS Output: 20-135MHz
- PLL requires No external components
- Flexible Input/Output mode
  1. Single/Dual TTL IN,Single/Dual LVDS OUT
  2. Double edge input for Single TTL IN/Dual LVDS OUT
- Clock edge selectable
- 2 LVDS data mapping for simplifying PCB layout.
- Pseudo Random pattern generation circuit
- Supports Reduced swing LVDS for Low EMI
- Power down mode
- Low power single 3.3V CMOS design
- Backward compatible with THC63LVD823/ THC63LVD823A
- 100pin TQFP

Block Diagram



Pin Out (top view)



Pin Description

<table>
<tr><th>Pin Name</th><th>Pin #</th><th>Type</th><th>Description</th></tr>
<tr><td>TA1+, TA1-</td><td>48, 49</td><td rowspan="4">LVDS OUT</td><td rowspan="4">The 1st Link.
The 1st pixel output data when Dual-Link.</td></tr>
<tr><td>TB1+, TB1-</td><td>46, 47</td></tr>
<tr><td>TC1+, TC1-</td><td>43, 44</td></tr>
<tr><td>TD1+, TD1-</td><td>39, 40</td></tr>
<tr><td>TCLK1+, TCLK1-</td><td>41, 42</td><td>LVDS OUT</td><td>LVDS Clock Out for 1st and 2nd Link.</td></tr>
<tr><td>TA2+, TA2-</td><td>36, 37</td><td rowspan="4">LVDS OUT</td><td rowspan="4">The 2nd Link.
These pins are disabled when Single Link.</td></tr>
<tr><td>TB2+, TB2-</td><td>34, 35</td></tr>
<tr><td>TC2+, TC2-</td><td>31, 32</td></tr>
<tr><td>TD2+, TD2-</td><td>27, 28</td></tr>
<tr><td>TCLK2+, TCLK2-</td><td>29, 30</td><td>LVDS OUT</td><td>Additional LVDS Clock Out. Identical to TCLK1+,-.
No connect if not used.</td></tr>
<tr><td>R17 ~ R10</td><td>60 -57, 54 - 51</td><td rowspan="3">IN</td><td rowspan="3">The 1st Pixel Data Inputs.</td></tr>
<tr><td>G17 ~ G10</td><td>68 - 61</td></tr>
<tr><td>B17 ~ B10</td><td>78 - 73, 70, 69</td></tr>
<tr><td>R27 ~ R20</td><td>86 - 79</td><td rowspan="3">IN</td><td rowspan="3">The 2nd Pixel Data Inputs.</td></tr>
<tr><td>G27 ~ G20</td><td>96 - 89</td></tr>
<tr><td>B27 ~ B20</td><td>6, 5, 2, 1,
100 - 97</td></tr>
<tr><td>DE</td><td>9</td><td>IN</td><td>Data Enable Input.</td></tr>
<tr><td>VSYNC</td><td>8</td><td>IN</td><td>Vsync Input.</td></tr>
<tr><td>HSYNC</td><td>7</td><td>IN</td><td>Hsync Input.</td></tr>
<tr><td>CLKIN</td><td>10</td><td>IN</td><td>Clock Input.</td></tr>
<tr><td>R/F</td><td>11</td><td>IN</td><td>Input Clock Triggering Edge Select.
H: Rising edge, L: Falling edge</td></tr>
<tr><td>RS</td><td>12</td><td>IN</td><td>LVDS swing mode, V_{REF} select. See Fig4 - 5.
<table>
<tr><th>RS</th><th>LVDS Swing</th><th>Small Swing Input Support</th></tr>
<tr><td>V_{IHM}</td><td>350mV</td><td>N/A</td></tr>
<tr><td>V_{IMM}</td><td>350mV</td><td>RS=V_{REF}[a]</td></tr>
<tr><td>V_{ILM}</td><td>200mV</td><td>N/A</td></tr>
</table>
a. V_{REF} is Input Reference Voltage.</td></tr>
<tr><td>MAP</td><td>14</td><td>IN</td><td>LVDS mapping table select. See Fig7 to 8 and Table4 to 7.
<table>
<tr><th>MAP</th><th>Mapping Mode</th></tr>
<tr><td>V_{IHM}</td><td>Mapping MODE1</td></tr>
<tr><td>V_{ILM}</td><td>Mapping MODE2</td></tr>
<tr><td>V_{IMM}</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>MODE1, MODE0</td><td>15, 16</td><td>IN</td><td>Pixel Data Mode.
<table>
<tr><th>MODE1</th><th>MODE0</th><th>Mode</th></tr>
<tr><td>L</td><td>L</td><td>Dual Link (Dual-in/Dual-out)</td></tr>
<tr><td>H</td><td>L</td><td>Dual Link (Single-in/Dual-out)</td></tr>
<tr><td>L</td><td>H</td><td>Single Link (Dual-in/Single-out)</td></tr>
<tr><td>H</td><td>H</td><td>Single Link (Single-in/Single-out)</td></tr>
</table></td></tr>
</table>

Pin Description (Continued)

Pin Name	Pin #	Type	Description
O/E	17	IN	Output enable. H: Output enable, L: Output disable (all outputs are Hi-Z).
/PDWN	19	IN	H: Normal operation, L: Power down (all outputs are Hi-Z)
PRBS [a]	20	IN	PRBS(Pseudo-Random Binary Sequence) generator is active in order to evaluate eye patterns when MODE<1:0> = LL(Dual-in/Dual-out mode). H: PRBS generator is enable. L: Normal Operation
Reserved	21	IN	Must be tied to GND.
DDRN	13	IN	DDR function is active when MODE<1:0> = HL(Single-in/Dual-out mode). Open or H: DDR(Double Edge input) function disable. L: DDR(Double Edge input) function enable.
N/C	22		Must be Open.
VCC	3, 55, 71, 87	Power	Power Supply Pins for TTL inputs and digital circuitry.
GND	4, 18, 56, 72, 88	Ground	Ground Pins for TTL inputs and digital circuitry.
LVCC	33, 45	Power	Power Supply Pins for LVDS Outputs.
LGND	26, 38, 50	Ground	Ground Pins for LVDS Outputs.
PVCC	24	Power	Power Supply Pin for PLL circuitry.
PGND	23, 25	Ground	Ground Pins for PLL circuitry.

a : Setting the PRBS pin high enables the internal test pattern generator. It generates Pseudo-Random Bit Sequence of 2^{23}-1. The generated PRBS is fed into input data latches, formatted as VGA video like data, encoded and serialized into TXOUT output. This function is normally to be used for analyzing the signal integrity of the transmission channel including PCB traces, connectors, and cables.

Absolute Maximum Ratings

Supply Voltage (V_{CC})	-0.3V ~ +4.0V
CMOS/TTL Input Voltage	-0.3V ~ (V_{CC} + 0.3V)
LVDS Driver Output Voltage	-0.3V ~ (V_{CC} + 0.3V)
Output Current	-30mA ~ 30mA
Junction Temperature	+125°C
Storage Temperature Range	-55°C ~ +125°C
Lead Temperature (Soldering, 4sec)	+260°C
Maximum Power Dissipation	1.35W

Recommended Operating Conditions

Parameter				**Min**	**Typ**	**Max**	**Units**
All Supply Voltage				3.0	3.3	3.6	V
Operating Ambient Temperature				-20		70	°C
Clock Frequency	MODE<1:0>=LL Dual-in/Dual-out		Input	20		135	MHz
			LVDS Output	20		135	MHz
	MODE<1:0>=LH Dual-in/Single-out		Input	10		67.5	MHz
			LVDS Output	20		135	MHz
	MODE<1:0>=HL Single-in/Dual-out	Single Edge Input (DDRN=Open/H)	Input	40		150	MHz
			LVDS Output	20		75	MHz
		Double Edge Input (DDRN=L)	Input	20		75	MHz
			LVDS Output	20		75	MHz
	MODE<1:0>=HH Single-in/Single-out		Input	20		135	MHz
			LVDS Output	20		135	MHz

Electrical Characteristics

CMOS/TTL DC Specifications

V_{CC} = VCC=PVCC=LVCC

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}[a]	High Level Data Input Voltage	RS=V_{IHM}or-V_{ILM}	2.0		V_{CC}	V
		RS=V_{IMM}	V_{REF}[b]+0.1			V
V_{IL}[a]	Low Level Data Input Voltage	RS=V_{IHM}or-V_{ILM}	GND		0.8	V
		RS=V_{IMM}			V_{REF}-0.1	V
V_{IHC}[c]	High Level Control Input Voltage		2.0		V_{CC}	V
V_{ILC}[c]	Low Level Control Input Voltage		GND		0.8	V
V_{IHM}[d]	High Level Control Input Voltage		0.8V_{CC}		V_{CC}	V
V_{IMM}[d]	Middle Level Control Input Voltage		0.6		1.4	V
V_{ILM}[d]	Low Level Control Input Voltage		GND		0.08V_{CC}	V
I_{INC}	Input Current(except DDRN)	GND ≤ V_{IN} ≤ V_{CC}			±10	μA
I_{INCD}	Input Current(Only DDRN)	GND ≤ V_{IN} ≤ V_{CC}			±20	μA

a. CLKIN,R10~R17,G10~G17,B10~B17,R20~R27,G20~G27,B20~B27,DE,HSYNC,VSYNC

b. V_{REF} is input voltage of RS pin.

c. R/F,DDRN,MODE0,MODE1,O/E,PDWN,PRBS

d. RS,MAP

LVDS Transmitter DC Specifications

V_{CC} = VCC=PVCC=LVCC

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
VOD	Differential Output Voltage	RL=100Ω	Normal swing RS= V_{CC}	250	350	450	mV
			Reduced swing RS= GND	100	200	300	mV
ΔVOD	Change in VOD between complementary output states	RL=100Ω				35	mV
VOC	Common Mode Voltage			1.125	1.25	1.375	V
ΔVOC	Change in VOC between complementary output states					35	mV
I_{OS}	Output Short Circuit Current	VOUT=GND, RL=100Ω				-24	mA
I_{OZ}	Output TRI-State current	/PDWN=GND, VOUT=GND to V_{CC}				±10	μA

Electrical Characteristics (Continued)

Supply Current

V_{CC} = VCC=PVCC=LVCC

Symbol	Parameter	Condition			Typ.	Max.	Units
I_{TCCW}	Transmitter Supply Current (Worst Case Pattern) Fig1.	RL=100Ω CL=5pF RS=V_{CC}	MODE<1:0>=HH Single-in/Single-out	CLKIN=65MHz		86	mA
				CLKIN=85MHz		100	mA
				CLKIN=135MHz		122	mA
			MODE<1:0>=HL Single-in/Dual-out DDRN=H or Open DDR Input Off	CLKIN=65MHz		114	mA
				CLKIN=85MHz		116	mA
				CLKIN=135MHz		155	mA
				CLKIN=150MHz		168	mA
			MODE<1:0>=HL Single-in/Dual-out DDRN=L DDR Input On	CLKIN=32.5MHz		114	mA
				CLKIN=42.5MHz		118	mA
				CLKIN=67.5MHz		155	mA
				CLKIN=75MHz		167	mA
			MODE<1:0>=LH Dual-in/Single-out	CLKIN=32.5MHz		84	mA
				CLKIN=42.5MHz		98	mA
				CLKIN=67.5MHz		120	mA
			MODE<1:0>=LL Dual-in/Dual-out	CLKIN=65MHz		144	mA
				CLKIN=85MHz		171	mA
				CLKIN=135MHz		217	mA
I_{TCCS}	Transmitter Power Down Supply Current	/PDWN = L, All Inputs = Fixed L or H				50	μA

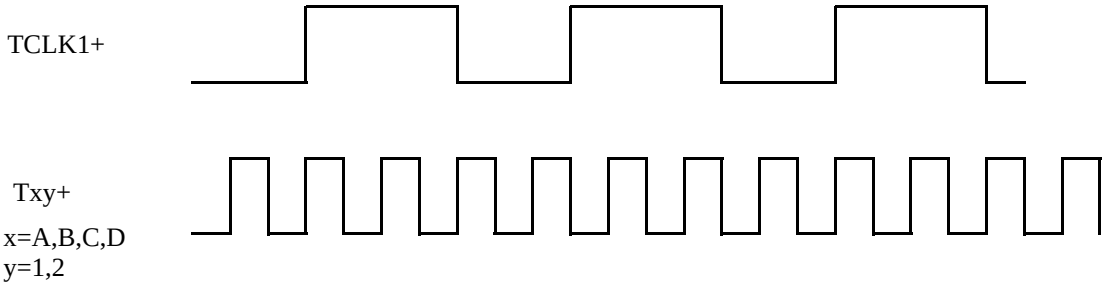


Fig1. Test Pattern
(LVDS Output Full Toggle Pattern)

Switching Characteristics

V_{CC} = VCC=PVCC=LVCC

Symbol	Parameter		Min.	Typ.	Max.	Units
t_{TCIP}	CLK IN Period(Fig4,5)		6.7		100	ns
t_{TCH}	CLK IN High Time(Fig4,5)		$0.35t_{TCIP}$	$0.5t_{TCIP}$	$0.65t_{TCIP}$	ns
t_{TCL}	CLK IN Low Time(Fig4,5)		$0.35t_{TCIP}$	$0.5t_{TCIP}$	$0.65t_{TCIP}$	ns
t_{TS}	TTL Data Setup to CLK IN(Fig4,5)		2.5			ns
t_{TH}	TTL Data Hold from CKL IN(Fig4,5)		0.0			ns
t_{TCD}	CLK IN to TCLK+/- Delay(Fig4,5) MODE<1:0>=LL Dual-in/Dual-out		$(4+3/7)t_{TCIP}$ +2.6		$(4+3/7)t_{TCIP}$ +7.5	ns
t_{TCOP}	CLK OUT Period(Fig6)		7.4		50	ns
t_{LVT}	LVDS Transition Time(Fig2)			0.6	1.5	ns
t_{TOP1}	Output Data Position0 (Fig6)	t_{TCOP} = 7.4ns	-0.15	0.0	+0.15	ns
t_{TOP0}	Output Data Position1 (Fig6)		$\frac{t_{TCOP}}{7} - 0.15$	$\frac{t_{TCOP}}{7}$	$\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP6}	Output Data Position2 (Fig6)		$2\frac{t_{TCOP}}{7} - 0.15$	$2\frac{t_{TCOP}}{7}$	$2\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP5}	Output Data Position3 (Fig6)		$3\frac{t_{TCOP}}{7} - 0.15$	$3\frac{t_{TCOP}}{7}$	$3\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP4}	Output Data Position4 (Fig6)		$4\frac{t_{TCOP}}{7} - 0.15$	$4\frac{t_{TCOP}}{7}$	$4\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP3}	Output Data Position5 (Fig6)		$5\frac{t_{TCOP}}{7} - 0.15$	$5\frac{t_{TCOP}}{7}$	$5\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP2}	Output Data Position6 (Fig6)		$6\frac{t_{TCOP}}{7} - 0.15$	$6\frac{t_{TCOP}}{7}$	$6\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TPLL}	Phase Lock Time(Fig3)				10.0	ms
t_{DEINT}	DE input period (Fig3-1) Single-in / Dual-out, DDR Off mode only(MODE<1:0>=HL, DDRN=Open or H)		$4t_{TCIP}$	tTCIP*(2n) [a]		ns
t_{DEH}	DE High time (Fig3-1) Single-in / Dual-out, DDR Off mode only(MODE<1:0>=HL, DDRN=Open or H)		$2t_{TCIP}$	tTCIP*(2m)[a]		ns
t_{DEL}	DE Low time(Fig3-1) Single-in / Dual-out, DDR Off mode only(MODE<1:0>=HL, DDRN=Open or H)		$2t_{TCIP}$			ns

a. Refer to Fig3-1 for details.

AC Timing Diagrams

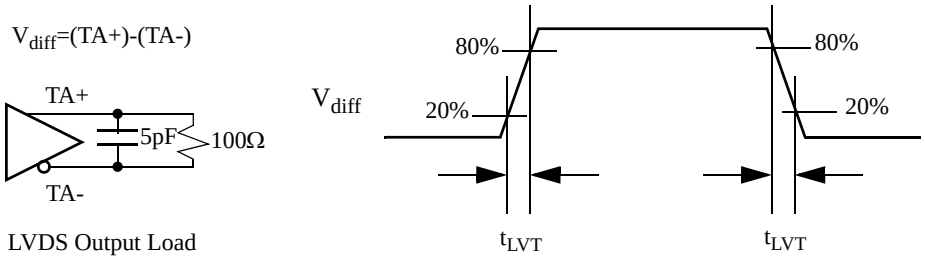


Fig2. LVDS Output Load and Transition Time

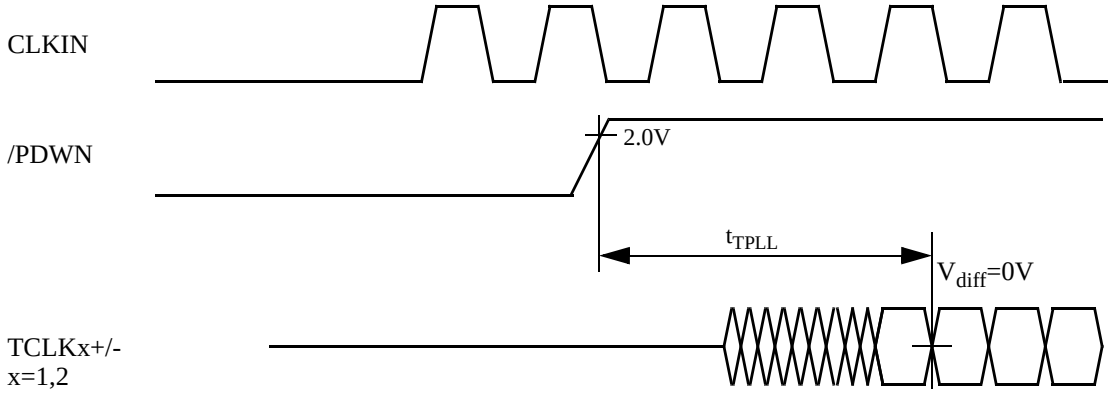
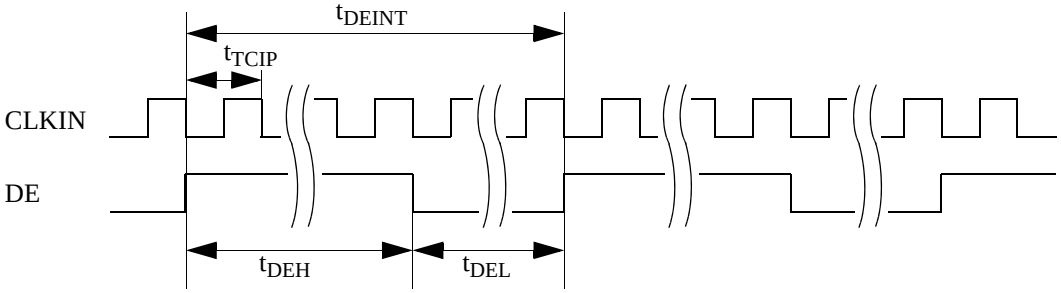


Fig3. PLL Lock Time



Note : In single-in/dual-out, DDR off mode (MODE<1:0>=HL, DDRN=Open or H),
the period between rising edges of DE (t_{DEINT}), high time of DE(t_{DEH})
should always satisfy following equations.

t_{DEH} = tTCIP * (2m)

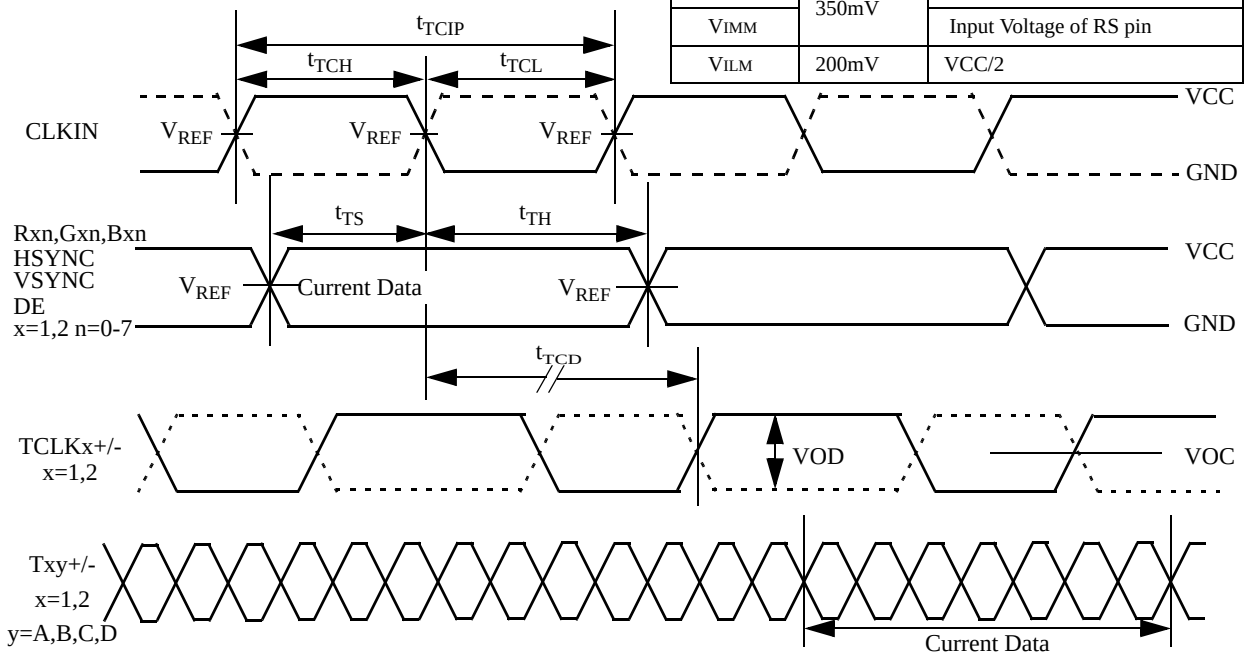
t_{DEINT} = tTCIP * (2n)

m,n=integer

Fig3-1. Single IN / Dual OUT, DDR off mode DE input timing

AC Timing Diagrams (Continued)

RS pin	VOD	VREF
VIHM	350mV	VCC/2
VIMM		Input Voltage of RS pin
VILM	200mV	VCC/2

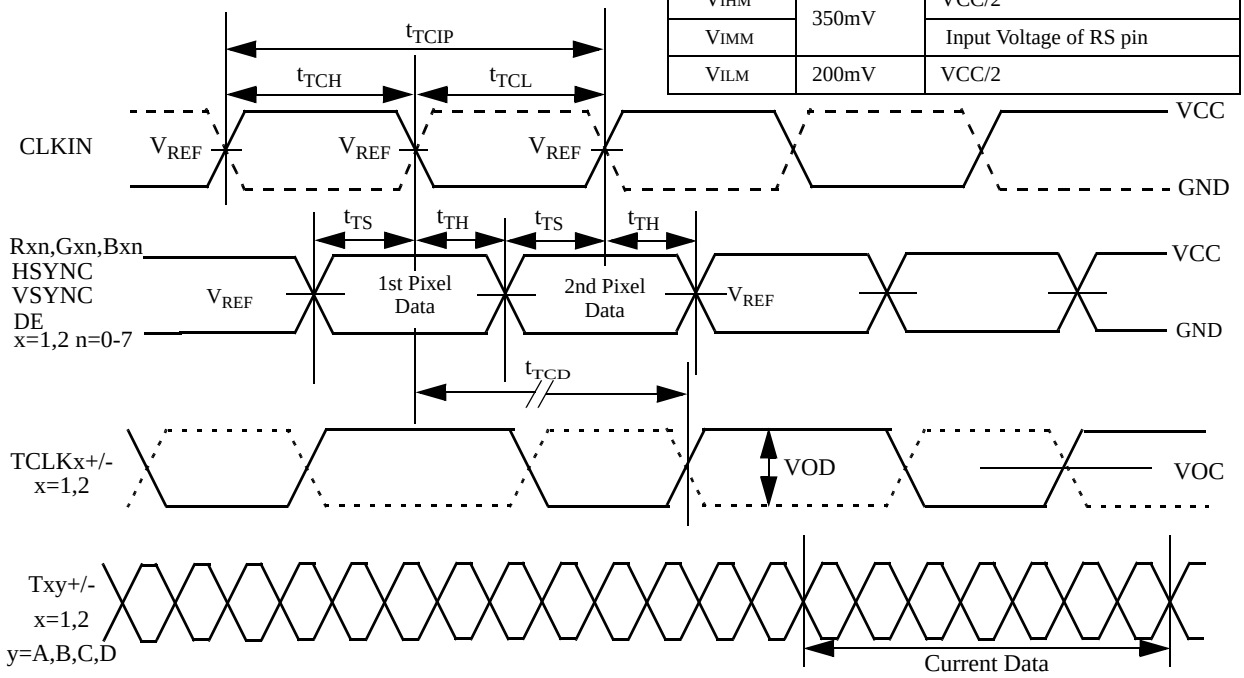


Note:

CLKIN : for R/F=GND, denote as solid line,
for R/F=VCC, denote as dashed line.

Fig4. CLKIN Period, High/Low Time, Setup/Hold Timing

RS pin	VOD	VREF
VIHM	350mV	VCC/2
VIMM		Input Voltage of RS pin
VILM	200mV	VCC/2

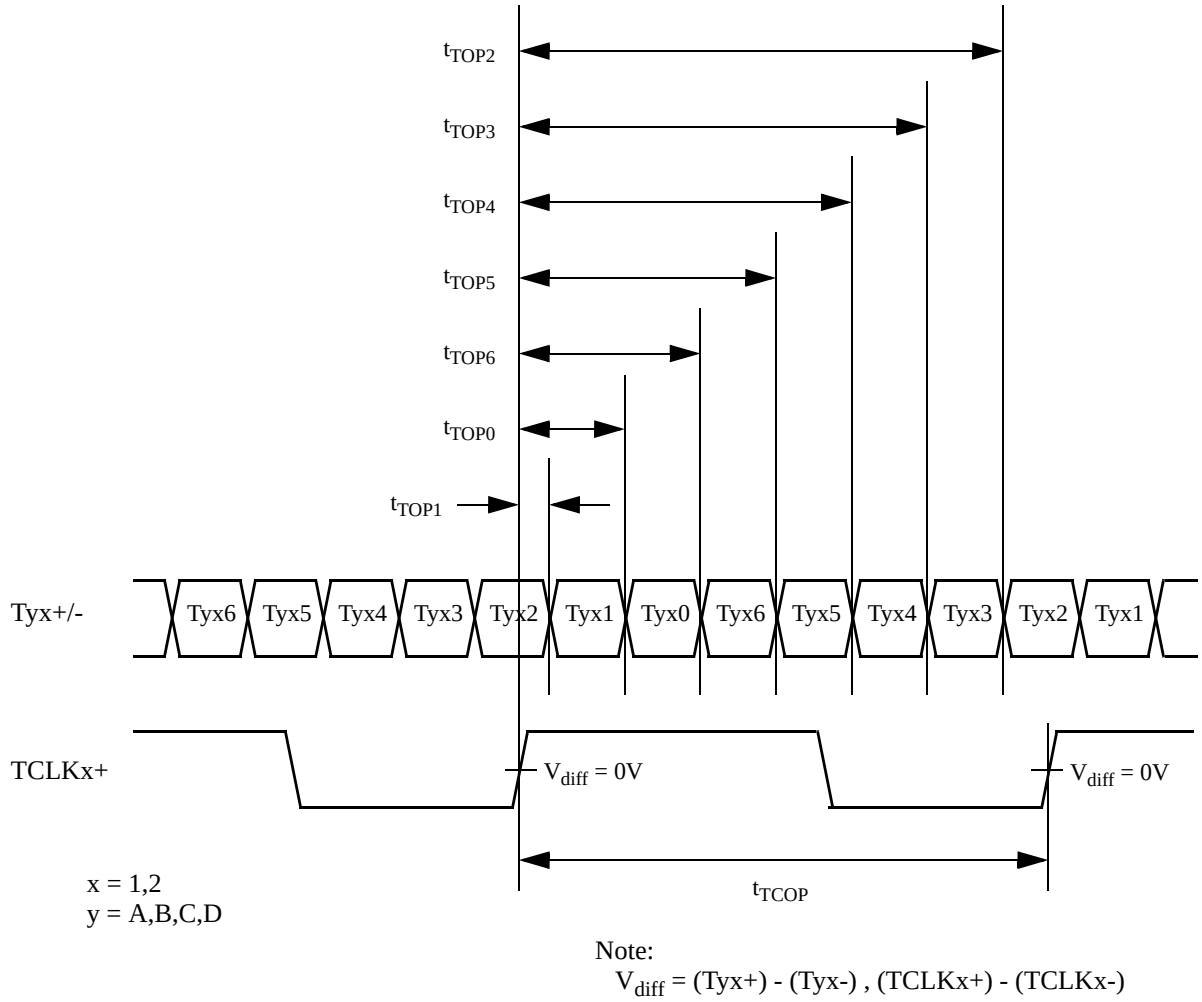


Note:

CLKIN : for R/F=GND, denote as solid line,
for R/F=VCC, denote as dashed line.

Fig5. CLKIN Period, High/Low Time, Setup/Hold Timing for Double Edge Input Mode(DDR)
MODE<1:0>=HL,DDRN=L

AC Timing Diagrams (Continued)



Note:
V_{diff} = (Tyx+) - (Tyx-) , (TCLKx+) - (TCLKx-)

Fig6. LVDS Output Data Position

Input Data Mapping

•Table1. Input Color Data naming rule

X	Y	Z	Description	
X=R			Red Color Data	
X=G			Green Color Data	
X=B			Blue Color Data	
	Y= None		Single Pixel	
	Y=E		Dual Pixel	1st Pixel Data
	Y=O			2nd Pixel Data
		Z=0-7	Bit number 0: LSB (Least Significant Bit) 7: MSB (Most Significant Bit)	

•Table2. TTL/CMOS Input Data Mapping (Single-in mode, MODE1=H)

Data Signals	Transmitter Input Pin Names
R0	R10
R1	R11
R2	R12
R3	R13
R4	R14
R5	R15
R6	R16
R7	R17
G0	G10
G1	G11
G2	G12
G3	G13
G4	G14
G5	G15
G6	G16
G7	G17
B0	B10
B1	B11
B2	B12
B3	B13
B4	B14
B5	B15
B6	B16
B7	B17

Input Data Mapping (Continued)

•Table3. TTL/CMOS Input Data Mapping (Dual-in mode, MODE1=L)

Data Signals	Transmitter Input Pin Names	Data Signals	Transmitter Input Pin Names
RE0	R10	RO0	R20
RE1	R11	RO1	R21
RE2	R12	RO2	R22
RE3	R13	RO3	R23
RE4	R14	RO4	R24
RE5	R15	RO5	R25
RE6	R16	RO6	R26
RE7	R17	RO7	R27
GE0	G10	GO0	G20
GE1	G11	GO1	G21
GE2	G12	GO2	G22
GE3	G13	GO3	G23
GE4	G14	GO4	G24
GE5	G15	GO5	G25
GE6	G16	GO6	G26
GE7	G17	GO7	G27
BE0	B10	BO0	B20
BE1	B11	BO1	B21
BE2	B12	BO2	B22
BE3	B13	BO3	B23
BE4	B14	BO4	B24
BE5	B15	BO5	B25
BE6	B16	BO6	B26
BE7	B17	BO7	B27

LVDS Output Data Mapping

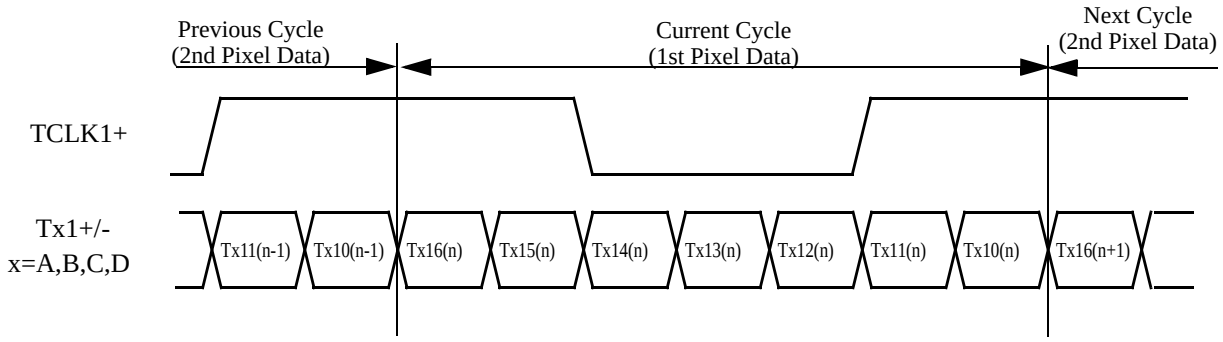


Fig7. TTL Data Inputs Mapped to LVDS outputs
MODE0= H (Single-out Mode)

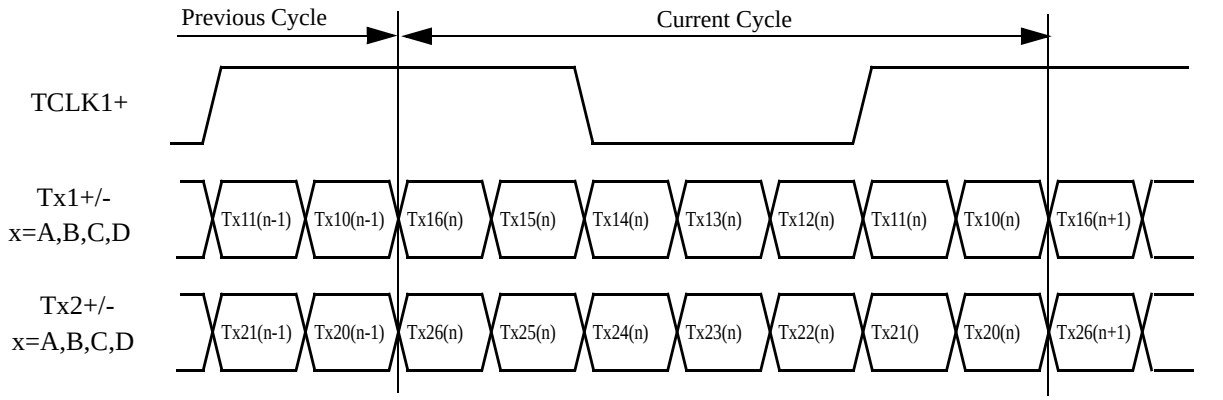


Fig8. TTL Data Inputs Mapped to LVDS outputs
MODE0= L (Dual-out Mode)

LVDS Output Data Mapping (Continued)

•Table4. LVDS Output Data Mapping (Single-in/Single-out, MODE<1:0>=HH)

LVDS Output Data	Mapping Mode(Input Pin Name)	
	Mode1 MAP=H	Mode2 MAP=L
TA10	R12	R10
TA11	R13	R11
TA12	R14	R12
TA13	R15	R13
TA14	R16	R14
TA15	R17	R15
TA16	G12	G10
TB10	G13	G11
TB11	G14	G12
TB12	G15	G13
TB13	G16	G14
TB14	G17	G15
TB15	B12	B10
TB16	B13	B11
TC10	B14	B12
TC11	B15	B13
TC12	B16	B14
TC13	B17	B15
TC14	HSYNC	HSYNC
TC15	VSYNC	VSYNC
TC16	DE	DE
TD10	R10	R16
TD11	R11	R17
TD12	G10	G16
TD13	G11	G17
TD14	B10	B16
TD15	B11	B17
TD16	N/A	N/A

LVDS Output Data Mapping (Continued)

•Table5. LVDS Output Data Mapping (Single-in/Dual-out, DDR On/Off, MODE<1:0>=HL, DDRN=Open/H/L)

LVDS Output Data (1st Link)	Mapping Mode(Input Pin Name)		LVDS Output Data (2nd Link)	Mapping Mode(Input Pin Name)	
	Mode1 MAP=H	Mode2 MAP=L		Mode1 MAP=H	Mode2 MAP=L
TA10	R12	R10	TA20	R12	R10
TA11	R13	R11	TA21	R13	R11
TA12	R14	R12	TA22	R14	R12
TA13	R15	R13	TA23	R15	R13
TA14	R16	R14	TA24	R16	R14
TA15	R17	R15	TA25	R17	R15
TA16	G12	G10	TA26	G12	G10
TB10	G13	G11	TB20	G13	G11
TB11	G14	G12	TB21	G14	G12
TB12	G15	G13	TB22	G15	G13
TB13	G16	G14	TB23	G16	G14
TB14	G17	G15	TB24	G17	G15
TB15	B12	B10	TB25	B12	B10
TB16	B13	B11	TB26	B13	B11
TC10	B14	B12	TC20	B14	B12
TC11	B15	B13	TC21	B15	B13
TC12	B16	B14	TC22	B16	B14
TC13	B17	B15	TC23	B17	B15
TC14	HSYNC	HSYNC	TC24	HSYNC	HSYNC
TC15	VSYNC	VSYNC	TC25	VSYNC	VSYNC
TC16	DE	DE	TC26	DE	DE
TD10	R10	R16	TD20	R10	R16
TD11	R11	R17	TD21	R11	R17
TD12	G10	G16	TD22	G10	G16
TD13	G11	G17	TD23	G11	G17
TD14	B10	B16	TD24	B10	B16
TD15	B11	B17	TD25	B11	B17
TD16	N/A	N/A	TD26	N/A	N/A

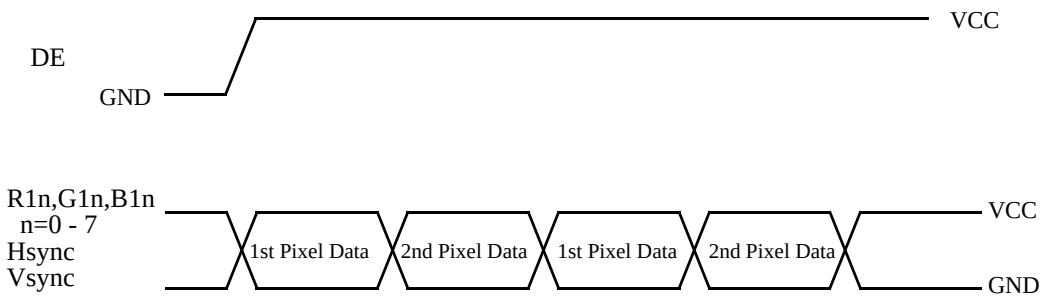


Fig9. The decision rule of 1st Pixel data in Single IN/Dual Out DDR Off
(MODE<1:0>=HL, DDRN=Open or H)

LVDS Output Data Mapping (Continued)

•Table6. LVDS Output Data Mapping (Dual-in/Single-out, MODE<1:0>=LH)

LVDS Output Data (1st Pixel)	Mapping Mode(Input Pin Name)		LVDS Output Data (2nd Pixel)	Mapping Mode(Input Pin Name)	
	Mode1 MAP=H	Mode2 MAP=L		Mode1 MAP=H	Mode2 MAP=L
TA10(n)	R12	R10	TA10(n+1)	R22	R20
TA11(n)	R13	R11	TA11(n+1)	R23	R21
TA12(n)	R14	R12	TA12(n+1)	R24	R22
TA13(n)	R15	R13	TA13(n+1)	R25	R23
TA14(n)	R16	R14	TA14(n+1)	R26	R24
TA15(n)	R17	R15	TA15(n+1)	R27	R25
TA16(n)	G12	G10	TA16(n+1)	G22	G20
TB10(n)	G13	G11	TB10(n+1)	G23	G21
TB11(n)	G14	G12	TB11(n+1)	G24	G22
TB12(n)	G15	G13	TB12(n+1)	G25	G23
TB13(n)	G16	G14	TB13(n+1)	G26	G24
TB14(n)	G17	G15	TB14(n+1)	G27	G25
TB15(n)	B12	B10	TB15(n+1)	B22	B20
TB16(n)	B13	B11	TB16(n+1)	B23	B21
TC10(n)	B14	B12	TC10(n+1)	B24	B22
TC11(n)	B15	B13	TC11(n+1)	B25	B23
TC12(n)	B16	B14	TC12(n+1)	B26	B24
TC13(n)	B17	B15	TC13(n+1)	B27	B25
TC14(n)	HSYNC	HSYNC	TC14(n+1)	HSYNC	HSYNC
TC15(n)	VSYNC	VSYNC	TC15(n+1)	VSYNC	VSYNC
TC16(n)	DE	DE	TC16(n+1)	DE	DE
TD10(n)	R10	R16	TD10(n+1)	R20	R26
TD11(n)	R11	R17	TD11(n+1)	R21	R27
TD12(n)	G10	G16	TD12(n+1)	G20	G26
TD13(n)	G11	G17	TD13(n+1)	G21	G27
TD14(n)	B10	B16	TD14(n+1)	B20	B26
TD15(n)	B11	B17	TD15(n+1)	B21	B27
TD16(n)	N/A	N/A	TD16(n+1)	N/A	N/A

LVDS Output Data Mapping (Continued)

•Table7. LVDS Output Data Mapping (Dual-in/Dual-out, MODE<1:0>=LL)

LVDS Output Data (1st Link)	Mapping Mode(Input Pin Name)		LVDS Output Data (2nd Link)	Mapping Mode(Input Pin Name)	
	Mode1 MAP=H	Mode2 MAP=L		Mode1 MAP=H	Mode2 MAP=L
TA10	R12	R10	TA20	R22	R20
TA11	R13	R11	TA21	R23	R21
TA12	R14	R12	TA22	R24	R22
TA13	R15	R13	TA23	R25	R23
TA14	R16	R14	TA24	R26	R24
TA15	R17	R15	TA25	R27	R25
TA16	G12	G10	TA26	G22	G20
TB10	G13	G11	TB20	G23	G21
TB11	G14	G12	TB21	G24	G22
TB12	G15	G13	TB22	G25	G23
TB13	G16	G14	TB23	G26	G24
TB14	G17	G15	TB24	G27	G25
TB15	B12	B10	TB25	B22	B20
TB16	B13	B11	TB26	B23	B21
TC10	B14	B12	TC20	B24	B22
TC11	B15	B13	TC21	B25	B23
TC12	B16	B14	TC22	B26	B24
TC13	B17	B15	TC23	B27	B25
TC14	HSYNC	HSYNC	TC24	HSYNC	HSYNC
TC15	VSYNC	VSYNC	TC25	VSYNC	VSYNC
TC16	DE	DE	TC26	DE	DE
TD10	R10	R16	TD20	R20	R26
TD11	R11	R17	TD21	R21	R27
TD12	G10	G16	TD22	G20	G26
TD13	G11	G17	TD23	G21	G27
TD14	B10	B16	TD24	B20	B26
TD15	B11	B17	TD25	B21	B27
TD16	N/A	N/A	TD26	N/A	N/A

Note

1)Cable Connection and Disconnection

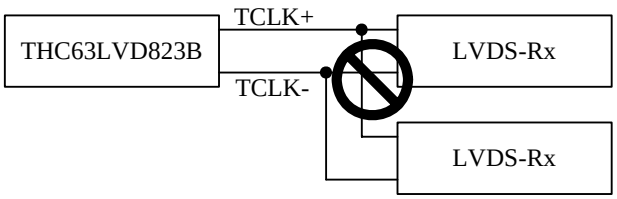
Don't connect and disconnect the LVDS cable , when the power is supplied to the system.

2)GND Connection

Connect the each GND of the PCB which THC63LVD823B and LVDS-Rx on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

3)Multi Drop Connection

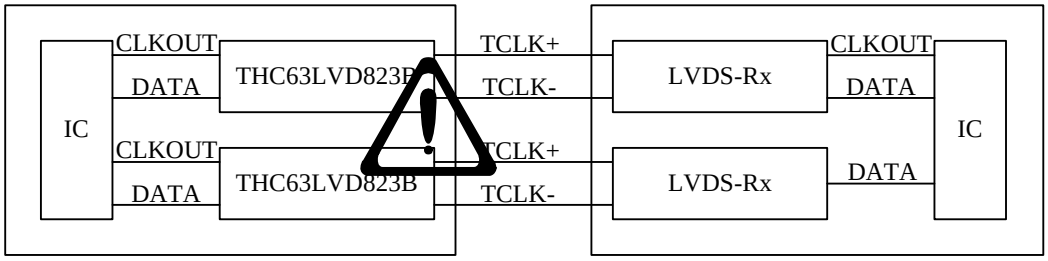
Multi drop connection is not recommended.

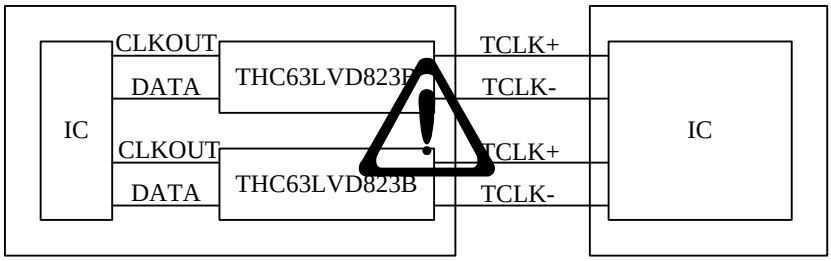


4)Asynchronous use

Asynchronous use such as following systems are not recommended. If it is not avoidable, please contact to

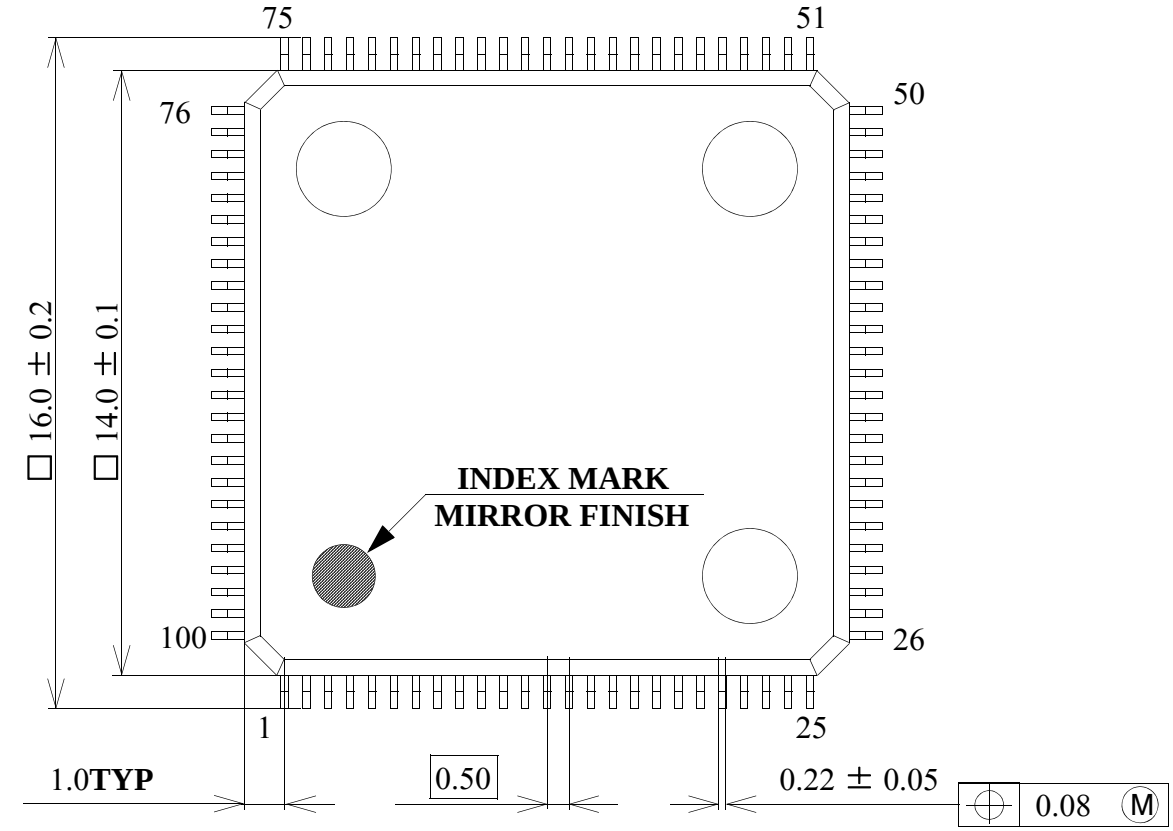
mspsupport@thine.co.jp (for FAE mailing list)

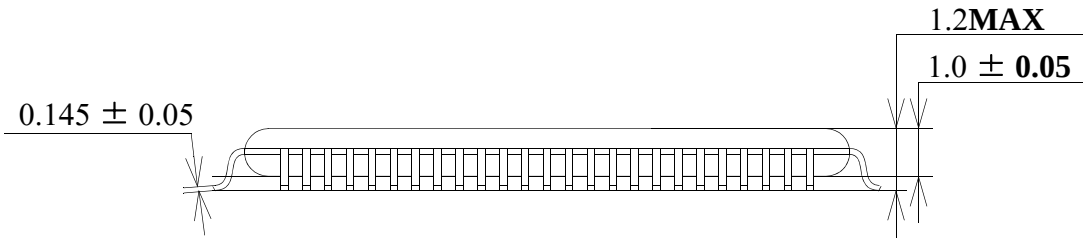




Package

TOP VIEW





Unit : mm

Notices and Requests

1.)The product specifications described in this material are subject to change without prior notice.
2.)The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
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7.)Please note that this product is not designed to be radiation-proof.
8.)Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.

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