Application Note	*THAN-00-001-05*

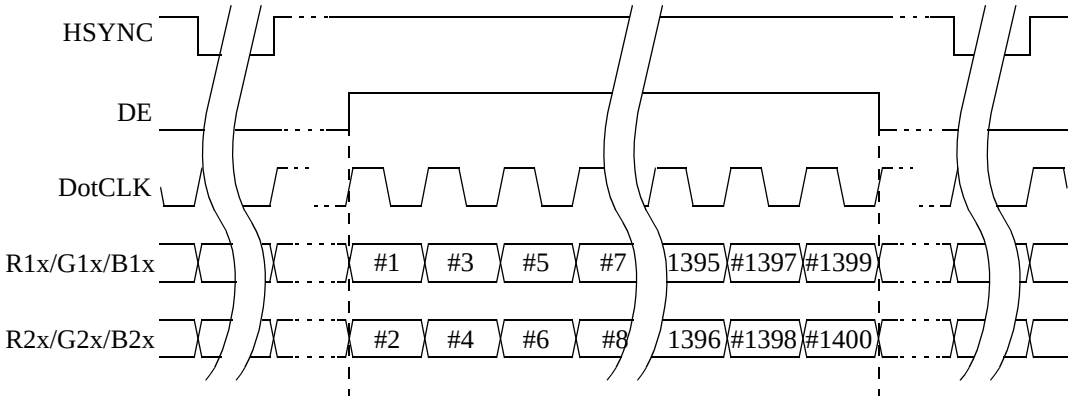
THC63LVD823/THC63LVD824 Application Note

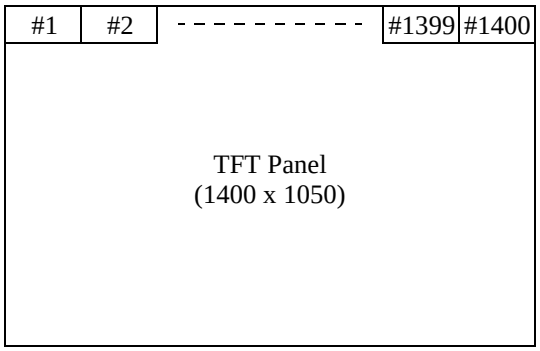
System Diagram and PCB Design Guide Line

Date	Revision	Contents
2000.03.02	THAN-00-001	new created
2001.05.31	THAN-00-001-02	revised miss description on cover page
2001.07.05	THAN-00-001-03	add reduced swing application
2001.07.18	THAN-00-001-04	revised miss description on Page 4
2002.06.27	THAN-00-001-05	revised miss description on Page 3,4,5,6

TTL DATA Timing Diagram

Following are 823 TTL data input timing example for SXGA+(1400 x 1050).





Note:

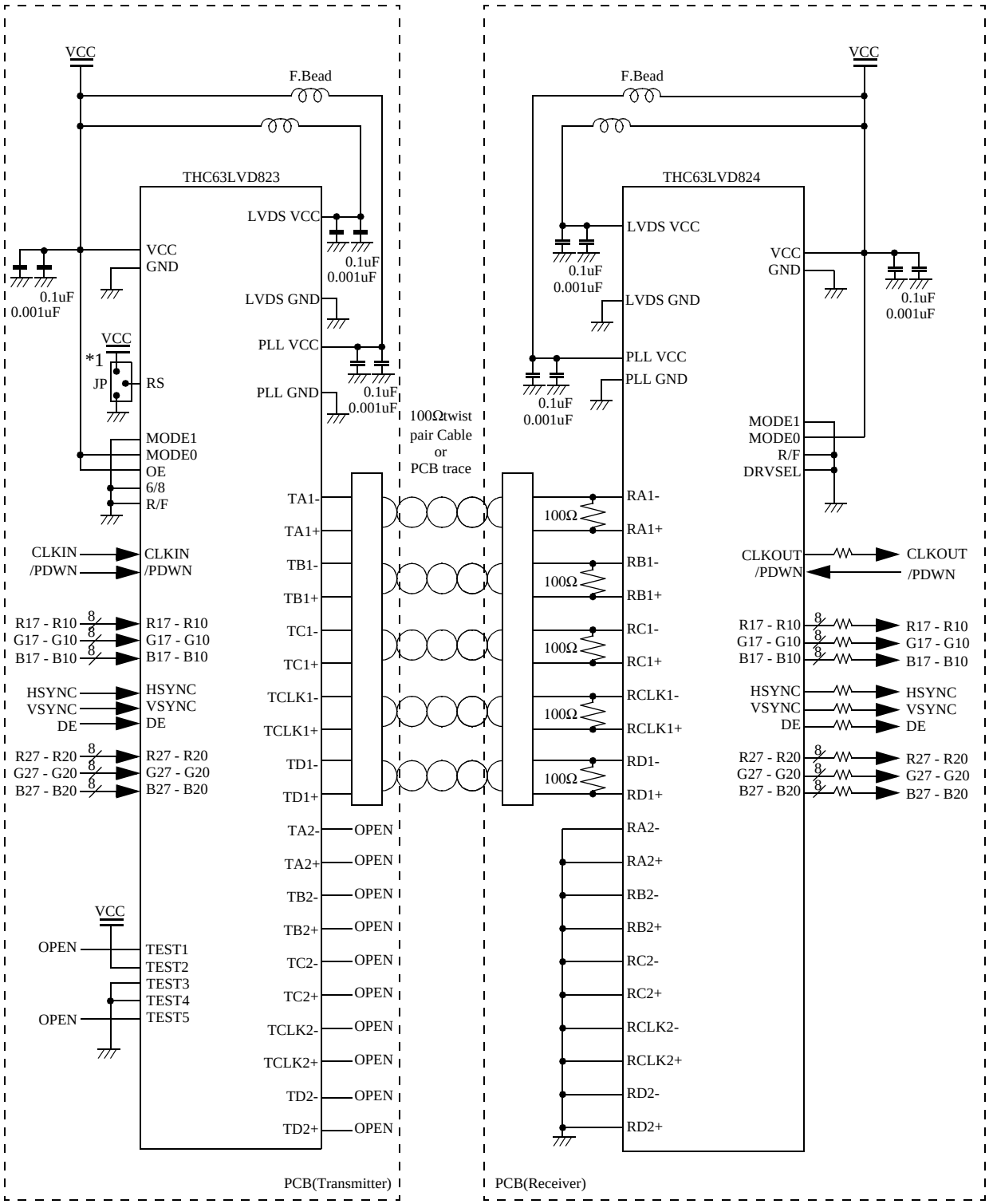
1)

	R1x	G1x	B1x	R2x	G2x	B2x
MSB	R17	G17	B17	R27	G27	B27
	R16	G16	B16	R26	G26	B26
	R15	G15	B15	R25	G25	B25
	R14	G14	B14	R24	G24	B24
	R13	G13	B13	R23	G23	B23
	R12	G12	B12	R22	G22	B22
	R11	G11	B11	R21	G21	B21
LSB	R10	G10	B10	R20	G20	B20

2) For single and dual link applications, min. pulse width of HSYNC/VSYNC/DE are 2pixels.

1) Single Link (XGA, SXGA, SXGA+)

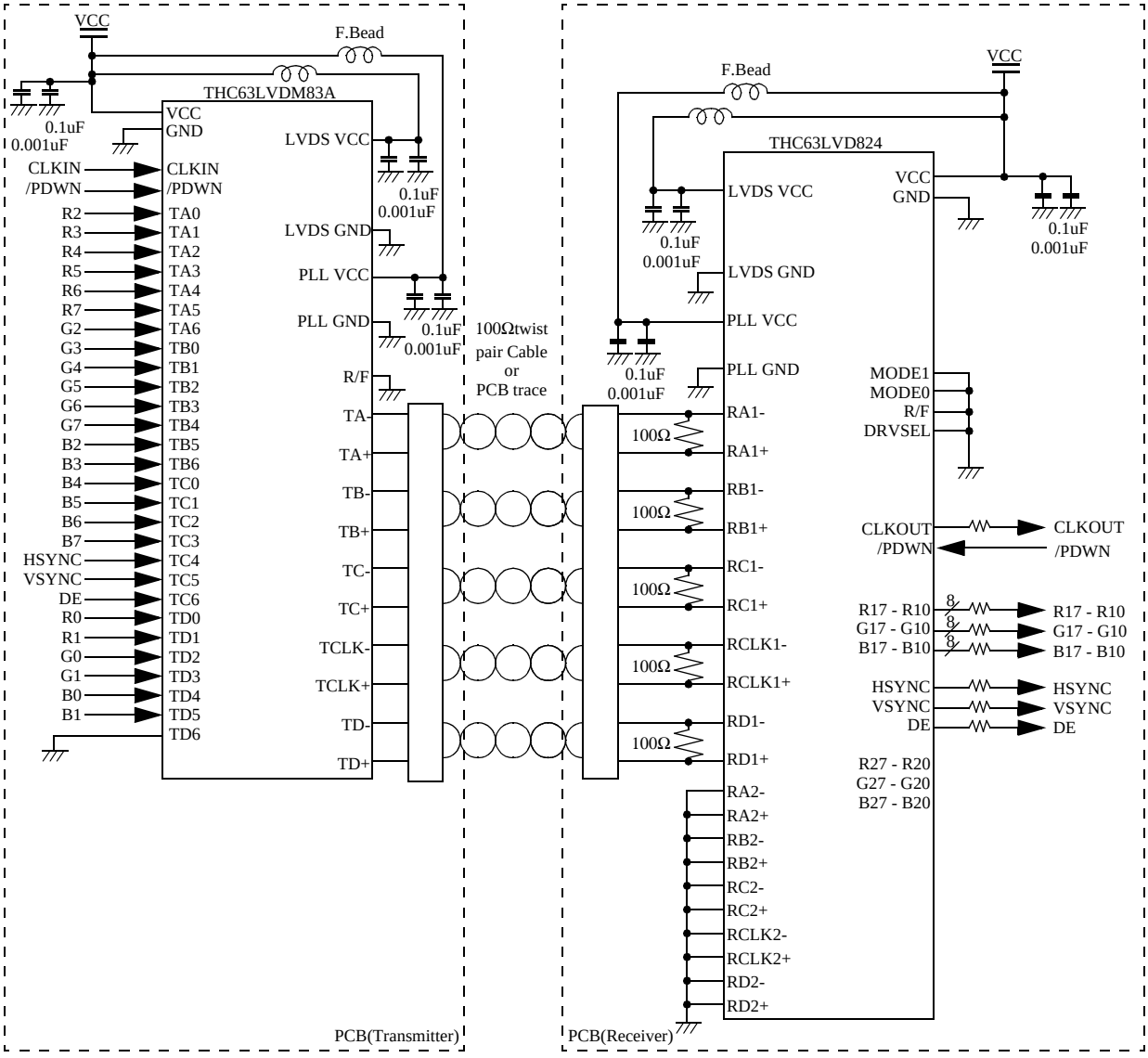
Example :
THC63LVD823 : Falling edge/8 bit/Dual in(TTL)-Single out(LVDS)
THC63LVD824 : Single in(LVDS)/Falling edge/8bit/Dual out(TTL)/Output driverbility Low



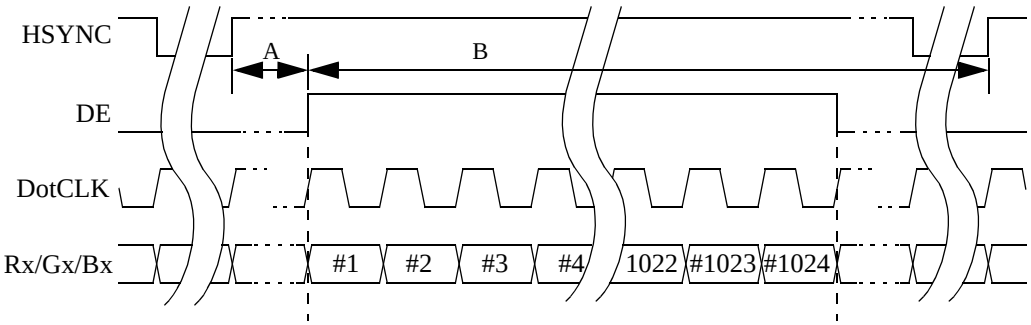
*1 : If RS pin tied to VCC, LVDS swing is 350mV.
If RS pin tied to GND, LVDS swing is 200mV.

2) Single Link (XGA)

Example :
THC63LVDM83A : Falling edge/8 bit
THC63LVD824 : Single in(LVDS)/Falling edge/8bit/Single out(TTL)/Output driverbility Low



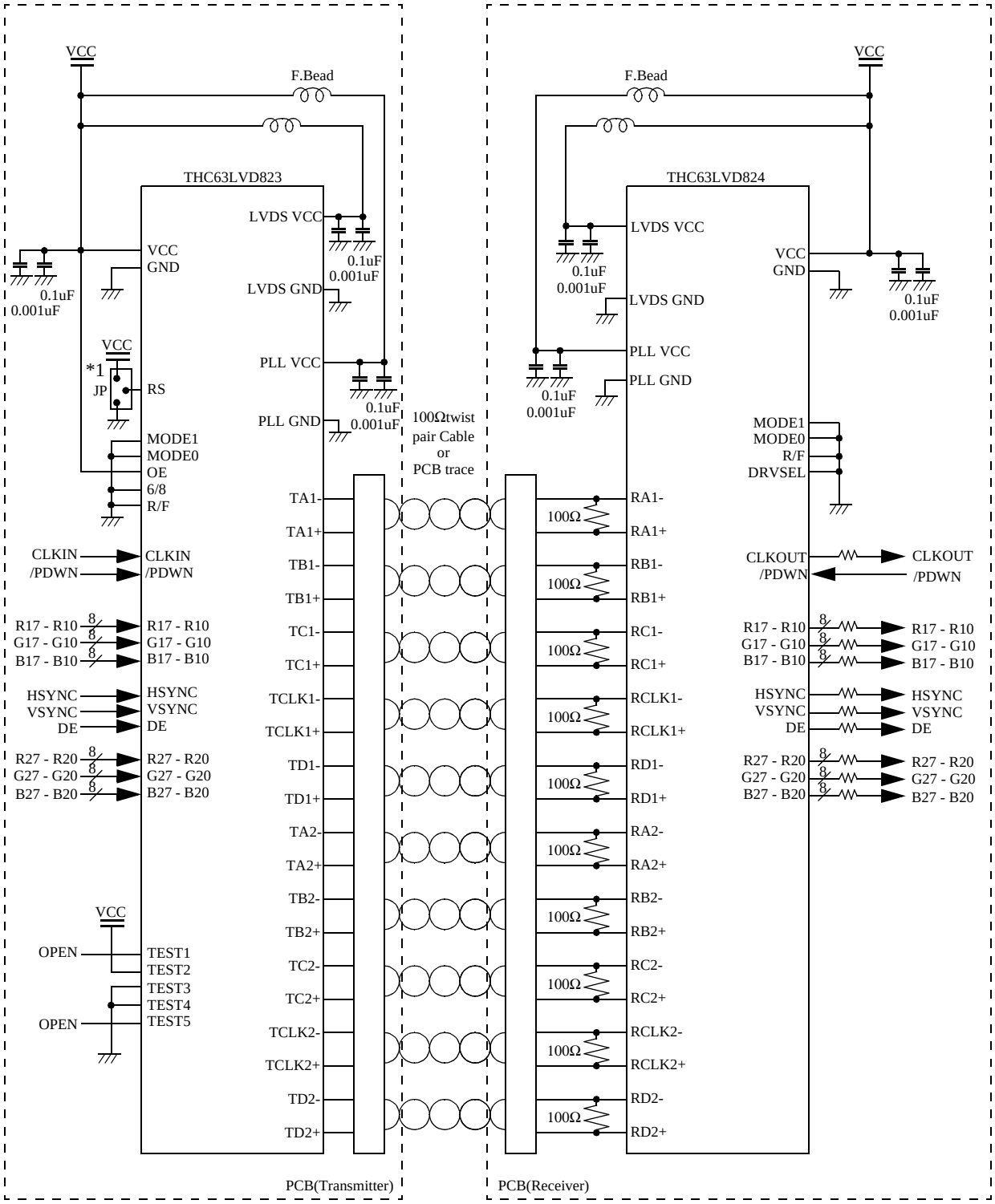
Following are M83A TTL data input timing example for XGA(1024 x 768).



Note:
A and B must be even number pixels.

3) Dual Link (SXGA, SXGA+, UXGA)

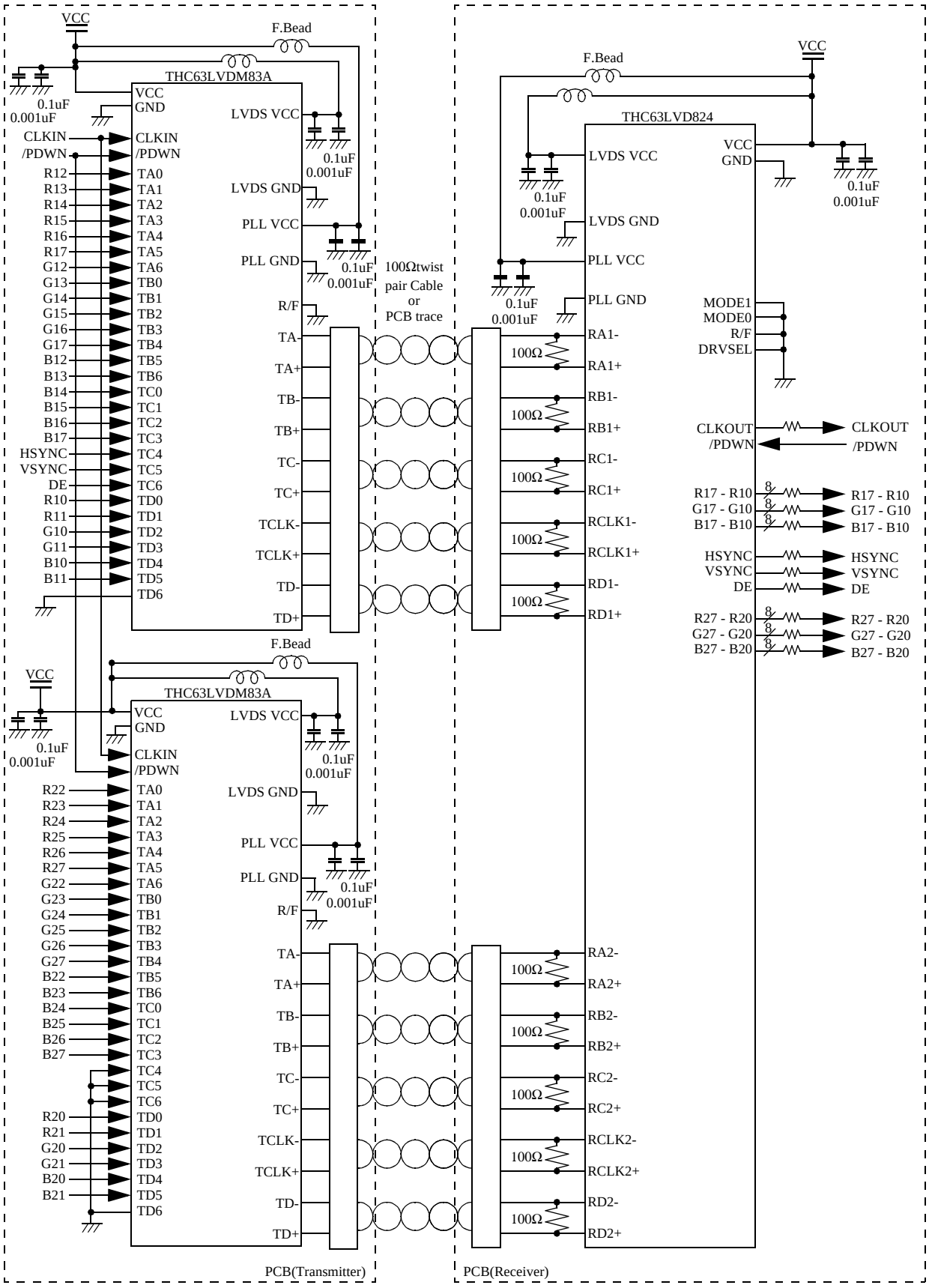
Example :
THC63LVD823 : Falling edge/8 bit/Dual in(TTL)-Dual out(LVDS)
THC63LVD824 : Dual in(LVDS)/Falling edge/8bit/Dual out(TTL)/Output driverbility Low



*1 : If RS pin tied to VCC, LVDS swing is 350mV.
If RS pin tied to GND, LVDS swing is 200mV.

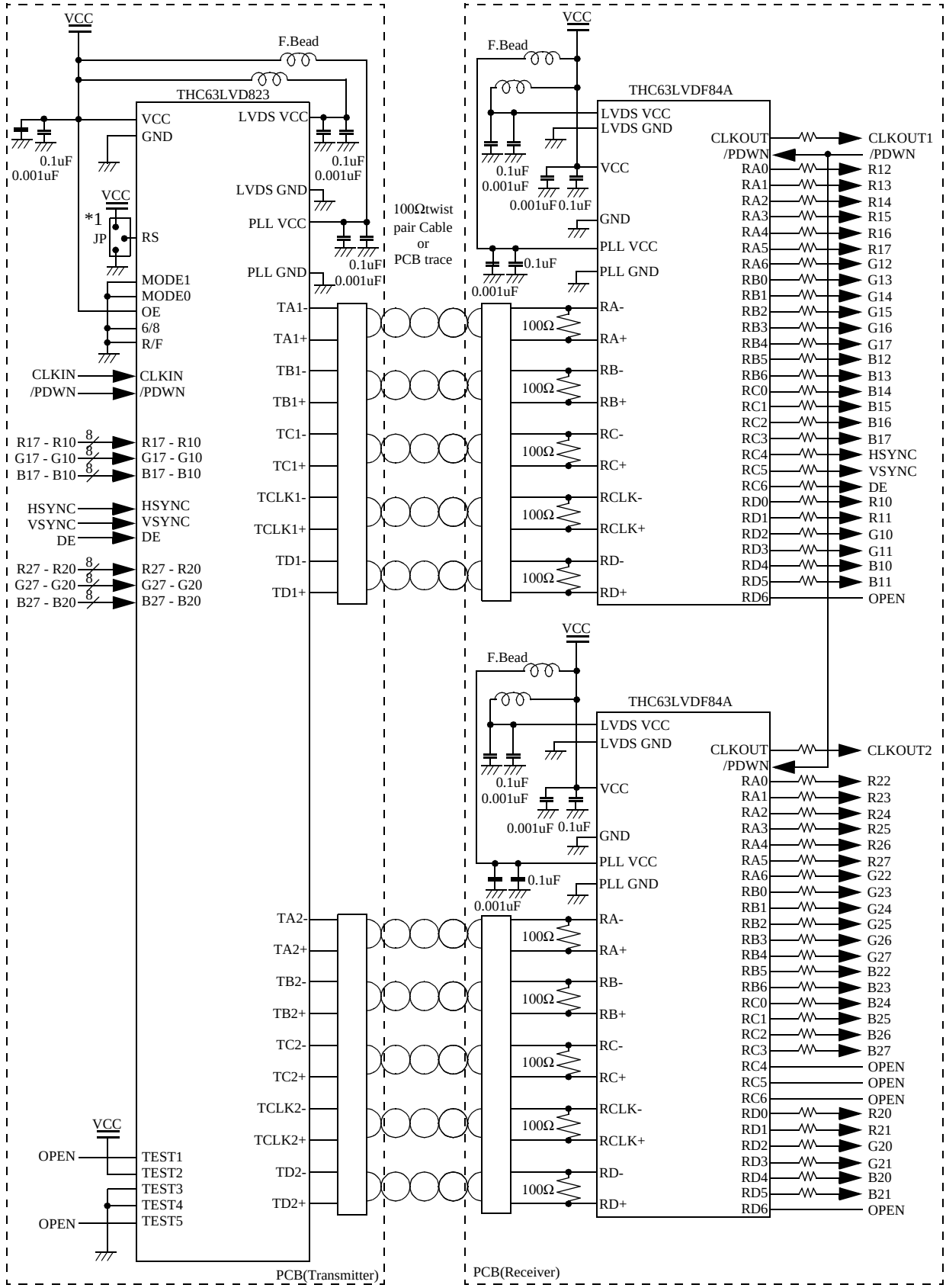
4) Dual Link (SXGA, SXGA+, UXGA)

Example :
THC63LVDM83A : Falling edge/8 bit
THC63LVD824 : Dual in(LVDS)/Falling edge/8bit/Dual out(TTL)/Output driverbility Low



5) Dual Link (SXGA, SXGA+, UXGA)

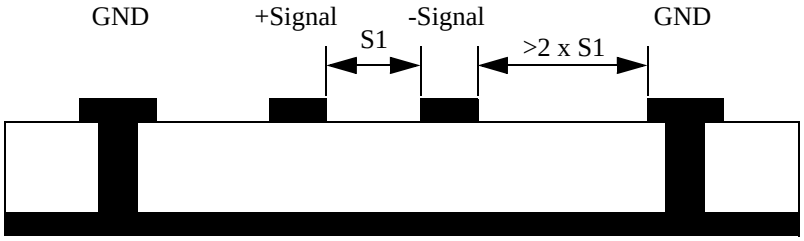
Example :
THC63LVD823 : Falling edge/8 bit/Dual in(TTL)-Dual out(LVDS)
THC63LVDF84A : Falling edge/8bit



*1: If RS pin tied to VCC, LVDS swing is 350mV.
If RS pin tied to GND, LVDS swing is 200mV.

PCB Design Guide Line for LVDS

- Interconnecting media between Transmitter and Receiver (i.e. PCB trace, connector, and cable) should be well balanced.(Keep all these differential impedance and the length of media as same as possible.).
- Locate by-pass capacitors adjacent to the device pins as close as possible.
- Minimize the distance between traces of a pair (S1) to maximize common mode rejection. See following figure.
- Place adjacent LVDS trace pair at least twice (>2 x S1) as far away.
- Avoid 90 degree bends.
- Minimize the number of VIA on LVDS traces.
- Match impedance of PCB trace, connector, media (cable) and termination to minimize reflections (emissions) for cabled applications (typically 100Ω differential mode characteristic impedance).
- Use 4 layer PCB (minimum).



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