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Revision History

V1.0 Initial Released

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Size: A	Document Number: Index and Revision History	Rev: 1
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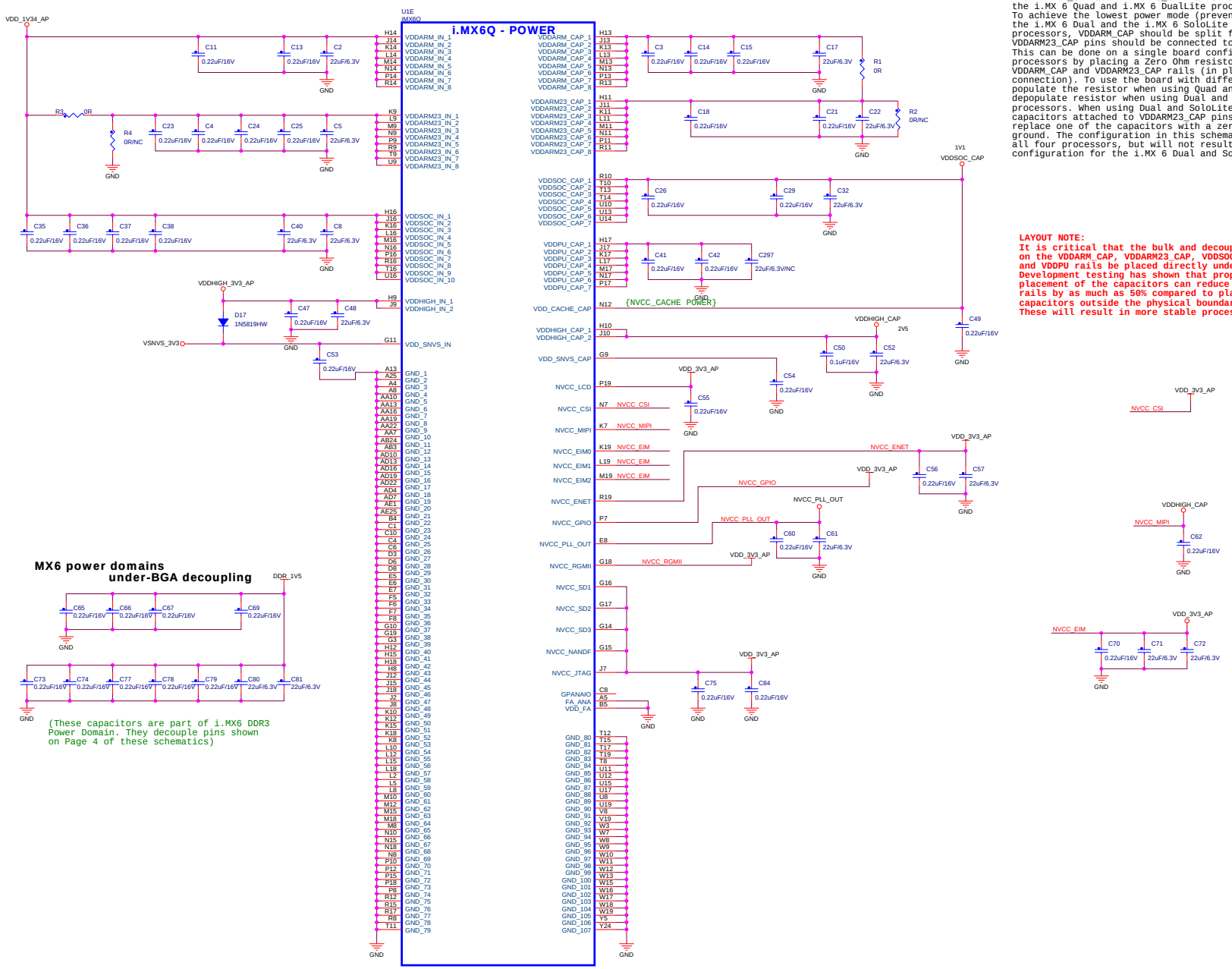

NOTE:
The VDDARM_CAP and VDDARM23_CAP rails have been optimized for use with the i.MX 6 Quad and i.MX 6 DualLite processors.
To achieve the lowest power mode (preventing internal leakage) when using the i.MX 6 Dual and the i.MX 6 SoloLite processors, VDDARM_CAP should be split from VDDARM23_CAP and the VDDARM23_CAP pins should be connected to ground.
This can be done on a single board configured for use with all four processors by placing a Zero Ohm resistor between the VDDARM_CAP and VDDARM23_CAP rails (in place of the straight net connection). To use the board with different processors, populate the resistor when using Quad and DualLite processors and depopulate resistor when using Dual and SoloLite processors. When using Dual and SoloLite processors, depopulate the capacitors attached to VDDARM23_CAP pins and replace one of the capacitors with a zero Ohm resistor to short pins to ground. The configuration in this schematic will work with all four processors, but will not result in the most power optimized configuration for the i.MX 6 Dual and Solo processors.

LAYOUT NOTE:
It is critical that the bulk and decoupling capacitors placed on the VDDARM_CAP, VDDARM23_CAP, VDDSOC_CAP and VDDPU rails be placed directly underneath the processors. Development testing has shown that proper placement of the capacitors can reduce ripple on the voltage rails by as much as 50% compared to placing capacitors outside the physical boundaries of the processor. These will result in more stable processor operations.

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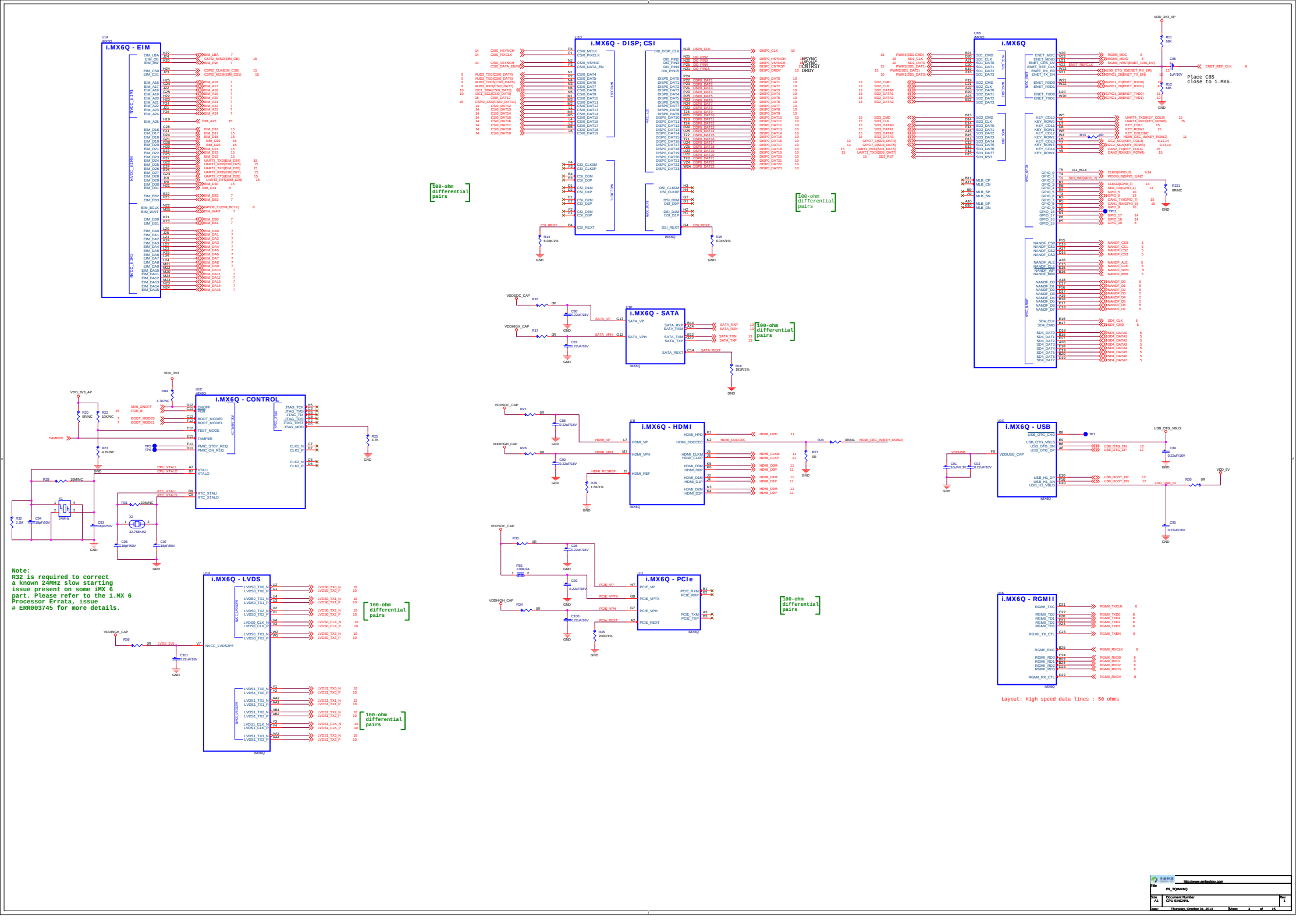
i.MX6Q - EIM
i.MX6Q - DISP; CSI
i.MX6Q
i.MX6Q - CONTROL
i.MX6Q - SATA
i.MX6Q - HDMI
i.MX6Q - USB
i.MX6Q - LVDS
i.MX6Q - PCIe
i.MX6Q - RGMII
100-ohm differential pairs
Place C85 close to i.MX6.
Note:
R32 is required to correct a known 24MHz slow starting issue present on some iMX 6 part. Please refer to the i.MX 6 Processor Errata, issue # ERR003745 for more details.
Layout: High speed data lines : 50 ohms
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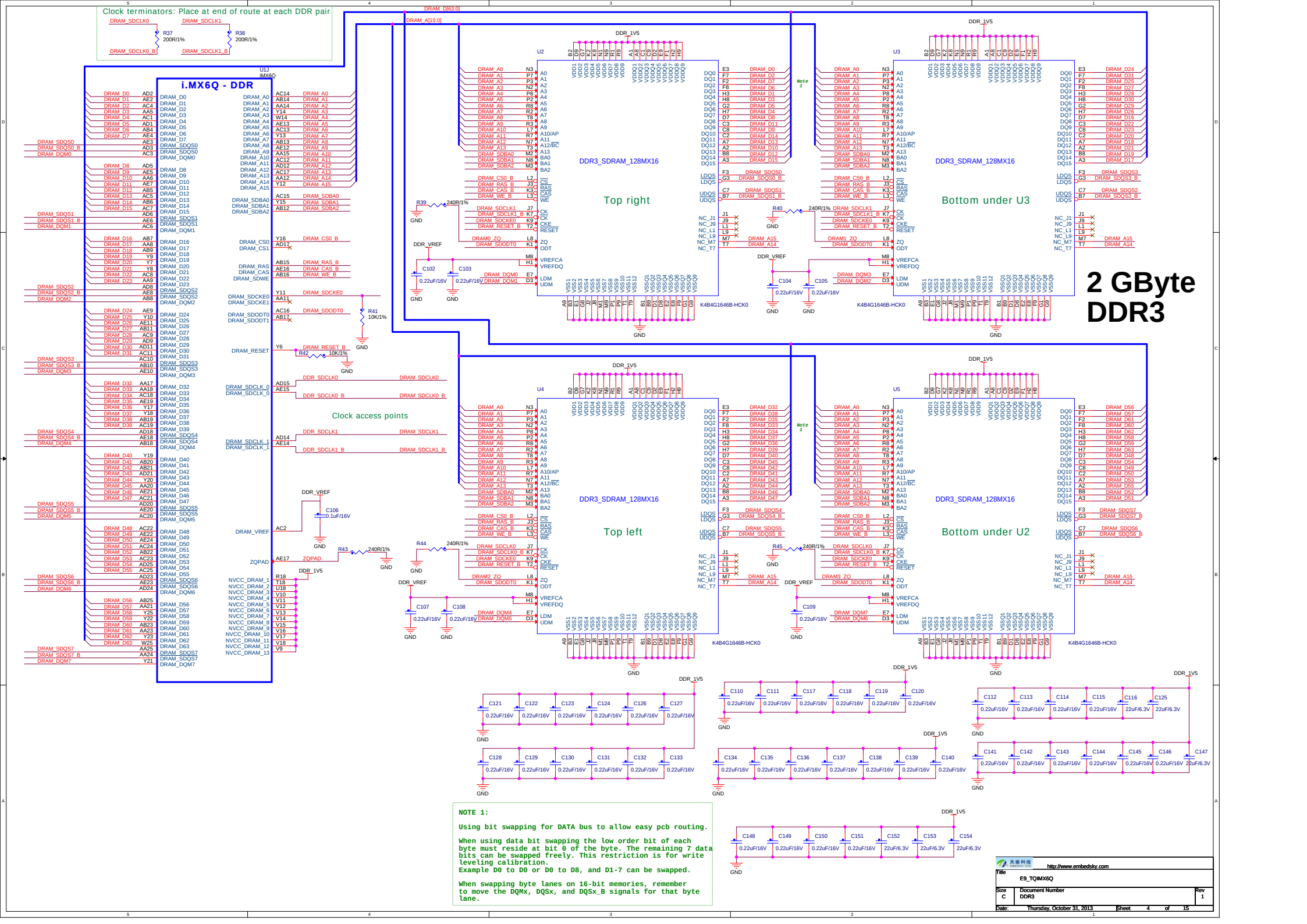
Clock terminators: Place at end of route at each DDR pair
DRAM_SDCLK0
DRAM_SDCLK1
R37 200R/1%
R38 200R/1%
DRAM_SDCLK0_B
DRAM_SDCLK1_B
i.MX6Q - DDR
U1J iMX6Q
DRAM_D[63:0]
DRAM_A[15:0]
U2
U3
U4
U5
DDR3_SDRAM_128MX16
K4B4G1646B-HCK0
Top right
Bottom under U3
Top left
Bottom under U2
Clock access points
2 GByte DDR3
Note 1
NOTE 1:
Using bit swapping for DATA bus to allow easy pcb routing.
When using data bit swapping the low order bit of each byte must reside at bit 0 of the byte. The remaining 7 data bits can be swapped freely. This restriction is for write leveling calibration.
Example D0 to D0 or D0 to D8, and D1-7 can be swapped.
When swapping byte lanes on 16-bit memories, remember to move the DQMx, DQSx, and DQSx_B signals for that byte lane.
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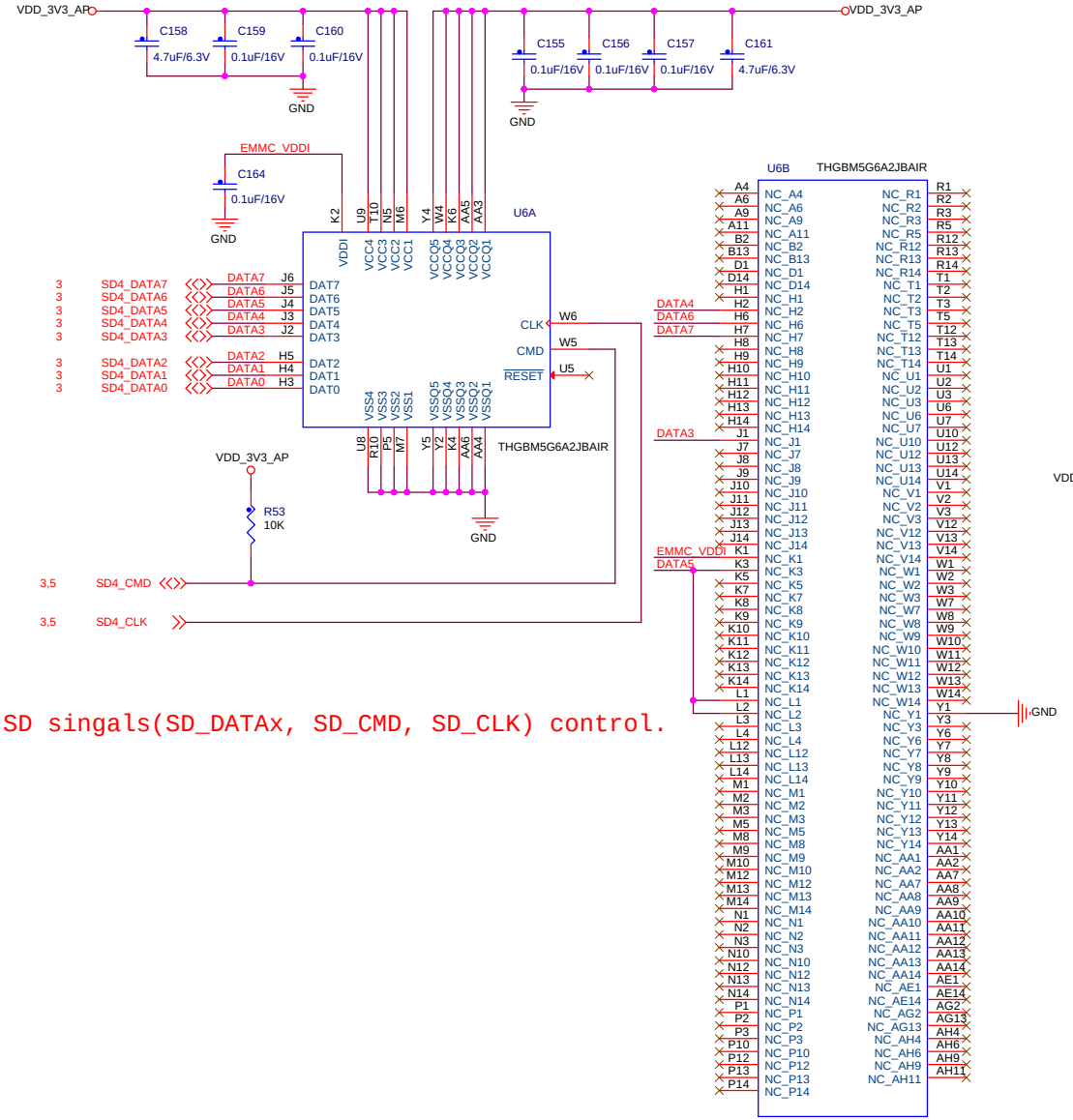
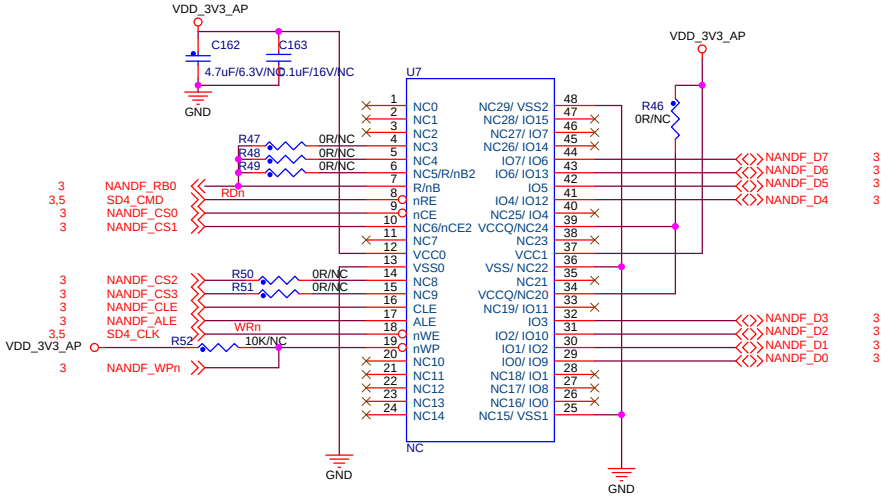
8GB eMMC MEMORY



NAND Flash memory



Layout:
50ohm, SD singals(SD_DATAx, SD_CMD, SD_CLK) control.

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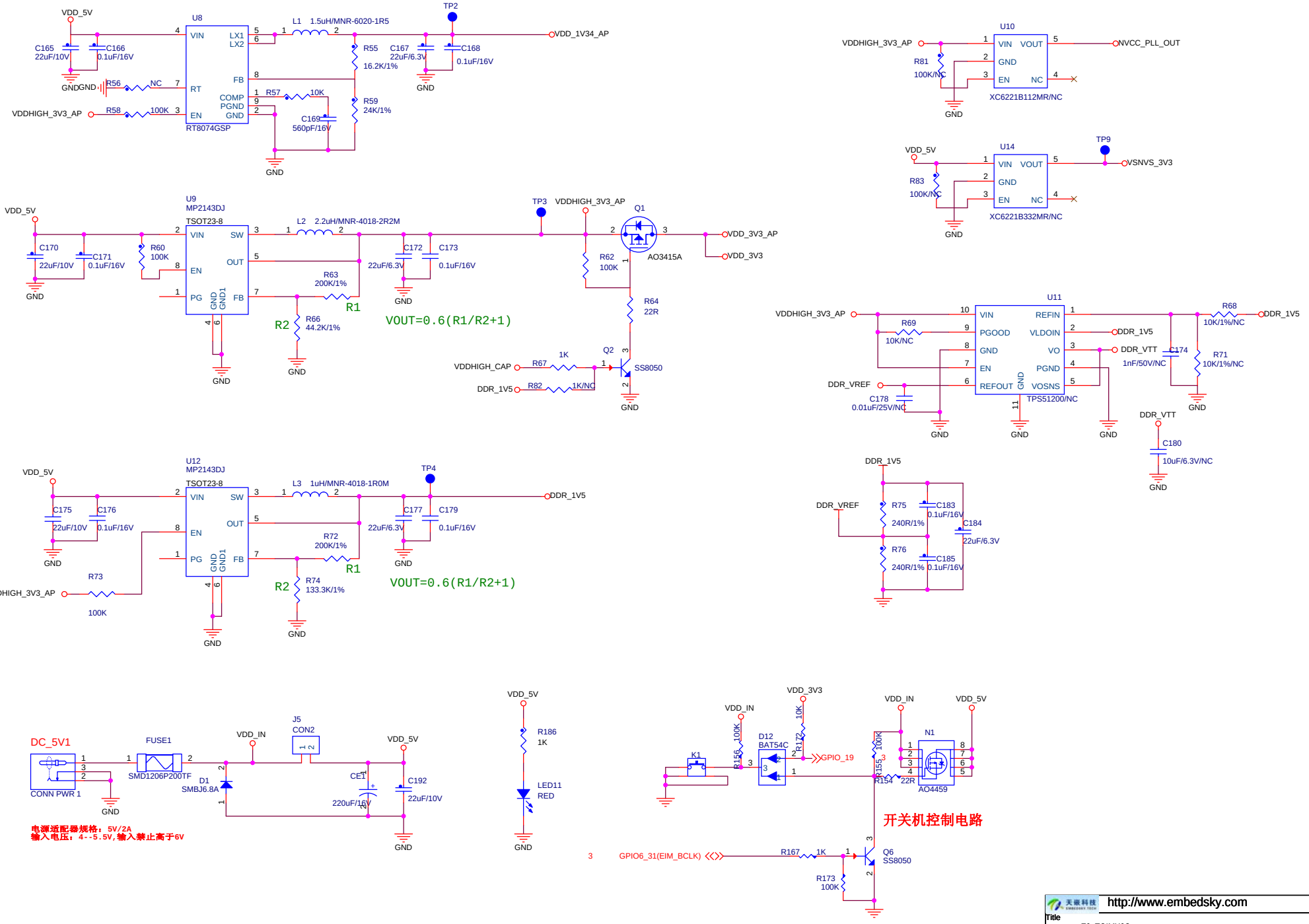
U8
RT8074GSP
L1 1.5uH/MNR-6020-1R5
VDD_5V
VDD_1V34_AP
TP2
VDDHIGH_3V3_AP
U9
MP2143DJ
TSOT23-8
L2 2.2uH/MNR-4018-2R2M
TP3
Q1
AO3415A
VDD_3V3_AP
VDD_3V3
R1
R2
VOUT=0.6(R1/R2+1)
VDDHIGH_CAP
DDR_1V5
Q2
SS8050
U12
L3 1uH/MNR-4018-1R0M
TP4
U10
XC6221B112MR/NC
NVCC_PLL_OUT
U14
XC6221B332MR/NC
TP9
VSNVS_3V3
U11
TPS51200/NC
DDR_VREF
DDR_VTT
DC_5V1
CONN PWR 1
FUSE1
SMD1206P200TF
D1
SMBJ6.8A
J5
CON2
VDD_IN
电源适配器规格：5V/2A
输入电压：4--5.5V,输入禁止高于6V
LED11
RED
K1
D12
BAT54C
GPIO_19
N1
AO4459
开关机控制电路
GPIO6_31(EIM_BCLK)
Q6
SS8050
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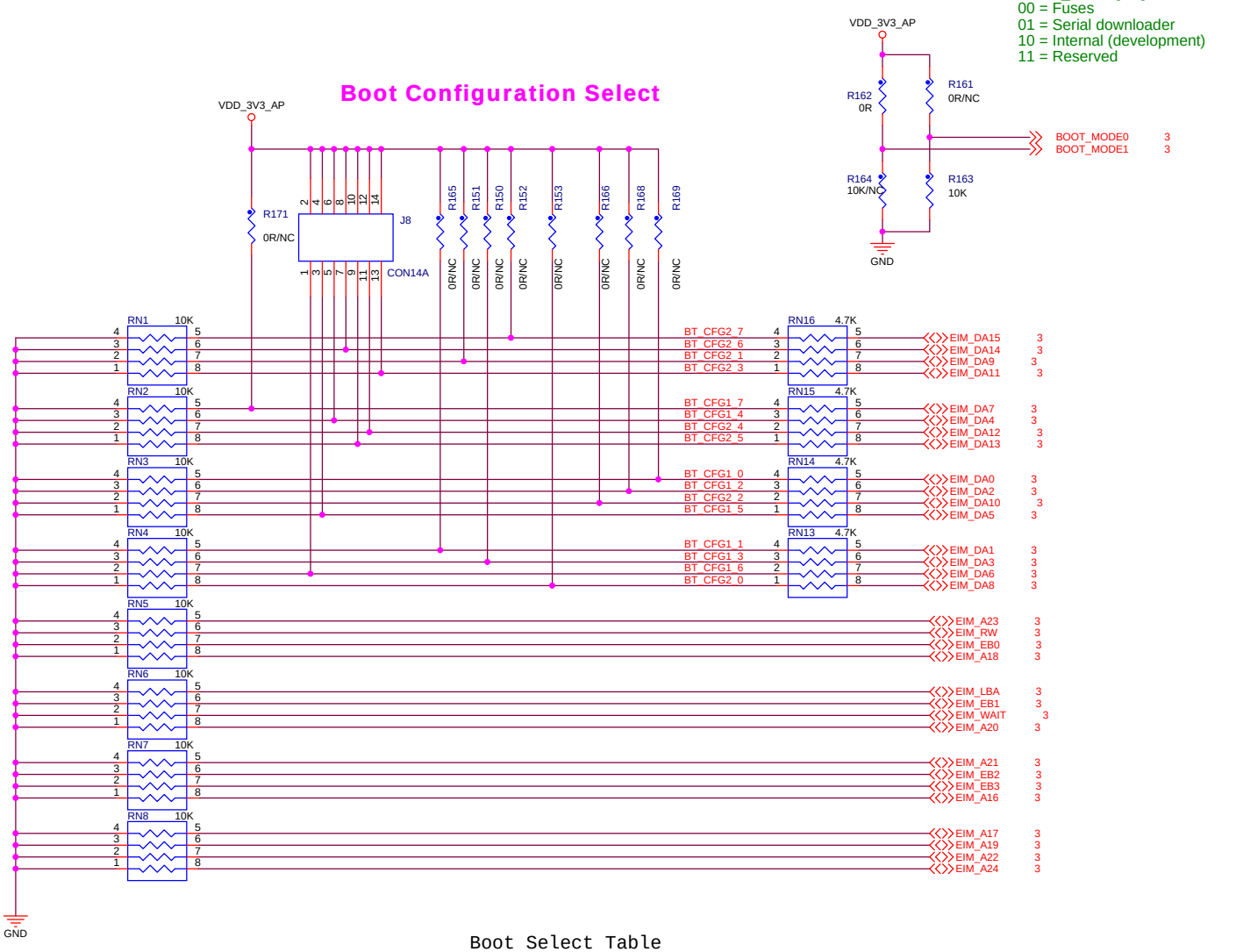
BOOT_MODE[1:0] SETTINGS
00 = Fuses
01 = Serial downloader
10 = Internal (development)
11 = Reserved

Boot Configuration Select



Boot Select Table

Boot Device	1 BT_CFG1_6	2 BT_CFG1_5	3 BT_CFG1_4	4 BT_CFG2_6	5 BT_CFG2_5	6 BT_CFG2_4	7 BT_CFG2_3
eMMC	1	1	X	X	1	1	1
SD	1	0	X	X	0	0	1
DownLoad	0	1	1	0	0	0	0

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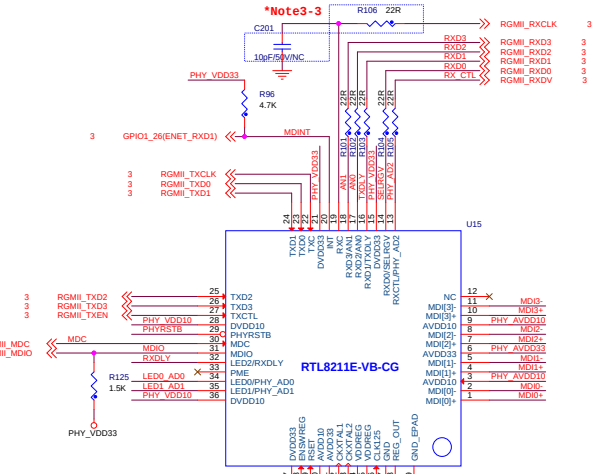
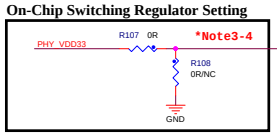
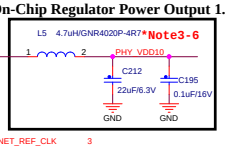
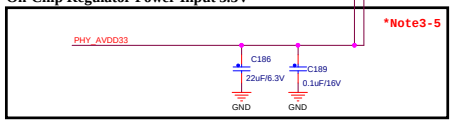
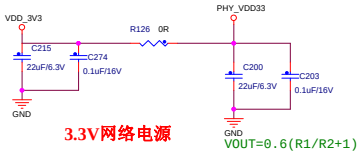
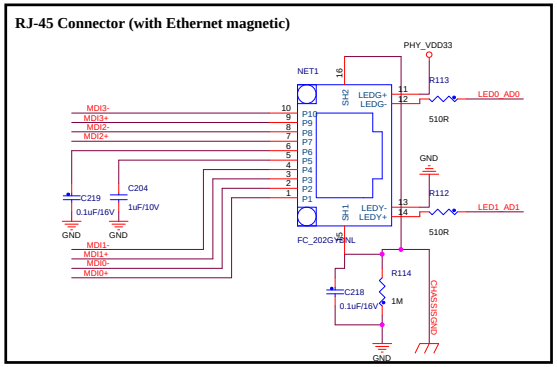


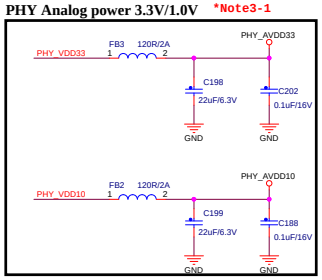


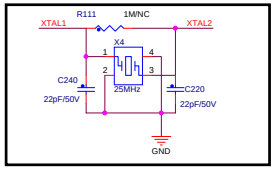


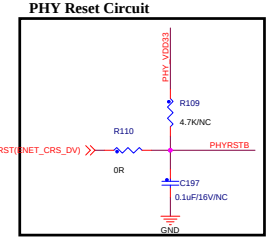


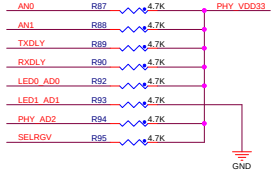












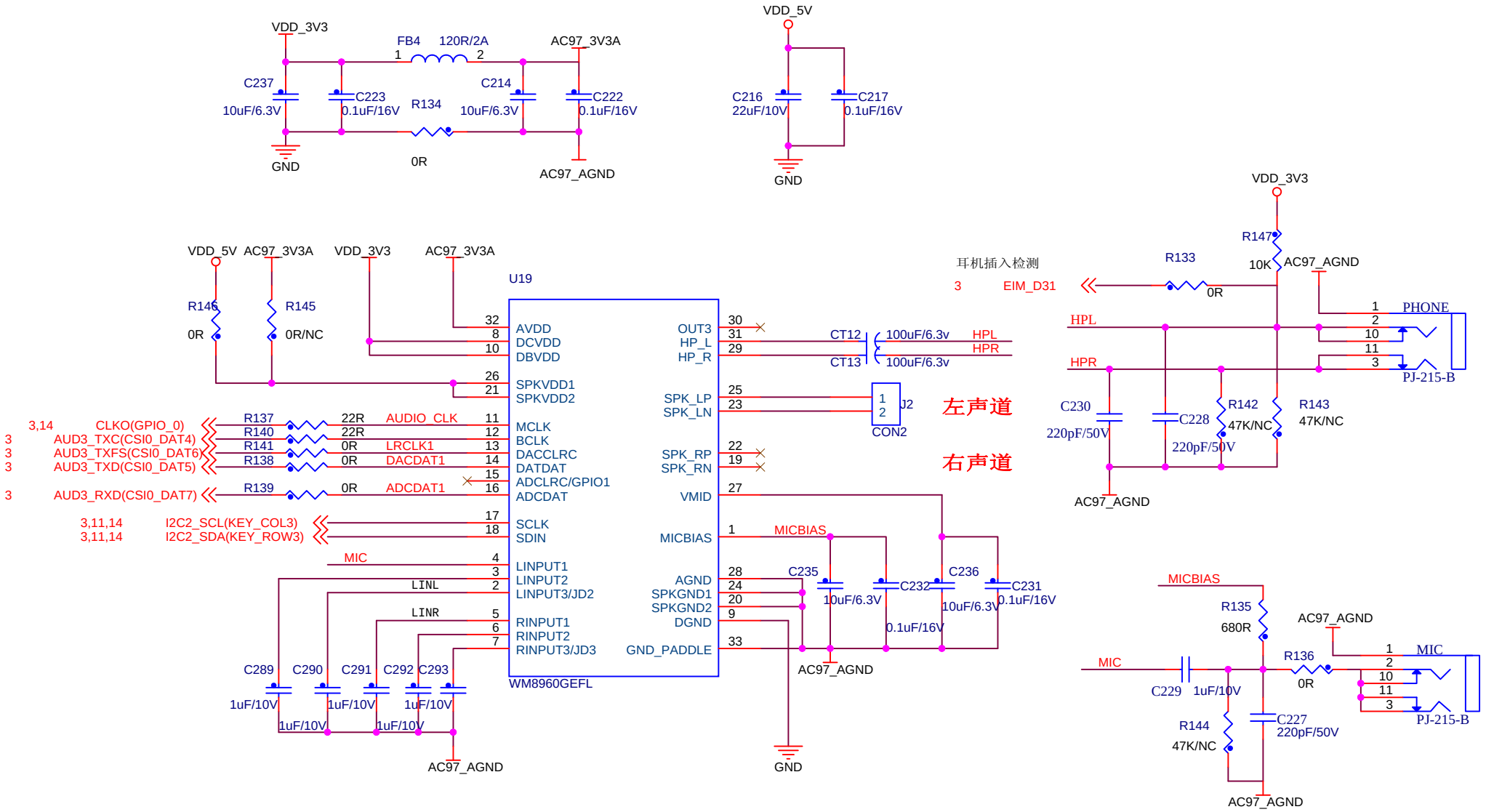
	AN0 Pull High	**AN1 Pull High**	**Enable all Nway capabilities**
	TXDLY Pull High	**RXDLY Pull High**	**Delay TXCLK/RXCLK 2ns**
AD2 Pull Low	**AD1 Pull Low**	**AD0 Pull High**	**PHY Address=001 (0x01)**
		SELREG Pull High	**Pull Up for 3.3V GMII/RGMII**

***Note3-3**
The R106 and C201 are reserved for EMI, please close to PHY as possible.

***Note3-4**
1. Enable On-chip Switch Regulator: (Default)
Connect ENSWREG to PHY_VDD33 (i.e. Mount R107and unmount R108)
2. Disable On-chip Switch Regulator:
Connect ENSWREG to GND (i.e. Mount R108 and unmount R107)

***Note3-5**
The 3.3V power input VDDREG trace should be wider than 100mils (Keep floating while disabling on-chip switching regulator)
The capacitors C186 and C189 as close to the VDDREG pin (within 200mils) for good power effeciency.
C186 must be a ceramic (X5R) capacitor
C189 is recommended to be ceramic capacitor

***Note3-6**
L5 (4.7uH) should be as close to RTL8211E REG_OUT pin (within 200mils).
The 1.05V power output REG_OUT trace should be wider than 60 mils.
The C212 and C195 capacitors as close to L2 if possible. (Keep floating while disabling on-chip switching regulator)
C212 must be a ceramic (X5R) capacitor
C195 is recommended to be ceramic capacitor



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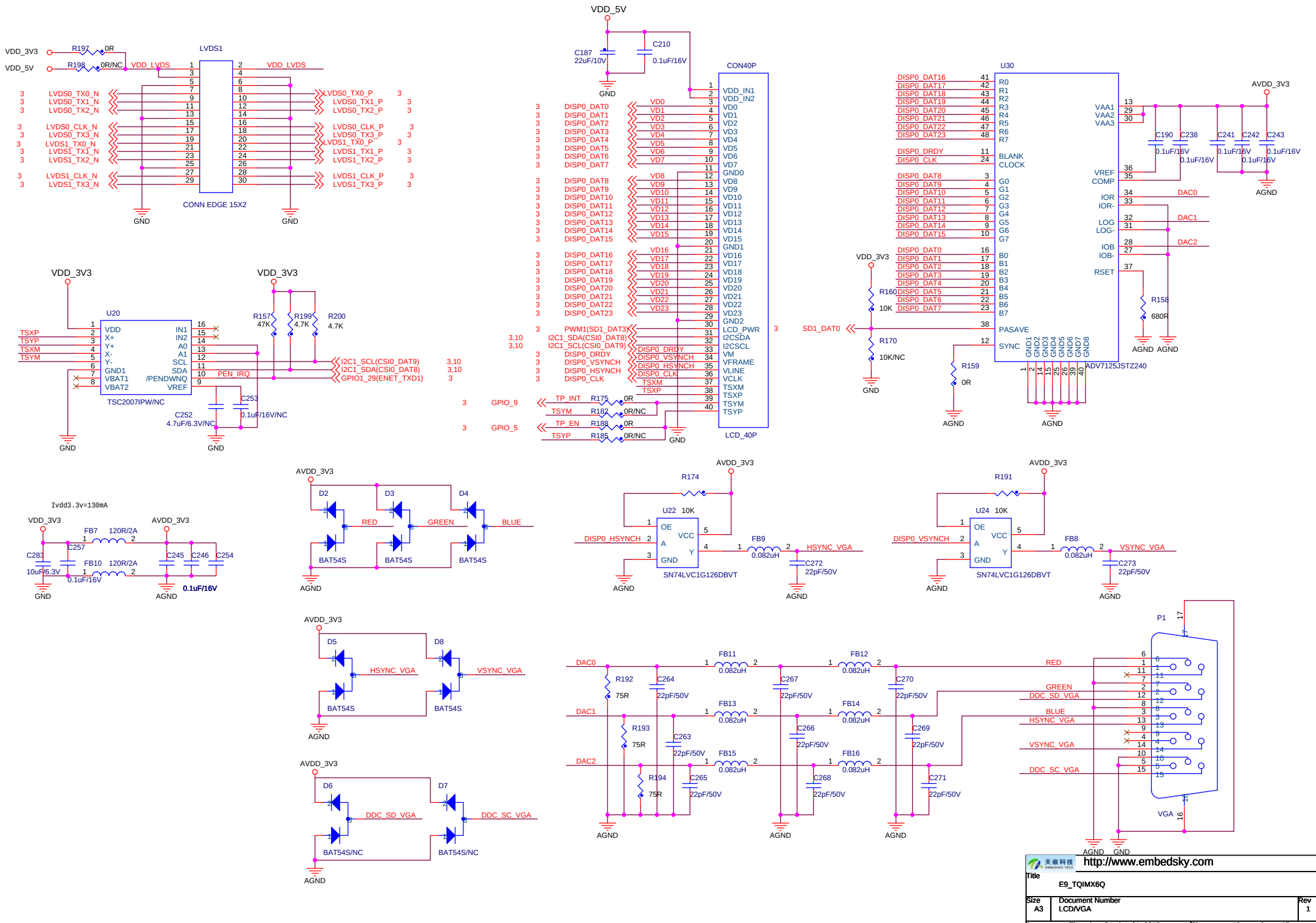

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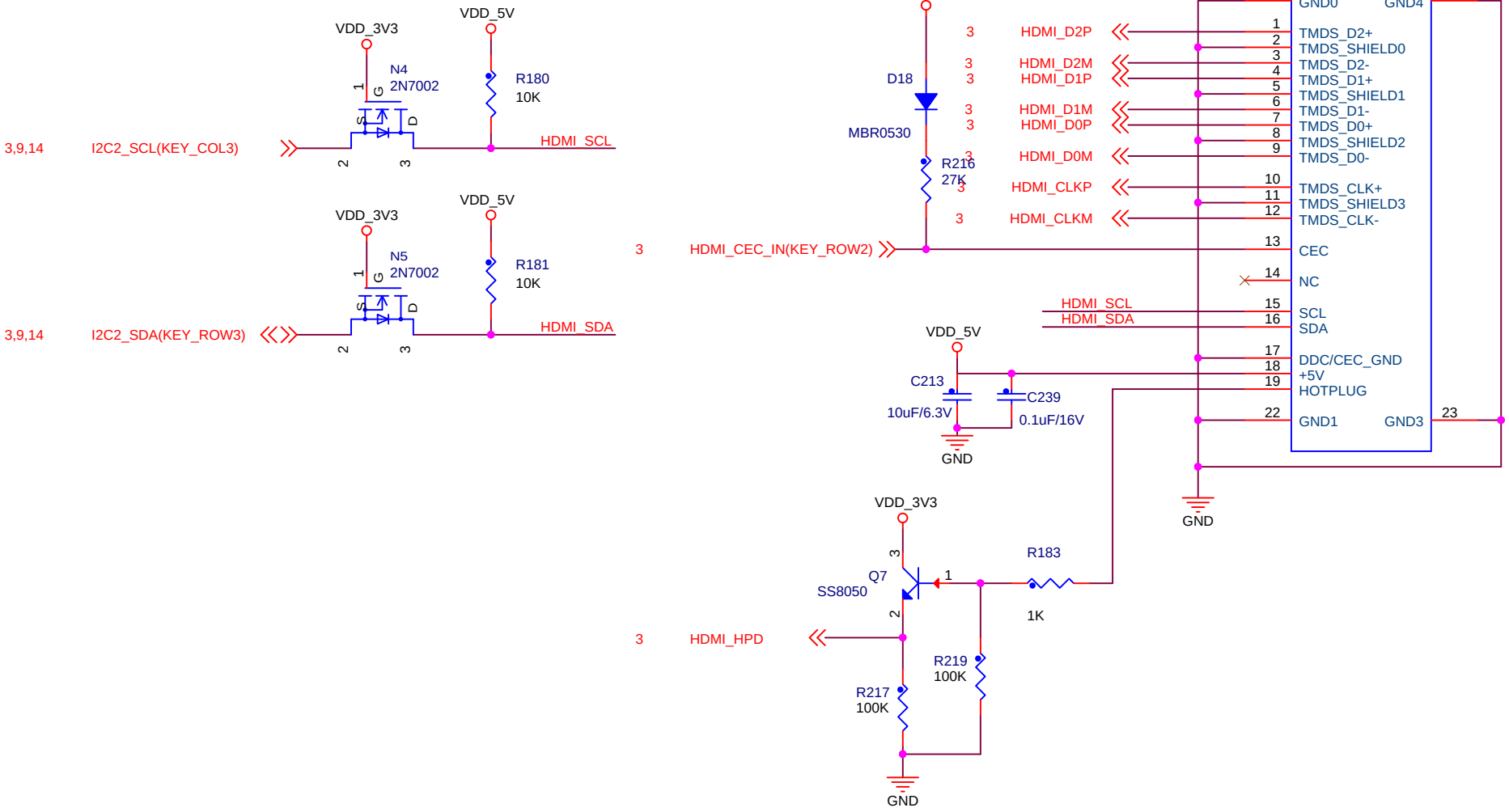
HDMI



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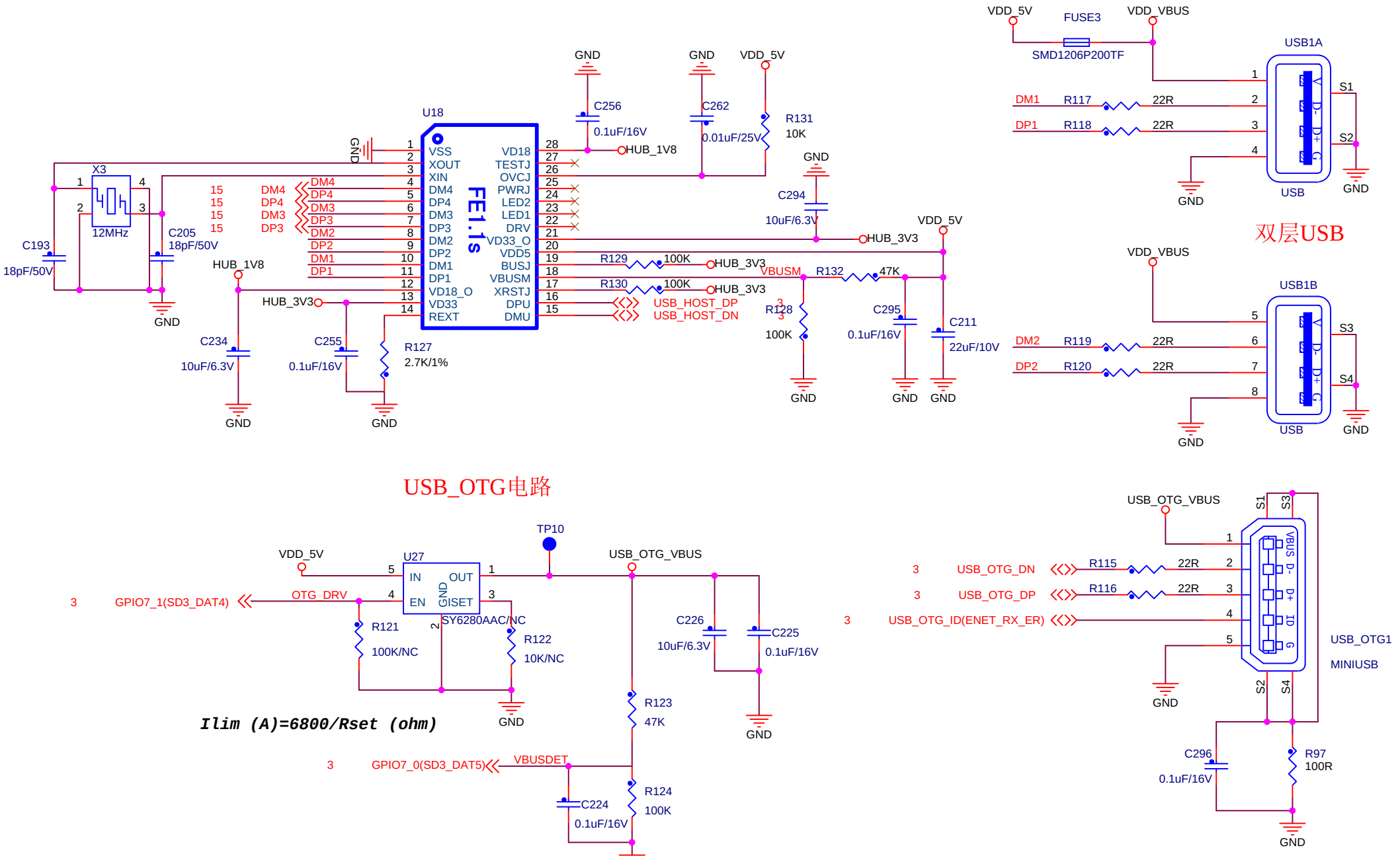

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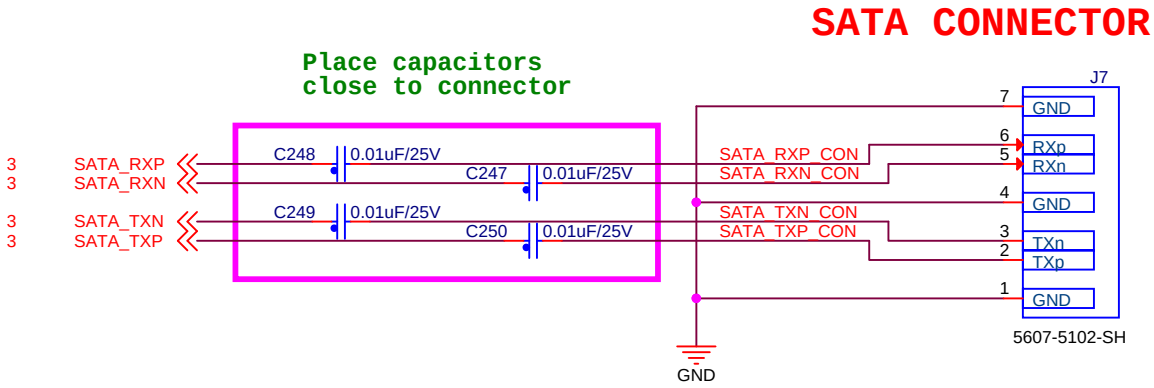
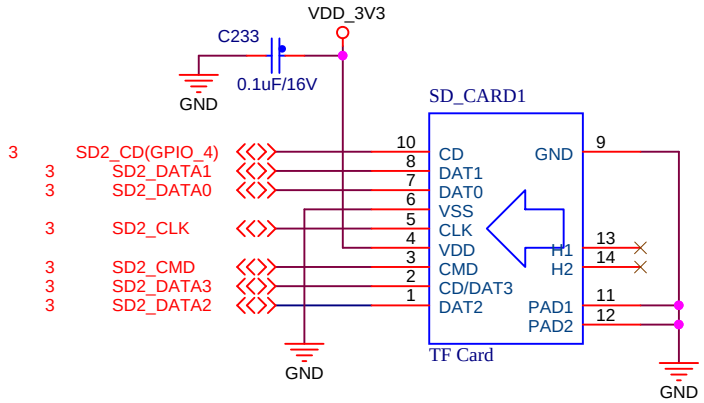
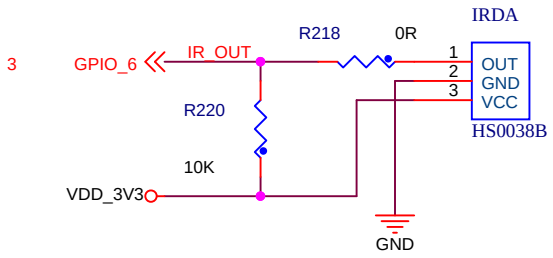
SATA CONNECTOR





红外电路



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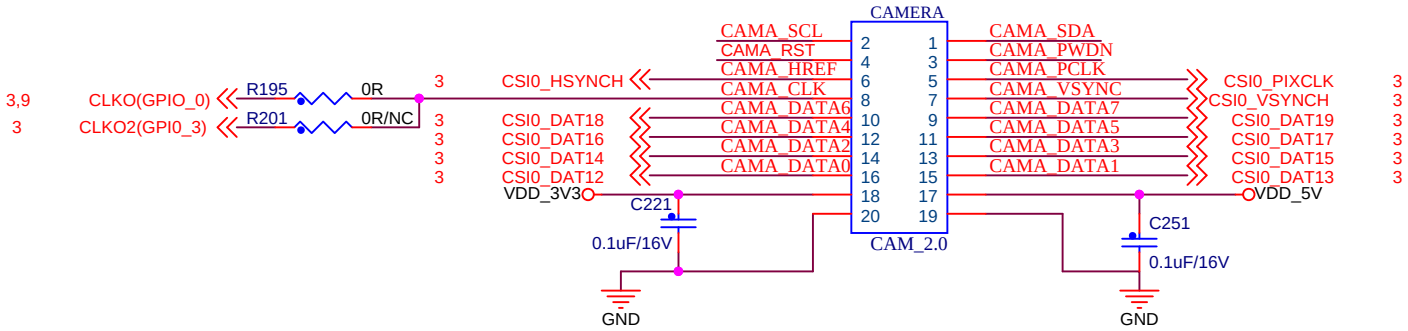
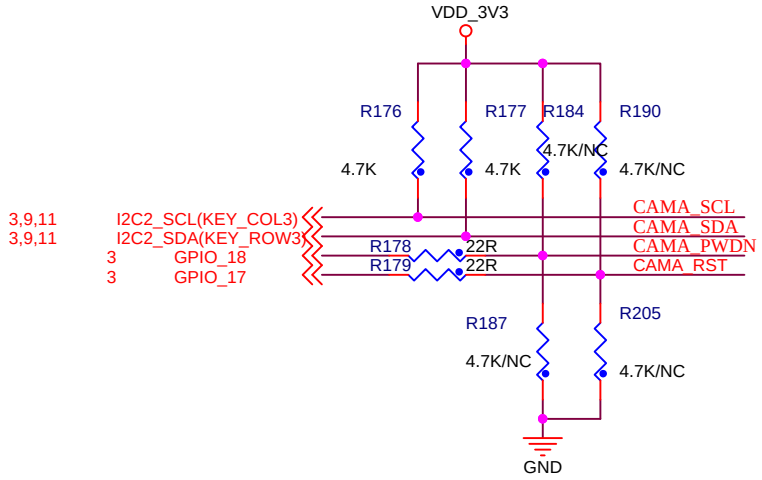
CAMMER A





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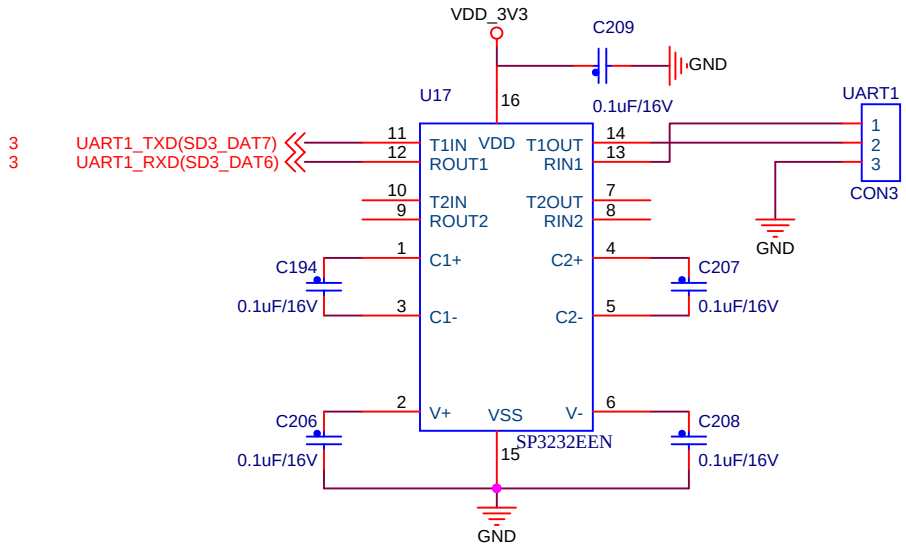
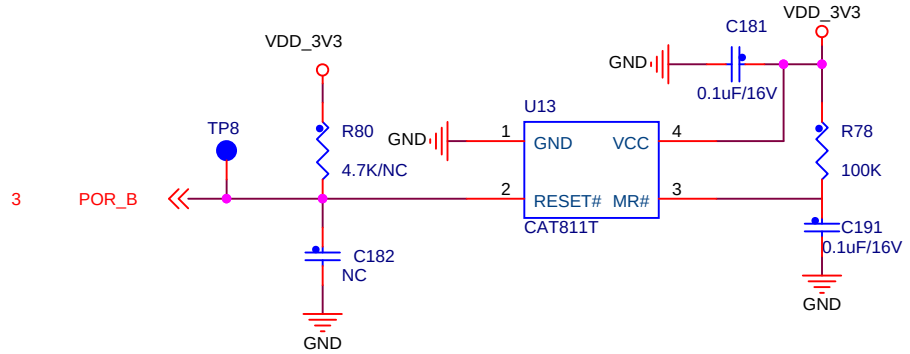
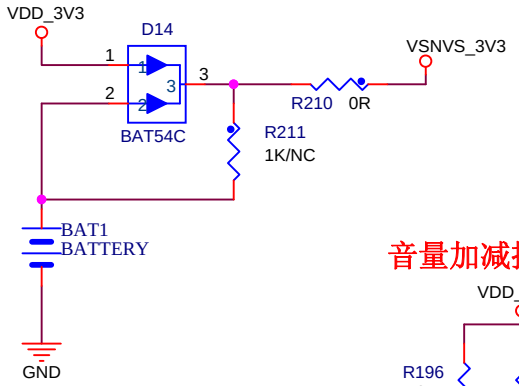




RTC电路



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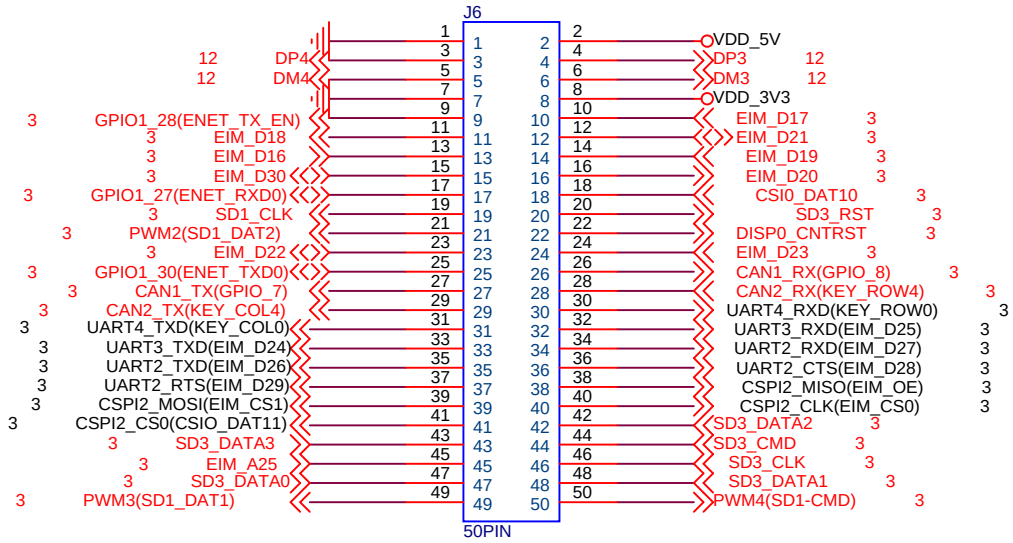
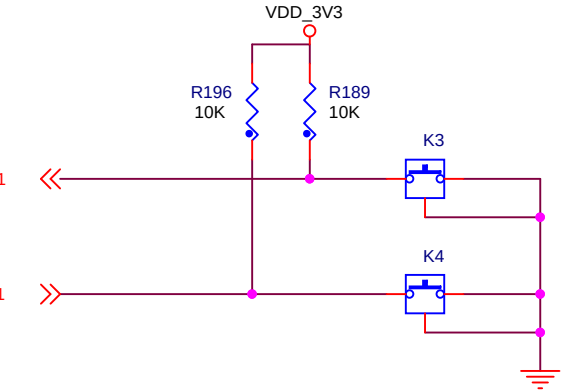


音量加减控制按键



H1
H2
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