# Specification for Approval

**PRODUCT NAME :** **RGS13128096WH000**
**PRODUCT NO.:** **9914201000**

| CUSTOMER |
| --- |
| |
| **APPROVED BY** |
| |
| **DATE:** |

| RITDISPLAY CORP. APPROVED |
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| |

# REVISION RECORD

| REV. | REVISION DESCRIPTION | REV. DATE | REMARK |
|---|---|---|---|
| X01 | INITIAL RELEASE | 2006. 01. 12 | |
| X02 | ■ Add the operating conditions for different luminance<br>■ Add the panel electrical specification<br>■ Modify the CIE specification<br>■ Add the application circuit | 2006. 03. 01 | Page 6, 7, 8 & 17 |
| A01 | ■ Modify features<br>■ Add the information of module weight<br>■ Modify lifetime specification<br>■ Modify panel electrical specifications – current, power consumption, luminance & contrast setting | 2006. 05. 08 | Page 4, 5, 6, 8 & 20 |
| A02 | ■ Correct description of pin assignments | 2006. 06. 02 | Page 10 |
| A03 | ■ Modify lifetime specification<br>■ Modify D.C electrical characteristics<br>■ Modify panel electrical specification – current, power consumption, luminance & contrast setting<br>■ Modify description of pin assignment<br>■ Modify 8080-series MPU parallel interface characteristics<br>■ Modify reliability test conditions<br>■ Modify seal dimension | 2006. 08. 14 | Page 6, 7, 8, 10, 13, 18 & 19 |
| A04 | ■ Modify specification of dark room contrast<br>■ Modify D.C electrical characteristics<br>■ Modify CIE tolerance (±0.4→±0.3)<br>■ Modify power on/off sequence | 2007. 05. 10 | Page 4, 7, 8 & 16 |

# CONTENTS

## 1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Ass'y Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

## 2. WARRANTY

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.
After the Warranty Period, all repairs or replacements of the products are subject to charge.

## 3. FEATURES

- Small Molecular Passive Organic Light Emission Diode.
- Color : White
- Panel matrix : 128*96
- Driver IC : SSD1329U2
- Excellent Quick response time : 10μs
- Extremely thin thickness for best mechanism design : 1.65mm.
- High contrast : 2000:1
- Wide viewing angle : 160°
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface.
- Wide range operating temperature : -40 to 70 °C
- Anti-glare polarizer.

## 4. MECHANICAL DATA

| NO | ITEM | SPECIFICATION | UNIT |
|---|---|---|---|
| 1 | Dot Matrix | 128 (W) x 96 (H) | dot |
| 2 | Dot Size | 0.19 (W) x 0.19 (H) | $mm^2$ |
| 3 | Dot Pitch | 0.21 (W) x 0.21 (H) | $mm^2$ |
| 4 | Aperture Rate | 82 | % |
| 5 | Active Area | 26.86 (W) x 20.14 (H) | $mm^2$ |
| 6 | Panel Size | 33 (W) x 26.8 (H) | $mm^2$ |
| 7 | Panel Thickness | 1.65 | mm |
| 8 | Module Size | 33 (W) x 41.6 (H) x 1.65 (T) | $mm^3$ |
| 9 | Diagonal A/A size | 1.3 | inch |
| 10 | Module Weight | 2.88 ± 10% | gram |

## 5. MAXIMUM RATINGS

| ITEM | MIN | MAX | UNIT | Condition | Remark |
|---|---|---|---|---|---|
| Supply Voltage ($V_{DD}$) | -0.3 | 3.5 | V | Ta = 25°C | IC maximum rating |
| Supply Voltage (Vcc) | 8 | 16 | V | Ta = 25°C | IC maximum rating |
| Operating Temp. | -40 | 70 | °C | | |
| Storage Temp | -40 | 85 | °C | | |
| Humidity | | 85 | % | | |
| Life Time | 10,000 | - | Hrs | 120 cd/m$^2$, 50% checkerboard | Note (1) |
| Life Time | 13,000 | - | Hrs | 100 cd/m$^2$, 50% checkerboard | Note (2) |
| Life Time | 16,000 | - | Hrs | 80 cd/m$^2$, 50% checkerboard | Note (3) |

Note:

(A) Under Vcc = 15V, Ta = 25°C, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 120 cd/m$^2$ :

- Contrast setting : 0x95
- Frame rate : 85Hz
- Duty setting : 1/96

(2) Setting of 100 cd/m$^2$ :

- Contrast setting : 0x72
- Frame rate : 85Hz
- Duty setting : 1/96

(3) Setting of 80 cd/m$^2$ :

- Contrast setting : 0x4F
- Frame rate : 85Hz
- Duty setting : 1/96

# 6. ELECTRICAL CHARACTERISTICS

## 6.1 D.C ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETERS | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Driver power supply (for OLED panel) | Ta=-20°C to +70°C | 14.5 | 15 | 15.5 | V |
| $V_{DD}$ | Logic operating voltage | Ta=-20°C to +70°C | 2.4 | 2.7 | 3.5 | V |
| $V_{DDIO}$ | MCU interface operating voltage | - | 1.7 | - | $V_{DD}$ | V |
| $V_{OH}$ | Hi logic output level | Iout=100 uA, 3.3MHz | 0.9* $V_{DDIO}$ | - | $V_{DDIO}$ | V |
| $V_{OL}$ | Low logic output level | Iout=100uA, 3.3MHZ | 0 | - | 0.1* $V_{DDIO}$ | V |
| $V_{IH}$ | Hi logic input level | Iout=100uA, 3.3MHZ | 0.8* $V_{DDIO}$ | - | $V_{DDIO}$ | V |
| $V_{IL}$ | Low logic input level | Iout=100uA, 3.3MHZ | 0 | - | 0.2* $V_{DDIO}$ | V |
| $I_{CC}$ | Operating current for $V_{CC}$ | Contrast=80 | 400 | 440 | 480 | uA |
| $I_{DD}$ | Operating current for $V_{DD}$ | Contrast=80 | 25 | 40 | 55 | uA |
| $I_{SEG}$ | Segment Output Current Setting: IREF = 10uA, Display ON, Segment pin under test is connected with a 20K resistive load to VSS. | Contrast=FF | 290 | 320 | 350 | uA |
| | | Contrast=AF | 200 | 220 | 240 | uA |
| | | Contrast=5F | 110 | 120 | 130 | uA |
| | | Contrast=0F | 15 | 20 | 25 | uA |

Note : $V_{DD}$=3.0V ; Frame rate= 85 Hz ; No panel attached.

## 6.2 ELECTRO-OPTICAL CHARACTERISTICS

### PANEL ELECTRICAL SPECIFICATIONS

| PARAMETER | MIN | TYP. | MAX | UNITS | COMMENTS |
|---|---|---|---|---|---|
| Normal mode current | - | 21 | 23 | mA | All pixels on (1) |
| Standby mode current | - | 1 | 3 | mA | Standby mode 10% pixels on (2) |
| Normal mode power consumption | - | 315 | 345 | mW | All pixels on (1) |
| Standby mode power consumption | - | 15 | 45 | mW | Standby mode 10% pixels on (2) |
| Normal mode Luminance | 80 | 100 | | $cd/m^2$ | Display Average |
| Standby mode Luminance | | 10 | | $cd/m^2$ | Display Average |
| CIEx (White) | 0.25 | 0.28 | 0.31 | | x, y (CIE 1931) |
| CIEy (White) | 0.31 | 0.34 | 0.37 | | |
| Dark Room Contrast | 2000:1 | | | | |
| Viewing Angle | 160 | | | degree | |
| Response Time | | 10 | | μs | |

(1) Normal mode condition :

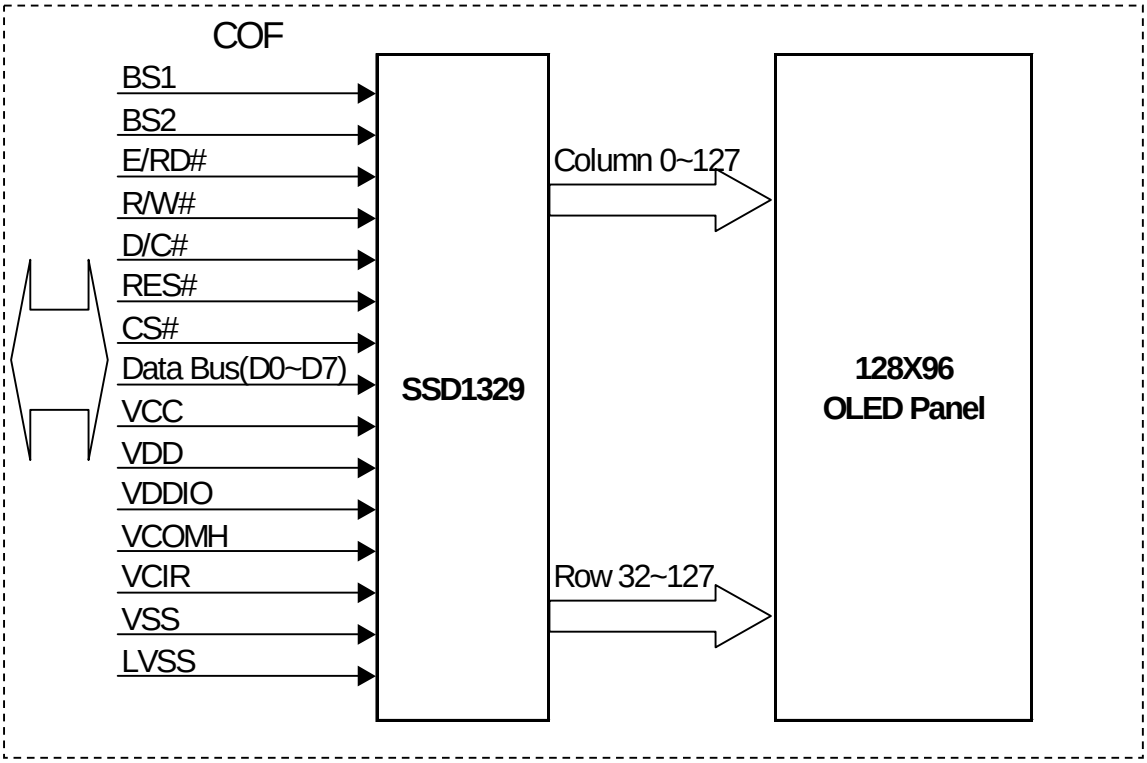
- Driving Voltage : 15V
- Contrast setting : 0x72
- Frame rate : 85Hz
- Duty setting : 1/96

(2) Standby mode condition :

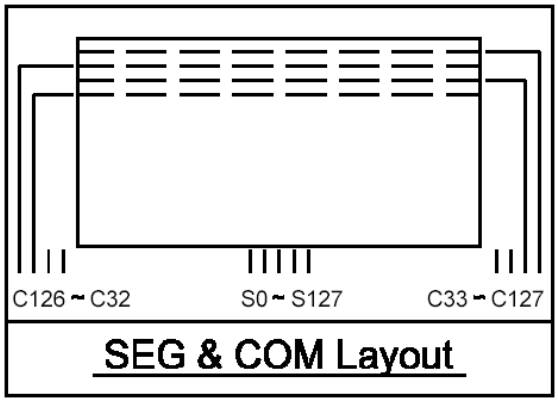
- Driving Voltage : 15V
- Contrast setting : 0x00
- Frame rate : 85Hz
- Duty setting : 1/96

# 7. INTERFACE

## 7.1 FUNCTION BLOCK DIAGRAM




## 7.2 PANEL LAYOUT DIAGRAM

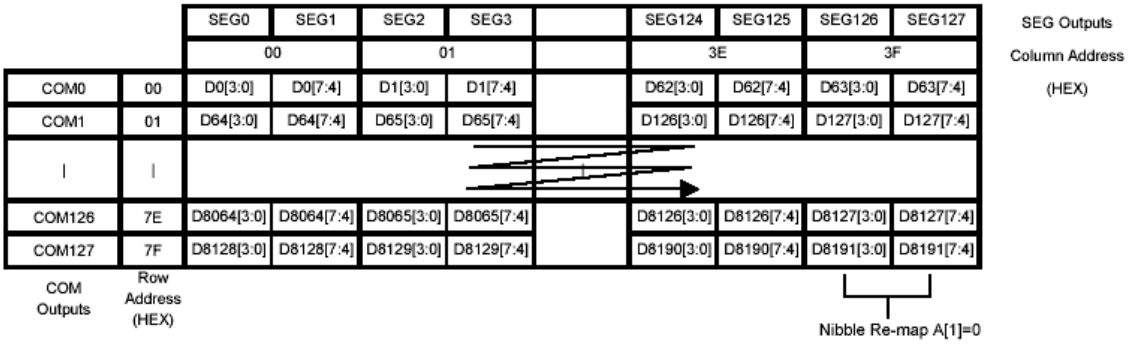


## 7.3 PIN ASSIGNMENTS

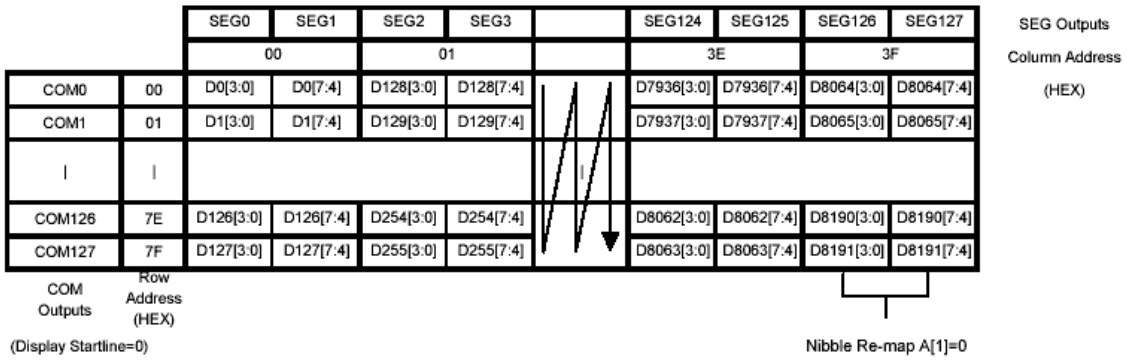
<table>
<tr><th>PIN NAME</th><th>PIN NO</th><th>DESCRIPTION</th></tr>
<tr><td>NC</td><td>1</td><td>No connection.</td></tr>
<tr><td>VCIR</td><td>2</td><td>No connection and left float.</td></tr>
<tr><td>VCOMH</td><td>3</td><td>Com Voltage Output. A capacitor should be connected between this pin and $V_{SS}$.</td></tr>
<tr><td>LVSS</td><td>4</td><td>Ground.</td></tr>
<tr><td>VSS</td><td>5</td><td>Ground.</td></tr>
<tr><td>BS1</td><td>6</td><td rowspan="2">MCU parallel interface selection input.
<table>
<tr><th></th><th>6800-parallel interface</th><th>8080-parallel interface</th><th>Serial interface</th></tr>
<tr><td>BS1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>BS2</td><td>1</td><td>1</td><td>0</td></tr>
</table></td></tr>
<tr><td>BS2</td><td>7</td></tr>
<tr><td>IREF</td><td>8</td><td>Reference current input pin.<br>A resistor should be connected between this pin and $V_{DD}$.</td></tr>
<tr><td>CS#</td><td>9</td><td>Chip select input.</td></tr>
<tr><td>RES#</td><td>10</td><td>Reset signal input.<br>When it’s low, initialization of SSD1329 is executed.</td></tr>
<tr><td>D/C#</td><td>11</td><td>Data/ Command control.<br>Pull high for write/read display data.<br>Pull low for write command or read status.</td></tr>
<tr><td>R/W#</td><td>12</td><td>MCU interface input.<br>Data write operation is initiated when it’s pull low.</td></tr>
<tr><td>E</td><td>13</td><td>MCU interface input. Data read operation is initiated when it’s pull low.</td></tr>
<tr><td>D0</td><td>14</td><td>Data bus(for parallel interface)</td></tr>
<tr><td>D1</td><td>15</td><td>Data bus(for parallel interface)</td></tr>
<tr><td>D2</td><td>16</td><td>Data bus(for parallel interface)</td></tr>
<tr><td>D3</td><td>17</td><td>Data bus(for parallel interface)</td></tr>
<tr><td>D4</td><td>18</td><td>Data bus(for parallel interface)</td></tr>
<tr><td>D5</td><td>19</td><td>Data bus(for parallel interface)</td></tr>
<tr><td>D6</td><td>20</td><td>Data bus(for parallel interface)</td></tr>
<tr><td>D7</td><td>21</td><td>Data bus(for parallel interface)</td></tr>
<tr><td>VDDIO</td><td>22</td><td>This pin is a power supply pin of I/O buffer.</td></tr>
<tr><td>VDD</td><td>23</td><td>Power supply for logic.</td></tr>
<tr><td>VCC</td><td>24</td><td>Power supply for analog circuit.</td></tr>
<tr><td>NC</td><td>25</td><td>No connection.</td></tr>
</table>

## 7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

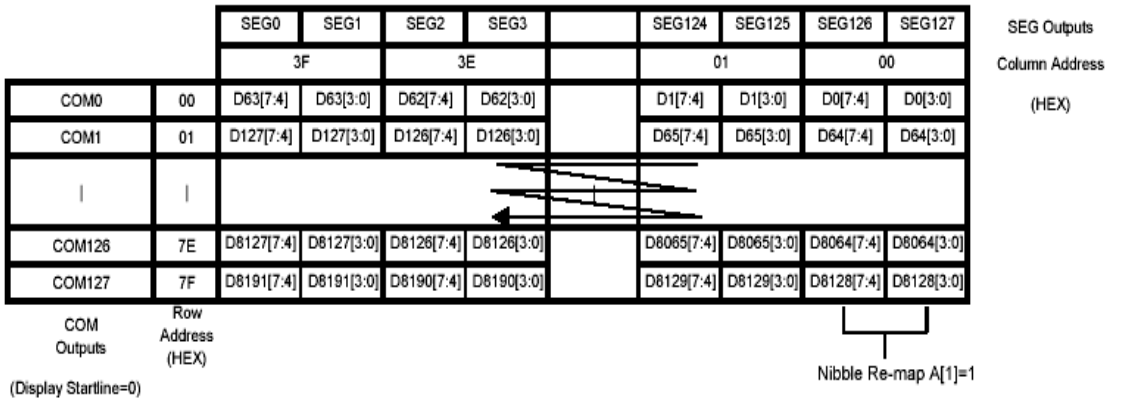
**GDDRAM Address Map - Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, Display Start Line=00H (Data byte sequence: D0, D1, D2 … D8191)**



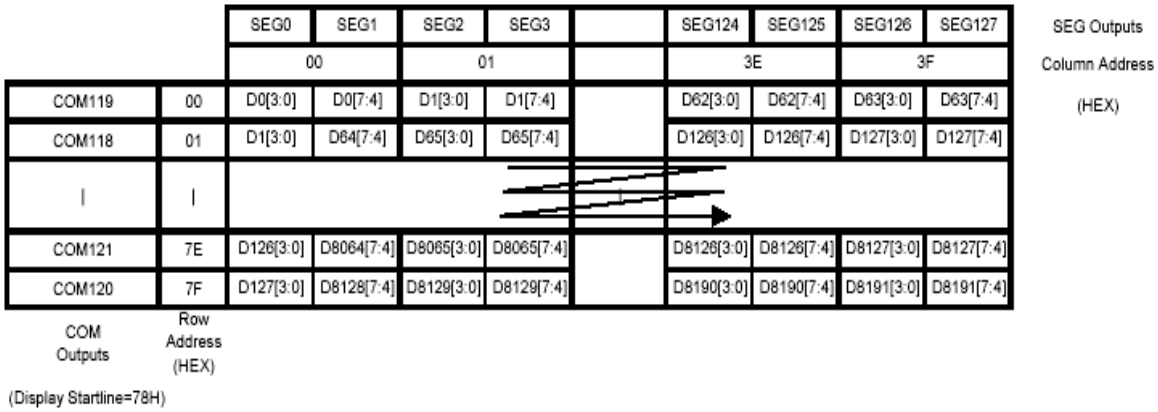

**GDDRAM Address Map - Vertical Address Increment A[2]=1, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, Display Start Line=00H (Data byte sequence: D0, D1, D2 … D8191)**



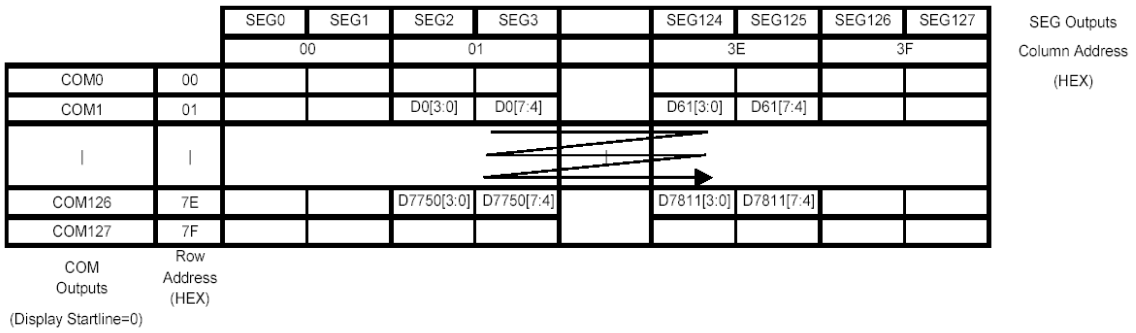

**GDDRAM Address Map - Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=1, Nibble Re-map A[1]=1, COM Re-map A[4]=0, Display Start line=00H (Data byte sequence: D0, D1, D2 … D8191)**



**GDDRAM Address Map - Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=1, Display Start Line=78H (Data byte sequence: D0, D1, D2 ... D8191)**



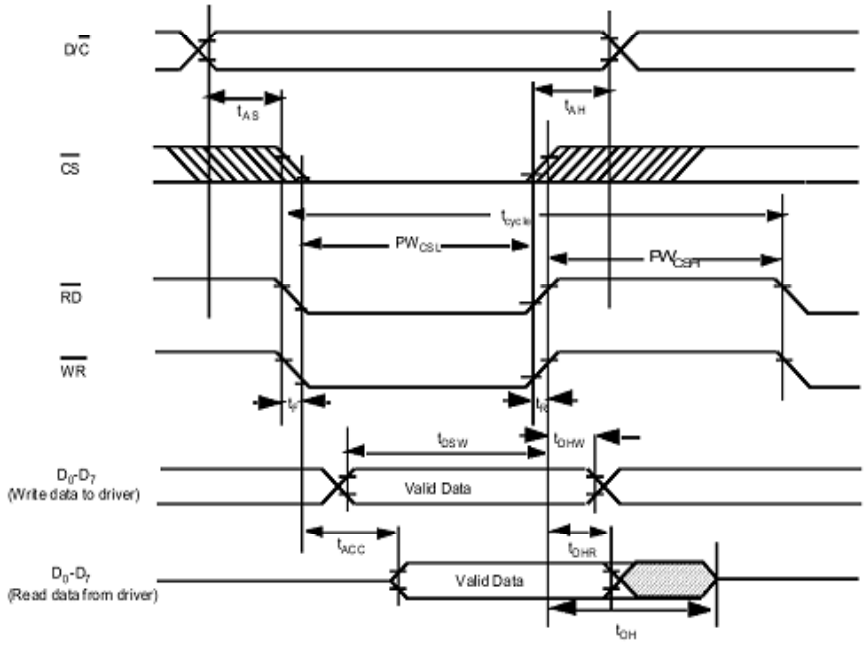

**GDDRAM Address Map - Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, Display Start Line=00H (Data byte sequence: D0, D1, D2 ... D7811), Column Start Address = 01H, Column End Address = 3EH, Row Start Address = 01H, Row End Address = 7EH**



## 7.5 INTERFACE TIMING CHART

**8080-Series MPU Parallel Interface Timing Characteristics ($V_{DD}$-$V_{SS}$ = 2.4 to 3.5V, $T_A$ = -30 to 85°C)**

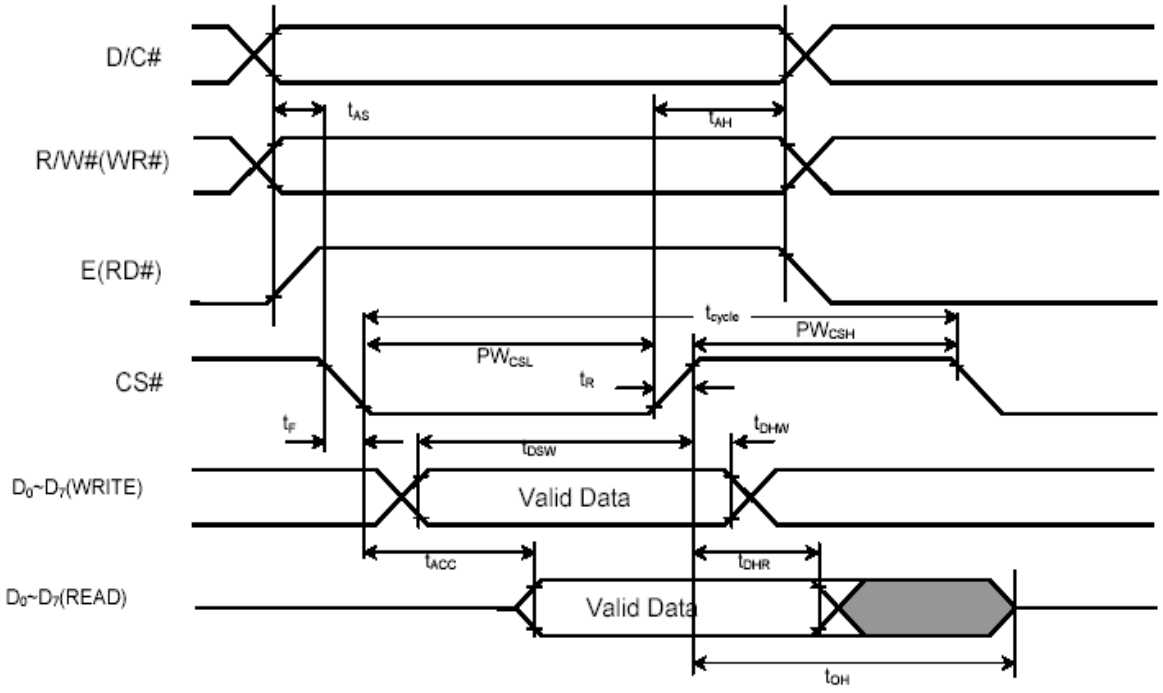
| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{cycle}$ | Clock Cycle Time | 300 | - | - | ns |
| $t_{AS}$ | Address Setup Time | 0 | - | - | ns |
| $t_{AH}$ | Address Hold Time | 0 | - | - | ns |
| $t_{DSW}$ | Write Data Setup Time | 40 | - | - | ns |
| $t_{DHW}$ | Write Data Hold Time | 15 | - | - | ns |
| $t_{DHR}$ | Read Data Hold Time | 20 | - | - | ns |
| $t_{OH}$ | Output Disable Time | - | - | 70 | ns |
| $t_{ACC}$ | Access Time | - | - | 140 | ns |
| $PW_{CSL}$ | Chip Select Low Pulse Width (read)<br>Chip Select Low Pulse Width (write) | 120<br>60 | - | - | ns |
| $PW_{CSH}$ | Chip Select High Pulse Width (read)<br>Chip Select High Pulse Width (write) | 60<br>60 | - | - | ns |
| $t_R$ | Rise Time | - | - | 15 | ns |
| $t_F$ | Fall Time | - | - | 15 | ns |




**8080-series MPU Parallel Interface Characteristics**

**6800-Series MPU Parallel Interface Timing Characteristics ($V_{DD}$ - $V_{SS}$ = 2.4 to 3.5V, $T_A$ = 25°C)**

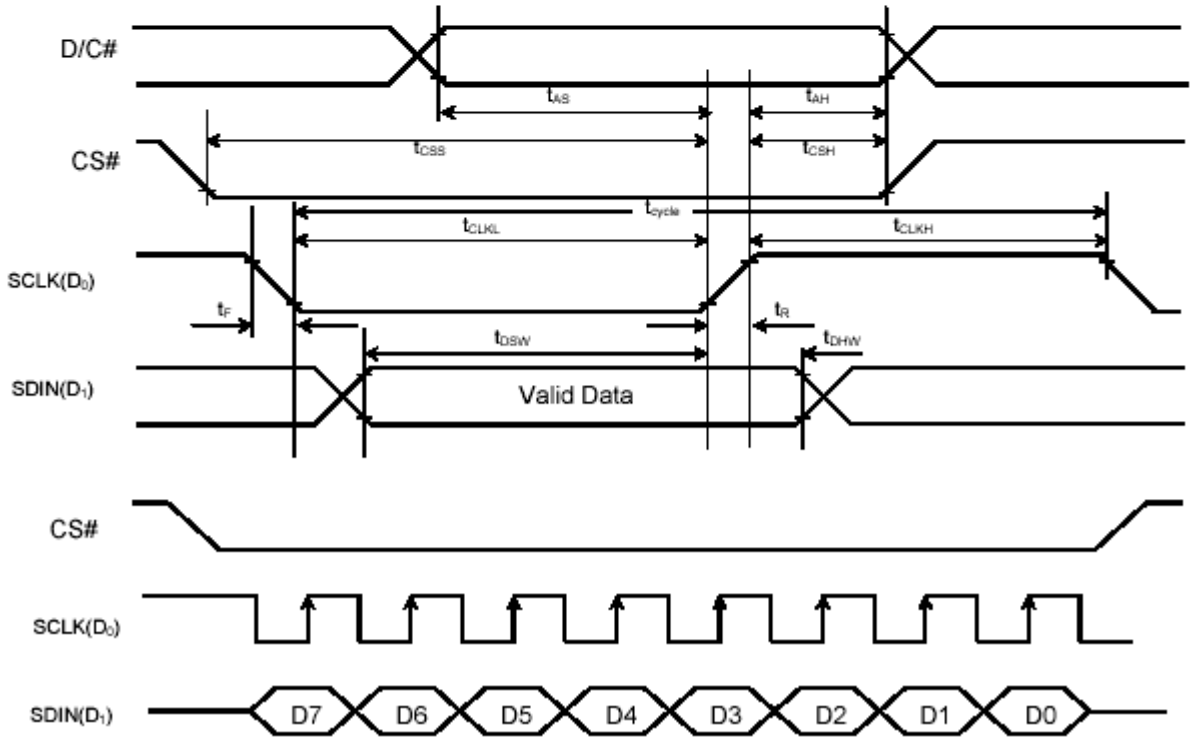
| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{cycle}$ | Clock Cycle Time | 300 | - | - | ns |
| $t_{AS}$ | Address Setup Time | 0 | - | - | ns |
| $t_{AH}$ | Address Hold Time | 0 | - | - | ns |
| $t_{DSW}$ | Write Data Setup Time | 40 | - | - | ns |
| $t_{DHW}$ | Write Data Hold Time | 15 | - | - | ns |
| $t_{DHR}$ | Read Data Hold Time | 20 | - | - | ns |
| $t_{OH}$ | Output Disable Time | - | - | 70 | ns |
| $t_{ACC}$ | Access Time | - | - | 140 | ns |
| $PW_{CSL}$ | Chip Select Low Pulse Width (read)<br>Chip Select Low Pulse Width (write) | 120<br>60 | - | - | ns |
| $PW_{CSH}$ | Chip Select High Pulse Width (read)<br>Chip Select High Pulse Width (write) | 60<br>60 | - | - | ns |
| $t_R$ | Rise Time | - | - | 15 | ns |
| $t_F$ | Fall Time | - | - | 15 | ns |




**6800-series MPU Parallel Interface Characteristics**

**Serial Interface Timing Characteristics ($V_{DD}$ - $V_{SS}$ = 2.4 to 3.5V, $T_A$ = 25°C)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{cycle}$ | Clock Cycle Time | 250 | - | - | ns |
| $t_{AS}$ | Address Setup Time | 150 | - | - | ns |
| $t_{AH}$ | Address Hold Time | 150 | - | - | ns |
| $t_{CSS}$ | Chip Select Setup Time | 120 | - | - | ns |
| $t_{CSH}$ | Chip Select Hold Time | 60 | - | - | ns |
| $t_{DSW}$ | Write Data Setup Time | 100 | - | - | ns |
| $t_{DHW}$ | Write Data Hold Time | 100 | - | - | ns |
| $t_{CLKL}$ | Clock Low Time | 100 | - | - | ns |
| $t_{CLKH}$ | Clock High Time | 100 | - | - | ns |
| $t_R$ | Rise Time | - | - | 15 | ns |
| $t_F$ | Fall Time | - | - | 15 | ns |



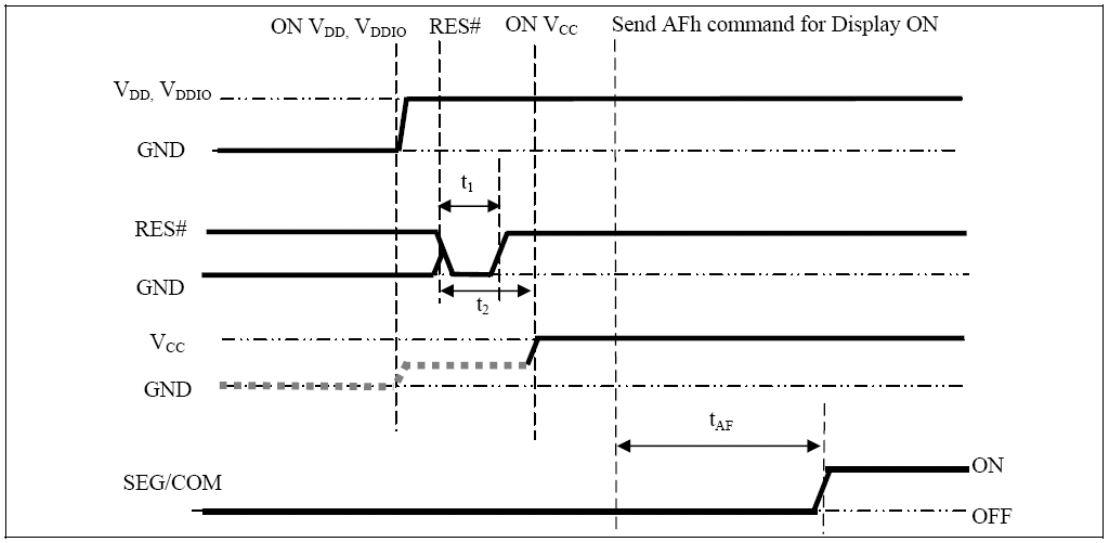

**Serial Interface Characteristics**

# 8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

## 8.1 POWER ON / OFF SEQUENCE

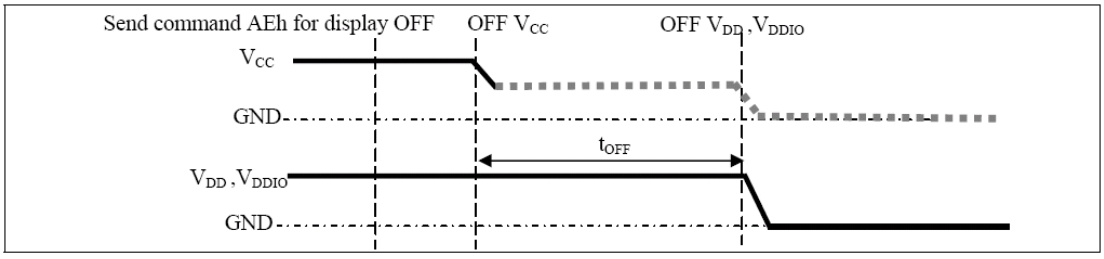
***Power ON sequence:***

1. Power ON $V_{DD}$, $V_{DDIO}$.
2. After $V_{DD}$, $V_{DDIO}$ become stable, set RES# pin LOW (logic low) for at least 3us($t_1$) and then HIGH (logic high).
3. After set RES# pin LOW (logic low ), wait for at least 3us($t_2$).Then Power ON $V_{CC}$.(1)
4. After $V_{CC}$ become stable, send command AFh for display ON. SEG/COM will be ON after 100ms($t_{AF}$).




***Power OFF sequence:***

1. Send command AEh for display OFF.
2. Power OFF $V_{CC}$. (1), (2)
3. Wait for $t_{OFF}$. Power OFF $V_{DD}$, $V_{DDIO}$. (where Minimum $t_{OFF}$=0ms, Typical $t_{OFF}$=100ms )

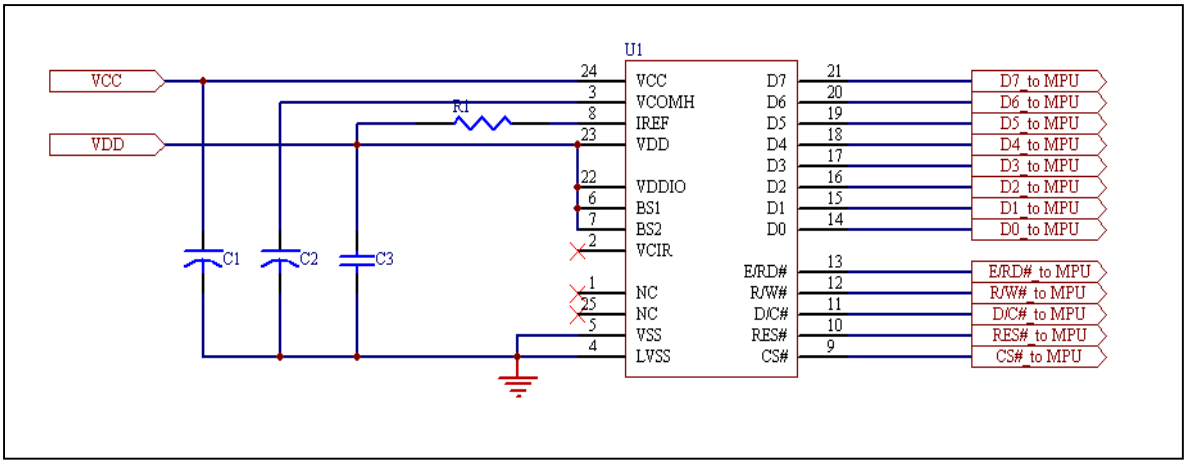



Note:

(1) Since an ESD protection circuit is connected between $V_{DD}$, $V_{DDIO}$ and $V_{CC}$, $V_{CC}$ becomes lower than $V_{DD}$ whenever $V_{DD}$, $V_{DDIO}$ is ON and $V_{CC}$ is OFF as shown in the dotted line of $V_{CC}$ in above figures.

(2) $V_{CC}$ should be disabled when it is OFF.

## 8.2 APPLICATION CIRCUIT




U1: 128x96 OLED module

C1: 4.7uF, tantalum type

C2: 1uF, tantalum type

C3: 0.1uF

R1: 200 K ohm, tolerance 1%

## 8.3 COMMAND TABLE

Refer to IC Spec.: SSD1329

## 9. RELIABILITY TEST CONDITIONS

| No. | Items | Specification | Quantity |
|---|---|---|---|
| 1 | High temp. (Non-operation) | 85°C, 240hrs | 5 |
| 2 | High temp. (Operation) | 70°C, 120hrs | 5 |
| 3 | Low temp. (Operation) | -40°C, 120hrs | 5 |
| 4 | High temp. / High humidity (Operation) | 65°C, 90%RH, 120hrs | 5 |
| 5 | Thermal shock (Non-operation) | -40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles | 5 |
| 6 | Vibration | Frequency : 5~50HZ, 0.5G<br>Scan rate : 1 oct/min<br>Time : 2 hrs/axis<br>Test axis : X, Y, Z | 1 Carton |
| 7 | Drop | Height: 120cm<br>Sequence : 1 angle、3 edges and 6 faces<br>Cycles: 1 | 1 Carton |
| 8 | ESD (Non-operation) | Air discharge model, ±8kV, 10 times | 5 |

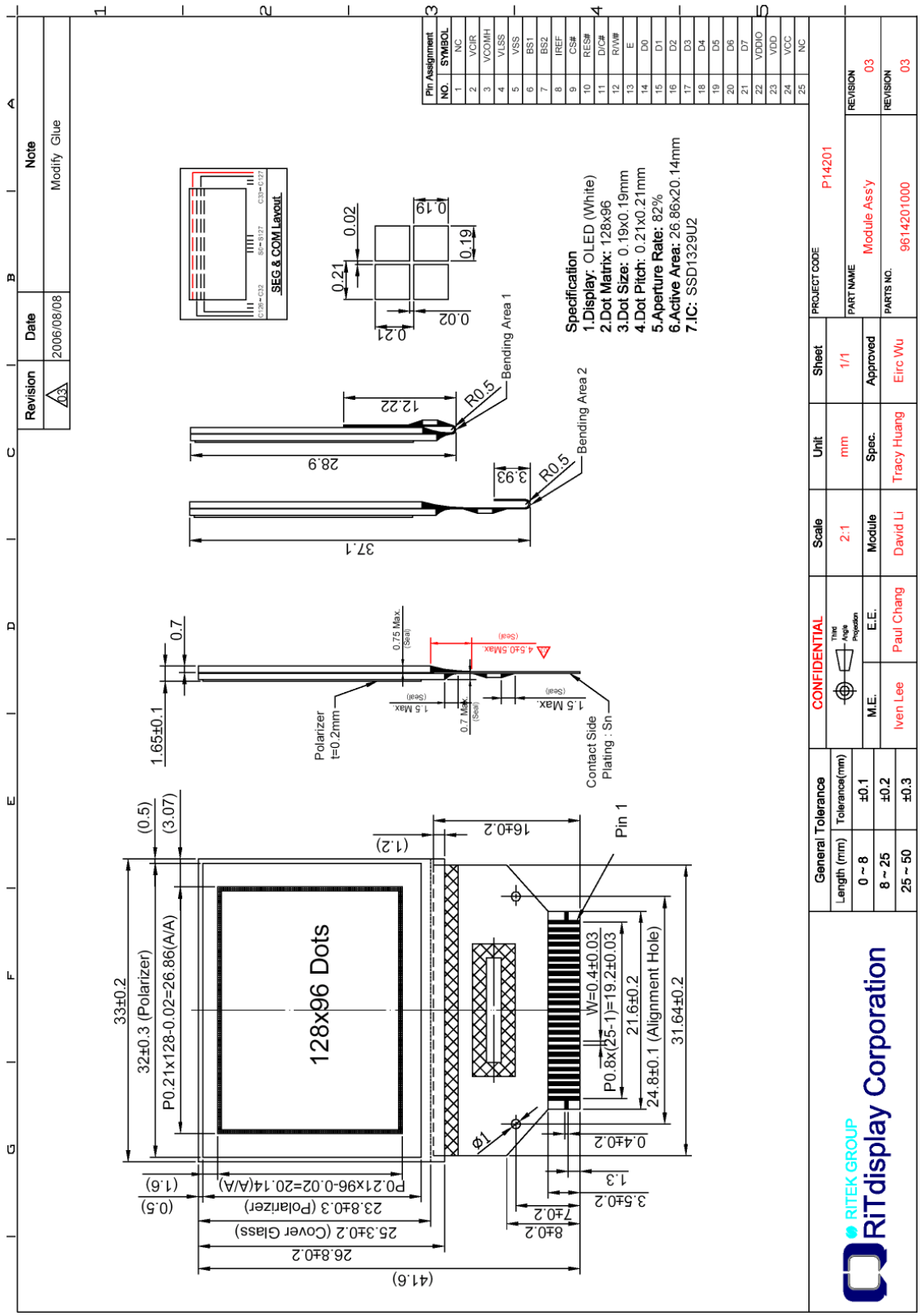
**Test and measurement conditions**

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

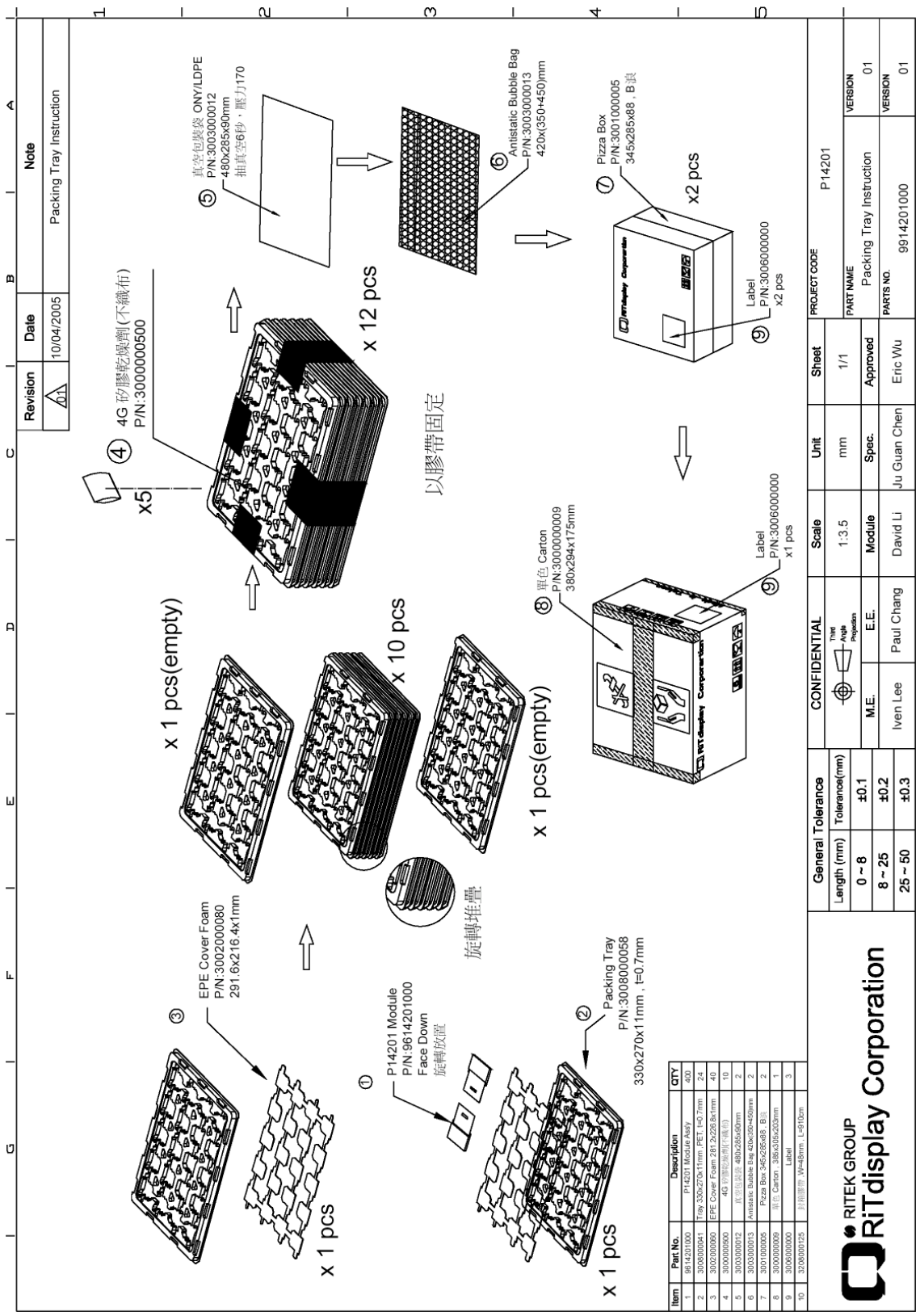
**Evaluation criteria**

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

# 10. EXTERNAL DIMENSION



# 11. PACKING SPECIFICATION




| Item | Part No. | Description | QTY |
|---|---|---|---|
| 1 | 9614201000 | P14201 Module Assy | 400 |
| 2 | 3008000041 | Tray 330x270x11mm, PET, t=0.7mm | 24 |
| 3 | 3002000080 | EPE Cover Foam 291.6x226.8x1mm | 40 |
| 4 | 3000000500 | 4G 矽膠乾燥劑(不織布) | 10 |
| 5 | 3003000012 | 真空包裝袋 480x285x90mm | 2 |
| 6 | 3003000013 | Antistatic Bubble Bag 420x(350+450)mm | 2 |
| 7 | 3001000005 | Pizza Box 345x285x88 B浪 | 2 |
| 8 | 3000000009 | 單色 Carton 385x295x203mm | 1 |
| 9 | 3006000000 | Label | 3 |
| 10 | 3009000125 | 封箱膠帶 W=48mm, L=91.5m | |

# 12. APPENDIXES

## APPENDIX 1: DEFINITIONS

### A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

### B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

### C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

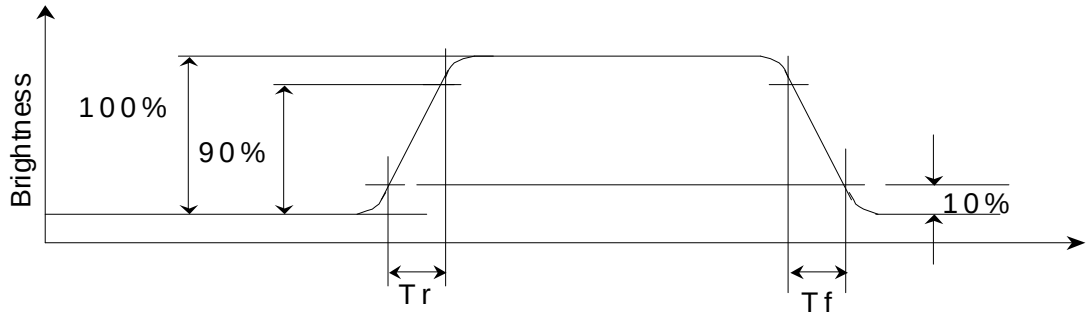



**Figure 2 Response time**

## D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

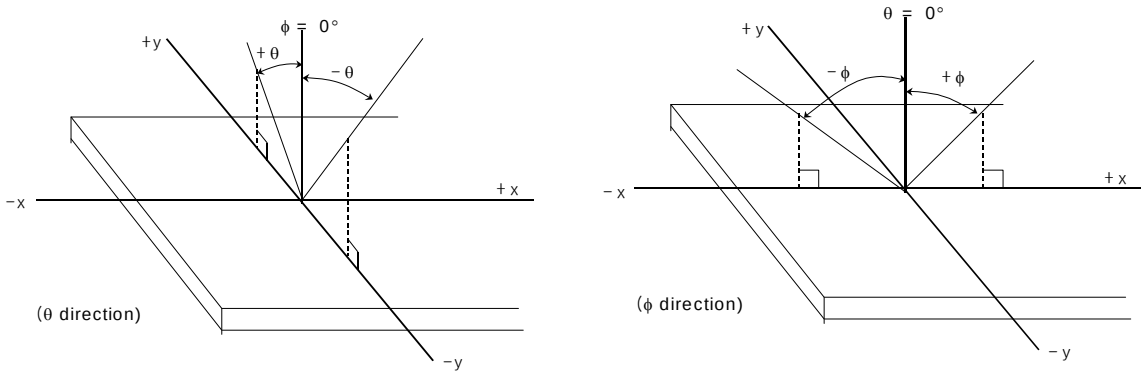
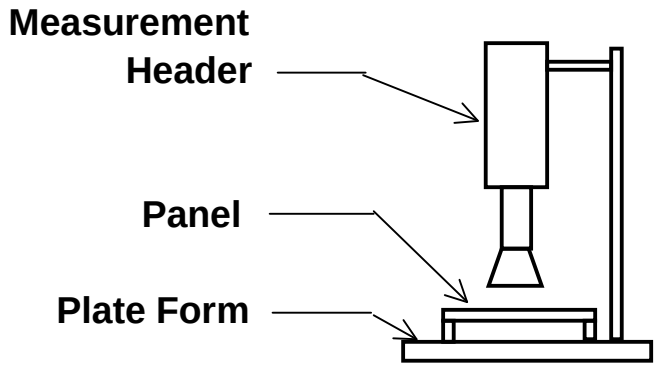



**Figure 3 Viewing angle**

## APPENDIX 2: MEASUREMENT APPARATUS

### A. LUMINANCE/COLOR COORDINATE

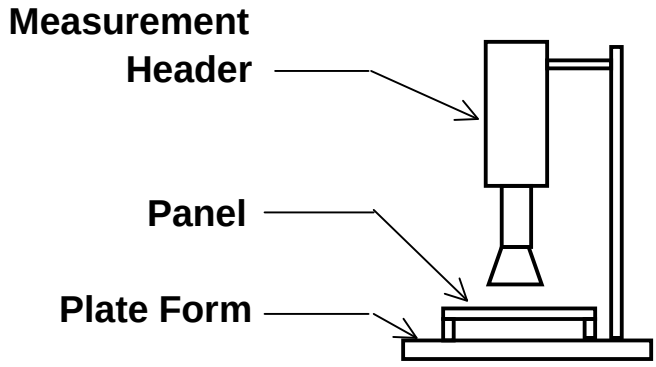
PHOTO RESEARCH PR-705, MINOLTA CS-100




**PR-705 /
MINOLTA CS-100
Color Analyzer**

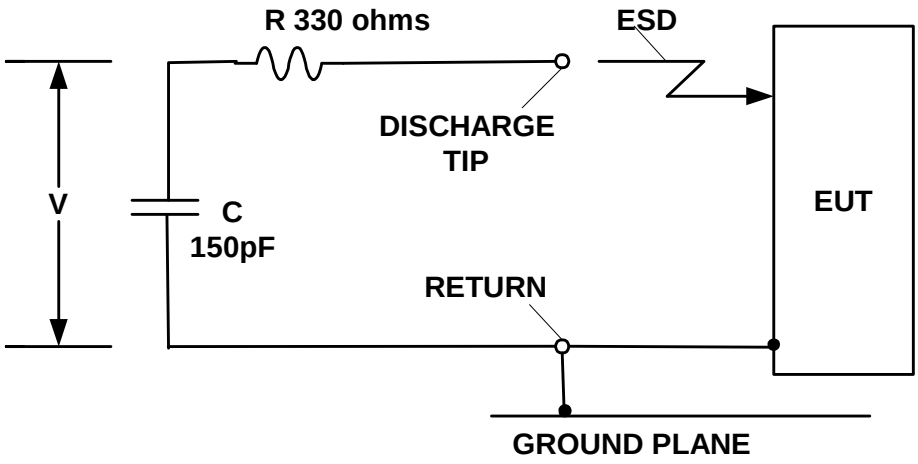
### B. CONTRAST / RESPONSE TIME / VIEW ANGLE

WESTAR CORPORATION FPM-510




**Westar FPM-510
Display Contrast /
Response time /
View angle Analyzer**

## C. ESD ON AIR DISCHARGE MODE



## APPENDIX 3: PRECAUTIONS

### A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.