Datasheet

Single Mode Bluetooth Low Energy (BLE) Module

Part # BL600-SA, BL600-SC, BL600-ST, BL620-SA, BL620-SC, BL620-ST

Version 4.1

REVISION HISTORY

Ver.	Date	Notes	Contributor(s)	Approver
1.0	16 Apr 13	Initial Release		Jonathan Kaye
1.1	5 July13	Added: ▪ To Table 1, *smart*BASIC runtime engine FW upgrade via UART. ▪ To Table 1, *smart*BASIC application download via OTA. ▪ Section OTA (Over-the-Air) smartBASIC Application Download Updated: ▪ Table 1 – make it clear number of SPI (x1), I2C(x1) interfaces and ADC channels. ▪ Table 2 – (pin list), footnote mentions SIO_7 has Internal Pull down (default in FW). ▪ Clocks section – corrected 32.768 crystal accuracy to +/-20ppm. Added 16MHz crystal accuracy (+/-10ppm). ▪ Circuit section – circuit HW integration suggestion), on SIO_7 pin and Over the Air *smart*BASIC application download feature. ▪ Figure 14: BL600 Mechanical drawings – BL600 Mechanical drawing to add measurements of the half-moon shaped positioning holes.		Jonathan Kaye
1.2	25 Oct 2013	Updated Recommended Operating Parameters notes to reflect 2.7 **ms** rather than 2.7 **µs**.		Jonathan Kaye
1.3	12 Dec 2013	Added baking schedule information.		Jonathan Kaye
1.4	20 Dec 2013	Added: ADC (AIN) input impedance into Table 6. AIN (ADC) impedance and external voltage divider setup into the Circuit.section.		Jonathan Kaye
1.5	10 Jan 2014	Updated TOC with correct page numbers. Added noted regarding smartBASIC firmware's lack of support for GPIO high drive state.		Jonathan Kaye
1.6	06 Feb 2014	Updated Bluetooth SIG Qualification section.		Jonathan Kaye
1.7	18 Feb 2014	Updated Operating temperature range		Jonathan Kaye
1.8	04 April 2014	Updated or added the following for the BL600-Sx-04: ▪ Lower power consumption figures (standby doze, deep sleep) and lower peripheral (UART, SPI, I2C, ADC) block currents for the BL600-Sx-04 (new Nordic silicon). ▪ Improved UART with deep RX buffer (6 bytes instead of 2 bytes). ▪ Increased the Absolute Max rating on the VCC pin from 3.6V to 3.9V. ▪ Added a note for External 12K resistor to GND on SWDCLK pin NOT required on BL600-Sx-04. Added the following for all BL600 module revisions to align with FW features: ▪ Section on PWM output and FREQ output signals. ▪ Note on GPIO high drive strength (5 mA). ▪ Note regarding internal DCDC convertor turned OFF on recommendation from chipset supplier until further notice. Updated Peak current consumption figures with DCDC turned OFF (with internal LDO ON).		Jonathan Kaye

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Ver.	Date	Notes	Contributor(s)	Approver
		▪ Added in the pin list the newly FW (1.5.66.0, April 2014) enabled internal pull-ups to prevent inputs from floating and to help with the issue of Standby Doze current drifting with time. ▪ Note on added coming out from Deep Sleep to Standby Doze through GPIO signal through the reset vector. ▪ New function to detect GPIO change with no current consumption, so UART closed but still able to detect for incoming data and be woken up so that the UART can be re-opened at the expense of losing that first character. ▪ Note that SIO_7 and AutoRUN (SIO_28) are **not both high** (externally), otherwise cannot load *smart*BASIC application script. Note on each module GND pin that must be connected to host PCB GND.		
1.9	11 June 2014	Updated BT SIG information		Jonathan Kaye
2.0	2 July 2014	Important information on pin 22 (reset) and pin 23 (SWDCLK).		Jonathan Kaye
2.1	14 July 2014	Updated SIO VIL max value in table 5		Jonathan Kaye
2.2	17 Oct 2014 24 Oct 2014	Added BL620 module information Added QD ID and note to section 14		Jonathan Kaye
2.3	30 April 2015	Updated Antenna information in External Antenna Integration with BL600-SC and BL600-ST		Jonathan Kaye
2.4	01 June 2015	Updated the BT SIG Qualification section.		Jonathan Kaye
2.5	10 Sept 2015	Added BL600-SA-32 part number to Ordering Info section.		Jonathan Kaye
3.0	19 April 2015	New template. Updated Land Pattern.		Jonathan Kaye
3.1	13 May 2016	Added Appendix 1: Locating the BL600-SX Revision Number		Jonathan Kaye
3.2	09 Aug 2016	Changed from *Hardware Integration Guide* to *Datasheet*		Sue White
3.3	08 Sept 2016	Updated Declaration of Conformity		Sue White
3.4	14 Nov 2016	Fixed Table 5 formatting and parameters		Sue White
3.5	10 Jan 2016	Minor textual/grammatical fixes		Sue White
3.6	14 Apr 2017	Added Laird part numbers for certification antennas		Jonathan Kaye
3.7	30 May 2017	Updated DoC for new RED standards		Tom Smith
3.8	07 Dec 2017	Added Taiwan as the Country of Origin		Jonathan Kaye
3.9	13 Feb 2019	Updated logos, URLs, template styles		Sue White
4.0	10 Dec 2020	Updated all regulatory information	Ryan Urness	Jonathan Kaye
4.1	14 Jan 2021	Moved all regulatory information to a separate document	Sue White	Jonathan Kaye

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1 Overview and Key Features

This Datasheet also applies to the Laird BL620. The BL620 uses the same module hardware as the BL600 but it has a new firmware that supports Central mode connectivity.

Note that the BL620 module supports a JTAG upgrade but has no capability to upgrade via UART.

Every BL600 Series module is designed to enable OEMs to add single-mode Bluetooth Low Energy (BLE) to small, portable, power-conscious devices. The BL600 modules are enabled with Laird's *smart* BASIC, an event-driven programming language that enables OEMs to make their BLE product development quicker and simpler, significantly reducing time to market. *smart* BASIC enables customers to develop a complete embedded application inside the compact BL600 hardware, connecting to a wide array of external sensors via its I2C, SPI, UART, ADC or GPIO interfaces.

Based on the world-leading Nordic Semiconductor nRF51822 chipset, the BL600 modules provide ultra-low power consumption with outstanding wireless range via 4 dBm of transmit power. A broad range of BLE profiles including Temperature and Heart Rate are available and *smart* BASIC provides the ideal mechanism to support any BLE profile development of your choice. This document should be read in conjunction with the *smart* BASIC user manual.

1.1 Features and Benefits

- Bluetooth v4.0 - Single Mode
- External or Internal Antennas
- smartBASIC programming language
- Full Bluetooth EPL
- Compact Footprint
- Programmable TX power 4 dBm to -20 dBm
- TX whisper mode (-30 dBm, -55 dBm)
- RX sensitivity: -91 dBm
- Ultra-low power consumption
- TX: 11.6 mA peak (at +4 dBm) (refer to Note1 in Power Consumption section)
- RX: 8.8 mA peak (refer to Note1 in Power Consumption section)
- Standby Doze: 2.6 uA typical
- Deep Sleep: 0.6 uA (refer to Note4 in Power Consumption section)
- UART, GPIO, ADC, PWM, FREQ output, TIMERS, I2C, and SPI interfaces
- Fast Time to Market
- FCC, EU, ISED, Taiwan (-SA version only) and Japan certified; other regulatory certifications on request
- No external components required

1.2 Application Areas

- Medical devices
- Wellness devices
- iOS "appcessories"
- Fitness sensors
- Location Awareness
- Home automation

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2 SPECIFICATIONS

2.1 Specification Summary

Table 1: Specifications

Categories	Feature	Implementation
Wireless Specification	Bluetooth®	V4.0 – Single Mode Slave (from base FW v1.1.50.0 onwards)
	Frequency	2.402 - 2.480 GHz
	Maximum Transmit Power Setting	4 dBm Conducted BL600-SA 4 dBm Conducted BL600-SC ~2.5 dBm Conducted BL600-ST (RSMA connector on dev board)
	Minimum Transmit Power Setting	-20 dBm (in 4 dB steps) with *smart*BASIC command -16 dBm -12 dBm - 8 dBm - 4 dBm 0 dBm
	TX Whisper Mode 1 Transmit Power	-30 dBm (min) with *smart*BASIC command
	TX Whisper Mode 2 Transmit Power	-55 dBm (min) with *smart*BASIC command
	Receive Sensitivity (0.1% BER)	-91 dBm typical
	Link Budget	95 dB (@ 1 Mbps)
	Range	Up to 100 m in free space
	TX Whisper Modes	Range reduction feature with TX Whisper modes with *smart*BASIC command.
	Range (TX Whisper Mode 2)	<~30 cm
	Raw Data Rates	1 Mbps (over the air)
Host Interface and Peripherals	TOTAL	28 x Multifunction I/O lines
	UART	TX, RX, CTS, RTS DCD, RI, DTR, DSR, CTS, RTS (Note 1) Default 9600, n,8, 1 From 1,200 to 115,200bps BL600-Sx-04 onwards has improved UART with Deep RX buffer (6 bytes instead 2 bytes).
	GPIO	Up to 28, with configurable: I/O direction, O/P drive strength (standard 0.5 mA or high 5 mA), Pull-up /pull-down
	ADC	Six 10-bit channels (including ADC reference) 10 bit resolution 1.2 V internal reference 1/1, 2/3, 1/3 pre-scaling
	PWM or FREQ output	Output a PWM or FREQ output on up to two GPIO output pins. PWM output duty cycle 0%-100%

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Categories	Feature	Implementation
		PWM output frequency: Up to 500 kHz (Note 7) FREQ output frequency: 0 MHz-4 MHz (50% duty cycle)
	I2C	One I2C interface (up to 400 kbps) (Note 2)
	SPI	One SPI Master interface (up to 4 Mbps) (Note 3)
Profiles	Services supported (Note 4) (FW v1.1.50.0)	▪ Heart Rate Service ▪ Health Thermometer Service ▪ Battery Alert Service ▪ Blood Pressure Service ▪ Device Information Service ▪ Immediate Alert Service ▪ IOPT (Interoperability) ▪ Link Loss Service ▪ Transmit Power Service Custom services (from base FW v1.2.54.0 onwards)
FW Upgrade	*smart* BASIC runtime engine FW upgrade (Note 5)	Via JTAG. Using the supplied J-link programmer. Via UART. **Note:** The BL620 supports a JTAG upgrade but has no capability to upgrade via UART.
Programmability	smart BASIC	On-board programming language similar to BASIC.
	smart BASIC application download	(1) Via UART. (2) Via Over the Air (if SIO_7 pin is pulled high externally).
Control Protocols	Any	User defined via smartBASIC
Operating Modes	Self-contained Run mode	Selected by nAutoRun pin status: LOW (0V). Then runs $autorun$ (*smart*BASIC application script) if it exists.
	Interactive / development mode	HIGH (VCC). Then runs via at+run (and “file name” of *smart*BASIC application script).
Supply Voltage	Supply (VCC)	2.1 – 3.6 V – internal DCDC converter (Note 5) 1.8 – 3.6 V – internal LDO DCDC switched on if VCC>2.1V at power-up.
Power Consumption	Active Modes Peak Current (for Max TX PWR 4 dBm)	Advertising or Connected mode: 11.6 mA peak TX, 8.9 mA peak RX
	Active Modes Peak Current for TX Whisper mode2 PWR -55 dBm)	Advertising or Connected mode: 5 mA peak TX, 8.5 mA peak RX
	Active Modes Average Current	Depends on many factors, see *Power Consumption*.
	Ultra-Low Power Modes	Standby Doze: 2.6 uA typical (Note 6) Deep Sleep: 600 nA (Note 6)
Antenna Options	Internal	Ceramic chip monopole antenna – on-board BL600-SA
	External – Option 1	Dipole antenna (with IPEX connector) Dipole PCB antenna (with IPEX connector)

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Categories	Feature	Implementation
		Connection via IPEX MH4 – BL600-SC
	External – Option 2	Dipole antenna (with RSMA connector) Connection via Trace Pads – BL600-ST
Physical	Dimensions	19 mm x 12.5 mm x 3 mm
	Weight	<1 gram
Environmental	Operating	-25 ˚C to +75 ˚C (VCC 1.8V-3.6V) -40 ˚C to +85 ˚C (VCC 3.3V+/-10%)
	Storage	-40 ˚C to +85 ˚C
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	1-Year Warranty
Development Tools	Development Kit	Development Kit DVK-BL600-Sx and Free Software Tools
Approvals	Bluetooth®	End Product Listing (EPL)
	FCC / ISED / EU / MIC	All BL600 Series
Country of Origin (CoO)	Taiwan	

Note 1: DSR, DTR, RI, and DCD can be implemented in the *smart* BASIC application.

Note 2: With I2C interface selected, pull-up resistors on I2C SDA and I2C SCL MUST be connected externally as per I2C standard.

Note 3: SPI interface (master) consists of SPI MOSI, SPI MISO and SPI CLK. SPI CS is created by customer using any spare SIO pin within their *smart*BASIC application script allowing multi-dropping.

Note 4: BL600 module comes loaded with *smart* BASIC runtime engine FW, but does not come loaded with any *smart* BASIC application script (as that is dependent on customer end application or use). Laird provides many sample *smart* BASIC application scripts covering the services listed. Additional BLE services being added every quarter.

Note 5: *smart* BASIC runtime engine firmware v1.2.54.0 (Jun2013) and subsequent versions, the internal DCDC convertor was switched off on recommendation from the chipset provider until future notice.

Note 6: Measured with BL600-Sx-04.
Deep Sleep current for BL600-Sx-02 and BL600-Sx-03 ~1000nA (typical).
Standby Doze current for BL600-Sx-02 and BL600-Sx-03 Standby Doze current 3.5uA (typical).

Note 7: PWM output signal has a frequency and duty cycle property. PWM output is generated using 32-bit hardware timers. The timers are clocked by a 1MHz (1uS period) clock source. Trade-off PWM output frequency with resolution. For example:
PWM output frequency of 500kHz (2uS) results in resolution of 1:2
PWM output frequency of 100kHz (10uS) results in resolution of 1:10
PWM output frequency of 10kHz (100uS) results in resolution of 1:100
PWM output frequency of 1kHz(1000uS) results in resolution of 1:1000
Refer to the *smart*BASIC user guide for details.

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3 HARDWARE SPECIFICATIONS

3.1 Block Diagram and Pin-out

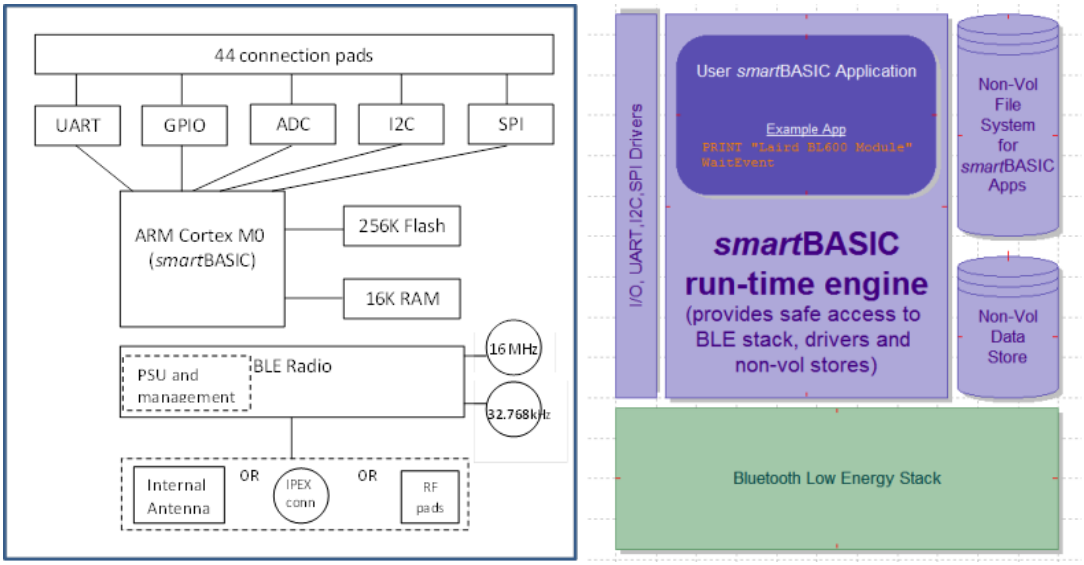

Figure 1: Functional HW and SW block Diagram for BL600 series BLE smartBASIC module

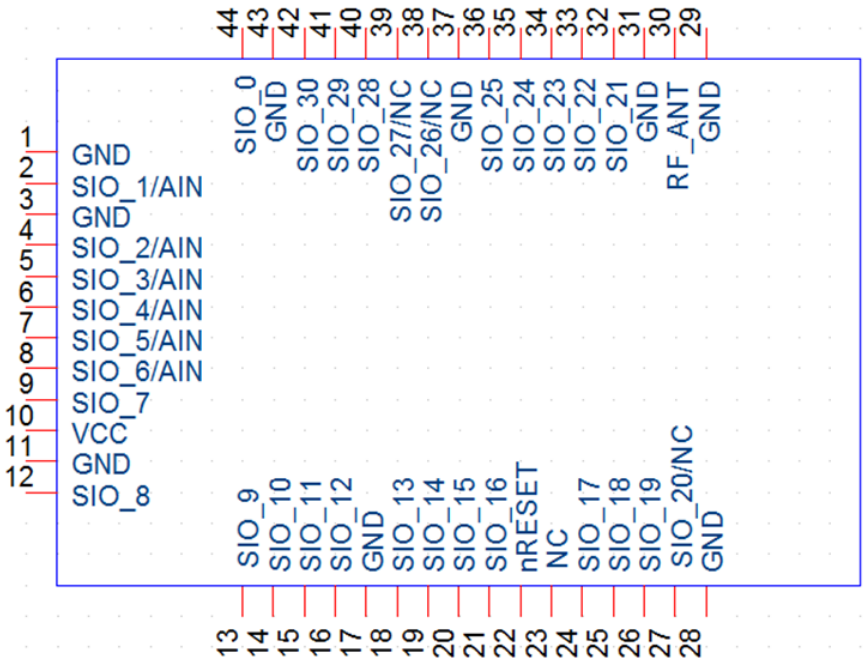

Figure 2: BL600-Sx module pin-out (top view)

Note: Pin 30 (RF_ANT) is for BL600-ST only. On the BL600-SA and BL600-SC, pin 30 is NC.

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3.2 Pin Definitions

Table 2: Pin definitions

Pin #	Pin Name	Default Function	Alt. Funct.	Default Direction Note14	Pull-up / Pull-down Note14	Notes	Comment
1	GND	-	-	-	-	-	-
2	SIO_1	DIO	AIN	IN	PULL-UP	1,2,3,4,5	8,9,10-bit resolution. Voltage scaling 1/1, 2/3, 1/3.
3	GND	-	-	-	-	-	-
4	SIO_2	DIO	AIN	IN	PULL-UP	1,2,3,4,5	8,9,10-bit resolution. Voltage scaling 1/1, 2/3, 1/3.
5	SIO_3	DIO	AIN	IN	PULL-UP	1,2,3,4,5	8,9,10-bit resolution, Voltage scaling 1/1, 2/3, 1/3.
6	SIO_4	DIO	AIN	IN	PULL-UP	1,2,3,4,5	8,9,10-bit resolution, Voltage scaling 1/1, 2/3, 1/3.
7	SIO_5	DIO	AIN	IN	PULL-UP	1,2,3,4,5	8,9,10-bit resolution, Voltage scaling 1/1, 2/3, 1/3.
8	SIO_6	DIO	AIN	IN	PULL-UP	1,2,3,4,5	8,9,10-bit resolution, Voltage scaling 1/1, 2/3, 1/3
9	SIO_7	DIO		IN	PULL-DOWN	1,2, 12, 13	Internal Pull down (default)
10	VCC	-	-	-	-	-	-
11	GND						
12	SIO_8	DIO	I2C SDA	IN	PULL-UP	1,2,4,5,6	I2COPEN() in *smart*BASIC selects I2C function
13	SIO_9	DIO	I2C SCL	IN	PULL-UP	1,2,4,5,6	
14	SIO_10	DIO	SPI MOSI	IN	PULL-UP	1,2,4,5,6	SPIOPEN() in *smart*BASIC selects SPI function, MOSI and CLK will be outputs when in SPI master mode. See Note 11.
15	SIO_11	DIO	SPI MISO	IN	PULL-UP	1,2,4,5,6	
16	SIO_12	DIO	SPI CLK	IN	PULL-UP	1,2,4,5,6	
17	GND	-	-	-	-	-	-
18	SIO_13	DIO		IN	PULL-UP	1,2	
19	SIO_14	DIO		IN	PULL-UP	1,2	
20	SIO_15	DIO		IN	PULL-UP	1,2	Laird Devkit : Buzzer output
21	SIO_16	DIO		IN	PULL-UP	1,2	Laird Devkit : Button 0 input
22	nRESET			IN		9,10	System Reset (Active low)
23	NC					9	DO NOT CONNECT
24	SIO_17	DIO		IN	PULL-UP	1,2	Laird Devkit : Button 1 input
25	SIO_18	DIO		IN	PULL-UP	1,2	Laird Devkit : LED 0
26	SIO_19	DIO		IN	PULL-UP	1,2	Laird Devkit : LED 1
27	SIO_20	NC					Reserved for future use
28	GND						
29	GND						
30	RF_ANT					8	Used on BL600-ST only.

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Pin #	Pin Name	Default Function	Alt. Funct.	Default Direction Note14	Pull-up / Pull-down Note14	Notes	Comment
31	GND						
32	SIO_21	DIO	UART TX	OUT	Set high in FW	1,2,4,6,7	UARTCLOSE() selects DIO functionality and UARTOPEN() selects uart comms behaviour
33	SIO_22	DIO	UART RX	IN	PULL-UP	1,2,4,6,7	
34	SIO_23	DIO	UART RTS	OUT	Set low in FW	1,2,4,6,7	
35	SIO_24	DIO	UART CTS	IN	PULL-DOWN	1,2,4,6,7	
36	SIO_25	DIO		IN	NONE	1,2	Laird Devkit : UART_DTR via CON12
37	GND						
38	SIO_26	NC					Reserved for future use. Do NOT connect.
39	SIO_27	NC					
40	SIO_28	nAutoRUN		IN	NONE	IN Only	Laird Devkit: UART_DSR via CON12
41	SIO_29	DIO		IN	NONE	1,2	Laird Devkit : UART_DCD via CON12
42	SIO_30	DIO		IN	NONE	1,2	Laird Devkit : UART_RI via CON12
43	GND						
44	SIO_0	DIO		IN	PULL-UP	1,2	

Note 1: Secondary function is selectable in *smart*BASIC application.

Note 2: DIO = Digital Input or Output. I/O voltage level tracks VCC.

Note 3: AIN = Analog Input

Note 4: DIO or AIN functionality is selected using the GpioSetFunc() function in *smart*BASIC.

Note 5: AIN configuration selected using GpioSetFunc() function.

Note 6: I2C, UART, SPI controlled by xxxOPEN() functions in *smart* BASIC.

Note 7: SIO_21 to SIO_24 are DIO by default when $autorun$ app runs on power up.

Note 8: RF_ANT pin (pin30) is on theBL600-ST module only. Customer MUST use 50-Ohm trace from RF_ANT pin to RSMA RF connector on host PCB. More details on 50-Ohm trace design refer to section ***50-OhmsRF Trace on Host PCB for BL600-ST***.

Note 9: Hidden JTAG (2-wire interface), pin22 (SWDIO) and pin23 (SWDCLK). Used for upgrading *smart*BASIC runtime engine FW only with Laird supplied J-link programmer. Using this hidden JTAG requires 12K resistor to GND (on pin23 SWDCLK) for BL600-Sx-02 and BL600-Sx-03 on customers host PCB and header connector Samtech FTSH-105-01-L-DV, refer to section *Miscellaneous (hidden JTAG)* for details. 12K resistor is NOT required on customers host PCB when using the BL600-Sx-04.

Note 10: Pull the nRESET pin (pin 22) low for minimum 100 mS in order for the BL600 to reset.

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For BL600-Sx-02 or BL600-Sx-03: To ensure nReset functions properly, you MUST place a 12K resistor to GND on BL600 pin 23 (NC/SWDCLK) on your host board.

For BL600-Sx-04: Do not fit a resistor to GND on BL600 pin 23 (NC/SWDCLK).

Note11: SPI CS is created by customer using any spare SIO pin within their *smart*BASIC application script allowing multi-dropping.

Note12: SIO_7 pin has to be pulled high externally to enable OTA (over the Air) *smart*BASIC application download. Refer to the latest FW release documentation for details.

Note13: User must ensure that SIO_7 and AutoRUN(SIO_28) are NOT BOTH HIGH (externally), otherwise in that state the UART is bridged to Virtual Serial Port service and so the BL600 module will not respond to AT commands and therefore cannot load *smart*BASIC application scripts (applies to all versions of the *smart* BASIC runtime engine firmware.

Note14: *smart* BASIC runtime engine FW 1.5.66.0(Apr2014) has DIO (Default Function) INPUT pins, have by default PULL-UP enabled. This was done to avoid floating inputs (which can also cause current consumption in low power modes (e.g. StandbyDoze) to drift with time. In any case customer can disable the PUL-UP through their *smart* BASIC application. ALL *smart* BASIC runtime engine FW versions before 1.5.66.0(Apr2014), the INPUT DIO pins have NO pull-up or pull-down enabled and would require the customer to enable pull-up through *smart* BASIC application script.

All the SIO pins (with a default function of DIO are inputs – apart from SIO_21 and SIO_23, which are outputs):

- **SIO_21** (alternative function UART_TX) is an output, set High (in FW).
- **SIO_23** (alternative function UART_RTS) is an output, set Low (in FW).
- **SIO_22** (alternative function UART_RX) is an input, set with internal pull-up (in FW).
- **SIO_24** (alternative function UART_CTS) is an input, set with internal pull-down (in FW).
- **SIO_7** is an input set with internal pull-down (in FW). It is used for over the air downloading of *smart*BASIC applications. Refer to the latest FW release documentation for details.

The BL600 module is delivered with the integrated *smart* BASIC runtime engine FW loaded (but no onboard *smart*BASIC application script). Because of this, it starts up in AT command mode by default.

At reset, all SIO lines are configured as the defaults shown above.

SIO lines can be configured through the *smart* BASIC application script to be either inputs or outputs with pull-ups or pull-downs. When an alternative SIO function is selected (such as I2C or SPI), the firmware does not allow the setup of internal pull-up/pull-down. Therefore, when I2C interface is selected, pull-up resistors on I2C SDA and I2C SCL **MUST** be connected externally as per I2C standard.

UART_RX, UART_TX, UART_CTS are 3.3 V level logic (if VCC is 3.3 V, i.e. SIO pin I/O levels track VCC). For example, when RX and TX are idle, they sit at 3.3 V (if VCC is 3.3 V). Conversely, handshaking pins CTS and RTS at 0 V are treated as assertions.

Pin 40 (nAutoRUN) is an input, with active low logic. In the development kit (DVK-BL600-sx) it is connected so that the state is driven by the host's DTR output line. The nAutoRUN pin must be externally held high or low to select between the following two BL600 operating modes:

- Self-contained Run mode (nAutoRUN pin held at 0 V).
- Interactive / development mode (nAutoRUN pin held at VCC).

*smart*BASIC runtime engine firmware checks for the status of nAutoRUN during power-up or reset. If it is low and if there is a *smart*BASIC application script named **$autorun$**, then the *smart*BASIC runtime engine FW executes the application script automatically; hence the name *Self-contained Run Mode*.

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3.3 Electrical Specifications

3.3.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below; exceeding these values causes permanent damage.

Table 3: Maximum Current Ratings

Parameter	Minimum	Maximum	Unit
Voltage at VCC pin	-0.3	+3.6 (Note 1)	V
Voltage at GND pin		0	V
Voltage at SIO pin	-0.3	VCC+0.3	V
Storage temperature	-40	+85	ºC

Note 1: Absolute Max Rating for VCC pin (max) is 3.6V for BL600-Sx-02 and BL600-Sx-03.
Absolute Max Rating for VCC pin (max) is 3.9V for BL600-Sx-04.

3.3.2 Recommended Operating Parameters

Table 4: Power Supply Operating Parameters

Parameter	Minimum	Typical	Maximum	Unit
VCC (with internal LDO)[1]	1.8	3	3.6	V
VCC (with internal DCDC enabled)[1]	2.1	3	3.6	V
VCC Maximum ripple or noise[2]			10	mV
VCC rise time (0 to 1.8V)[3]			60	mS
Operating Temperature Range				
3.3V +/- 10%	-40	-	+85	ºC
(contact Laird with any queries) 1.8V	-25	-	+75	ºC

Note 1: Internal DCDC is used if VCC >2.1 V on power-up; otherwise internal LDO is used. 4.7 uF internal to module on VCC. *smart*BASIC runtime engine firmware v1.2.54.0(Jun2013) and subsequent versions, the internal DCDC convertor was switched off on recommendation from the chipset provider until future notice.

Note 2: The maximum VCC ripple or noise (at any frequency) that does not disturb the radio.

Note 3: The on-board power-on reset circuitry may not work for rise times outside the noted interval.
Time reset is active from VCC reaches 1.7 V with 50 mS rise time is 29 mS typical.
Time reset is active from VCC reaches 1.7 V with 1 uS rise time is 2.7 mS typical.

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Table 5: Signal Levels for Interface, SIO

Parameter	Minimum	Typical	Maximum	Unit
VIH Input high voltage	0.7 VCC		VCC	V
VIL Input low voltage	VSS		0.3 VCC	V
VOH Output high voltage				
(std. drive, 0.5mA)	VCC-0.3		VCC	V
(high-drive, 5mA) (Note 1)	VCC-0.3		VCC	V
VOL Output low voltage				
(std. drive, 0.5mA)	VSS		0.3	V
(high-drive, 5mA) (Note 1)	VSS		0.3	V
Pull up resistance	11	13	16	kΩ
Pull down resistance	11	13	16	kΩ

Note 1: Maximum number of pins with 5mA high drive is three.
*smart*BASIC firmware 1.5.65.0(Feb2014) and subsequent versions support high drive (as well standard drive).

Table 6: SIO pin alternative function AIN (ADC) specification

Parameter	Minimum	Typical	Maximum	Unit
ADC Internal reference voltage	-1.5%	1.2 V	+1.5%	%
ADC pin input internal selectable scaling		1/1, 1/3, 2/3		Scaling
ADC input pin (AIN) voltage maximum without damaging ADC w.r.t VCC Prescaling				
3.6 V 1/1			2.4	V
3.6 V 2/3			3.6	V
3.6 V 1/3			3.6	V
3.3 V 1/1			2.4	V
3.3 V 2/3			3.6	V
3.3 V 1/3			3.6	V
1.8 V 1/1			2.1	V
1.8 V 2/3			2.1	V
1.8 V 1/3			2.1	V
ADC input pin (AIN) voltage maximum without saturating ADC (with 1.2V internal reference)[1]				
1/1 prescaling			1.2	V
2/3 prescaling			1.8	V
1/3 prescaling			3.6	V
Time required to convert single sample in				
10bit mode		68		uS
9bit mode[2]		36		uS
8 bit mode[2]		20		uS
ADC input impedance (during operation)[3]				

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Note 1: Stay within internal 1.2 V reference voltage with given prescaling on AIN pin and do not violate ADC maximum input voltage (for damage) for a given VCC, e.g. If VCC is 1.8 V can only expose AIN pin to 2.1 V (VCC+0.3).

Note 2: Currently, the *smart*BASIC runtime engine firmware only allows 10-bit mode.

Note 3: ADC input impedance is estimated mean impedance of the ADC (AIN) pins. The tolerance is +/-20%. The ADC is highly sensitive to the impedance of the source. The ADC (AIN) input impedance is 200k-600k depending on your ADC gain (pre-scaling) setting. Normally, when not sampling, the ADC (AIN) impedance will have very high value and can consider it to be an open circuit. The moment ADC is sampling, ADC(AIN) impedance is 200k-600k.

3.3.3 nAutoRUN Pin and Operating Modes

Operating modes (refer to the *smart* BASIC manual for details):

- Self-contained mode
- Interactive/Development mode

Table 7: nAutoRUN pin

Signal Name	Pin #	I/O	Comments
nAutoRUN (SIO_28)	28	I	Input with active low logic. Operating mode selected by nAutoRun pin status: If Low (0V), runs $autorun$ if it exists; If High (VCC), runs via at+run (and “file name” of application).

Pin 40 (nAutoRUN) is an input, with active low logic. In the development board (DVK-BL600-sx) it is connected so that the state is driven by the host’s DTR output line. nAutoRUN pin needs to be externally held high or low to select between the two BL600 operating modes:

- Self-contained Run mode (nAutoRUN pin held at 0V).
- Interactive/Development mode (nAutoRUN pin held at VCC)

*smart*BASIC runtime engine firmware checks for the status of nAutoRUN during power-up or reset. If it is low and if there is a *smart*BASIC application named $autorun$ then the *smart*BASIC runtime engine executes the application automatically; hence the name *self-contained run mode*.

3.3.4 OTA (Over-the-Air) *smart*BASIC Application Download

Refer to latest FW release documentation (FW release notes and *smart* BASIC user manual) for details. This feature was first added the *smart*BASIC runtime engine firmware (v1_2_54_0-r2).

Table 8: OTA mode

Signal Name	Pin #	I/O	Comments
SIO_7	9	I	Internal pull down (default). OTA mode selected by externally pulling SIO_7 pin: **High (VCC),** then OTA *smart*BASIC application download is possible.

The OTA *smart*BASIC application download feature can be useful for a customer’s production because it allows the module to be soldered into an end product without preconfiguration; the application can then be downloaded over the air once the product has been pre-tested.

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Note: It is the *smart* BASIC application that is downloaded over the air and NOT the firmware. Due to this principle reason for use in production, to facilitate multiple programming stations in a locality the transmit power is limited (to lower Tx power), refer to ***smart*BASIC user manual** for more details.

4 Power Consumption

Data taken at VCC 3.3V with internal (to chipset) LDO ON or with internal (to chipset) DCDC ON (see Note1) and 25ºC.

Table 9: Power consumption

Parameter	Min	Typical	Max	Unit
Active Mode 'peak' current – Note 1		With LDO (withDCDC)		
(Advertising or Connection)				
TX only run peak current @TXpwr= +4 dBm		16 (11.6)		mA
TX only run peak current @T pwr= 0 dBm		10.5 (8.4)		mA
TX only run peak current @TXpwr= -4 dBm		8 (7.1)		mA
TX only run peak current @TXpwr= -8 dBm		7 (6.9)		mA
TX only run peak current @TXpwr= -12 dBm		6.5 (6.4)		mA
TX only run peak current @TXpwr= -16 dBm		6 (6.1)		mA
T X only run peak current @TXpwr= -20 dBm		5.5 (5.5)		mA
TX Whisper Mode 1 (Note 2)				
TX only run peak current @TXpwr= -30 dBm		5.5 (5.4)		mA
TX Whisper Mode 2 (Note 2)				
TX only run peak current @TXpwr= -55 dBm		5 (5.0)		mA
Active Mode				
RX only 'peak' current (Note2)		8.7 (8.7)		mA
Ultra Low Power Mode1 (Note 3)				
Standby Doze		2.6		uA
Ultra Low Power Mode2 (Note 4)				
Deep Sleep (no RAM retention)		600 (Note 4)		nA
Active Mode Average current (Note 5)				
Advertising Average Current draw				
Max with advertising interval (min) 20 mS		~800		uA
Min with advertising interval (max) 10240 mS		~2.6-4.1		uA
Connection Average Current draw				
Max with connection interval (min) 7.5 mS				uA
with connection interval 67.5 mS		~400		uA
Min with connection interval (max) 4000 mS		~2.6-4.1		uA

Note 1: With VCC 3.3V with internal LDO ON (or with internal DCDC ON). If VCC reduces to 2.1V (operating range of DCDC, the peak current consumption would increase from 11.6mA to ~15.5mA for TX power setting of +4dBm. *smart* BASIC runtime engine firmware v1.2.54.0(Jun2013) and subsequent versions, the internal DCDC convertor was switched off on recommendation from the chipset provider until future notice.

Note 2: Firmware version 1.1.50.0 (only) has an issue that TX PWR settings need to -40 dBm to produce -30 dBm and -65 dBm to produce -55 dBm.

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Note 3: BL600-Sx-02 and BL600-Sx-03: Standby Doze current 3.5uA typical.
BL600-Sx-04: Standby Doze is 2.6uA typical. Standby Doze is entered automatically (when *waitevent* statement is encountered within a *smart*BASIC application script). In Standby Doze, all peripherals that are enabled stay on and may re-awaken the chip. Depending on active peripherals, current consumption ranges from ~2-4 µA to > 1 mA. See individual peripherals current consumption in tables in section ***Peripheral block current consumption 4.3***. Since *smart* BASIC runtime engine firmware v1.3.57.0 (Sept. 2013) has added new function to detect GPIO change with no current consumption cost which means it is possible to close the UART and get to the 2.6-4 uA current consumption regime and yet still be able to detect for incoming data and be woken up so that the UART can be re-opened at expense of losing that first character.

Note 4: In Deep Sleep, everything is disabled and the only wake-up sources are reset and changes on pins on which sense is enabled. The current consumption seen is ~600 nA typical in BL600-Sx-04. BL600-Sx-02 and BL600-Sx-03 this figure is ~1000nA.
smart BASIC runtime engine firmware v1.1.50.0 requires a hardware reset to come out of deep sleep. *smart* BASIC runtime engine firmware v1.2.54.0(Jun2013) release allows coming out from Deep Sleep to Standby Doze through GPIO signal through the reset vector. Deep Sleep mode is entered (with a command in *smart* BASIC application script).

Note 5: Data taken with TX power 4 dBm and all peripherals off (UART OFF after radio event), slave latency of 0 (in a connection). Average current consumption depends on a number of factors [including TX power, VCC accuracy of 16 MHz and 32.768 kHz). With these factors fixed, the largest variable is the advertising or connection interval set.

Advertising Interval range:
20 ms to 10240 ms in multiples of 0.625 ms for Advert type=ADV_IND and ADV_DIRECT_IND.
100 ms to 10240 ms in multiples of 0.625 ms for Advert type=ADV_SCAN_IND and ADV_NONCONN_IND.
For advertising timeout, if the advert type is ADV_DIRECT_IND, then the timeout is limited to 1.28 seconds (1280 ms).

For an advertising event:
- The minimum average current consumption is when the advertising interval is large 10240 mS (although this may cause long discover times (for the advertising event) by scanners

- The maximum average current consumption is when the advertising interval is small 20 mS

Other factors that are also related to average current consumption include the advertising payload bytes in each advertising packet and whether continuously advertising or periodically advertising.

Connection Interval Range:
7.5 ms to 4000 ms in multiples of 1.25 ms.

For a connection event:
- The minimum average current consumption is when the connection interval is large 4000 mS

– The maximum average current consumption is with the shortest connection interval of 7.5 ms; no slave latency. Other factors that are also related to average current consumption include whether transmitting 6 packets per connection interval & each packet contains 20 bytes (which is the maximum for each packet) and an inaccurate 32 kHz master clock accuracy would increase the average current consumption.

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4.1 Measured Peak Current Waveforms during Advertising and Connection

The following figures illustrate current waveforms observed as the BL600 module performs advertising and connection functionality.

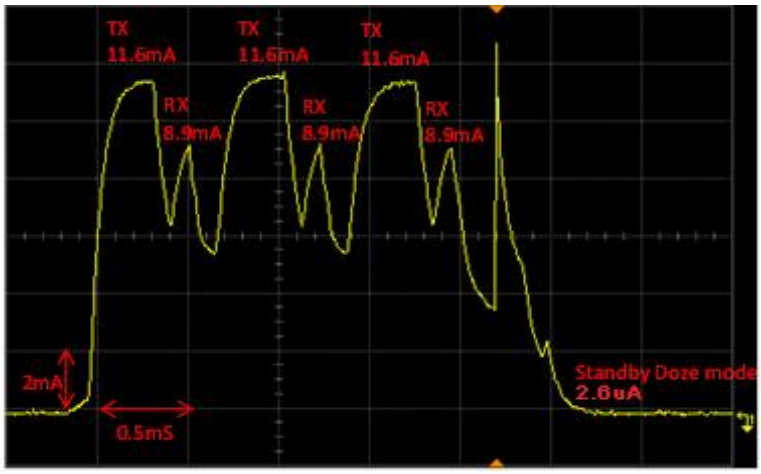

Figure 3: Typical peak current consumption profile (with DCDC ON) during advertising in slave mode @ TX PWR +4dBm. UART is OFF. Last spike is DCDC being turned off.

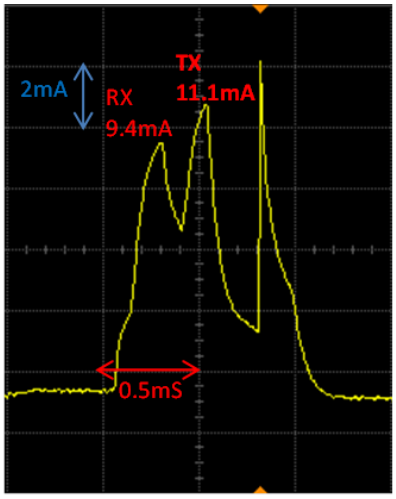

Figure 4: Typical peak current consumption profile (with DCDC ON) during data connection event in slave mode @ TX PWR +4dBm. UART is ON. Last spike is DCDC being turned off

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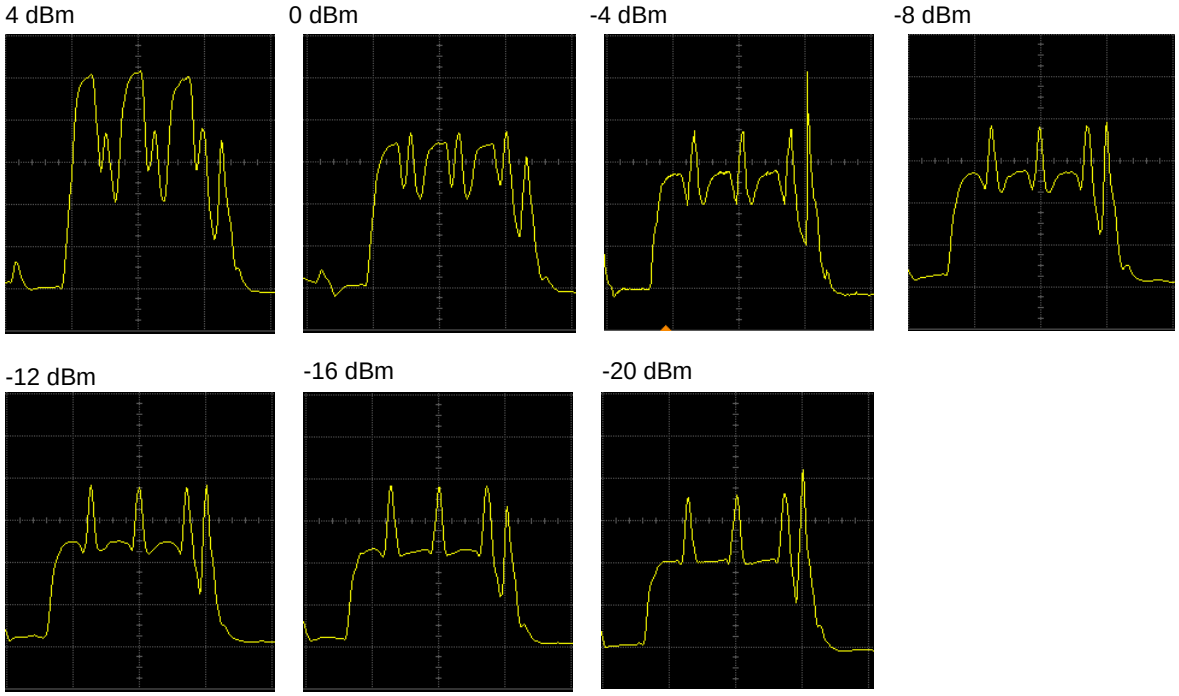


Figure 5: Typical peak current consumption profile (with DCDC ON) during advertising in slave mode versus TX PWR

Advertising (with Whisper Mode TX powers)

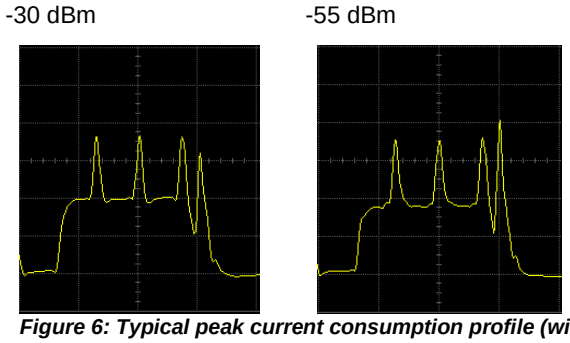
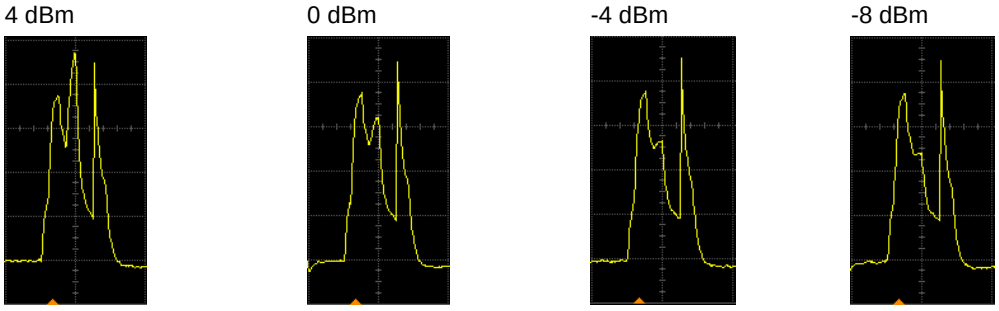


Figure 6: Typical peak current consumption profile (with DCDC ON) during advertising in slave mode with TX Whisper Mode TX PWR -30 dBm (TX Whisper Mode1) and -55 dBm (TX Whisper Mode2)

Note: In the above pictures, UART is ON. X-axis time (1 mS per square), Y-axis current (2 mA per square).



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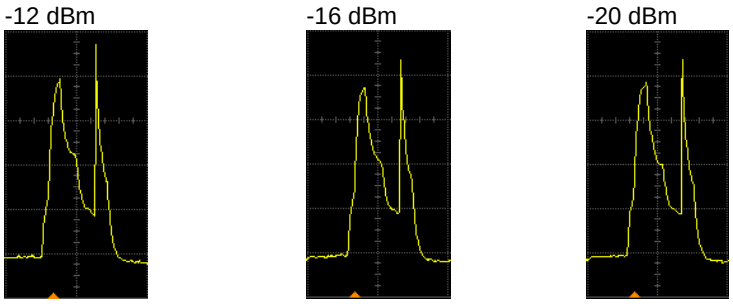

Figure 7: Typical peak current consumption profile (with DCDC ON) during connection event in slave mode versus TX PWR.

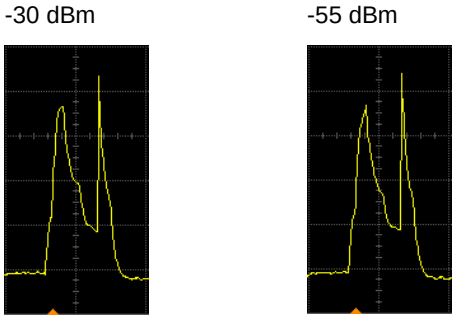

Figure 8: Typical peak current consumption profile during connection event in slave mode with TX Whisper mode TX PWR -30 dBm (TX Whisper Mode1) and -55 dBm (TX Whisper Mode2).

Note: In the above pictures, UART is ON. X-axis time (1 mS per square), Y-axis current (2 mA per square).

4.2 Peripheral Block Current Consumption

The values below are calculated for a typical operating voltage of 3 V.

Table 10: UART Power Consumption

Parameter	Min	Typ	Max	Unit
UART Run current @ 115200 bps		220		uA
UART Run current @ 1200 bps		210		uA
UART Baud rate	1.2		115.2	kbps

Table 11: SPI Power Consumption

Parameter	Min	Typ	Max	Unit
SPI Master Run current @ 125 kbps		180		uA
SPI Master Run current @ 4 Mbps		200		uA
SPI bit rate	0.125		4	Mbps

Table 12: I2C Power Consumption

Parameter	Min	Typ	Max	Unit
I2C Run current @ 100 kbps		380		uA
I2C Run current @ 400 kbps		400		uA
I2C Bit rate	100		400	kbps

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Table 13: ADC Power Consumption

Parameter	Min	Typ	Max	Unit
ADC current during conversion		260		uA

The above current consumption is for the particular peripheral only and to operate that peripheral requires some other internal blocks which consume fixed amount of base current (~740uA). Nordic silicon used in BL600-Sx0-2, BL600-Sx-03, this fixed base current is bit higher (by ~400uA). This base current of ~1140 uA (= ~740uA+400uA) is consumed when the UART, SPI, I2C, or ADC is opened (operated). Therefore BL600-Sx-02 and BL600-Sx-03 would consume total for each peripheral of:

UART (115.2 kbps)	1360 uA (= 1140 uA <base current> + 220 uA)
SPI (master, 8 Mbps	1340 uA (=1140 uA <base current> 200uA).
I2C (400 kbps)	1540 uA (=1140 uA <base current> + 400 uA)
ADC	1430 uA (=1140 uA <base current> + 290 uA)

For the BL600-Sx-04 would consume total for each peripheral of:

UART (115.2 kbps)	1030 uA (= 810 uA <base current> + 220 uA)
SPI (master, 4 Mbps	1010 uA (= 810 uA <base current> 200 uA)
I2C (400 kbps)	1210 uA (= 810 uA <base current> 400 uA)
ADC	1070 uA (= 810 uA <base current> + 260 uA)

For asynchronous interface like the UART (asynchronous as the other end can communicate at any time), the UART (on BL600) must kept open (by a command in *smart*BASIC application script) resulting in the base current consumption penalty.

For synchronous interface like the I2C or SPI (since BL600 side is the master), the interface can be closed and opened only (by a command in *smart*BASIC application script) when needed, resulting in current saving (no base current consumption penalty). Similar argument for ADC (open ADC when needed).

5 Functional Description

The BL600 BLE module is a self-contained Bluetooth Low Energy product and requires only power and a user's *smart*BASIC application to implement full BLE functionality. The integrated, high performance antenna combined with the RF and Base-band circuitry provides the Bluetooth Low Energy wireless link, and any of the SIO lines provide the OEM's chosen interface connection to the sensors. The user's *smart*BASIC application binds the sensors to the BLE wireless functionality.

The variety of hardware interfaces and the *smart*BASIC programming language allow the BL600 module to serve a wide range of wireless applications, whilst reducing overall time to market and the learning curve for developing BLE products.

To provide the widest scope for integration a variety of physical host interfaces / sensors are provided. The major BL600 series module functional blocks described below.

5.1 Power Management (includes brown-out and power on reset)

Power management features:

- System Standby Doze / Deep Sleep modes.
- Brownout Reset.
- Open /Close Peripherals (UART, SPI, I2C, SIO's and ADC). Peripherals consume current when open; each peripheral can be individually closed to save power consumption (with a command in *a smart*BASIC application script).
- 2-region RAM retention (No RAM retention in Deep Sleep mode).
- Enable DCDC on power-up if VCC is >2.1V, see Note1.
- *smart*BASIC command allows the VCC voltage to be read (through the internal ADC).
- Pin wake-up system from Deep sleep (since *smart*BASIC runtime engine firmware v1.2.54.0, Jun 2013).

Power supply features:

- Supervisor HW to manage power on reset, brownout (and power fail).
- 1.8V to 3.6V supply range using internal LDO regulator.
- 2.1 to 3.6V supply range using internal DCDC convertor, see Note1.

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Note 1: With *smart*BASIC runtime engine firmware v1.2.54.0 (June 2013) and subsequent versions, the internal DCDC convertor was switched off on recommendation of the chipset provider until future notice. The benefits of re-adding the DCDC feature (in the future) include:
- The DCDC convertor could be disabled when supply voltage drops to below 2.1V so LDO can be used for low supply voltages.
- When enabled, DCDC operation would automatically suspend when only the internal low current LDO is needed. This feature is useful for applications using battery technologies with higher nominal cell voltages. The reduction in supply voltage level from a high voltage to a low voltage reduces the peak power drain from the battery. Used with a 3 V coin-cell battery, the peak current drawn from the battery is reduced by approximately 30% (with DCDC enabled).

5.2 Clocks and Timers

5.2.1 Clocks

The integrated high accuracy (+/-20ppm) 32.768kHz crystal oscillator provides protocol timing and helps with Radio power consumption in the system Standby Doze /Deep sleep modes by reducing the time that the RX window needs to be open. Standard accuracy clocks tend to have lower accuracy +/-250 ppm.

The integrated high accuracy 16 MHz (+/-10ppm) crystal oscillator helps with Radio operation and also helps reduce power consumption in the Active modes.

5.2.2 Timers

In keeping with the event driven paradigm of *smart* BASIC, the timer subsystem enables *smart* BASIC applications to be written which allow future events to be generated based on timeouts.

Regular Timer: There are 8 built-in timers (regular timer) derived from a single RTC clock which are controlled solely by *smart* BASIC functions. The resolution of the regular timer is 976 microseconds.

Tick Timer is a 31 bit free running counter that increments every 1 millisecond. The resolution of this counter is 488 microseconds. This counter can be accessed using the functions GetTickCount() and GetTickSince().

Refer to the *smart*BASIC user manual.

5.3 Memory for *smart*BASIC Application Code

User has up to 4 Kbytes of data memory available for *smart*BASIC application script.

5.4 RF

- 2402–2480MHz Bluetooth Low Energy radio (1Mbps over the air data rate).
- TX output power of +4dBm programmable (via smartBASIC command) to -20dBm in steps of 4dB.
- TX Whisper mode1 -30dBm (via smartBASIC command).
- TX Whisper mode2 -55dBm (via smartBASIC command).
- Receiver (with integrated channel filters) to achieve maximum sensitivity -91dBm @ 1Mbps BLE.
- RF conducted interface available in 3-ways:
  - BL600-SA: RF connected to on-board antenna on the BL600-SA
  - BL600-SC: RF connected to on-board IPEX MH4 RF connector on BL600-SC
  - BL600-ST: RF connected to RF pad on BL600-ST
- Antenna options:
  - Integrated monopole chip antenna on BL600-SA
  - External dipole antenna connected with to IPEX MH4 RF connector on BL600-SC.
  - External dipole antenna connected to RSMA RF connector which then is connected with 50-Ohms RF track on host PCB to RF pad on BL600-ST.

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5.5 UART Interface

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control support (UART_CTS, UART_RTS) in HW up to 1 Mbps baud. Parity checking and generation for the 9th data bit are supported.

UART_TX, UART_RX, UART_RTS, and UART_CTS form a conventional asynchronous serial data port with handshaking. The interface is designed to operate correctly when connected to other UART devices such as the 16550A. The signalling levels are nominal 0 V and 3.3 V (tracks VCC) and are inverted with respect to the signalling on an RS232 cable.

Two-way hardware flow control is implemented by UART_RTS and UART_CTS. UART_RTS is an output and UART_CTS is an input. Both are active low.

These signals operate according to normal industry convention. UART_RX, UART_TX, UART_CTS, UART_RTS are all 3.3 V level logic (tracks VCC). For example, when RX and TX are idle they sit at 3.3 V. Conversely for handshaking pins CTS, RTS at 0 V is treated as an assertion.

The module communicates with the customer application using the following signals (Figure 9):

- Port /TXD of the application sends data to the module's UART_RX signal line
- Port /RXD of the application receives data from the module's UART_TX signal line

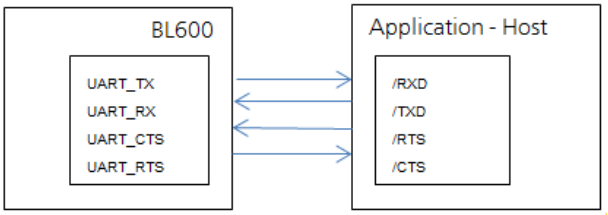

Figure 9: UART Signals

Note: The BL600 serial module output is at 3.3V CMOS logic levels (tracks VCC). Level conversion must be added to interface with an RS-232 level compliant interface.

Some serial implementations link CTS and RTS to remove the need for handshaking. Laird does not recommend linking CTS and RTS other than for testing and prototyping. If these pins are linked and the host sends data at the point that the BL600 deasserts its RTS signal, then there is significant risk that internal receive buffers will overflow, which could lead to an internal processor crash. This will drop the connection and may require a power cycle to reset the module. Laird recommends that the correct CTS/RTS handshaking protocol be adhered to for proper operation.

Table 14: UART Interface

Signal Name	Pin #	I/O	Comments
SIO_21 / UART_TX	32	O	SIO_21 (alternative function UART_TX) is an output, set high (in FW).
SIO_22 / UART_RX	33	I	SIO_22 (alternative function UART_RX) is an input, set with internal pull-up (in FW).
SIO_23 / UART_RTS	34	O	SIO_23 (alternative function UART_RTS) is an output, set low (in FW).
SIO_24 / UART_CTS	35	I	SIO_24 (alternative function UART_CTS) is an input, set with internal pull-down (in FW).

The UART interface is also used to load customer developed *smart* BASIC application script.

BL600-Sx-04 module HW has an improved UART with a deep buffer (increased the UART_RX receive buffer from 2 bytes to 6bytes).

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5.6 SPI Bus

The SPI interface is an alternate function on SIO pins, configurable by *smart* BASIC.

The Module is a master device that uses terminals SPI_MOSI, SPI_MISO, and SPI_CLK. SPI_CSB is implemented using any spare SIO digital output pins to allow for multi-dropping.

The SPI interface enables full duplex synchronous communication between devices. It supports a 3-wire (SPI_MOSI, SPI_MISO, SPI_SCK,) bidirectional bus with fast data transfers to and from multiple slaves. Individual chip select signals will be necessary for each of the slave devices attached to a bus, but control of these is left to the application through use of SIO signals. I/O data is double buffered.

The SPI peripheral supports SPI mode 0, 1, 2, and 3.

Table 15: Peripheral supports

Signal Name	Pin #	I/O	Comments
SPI_MOSI	14	O	This interface is an alternate function configurable by smart BASIC. Default in the FW pin 14 and 16 are inputs. SPIOPEN() in smart BASIC selects SPI function and changes pin14 and 16 to outputs (when in SPI master mode).
SPI_MISO	15	I	
SPI_CLK	16	O	

5.7 I2C Interface

The I2C interface is an alternate function on SIO pins, configurable by *smart*BASIC command.

The Two-wire interface can interface a bi-directional wired-OR bus with two lines (SCL, SDA) and has master /slave topology. The interface is capable of clock stretching. Data rates of 100 kbps and 400 kbps are supported.

An I2C interface allows multiple masters and slaves to communicate over a shared wired-OR type bus consisting two lines which normally sit at VCC. The BL600 module can only be configured as an I2C master with additional constraint that it be the only master on the bus. The SCL is the clock line which is always sourced by the master and SDA is a bi-directional data line which can be driven by any device on the bus.

IMPORTANT: **It is essential to remember that pull-up resistors on both SCL and SDA lines are not provided in the module and MUST be provided external to the module.**

Table 16: I2C Interface

Signal Name	Pin #	I/O	Comments
I2C_SDA	12	I/O	This interface is an alternate function on each pin, configurable by *smart*BASIC. I2COPEN() in *smart*BASIC selects I2C function.
I2C_SCL	13	I/O	

5.8 General Purpose I/O, ADC, PWM/FREQ and Quadrature Decoder

5.8.1 GPIO

The 28 SIO pins are configurable by *smart*BASIC. They can be accessed individually. Each has the following user configured features:

- Input/output direction
- Output drive strength (standard drive 0.5mA or high drive 5mA)

Note: The *smart*BASIC firmware does support high drive since v1.5.65.0 (Feb. 2014).

- Internal pull up and pull down resistors (13K typical) or no pull-up/down
- Wake-up from high or low-level triggers on all pins

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5.8.2 Quadrature Decoder

The following feature exists in hardware but cannot be configured in the firmware currently:

- The quadrature decoder provides buffered decoding of quadrature-encoded sensor signals. It is suitable for mechanical and optical sensors with an optional LED output signal and input debounce filters. The sample period and accumulation are configurable to match application requirements. All pins individually can be configured to carry quadrature demodulator signals.

5.8.3 ADC

The ADC is an alternate function on SIO pins, configurable by *smart*BASIC.

The BL600 provides access to six-channel 10-bit incremental ADC. This enables sampling up to six external signals through a front end MUX. The ADC has configurable input and reference prescaling and sample resolution (8, 9, and 10 bit).

Note: Current *smart*BASIC runtime engine firmware (since v1.1.50.0) provides access to 10-bit mode resolution only.

5.8.3.1 Analog Interface (ADC)

Table 17: Analog interface

Signal Name	Pin No	I/O	Comments
AIN – Analog Input	2	I	This interface is an alternate function on each pin, configurable by *smart*BASIC. AIN configuration selected using GpioSetFunc() function. 8, 9, 10 bit resolution. Voltage scaling 1/1, 2/3, 1/3.
AIN – Analog Input	4	I	
AIN – Analog Input	5	I	
AIN – Analog Input	6	I	
AIN – Analog Input	7	I	
AIN – Analog Input	8	I	

5.8.4 PWM and FREQ Signal Output on up to Two SIO Pins

The PWM and FREQ output is an alternate function on SIO pins, configurable by *smart*BASIC.

The ability to output a PWM (Pulse Width Modulated) signal or FREQ output signal on up to 2 GPIO (SIO) output pins has been added since *smart*BASIC runtime engine firmware v1.3.57.0 and can be selected using GpioSetFunc() function.

PWM output signal has a frequency and duty cycle property. PWM output is generated using 32-bit hardware timers. The timers are clocked by a 1MHz clock source. Frequency is adjustable (up to 1 MHz) and the Duty cycle can be set over range from 0% to 100% (both configurable by *smart*BASIC command). Note, the frequency driving each of the 2 SIO pins is the same but the duty cycle can be independently set for each pin.

FREQ output signal frequency can be set over a range of 0Hz to 4MHz (with 50% mark-space ratio).

5.9 nRESET Pin

Table 18: nRESET pin

Signal Name	Pin No	I/O	Comments
nRESET	22	I	BL600 HW reset (active low). Pull the nRESET pin low for minimum 100mS in order for the BL600 to reset.

Note: For BL600-Sx-02 or BL600-Sx-03: To ensure nReset functions properly, you MUST place a 12K resistor to GND on BL600 pin 23 (NC/SWDCLK) on your host board.

For BL600-Sx-04 or higher: Do not fit a resistor to GND on BL600 pin 23 (NC/SWDCLK).

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5.10 nAutoRUN Pin

Refer to section *nAutoRUN pin and Operating Modes* regarding operating modes and the nAutoRUN pin.

- Self-contained Run mode
- Interactive / Development mode

5.11 Miscellaneous (Hidden JTAG)

The BL6x0 SW consists of 3 parts:

- Nordic Soft Device BT4.1 Low Energy single-mode protocol stack (included as part of the Laird BL6x0 *smart*BASIC FW image)
- BL6x0 *smart*BASIC runtime engine FW
- BL6x0 *smart*BASIC application script developed by customer

Laird BL6x0 *smart*BASIC firmware (FW) image part numbers are referenced as w.x.y.z (ex. v1.5.70.0), where the first 2 numbers (w.x) are the Nordic Soft Device and revision (S110==1.x and S120==12.x) and the remaining numbers (y.z) are the Laird BL6x0 *smart*BASIC runtime engine FW revision. The Nordic Soft Device and Laird BL6x0 *smart*BASIC runtime engine are packaged together in a single FW image that is loaded to the BL6x0 module by Laird at the time of Production.

BL600 *smart*BASIC runtime engine FW can be upgraded by the customer over the UART interface (since v1.2.54.0) only if the new FW image is within the same Nordic Soft Device revision (v1.5.66.0 to v1.5.70.0). Upgrading the BL600 to a *smart*BASIC FW image which includes a new Nordic Soft Device revision (i.e. v1.3.57.0 to v1.5.70.0), customers must use the hidden 2-wire (JTAG) interface (supported since v1.1.50.0).

Customers also have the option to use the hidden 2-wire (JTAG) interface, during production, to clone the file system of a Golden preconfigured BL6x0 to others using the Flash Cloning process described in the app note Flash Cloning for the BL600.

Note: The BL620 supports the JTAG FW upgrade only and has no capability to upgrade FW via UART. The smartBASIC application script developed by the customer can still be upgraded over the UART.

Signal Name (hidden name)	Pin No	I/O	Comments
nRESET (SWDIO)	22	I/O	
NC (SWDCLK)	23	I	Connect 12 K resistor to GND (BL600-Sx-02 and BL600-Sx-03 only).

Only requirement is that the customer should use the following JTAG connector on the host PCB.

The JTAG connector MPN is as follows:

Reference	Part	Description
JP1 Note1	FTSH-105	Header, 1.27mm, SMD, 10-way, FTSH-105-01-L-DV Samtech

Note 1: Reference on BL600 development board schematic. Figure 10 shows the BL600-Sx-02 and BL600-Sx-03 development schematic wiring only for the JTAG connector and BL600 module hidden JTAG pins.

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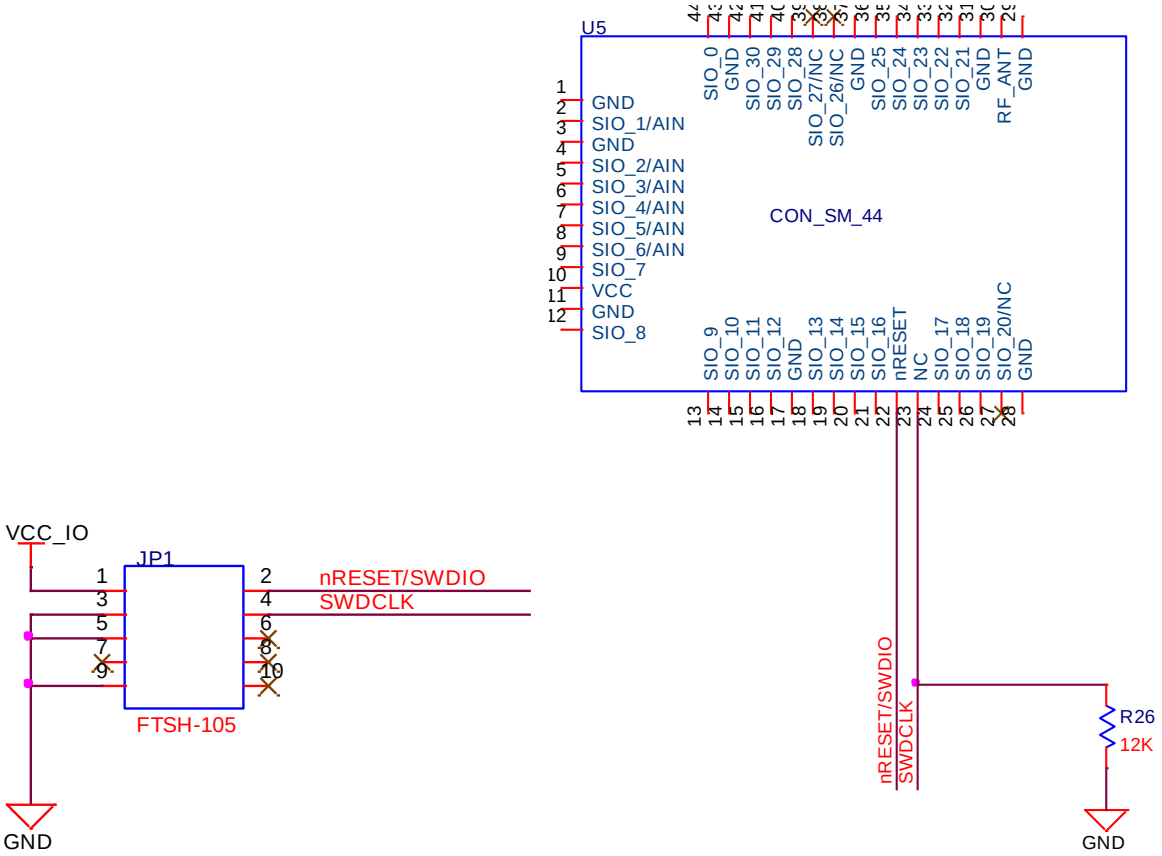

Figure 10: Wiring for JTAG connector to hidden JTAG on BL600 module

Note: Customers MUST NOT fit the 12K resistor on their host board when using the BL600-Sx-04.

5.12 BL600-SA on-board chip antenna characteristics

The BL600-SA on-board chip monopole antenna radiated performance depends on the host PCB layout.

BL600 development board was used for BL600 development and antenna performance evaluation. To obtain similar performance follow guidelines in section *PCB Layout on Host PCB for BL600-SA* to allow the on-board antenna to radiate and reduce proximity effects due to nearby host PCB GND copper or metal covers.

BL600-SA on-board antenna datasheet: http://www.acxc.com.tw/product/at5020/AT5020-E3R0HBAN_071204.pdf

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6 HARDWARE INTEGRATION SUGGESTIONS

6.1 Circuit

The BL600-series module is easy to integrate requiring no external components on the customer's board apart from those required by customer for development and in customers end application.

Checklist (for Schematic):

- **VCC**
  External power source within the operating range, rise time and noise/ripple specification of BL600. Add decoupling capacitors for filtering the external source. Power-on reset circuitry within BL600 series module incorporates brown-out detector, thus simplifying power supply design. Upon application of power, the internal power-on reset ensures module starts correctly.

- **VCC and coin-cell operation**
  With built-in DCDC (operating range 2.1V to 3.6V), reduces the peak current required from a coin-cell (CR2032), making it easier to use with coin-cell.

- **AIN (ADC) and SIO pin IO voltage levels**
  BL600 SIO voltage levels are at VCC. Ensure input voltage levels into SIO pins are at VCC also (if VCC source is a battery whose voltage will drop). Ensure ADC pin maximum input voltage for damage is not violated.

- **AIN (ADC) impedance and external voltage divider setup**
  If one wanted to measure with ADC, a voltage higher than 3.6V then then one can connect a high impedance voltage divider to lower the voltage to the ADC input pin. Other methods are to use a voltage buffer or FET transistor in conjunction with a low resistance voltage divider.
  High impedance values of a voltage divider connected to an AIN pin will introduce ADC inaccuracy. Laird recommends the following solution for setup of a voltage divider when used with the BL600 ADC:
  - Connect a capacitor between AIN and ground (if the voltage divider presents high impedance).
    Normally, when ADC is not sampling, the ADC (AIN) impedance is a very high value and can be considered an open circuit. The moment ADC is sampling, ADC (AIN) impedance is 200k-600k and lowers the AIN voltage. However, when the capacitor is connected it should keep the AIN voltage at previous level for an adequate time period while sampling, minimizing the effect of the high resistance value of the external voltage divider. The capacitor should be big enough to hold voltage up for the required time period, i.e. 20 us for 8 bit sampling or 68 us for 10 bit sampling. If you use a FET transistor to open the current flow through the circuit momentarily before sampling, allow enough time for the capacitor to fully charge before sampling. During the sampling period, multiple samples are made and the ADC output value is the mean value from the sample pool. The sample pool is created during 20 us period for 8-bit sampling, 36 us period for 9-bit sampling, and 68 bit period for 10-bit sampling.

- **JTAG**
  Required if *smart*BASIC runtime engine FW upgrade capability is required (to upgrade to future /later releases from Laird) or Flash Cloning will be used during production to load BL6x0 *smart*BASIC application script, add JTAG connector and 12K resistor to GND (BL600-Sx-02/-03 only) as detailed in section *Miscellaneous (hidden JTAG)*

Note: Customers MUST NOT fit the 12K resistor on their host board when using the BL600-Sx-04.

Note: The BL620 supports a JTAG upgrade but has no capability to upgrade via UART.

- **UART**
  Required for loading customer *smart*BASIC application script during development (or for subsequent upgrade unless using JTAG for FW upgrades and/or Flash Cloning of the *smart*BASIC application script). Add connector to allow UART to be interfaced to PC (via UART –RS232 or UART- USB).

  Note: The BL620 supports a JTAG upgrade but has no capability to upgrade via UART.

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- **UART_RX and UART_CTS**
  SIO_22 (alternative function UART_RX) is an input, set with internal weak pull-up (in FW). The pull-up prevents the module from going into deep sleep when UART_RX line is idling.
  SIO_24 (alternative function UART_CTS) is an input, set with internal weak pull-down (in FW). This pull-down ensures the default state of the UART_CTS will be asserted which means can send data out of the UART_TX line. In the case when UART_CTS is not connected (which we do not recommend).

- **nAutoRUN pin and operating mode selection**
  nAutoRUN pin needs to be externally held high or low to select between the two BL600 operating modes at power-up:
  - Self-contained Run mode (nAutoRUN pin held at 0V).
  - Interactive / development mode (nAutoRUN pin held at VCC).

- Make provision to allow operation in the required mode. Add jumper to allow nAutoRUN pin to be held high or low (via 10K resistor) OR driven by host GPIO.

- **I2C**
  It is essential to remember that pull-up resistors on both I2C_SCL and I2C_SDA lines are not provided in the BL600 module and MUST be provided external to the module as per I2C standard.

- **SPI**
  Implement SPI chip select using any unused SIO pin within your *smart*BASIC application script then SPI_CS is controlled from *smart*BASIC application allowing multi-dropping.

- **SIO pin direction**
  BL600 modules shipped from production with *smart* BASIC runtime engine FW, all SIO pins (with "default function" of "DIO") are mostly digital inputs (see Pin Definitions Table2). Remember to change the direction SIO pin (in your *smart* BASIC application script) if that particular pin is wired to a device that expects to be driven by the BL600 SIO pin configured as an output. Also these SIO pins that are inputs have by default (in FW) have internal pull-up or pull-down resistor-enabled (see Pin Definitions Table2), *since smart* BASIC runtime engine FW 1.5.66.0(Apr2014). This was done to avoid floating inputs (which can also cause current consumption in low power modes (e.g. StandbyDoze) to drift with time. In any case customer can disable the PUL-UP through their *smart* BASIC application.

- ALL *smart* BASIC runtime engine FW versions before 1.5.66.0(Apr2014), the INPUT DIO pins have NO pull-up or pull-down enabled and would require the customer to enable pull-up through *smart* BASIC application script.

Note:	Internal pull-up, pull down will take current from VCC.

- **SIO_7 pin** and Over the Air *smart*BASIC application download feature
  SIO_7 is an input, set with internal pull-down (in FW). Refer to latest FW release documentation on how SIO_7 is used for Over the Air *smart*BASIC application download feature. SIO_7 pin has to be pulled high externally to enable the feature. Decide if this feature is required in production. When SIO_7 is high, ensure SIO_28 (nAutoRun) is NOT high at same time, otherwise you cannot load the *smart* BASIC application script.

- **nRESET pin (active low)**
  Hardware reset. Wire out to push button or drive by host.
  By default module is out of reset when power applied to VCC pin.
  For BL600-Sx-02 or BL600-Sx-03: To ensure nReset functions properly, you MUST place a 12K resistor to GND on BL600 pin 23 (NC/SWDCLK) on your host board.
  For BL600-Sx-04: Do not fit a resistor to GND on BL600 pin 23 (NC/SWDCLK).

- **50-Ohm RF track for interfacing with BL600-ST RF pin (pin 30)**
  BL600-ST brings out the RF on trace pad (pin 30) and this must be tracked to–RSMA connector using 50-Ohms track on host PCB (to stay with regulatory certifications). More details in Checklist for PCB layout for BL600-ST.

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6.2 PCB Layout on Host PCB - General

Checklist (for PCB):

- MUST locate BL600-Sx module close to the edge of PCB (mandatory for BL600-SA for on-board chip antenna to radiate properly).
- Use solid GND plane on inner layer (for best EMC and RF performance).
- All module GND pins MUST be connected to host PCB GND.
- Place GND vias close to module GND pads as possible.
- Unused PCB area on surface layer can flooded with copper but place GND vias regularly to connect copper flood to inner GND plane. If GND flood copper underside the module then connect with GND vias to inner GND plane.
- Route traces to avoid noise being picked up on VCC supply and AIN(analogue) and SIO (digital) traces.
- Do NOT run any track near NC pins pin38 and 39 of BL600-Sx.
- Ensure no exposed copper underside of the module (refer to land pattern of BL600 development board).

6.3 PCB Layout on Host PCB for BL600-SA

6.3.1 Antenna keep-out on host PCB

The BL600-SA has an integrated chip antenna and its performance is sensitive to host PCB. It is critical to locate the BL600-SA on the edge of the host PCB (or corner) to allow the antenna to radiate properly. Refer to guidelines in section ***PCB land pattern and antenna keep-out area for BL600-SA***. Some of those guidelines repeated below.

- Ensure there is no copper in the antenna keep-out area on any layers of the host PCB. Keep all mounting hardware and metal clear of the area to allow proper antenna radiation.
- For best antenna performance, place the BL600-SA module on the edge of the host PCB, preferably in the corner with the antenna facing the corner.
- The BL600 development board has the BL600-SA module on the edge of the board (not in the corner). The antenna keep-out area is defined by the BL600 development board which was used for module development and antenna performance evaluation is shown in Figure 11, where the antenna keep-out area is ~4.2 mm wide, 34.2 mm long; with PCB dielectric (no copper) height 1.539 mm sitting under the BL600-SA antenna.
- A different host PCB thickness dielectric will have small effect on antenna.
- The antenna-keep-out defined in Figure 11 applies when the BL600-SA is placed in the corner of the host PCB. When BL600-SA cannot be placed as such, it must be placed on the edge of the host PCB and the antenna keep out must be observed. An example is shown in Figure 11.

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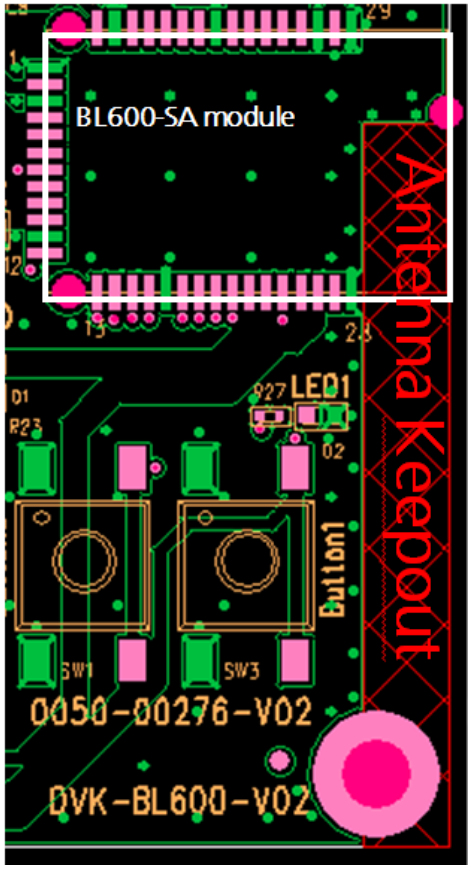

Figure 11: Antenna keep-out area (shown in red), corner of the BL600 development board for BL600-SA module.

Note: 1. BL600 module placed on edge of host PCB.

2. Copper cut-away on all layers in “antenna Keep-out” area under BL600 on host PCB.

6.3.2 Antenna keep-out and Proximity to Metal or Plastic

Checklist (for metal /plastic enclosure):

- Minimum safe distance for metals without seriously compromising the antenna (tuning) is 40mm top/bottom and 30mm left or right.
- Metal close to the BL600-SA chip monopole antenna (bottom, top, left, right, any direction) will have degradation on the antenna performance. How much; that is entirely system dependent which means some testing by customer required (in their host application).
- Anything metal closer than 20mm will start to significantly degrade performance (S11, gain, radiation efficiency).
- It is best that the customer tests the Range with mock-up (or actual prototype) of the product to assess effects of enclosure height (and material whether metal or plastic).

6.4 50-Ohms RF trace on Host PCB for BL600-ST

Checklist (for PCB):

- RF_ANT pin (pin30) is on the BL600-ST module only. You MUST use a 50-Ohm trace from RF_ANT pin to RSMA RF antenna connector on host PCB.

Figure 12 shows the 10 mm length 50-Ohms RF trace (implemented as GCPW) from the BL600-ST module RF trace pads (GND, RF_ANT, GND) on BL600 development board.

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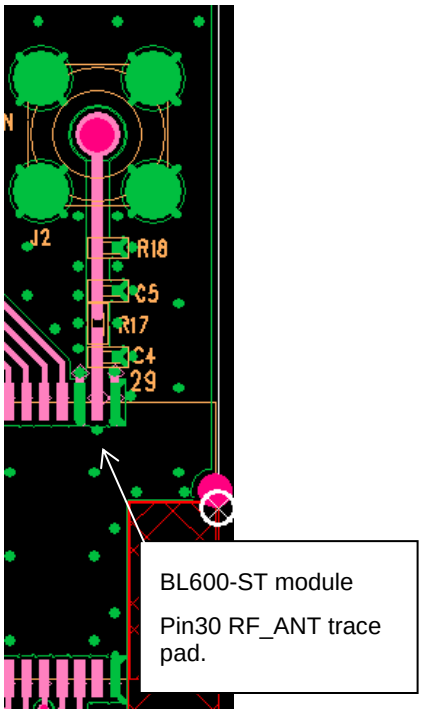

Figure 12: 50-Ohm trace design on BL600 development board (or host PCB) for use with BL600-ST module.

To ensure compliance, observe the following considerations for 50-Ohms RF trace design and test verification:

- Follow the 50-Ohms trace design used on the BL600 development board (PCB stack-up in Figure 11). If this PCB-stack-up is not practical on customer design then design 50-Ohms for differing PCB stack-up.
- Use the same PCB material (FR4)
- The 50-Ohms trace should be a controlled-impedance trace e.g. ±10%.
- The 50-Ohms RF trace length should be 10 mm (recommended) as on the BL600 development board to reduce the trace length.
- Use the same 50-Ohm track width. BL600-ST module RF_ANT pad and land pad widths are 0.5 mm. Therefore 50-Ohm RF trace width may be 0.5 mm width. If 50-Ohm trace is wider, a tapered section should be designed to gradually go from wider width to 0.5 mm RF_ANT (land pad) width.
- Place GND vias regularly spaced either side of 50-Ohms trace to form GCPW (Grounded coplanar waveguide) transmission line.
- Use spectrum analyser to confirm the radiated (and conducted) signal is within the certification limit.

To copy the BL600 development board 50-Ohms RF trace:

- Use the same PCB material (FR4)
- 0.5 mm track width
- Use the same board L1 to L2 thickness (0.2032 mm = 8Mil) for 50-Ohms impedance RF trace design.
- Place regular spaced through-hole GND vias (GCPW transmission line). BL600 development board uses 0.5mm diameter through-hole GND via with 2 to 4 mm distance apart. Gap between RF_ANT trace and GND either side is 0.2 mm for below 50-Ohms impedance RF trace design.

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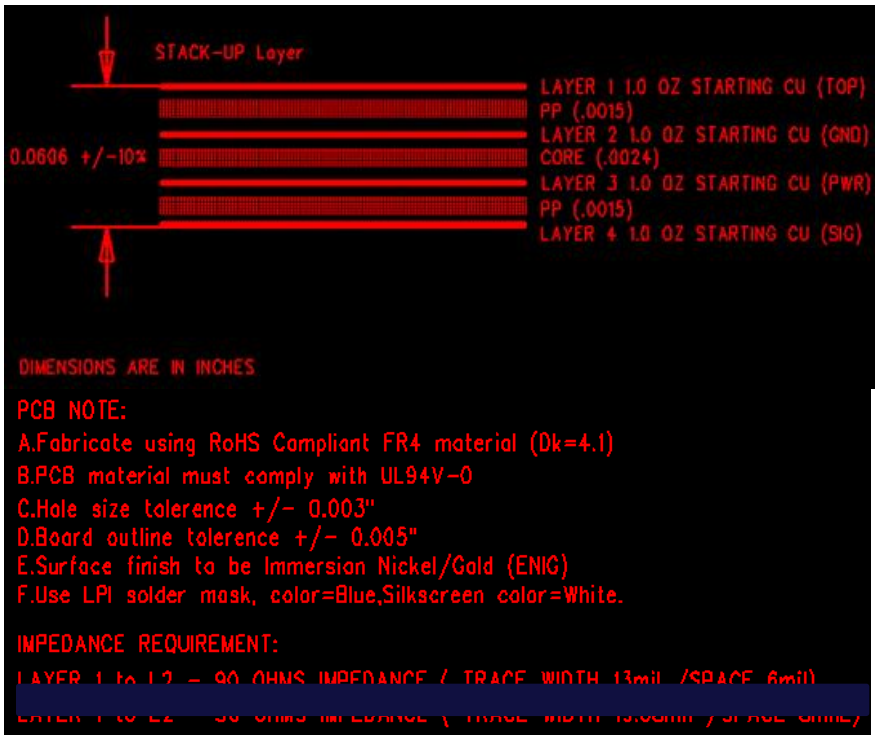

Figure 13: BL600 development board PCB stack-up and L1 to L2 50-Ohms impedance RF trace design.

6.5 External Antenna Integration with BL600-SC and BL600-ST

Please refer to the regulatory sections for FCC, ISED, EU, and Japan for details of use of BL600-Sx with external antennas in each regulatory region.

The BL600 family has been designed to operate with the below external antennas (with a maximum gain of 2.21 dBi). The required antenna impedance is 50 ohms. See Table 19. External antennas improve radiation efficiency.

Table 19: External antennas for the BL600

External Antenna Part Number	Laird Part Number	Mfg.	Type	Gain (dBi)	Connector Type	BL600 Part number
EDA-8709-2G4C1-B27-CY	0600-00057	MAG. Layers	Dipole	2.0	IPEX-4 (See Note1)	BL600-SC
PCA-4606-2G4C1-A33-CY	0600-00056	MAG. Layers	PCB Dipole	2.21	IPEX-4 (See Note1)	BL600-SC
EDA-8709-2G4R2-A40-CY	N/A	MAG. Layers	Dipole	2.0	R-SMA Male	BL600-ST

Note 1: Integral RF co-axial cable (1.13 mm OD) with length 100±5 mm and IPEX-4 compatible connector. These antennas are available through Laird, Mouser, or Digikey. Search their stock for part numbers 0600-00056 and 0600-00057.

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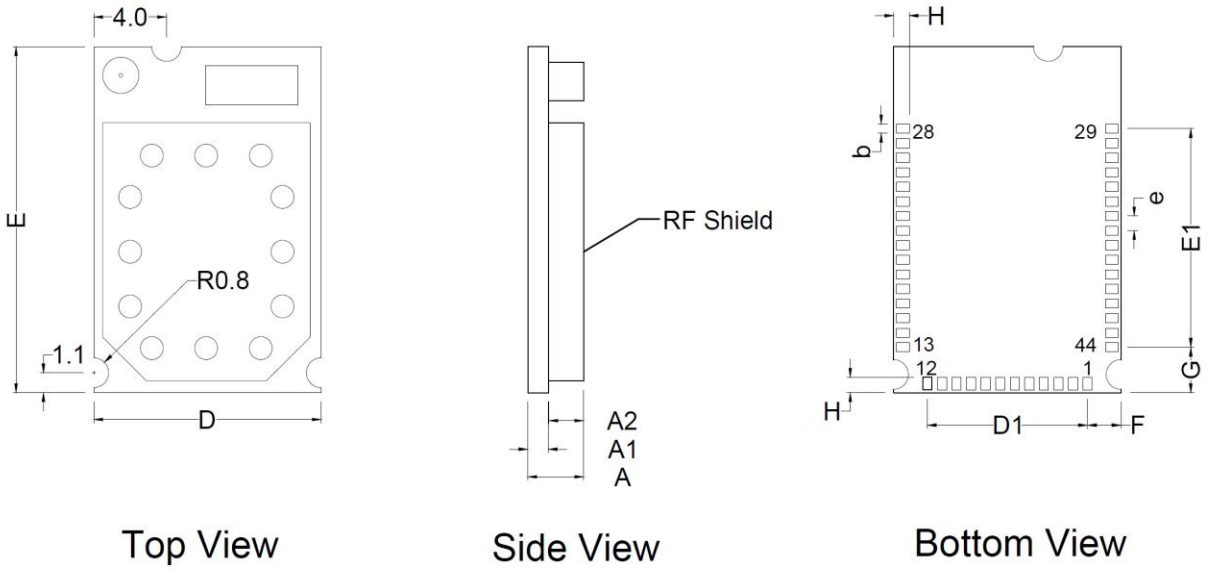
7 MECHANICAL DETAILS

7.1 BL600 Mechanical Details



Description	BL600			
Size	19 x 12.5 x 3.05mm			
Pitch	.8mm			
Dimension	Minimum	Typical	Maximum	Notes
A	3.05	3.16	3.27	
A1	1.06	1.16	1.26	PCB Thickness
A2	1.99	2	2.01	RF Shield Height
b	.45	.5	.55	Global pad width
D	12.4	12.5	12.6	
E	18.9	19	19.1	
e		.8		Global pitch
D1		8.8		
E1		12		
F		1.85		Pad Center to Board edge
G		2.50		Pad Center to Board edge
H		.85		Global length of pad to edge of board
Units	mm			

Title: Module Package Dimensions			
TOLERENCE UNLESS STATED		MATERIAL	DRAWN: D Chapman
x +/-0.3	x.xx +/-0.03	FINISH	CHECKED
x.x+/-0.1		COLOUR	APPROVED
DIMENSIONS IN MM UNLESS STATED	SCALE	THIRD ANGLE PROJECTION	DWG No. BL600
PROJECT: BL600			

Figure 14: BL600 Mechanical drawings

Development Kit Schematics can be found in the software downloads tab of the BL600 product page:
https://connectivity.lairdtech.com/wireless-modules/bluetooth-modules/bluetooth-42-and-40-modules/bl600-series

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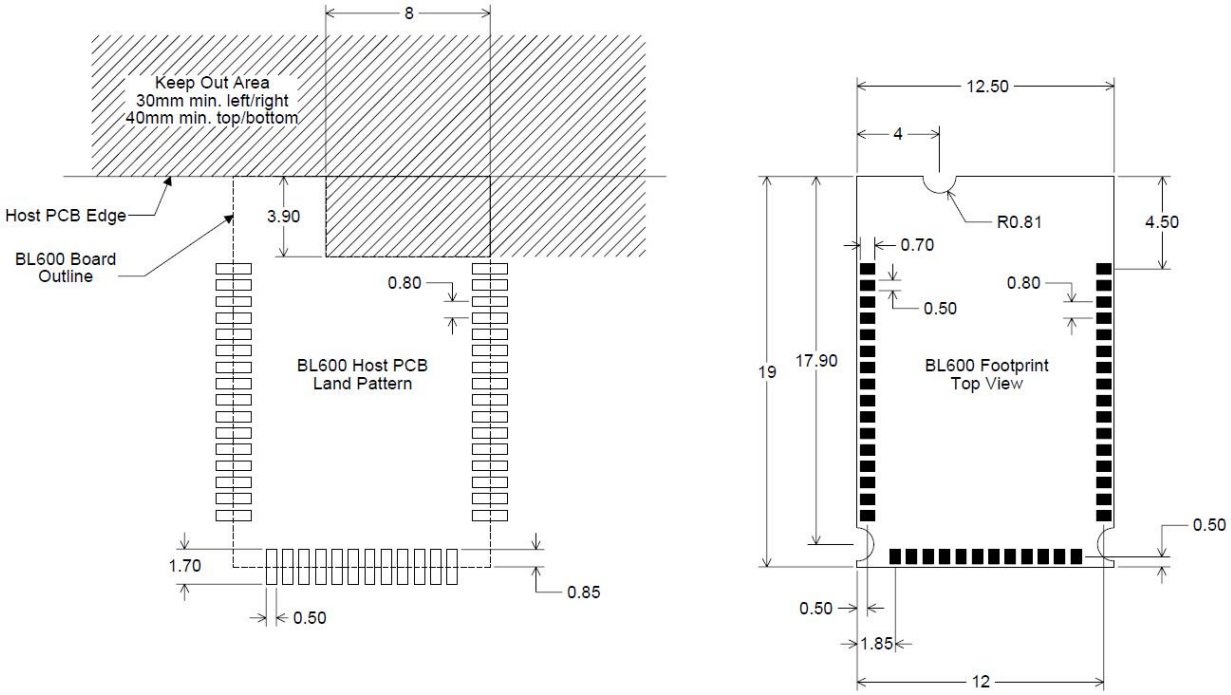
7.2 Host PCB Land Pattern and Antenna Keep-out for BL600-SA



Dimensions in mm.

Application Notes

1. "RF Out" on pin30 is for BL600-ST only. BL600-ST brings out the RF on trace pad (pin 30) and this MUST be tracked with a 50-Ohms RF transmission line (preferably GCPW) on the customers host PCB. More details in section *50-Ohms RF trace on Host PCB for BL600-ST.*

2. Ensure there is no copper in the antenna 'keep out area' on any layers of the host PCB. Also keep all mounting hardware or any metal clear (Refer to 0) on of the area to reduce effects of proximity detuning the antenna and to help antenna radiate properly.

3. For BL600-SA (has on-board chip antenna) best antenna performance, the module BL600-SA MUST be placed on the edge of the host PCB and preferably in the corner with the antenna facing the corner. Above "Keep Out Area" is the module placed in corner of PCB. If BL600-SA is not placed in corner but on edge of host PCB, the antenna "Keep Out Area" is extended (see Note 4).

4. BL600 development board has BL600-SA placed on the edge of the PCB board (and not in corner) for that the Antenna keep out area is extended down to the corner of the development board, see section *PCB Layout on Host PCB for BL600-SA*, Figure10. This was used for module development and antenna performance evaluation.

5. Ensure no exposed copper under module on host PCB.

6. The user may modify the PCB land pattern dimensions based on their experience and / or process capability.

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8 Application Note for Surface Mount Modules

8.1 Introduction

Laird Connectivity surface mount modules are designed to conform to all major manufacturing guidelines. This application note is intended to provide additional guidance beyond the information that is presented in the User Manual. This Application Note is considered a living document and will be updated as new information is presented.

The modules are designed to meet the needs of a number of commercial and industrial applications. They are easy to manufacture and conform to current automated manufacturing processes.

8.2 Shipping

Modules are shipped in ESD (Electrostatic Discharge) safe trays that can be loaded into most manufacturers pick and place machines. Layouts of the trays are provided in Figure 15.

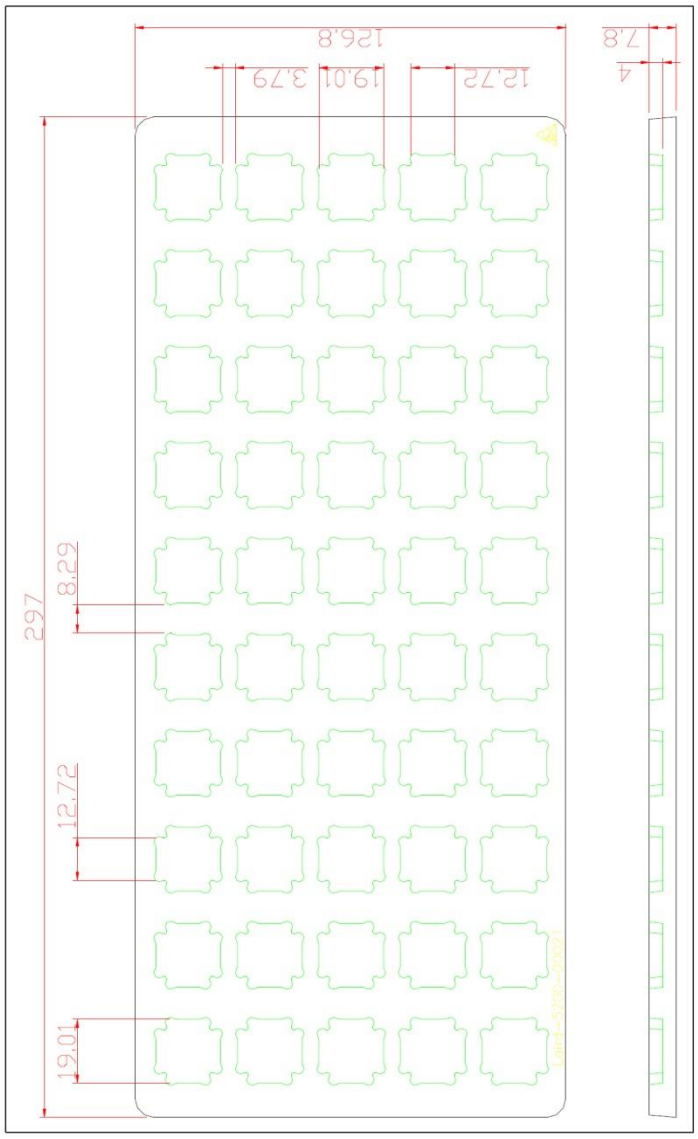

Figure 15: BL600 Shipping Tray Details

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8.3 Reflow Parameters

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to *bake units* on the card, see Table 20 and follow instructions specified by IPC/JEDEC J-STD-033. A copy of this standard is available from the JEDEC website: http://www.jedec.org/sites/default/files/docs/jstd033b01.pdf

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in in Table 20, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment ≤30°C/60%RH.

Table 20: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Laird surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Laird surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

Important: During reflow, modules should not be above 260° and not for more than 30 seconds.

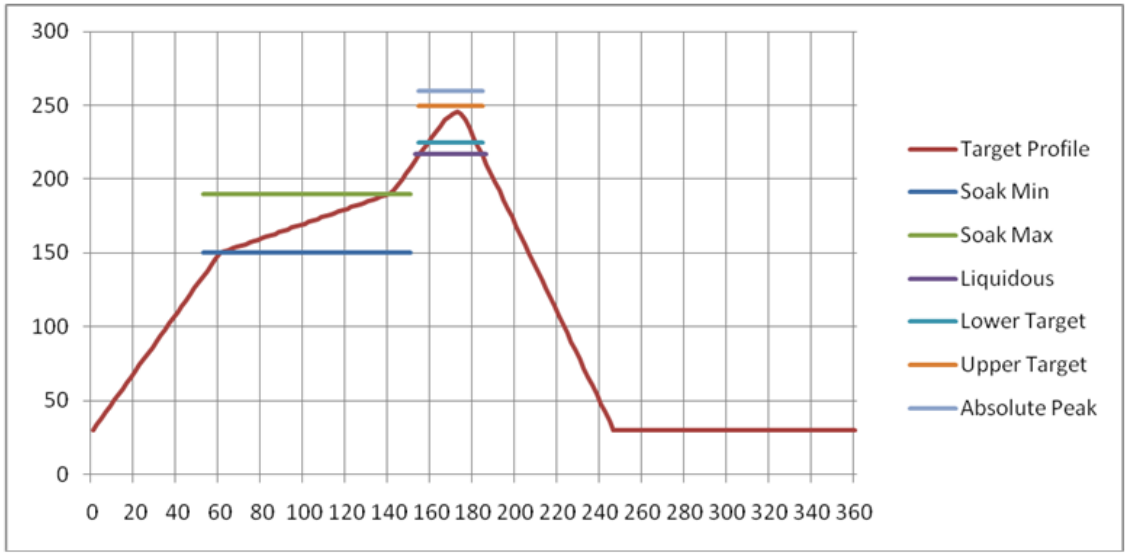

Figure 16: Recommended Reflow Temperature

Temperatures should not exceed the minimums or maximums presented in Table 21.

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Table 21: Recommended Maximum and minimum temperatures

Specification	Value	Unit
Temperature Inc./Dec. Rate (max)	1~3	°C / Sec
Temperature Decrease rate (goal)	2-4	°C / Sec
Soak Temp Increase rate (goal)	.5 - 1	°C / Sec
Flux Soak Period (Min)	70	Sec
Flux Soak Period (Max)	120	Sec
Flux Soak Temp (Min)	150	°C
Flux Soak Temp (max)	190	°C
Time Above Liquidous (max)	70	Sec
Time Above Liquidous (min)	50	Sec
Time In Target Reflow Range (goal)	30	Sec
Time At Absolute Peak (max)	5	Sec
Liquidous Temperature (SAC305)	218	°C
Lower Target Reflow Temperature	240	°C
Upper Target Reflow Temperature	250	°C
Absolute Peak Temperature	260	°C

9 REGULATORY

Note: For complete regulatory information, refer to the BL600 Regulatory Information document which is also available from the BL600 product page.

The BL600 holds current certifications in the following countries:

Country/Region	Regulatory ID
USA (FCC)	BL600-SA/BL600-SC: PI4BL600 BL600-ST: PI4BL600T
EU	N/A
Canada (ISED)	BL600-SA/BL600-SC: 1931B-BL600 BL600-ST: 1931B-BL600T
Japan (MIC)	BL600-SA: 204-320049 BL600-SC: 204-320050 BL600-ST: 204-320048
Taiwan (NCC)	CCAF14LP0320T2

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10 Ordering Information

Part Number	Description
BL600-SA	Single Mode BLE Module featuring *smart*BASIC – integrated antenna
BL600-SC	Single Mode BLE Module featuring *smart*BASIC – u.FL Connector
BL600-ST	Single Mode BLE Module featuring *smart*BASIC – Trace Pad
BL600-SA-32	Single Mode BLE Module – Nordic nRF51822-QFAC (256 / 32) – NO *s*BASIC
DVK – BL600-SA	Development board with BL600-SA module soldered in place
DVK – BL600-SC	Development board with BL600-SC module soldered in place
DVK – BL600-ST	Development board with BL600-ST module soldered in place

10.1 General Comments

This is a preliminary datasheet. Please check with Laird for the latest information before commencing a design. If in doubt, ask.

11 Bluetooth SIG Qualification

11.1 Overview

The BL600 module is listed on the Bluetooth SIG website as a qualified End Product.

Design Name	Owner	Declaration ID	QD ID	Link to listing on the SIG website
BL600	Laird Connectivity	B020700	45362	https://www.bluetooth.org/tpg/QLI_viewQDL.cfm?qid=20700
BL600*	Laird Connectivity	D023023	57149	https://www.bluetooth.org/tpg/QLI_viewQDL.cfm?qid=23023

(* Modules with firmware v1.5.x.x)

It is a mandatory requirement of the Bluetooth Special Interest Group (SIG) that every product implementing Bluetooth technology has a Declaration ID. Every Bluetooth design is required to go through the qualification process, even when referencing a Bluetooth Design that already has its own Declaration ID. The Qualification Process requires each company to register as a member of the Bluetooth SIG – www.bluetooth.org

The following is a link to the Bluetooth Registration page: https://www.bluetooth.org/login/register/

For each Bluetooth Design it is necessary to purchase a Declaration ID. This can be done before starting the new qualification, either through invoicing or credit card payment. The fees for the Declaration ID will depend on your membership status, please refer to the following webpage:

https://www.bluetooth.org/en-us/test-qualification/qualification-overview/fees

For a detailed procedure of how to obtain a new Declaration ID for your design, please refer to the following SIG document:

https://www.bluetooth.org/DocMan/handlers/DownloadDoc.ashx?doc_id=283698&vId=317486

Qualification Steps When Referencing a Laird End Product Design

To qualify your product when referencing a Laird end-product design, follow these steps:

1. To start a listing, go to: https://www.bluetooth.org/tpg/QLI_SDoc.cfm

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Note: A user name and password are required to access this site.

2. In step 1, select the option, New Listing and Reference a Qualified Design.
3. Enter 45362 or 57149 in the End Product table entry.
4. Select your pre-paid Declaration ID from the drop-down menu or go to the Purchase Declaration ID page.

Note: Unless the Declaration ID is pre-paid or purchased with a credit card, you cannot proceed until the SIG invoice is paid.

5. Once all the relevant sections of step 1 are finished, complete steps 2, 3, and 4 as described in the help document accessible from the site.

   Your new design will be listed on the SIG website and you can print your Certificate and DoC.

For further information please refer to the following training material:

https://www.bluetooth.org/en-us/test-qualification/qualification-overview/listing-process-updates

Note: If using the BL600 with Laird Firmware and *smart*BASIC script, you can skip Controller Subsystem, Host Subsystem, and Profile Subsystem.

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11.2 Qualification Steps When Deviating From a Laird End Product Design

If you wish to deviate from the standard End Product designs listed under B020700 or D023023, the qualification process follows the New Listing route (without referencing a Qualified Design). When creating a new design it is necessary to complete the full qualification listing process and also maintain a compliance folder for the design.

If your design is based on un-modified BL600 hardware, follow these steps:

1. Reference the existing RF-PHY test report from the BL600 listing.

Note: This report is available from Laird: https://connectivity.lairdtech.com/resources/support

2. Combine the relevant Nordic Link Layer (LL).
3. Combine the relevant Nordic Link Layer (LL).
4. Combine in a Host Component (covering L2CAP, GAP, ATT, GATT, SM).
5. Test any standard SIG profiles that are supported in the design, (customs profiles are exempt).

The first step is to generate a project on the TPG (Test Plan Generator) system, select 'Traditional Project'. This determines which test cases apply to demonstrate compliance with the Bluetooth Test Specifications, from the TPG you generate a Test Declaration, (Excel format). If you are combining pre-tested and qualified components in your design, and they are within their 3 year listing period, you are not required to re-test those layers covered by those components.

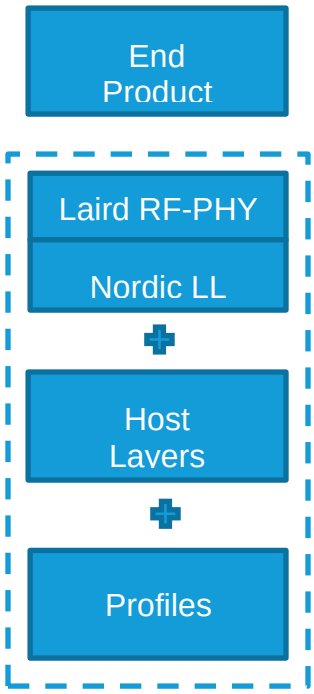

Figure 17: Scope of the qualification for an End Product Design.

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Examples of LL components that can be combined into a new design are:

Listing reference	Design Name	Core Spec Version
20269	nRF51xxx stack: S110 link layer	4.0
22379	Sx20_nRF51xxx link layer	4.1
26392	S130_nRF51xxx link layer	4.2

***Note:** Please check with Laird/Nordic for applicable LL components.

Examples of Host Stack components that can be integrated into the new design are;

Listing reference	Design Name	Core Spec Version
20552	nRF51xxx stack: S110 host layer	4.0
25416	Sx20_nRF51xxx host layer	4.1
26393	S130_nRF51xxx host layer	4.2

***Note:** You may choose any Host Stack and optional profiles in you design.

If the design incorporates any standard SIG LE profiles (such as Heart Rate Profile, refer to section, External to the Core - Current and Qualifiable GATT-based Profile and Service Test Requirements), it is necessary to test these profiles using PTS or other tools where permitted; the results are added to the compliance folder.

You are required to upload your test declaration and test reports (where applicable) and complete the final listing steps on the SIG website. Remember to purchase your Declaration ID before you start the qualification process; you cannot complete the listing without it.

To start a listing, go to: https://www.bluetooth.org/tpg/QLI_SDoc.cfm. In step 1, select the option, **New Listing, (without referencing a Qualified Design).**

12 Additional Assistance

Please contact your local sales representative or our support team for further assistance:

Laird Connectivity
Support Centre: https://www.lairdconnect.com/resources/support
Email: wireless.support@lairdconnectivity.com
Phone: Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852 2923 0610
Web: https://www.lairdconnect.com/products

Note: Information contained in this document is subject to change.

13 Appendix I – Locating the BL600-SX Revision Number

The yellow highlighted area shows the position of the revision number on the BL600 product

Module	Revision	Firmware	Nordic HW Variant
BL600-Sx	-01	1.1.50.0	nRF51822-QFAA-C0
BL600-Sx	-02	1.2.54.0	nRF51822-QFAA-C0
BL600-Sx	-03	1.3.57.0	nRF51822-QFAA-C0
BL600-Sx	-04	1.5.66.0	nRF51822-QFAA-G0
BL600-Sx	-05	1.5.70.0	nRF51822-QFAA-G0
BL600-Sx	-07	1.8.88.0	nRF51822-QFAA-H0
BL600-SA-32	-01	N/A	nRF51822-QFAC-A0
BA600, BB600, BC600	-01	1.8.88.0	nRF51822-QFAA-H0

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