# DDR3 SODIMM

# Product Datasheet

# Index

Rev. 1.5a Nov. 2012

# Revision History

| Revision No. | Date | Remarks |
|---|---|---|
| 1.0 | 2009/08/25 | First release |
| 1.1 | 2010/4/22 | |
| 1.2 | 2011/01/19 | Add DDR3-1600H |
| 1.3 | 2011/08 | |
| 1.4 | 2011/12 | |
| 1.5 | 2012/5 | Add 512Mx8 type |
| 1.5a | 2012/5 | Update 512Mx8 Dual Channel Package. |

Rev. 1.5a Nov. 2012

# Description

The Silicon Power Computer & Communications STU series products are 200-Pin Double Data Rate 3 (DDR3) Synchronous DRAM Small Outline Dual In-Line Memory Module (SODIMM), organized as a one rank 128Mx64 or 256Mx64, high-speed memory array or two ranks 128Mx64, 256Mx64, 512Mx64 high-speed memory array, The module uses four 128x16(1GB), eight 64Mx16(1GB), 128Mx8 (1GB), 128Mx16(2GB), 256Mx8 (2GB), 512Mx8 (4GB), sixteen 128Mx8 (2GB), 256Mx8 (4GB), 512Mx8 (8GB) DDR3 SDRAMs in BGA packages

This DIMM are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers.

DDR3 SDRAM DIMM provide a high-performance, flexible 8-byte interface in a space-saving footprint.

The DIMM is intended for use in applications operating of 533MHz, 667MHz, 800MHz clock speeds and achieves high-speed data transfer rates of 1066, 1333, 1600Mbps. Prior to any access operation, the device CAS latency and burst/length/operation type must be programmed into the DIMM by address inputs A0-A12(64Mx16), A0-A13(128Mx16 or 128Mx8), A0-A14(256Mx8), A0-A15 (512Mx8) and I/O inputs BA0~BA2 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial EEPROM using a standard IIC protocol.

# Features

- DDR3 functionality and operations supported as defined in the component data sheet
- 204pin, small-outline dual in-line memory module (SODIMM)
- Fast data transfer rates: PC3-8500, PC3-10600,PC3-12800
- Single or Dual rank
- 1GB(128 Meg x 8), 2GB (256 Meg x 64), 4GB (512Meg x 64), 8GB (1Giga x 64)
- $V_{DD} = V_{DDQ}$ = 1.5V ±0.075V
- $V_{DDSPD}$ = 3.0V to 3.6V
- Reset pin for improved system stability
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Adjustable data-output drive strength
- Fly-by topology
- Terminated control, command, and address bus
- Serial presence-detect (SPD) EEPROM
- Gold edge contacts
- Pb-free

## Module Specification

| Part Number | Module Density & Configuration | Bandwidth | Data Rate | Timing (tCL-tRCD-tRP) |
|---|---|---|---|---|
| SP001GBSTU106S01(2) | 1GB (128Mx64) 128Mx8 1Rank | PC3-8500 | DDR3-1066 | 7-7-7 |
| SP001GBSTU133S01(2) | | PC3-10600 | DDR3-1333 | 9-9-9 |
| SP001GBSTU106T01(2) | 1GB (128Mx64) 128Mx16 1Rank | PC3-8500 | DDR3-1066 | 7-7-7 |
| SP001GBSTU133T01(2) | | PC3-10600 | DDR3-1333 | 9-9-9 |
| SP001GBSTU106Q01(2) | 1GB (128Mx64) 64Mx16 2Ranks | PC3-8500 | DDR3-1066 | 7-7-7 |
| SP001GBSTU133Q01(2) | | PC3-10600 | DDR3-1333 | 9-9-9 |
| SP002GBSTU106V01(2) | 2GB (256Mx64) 256Mx8 1Rank | PC3-8500 | DDR3-1066 | 7-7-7 |
| SP002GBSTU133V01(2) | | PC3-10600 | DDR3-1333 | 9-9-9 |
| SP002GBSTU160V01(2) | | PC3-12800 | DDR3-1600 | 11-11-11 |
| SP002GBSTU106S01(2) | 2GB (256Mx64) 128Mx8 2Ranks | PC3-8500 | DDR3-1066 | 7-7-7 |
| SP002GBSTU133S01(2) | | PC3-10600 | DDR3-1333 | 9-9-9 |
| SP002GBSTU160S01(2) | | PC3-12800 | DDR3-1600 | 9-9-9 |
| SP002GBSTU106T01(2) | 2GB (256Mx64) 128Mx16 2Ranks | PC3-8500 | DDR3-1066 | 7-7-7 |
| SP002GBSTU133T01(2) | | PC3-10600 | DDR3-1333 | 9-9-9 |
| SP004GBSTU106V01(2) | 4GB (512Mx64) 256Mx8 2Ranks | PC3-8500 | DDR3-1066 | 7-7-7 |
| SP004GBSTU133V01(2) | | PC3-10600 | DDR3-1333 | 9-9-9 |
| SP004GBSTU160V01(2) | | PC3-12800 | DDR3-1600 | 11-11-11 |
| SP004GBSTU133N01(2) | 4GB (512Mx64) 512Mx8 1Rank | PC3-10600 | DDR3-1333 | 9-9-9 |
| SP004GBSTU160N01(2) | | PC3-12800 | DDR3-1600 | 11-11-11 |
| SP008GBSTU133N01(2) | 8GB (1Gx64) 512Mx8 2Ranks | PC3-10600 | DDR3-1333 | 9-9-9 |
| SP008GBSTU160N01(2) | | PC3-12800 | DDR3-1600 | 11-11-11 |
| SP008GBSTU106V21(2) | 4GB x 2 Kit Package | PC3-8500 | DDR3-1066 | 7-7-7 |
| SP008GBSTU133V21(2) | | PC3-10600 | DDR3-1333 | 9-9-9 |
| SP008GBSTU160V21(2) | | PC3-12800 | DDR3-1600 | 11-11-11 |
| SP016GBSTU133N21(2) | 8GB x 2 Kit Package | PC3-10600 | DDR3-1333 | 9-9-9 |
| SP016GBSTU160N21(2) | | PC3-12800 | DDR3-1600 | 11-11-11 |

Note:

1. This document supports all STU Series DDR3 204Pin SODIMM products.

2. Some item was being EOL in this list, Please contact with our sales Dep.

3. All part numbers end with a double-digit code is for customize use only.

   Example: SP001GBSTU133S02-XX

# Pin Assignments

| 204-Pin DDR3 SODIMM Front | | | | | | | |
|---|---|---|---|---|---|---|---|
| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
| 1 | VREFDQ | 53 | DQ19 | 105 | VDD | 157 | DQ42 |
| 3 | VSS | 55 | VSS | 107 | A10 | 159 | DQ43 |
| 5 | DQ0 | 57 | DQ24 | 109 | BA0 | 161 | VSS |
| 7 | DQ1 | 59 | DQ25 | 111 | VDD | 163 | DQ48 |
| 9 | VSS | 61 | VSS | 113 | WE# | 165 | DQ49 |
| 11 | DM0 | 63 | DM3 | 115 | CAS# | 167 | VSS |
| 13 | VSS | 65 | VSS | 117 | VDD | 169 | DQS6# |
| 15 | DQ2 | 67 | DQ26 | 119 | A13 | 171 | DQS6 |
| 17 | DQ3 | 69 | DQ27 | 121 | S1# | 173 | VSS |
| 19 | VSS | 71 | VSS | 123 | VDD | 175 | DQ50 |
| 21 | DQ8 | 73 | CKE0 | 125 | NC | 177 | DQ51 |
| 23 | DQ9 | 75 | VDD | 127 | VSS | 179 | VSS |
| 25 | VSS | 77 | NC | 129 | DQ32 | 181 | DQ56 |
| 27 | DQS1# | 79 | BA2 | 131 | DQ33 | 183 | DQ57 |
| 29 | DQS1 | 81 | VDD | 133 | VSS | 185 | VSS |
| 31 | VSS | 83 | A12 | 135 | DQS4# | 187 | DM7 |
| 33 | DQ10 | 85 | A9 | 137 | DQS4 | 189 | VSS |
| 35 | DQ11 | 87 | VDD | 139 | VSS | 191 | DQ58 |
| 37 | VSS | 89 | A8 | 141 | DQ34 | 193 | DQ59 |
| 39 | DQ16 | 91 | A5 | 143 | DQ35 | 195 | VSS |
| 41 | DQ17 | 93 | VDD | 145 | VSS | 197 | SA0 |
| 43 | VSS | 95 | A3 | 147 | DQ40 | 199 | VDDSPD |
| 45 | DQS2# | 97 | A1 | 149 | DQ41 | 201 | SA1 |
| 47 | DQS2 | 99 | VDD | 151 | VSS | 203 | VTT |
| 49 | VSS | 101 | CK0 | 153 | DM5 | – | – |
| 51 | DQ18 | 103 | CK0# | 155 | VSS | – | – |

| 204-Pin DDR3 SODIMM Back | | | | | | | |
|---|---|---|---|---|---|---|---|
| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
| 2 | VSS | 54 | VSS | 106 | VDD | 158 | DQ46 |
| 4 | DQ4 | 56 | DQ28 | 108 | BA1 | 160 | DQ47 |
| 6 | DQ5 | 58 | DQ29 | 110 | RAS# | 162 | VSS |
| 8 | VSS | 60 | VSS | 112 | VDD | 164 | DQ52 |
| 10 | DQS0# | 62 | DQS3# | 114 | S0# | 166 | DQ53 |
| 12 | DQS0 | 64 | DQS3 | 116 | ODT0 | 168 | VSS |
| 14 | VSS | 66 | VSS | 118 | VDD | 170 | DM6 |
| 16 | DQ6 | 68 | DQ30 | 120 | ODT1 | 172 | VSS |
| 18 | DQ7 | 70 | DQ31 | 122 | NC | 174 | DQ54 |
| 20 | VSS | 72 | VSS | 124 | VDD | 176 | DQ55 |
| 22 | DQ12 | 74 | CKE1 | 126 | VREFCA | 178 | VSS |
| 24 | DQ13 | 76 | VDD | 128 | SS | 180 | DQ60 |
| 26 | VSS | 78 | NC | 130 | DQ36 | 182 | DQ61 |
| 28 | DM1 | 80 | NC/A14 | 132 | DQ37 | 184 | VSS |
| 30 | RESET# | 82 | VDD | 134 | VSS | 186 | DQS7# |
| 32 | VSS | 84 | A11 | 136 | DM4 | 188 | DQS7 |
| 34 | DQ14 | 86 | A7 | 138 | VSS | 190 | VSS |
| 36 | DQ15 | 88 | VDD | 140 | DQ38 | 192 | DQ62 |
| 38 | VSS | 90 | A6 | 142 | DQ39 | 194 | DQ63 |
| 40 | DQ20 | 92 | A4 | 144 | VSS | 196 | VSS |
| 42 | DQ21 | 94 | VDD | 146 | DQ44 | 198 | EVENT# |
| 44 | VSS | 96 | A2 | 148 | DQ45 | 200 | SDA |
| 46 | DM2 | 98 | A0 | 150 | VSS | 202 | SCL |
| 48 | VSS | 100 | VDD | 152 | DQS5# | 204 | VTT |
| 50 | DQ22 | 102 | CK1 | 154 | DQS5 | – | – |
| 52 | DQ23 | 104 | CK1# | 156 | VSS | – | – |

# Pin Description

| Symbol | Type | Description |
|---|---|---|
| A0–A15 | Input | **Address inputs:** Provide the row address for ACTIVE commands and the column address and auto precharge bit for READ/WRITE commands to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. The address inputs also provide the opcode during mode register command set. A0–A13 (128Mx8) A0–A14 (256Mx8). A0–A15 (512Mx8). |
| BA0–BA2 | Input | **Bank address inputs:** BA0, BA1 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0, BA1 define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command. |
| CK0, CK0#, CK1, CK1# | Input | **Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#. |
| CKE0, CKE1 | Input | **Clock enable:** CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR3 SDRAM. |
| DM0–DM7 | Input | **Data input mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS7pins. |
| ODT0 ODT1 | Input | **On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to the following pins: DQ, DQS, DQS# and DM. The ODT input will be ignored if disabled via the LOAD MODE command. |
| RAS#, CAS#, WE# | Input | **Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered. |
| RESET# | Input (LVCMOS) | **Reset:** RESET# is an active LOW CMOS input referenced to $V_{SS}$. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 ×$V_{DD}$ and DC LOW ≤ 0.2 ×$V_{DD}$. |
| S0#, S1# | Input | **Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder. |
| SA[2:0] | Input | **Presence-detect address inputs:** These pins are used to configure the SPD EEPROM address range. |
| SCL | Input | **Serial clock for presence-detect:** SCL is used to synchronize the presence-detect data transfer to and from the module. |
| DQ0–DQ63 | I/O | **Data input/output:** Bidirectional data bus. |
| DQS0–DQS7 DQS0#–DQS7# | I/O | **Data strobe:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. |
| SDA | I/O | **Serial presence-detect data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the SPD EEPROM on the module. |
| $V_{DD}$ | Supply | **Power supply:** 1.5V ±0.075V. The component $V_{DD}$ and $V_{DDQ}$ are connected to the module $V_{DD}$. |
| $V_{DDSPD}$ | Supply | **Temperature sensor/SPD EEPROM power supply:** +3.0V to +3.6V. |
| $V_{REFCA}$ | Supply | **Reference voltage:** Control, command, and address ($V_{DD}$/2). |
| $V_{REFDQ}$ | Supply | **Reference voltage:** DQ, DM ($V_{DD}$/2). |
| $V_{SS}$ | Supply | Ground. |
| $V_{TT}$ | Supply | **Termination voltage:** Used for control, command, and address ($V_{DD}$/2). |
| NC | – | **No connect:** These pins are not connected on the module. |
| NU | – | **Not used:** These pins are not used in specific module configuration/operations. |

# Environmental Requirements

| Symbol | Parameter | Rating | Units | Note |
|---|---|---|---|---|
| $T_{OPR}$ | Module Operating Temperature Range (ambient) | 0 to 55 | °C | 3 |
| $H_{OPR}$ | Operating Humidity (relative) | 10 to 90 | % | 1 |
| $T_{STG}$ | Storage Temperature (Plastic) | -55 to 100 | °C | 1 |
| $H_{STG}$ | Storage Humidity (without condensation) | 5 to 95 | % | 1 |
| $P_{BAR}$ | Barometric Pressure (operating & storage) | 105 to 69 | K Pascal | 1, 2 |

Note:

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Up to 9850 ft.

3. The component maximum case temperature shall not exceed the value specified in the component spec.

# Absolute Maximum DC Ratings

| Symbol | Parameter | Rating | Units | Note |
|---|---|---|---|---|
| $V_{DD}$ | Voltage on $V_{DD}$ pins relative to $V_{SS}$ | -0.4 V ~ 1.975 V | V | 1, 3 |
| $V_{DDQ}$ | Voltage on $V_{DDQ}$ pins relative to $V_{SS}$ | -0.4 V ~ 1.975 V | V | 1, 3 |
| $V_{IN}$, $V_{OUT}$ | Voltage on I/O pins relative to $V_{SS}$ | -0.4 V ~ 1.975 V | V | 1 |
| $T_{STG}$ | Storage Temperature | -55 to +100 | °C | 1, 2 |

Note:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Storage Temperature is the case surface temperature on the center/top side of the DRAM.

3. $V_{DD}$ and $V_{DDQ}$ must be within 300 mV of each other at all times; and $V_{REF}$ must be not greater

# Operating temperature Conditions

| Symbol | Parameter | Rating | Units | Note |
|---|---|---|---|---|
| $T_{OPER}$ | Normal Operating Temperature Range | 0 to 85 | °C | 1, 2 |
| | Extended Temperature Range (Optional) | 85 to 95 | °C | 1,3 |

Note:

1. Operating Temperature $T_{OPER}$ is the case surface temperature on the center / top side of the DRAM.

2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under all operating conditions

3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are supported in this range, but the following additional conditions apply:

   a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.

   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode(MR2 A6 = 1b and MR2 A7 = 0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

# DC Electrical Characteristics and Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 1.425 | 1.5 | 1.575 | V | 1,2 |
| $V_{DDQ}$ | Output Supply Voltage | 1.425 | 1.5 | 1.575 | V | 1,2 |

Note:

1. Under all conditions $V_{DDQ}$ must be less than or equal to $V_{DD}$.

2. $V_{DDQ}$ tracks with $V_{DD}$. AC parameters are measured with $V_{DD}$ and $V_{DDQ}$ tied together.

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# Single-Ended AC and DC Input Levels for Command and Address

| Symbol | Parameter | DDR3-1066 | | DDR3-1333 | | Units | Note |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| VIH.CA(DC) | DC Input Logic High | Vref + 0.100 | VDD | Vref + 0.100 | VDD | V | 1 |
| VIL.CA(DC) | DC Input Logic Low | VSS | Vref - 0.100 | VSS | Vref - 0.100 | V | 1 |
| VIH.CA(AC) | AC Input Logic High | Vref + 0.175 | Note 2 | Vref + 0.175 | Note 2 | V | 1, 2 |
| VIL.CA(AC) | AC Input Logic Low | Note 2 | Vref - 0.175 | Note 2 | Vref - 0.175 | V | 1, 2 |
| VIH.CA(AC150) | AC Input Logic High | - | - | Vref + 0.15 | Note 2 | V | 1, 2 |
| VIL.CA(AC150) | AC Input Logic Low | - | - | Note 2 | Vref - 0.15 | V | 1, 2 |
| VRefCA(DC) | Reference Voltage for ADD, CMD Inputs | 0.49 x VDD | 0.51 x VDD | 0.49 x VDD | 0.51 x VDD | V | 3, 4 |

Note:

1. For input only pins except . Vref = VrefCA(DC).

2. See "Overshoot and Undershoot Specifications" in the device datasheet.

3. The ac peak noise on VRef may not allow VRef to deviate from VRefDQ(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).

4. For reference: approx. VDD/2 +/- 15 mV.


# Single-Ended AC and DC Input Levels for DQ and DM

| Symbol | Parameter | DDR3-1066 | | DDR3-1333 | | Units | Note |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| VIH.DQ(DC) | DC Input Logic High | Vref + 0.100 | VDD | Vref + 0.100 | VDD | V | 1 |
| VIL.DQ(DC) | DC Input Logic Low | VSS | Vref - 0.100 | VSS | Vref - 0.100 | V | 1 |
| VIH.DQ(AC) | AC Input Logic High | Vref + 0.175 | Note 2 | Vref + 0.15 | Note 2 | V | 1, 2, 5 |
| VIL.DQ(AC) | AC Input Logic Low | Note 2 | Vref - 0.175 | Note 2 | Vref - 0.15 | V | 1, 2, 5 |
| VRefDQ(DC) | Reference Voltage for DQ, DM Inputs | 0.49 x VDD | 0.51 x VDD | 0.49 x VDD | 0.51 x VDD | V | 3, 4 |

Note: 1. For input only pins except. Vref = VrefDQ(DC).

2. See "Overshoot and Undershoot Specifications" in the device datasheet.

3. The ac peak noise on VRef may not allow VRef to deviate from VRefDQ(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).

4. For reference: approx. VDD/2 +/- 15 mV.

5. Single-ended swing requirement for DQS, DQS# is 350 mV (peak to peak). Differential swing requirement for DQS - DQS# is 700 mV(peak to peak).
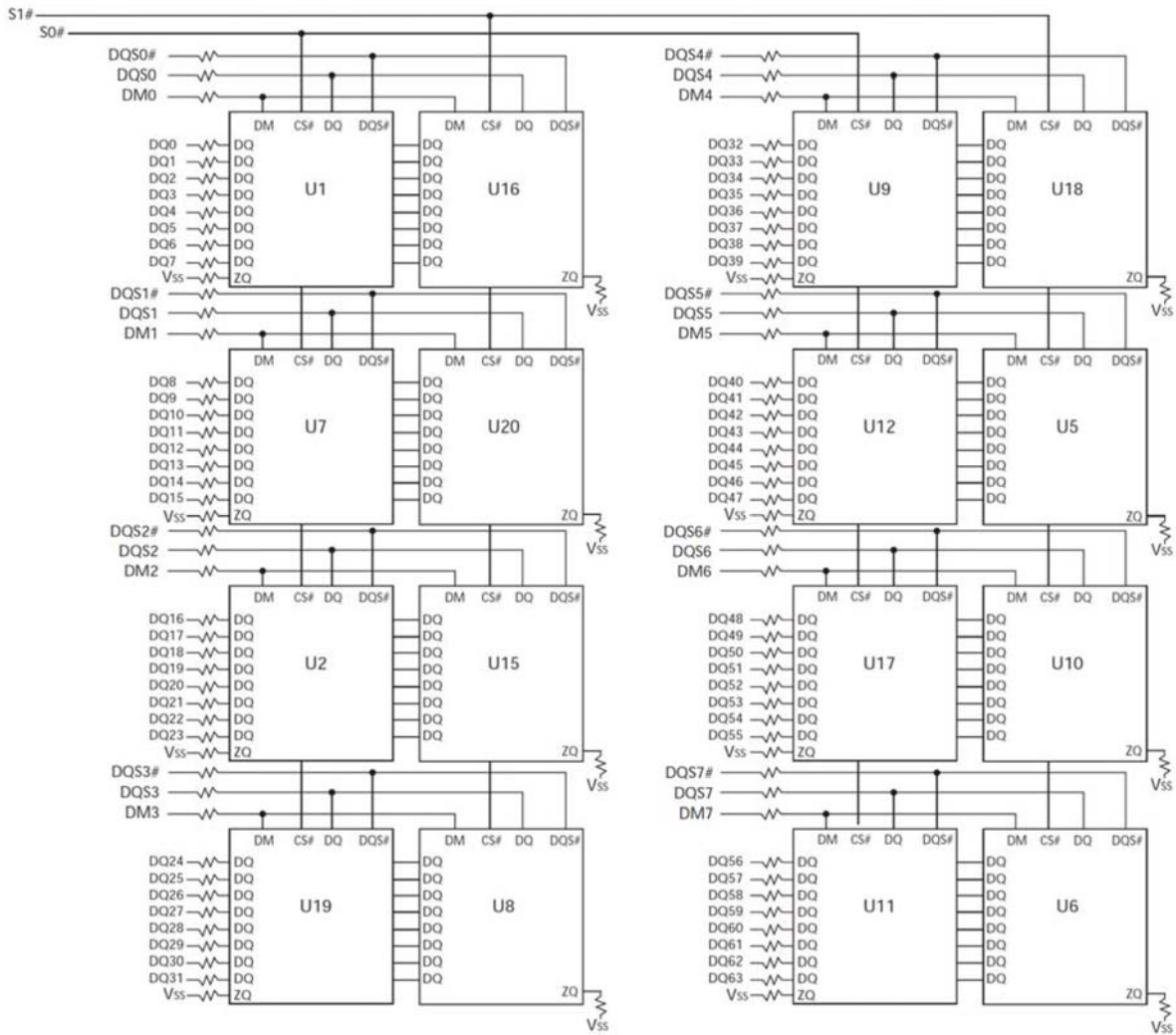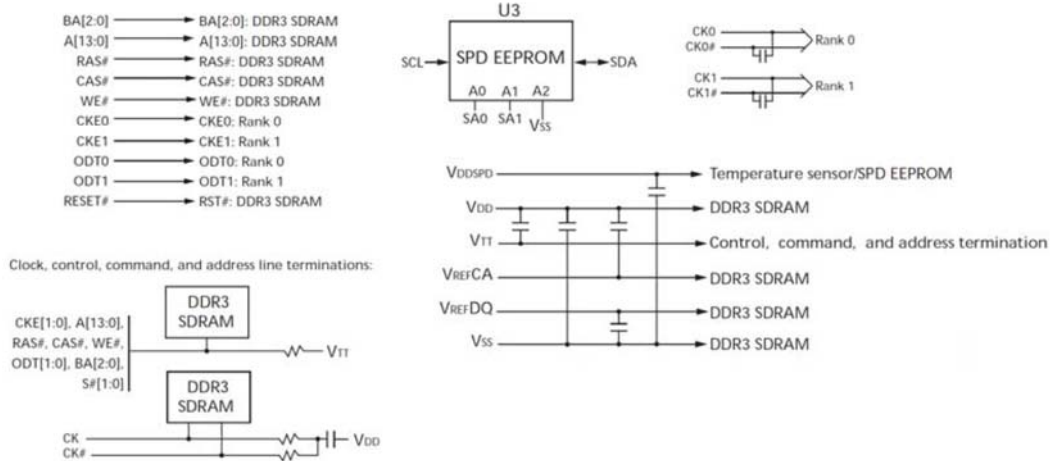
# Block Diagram(x8 1Rank)
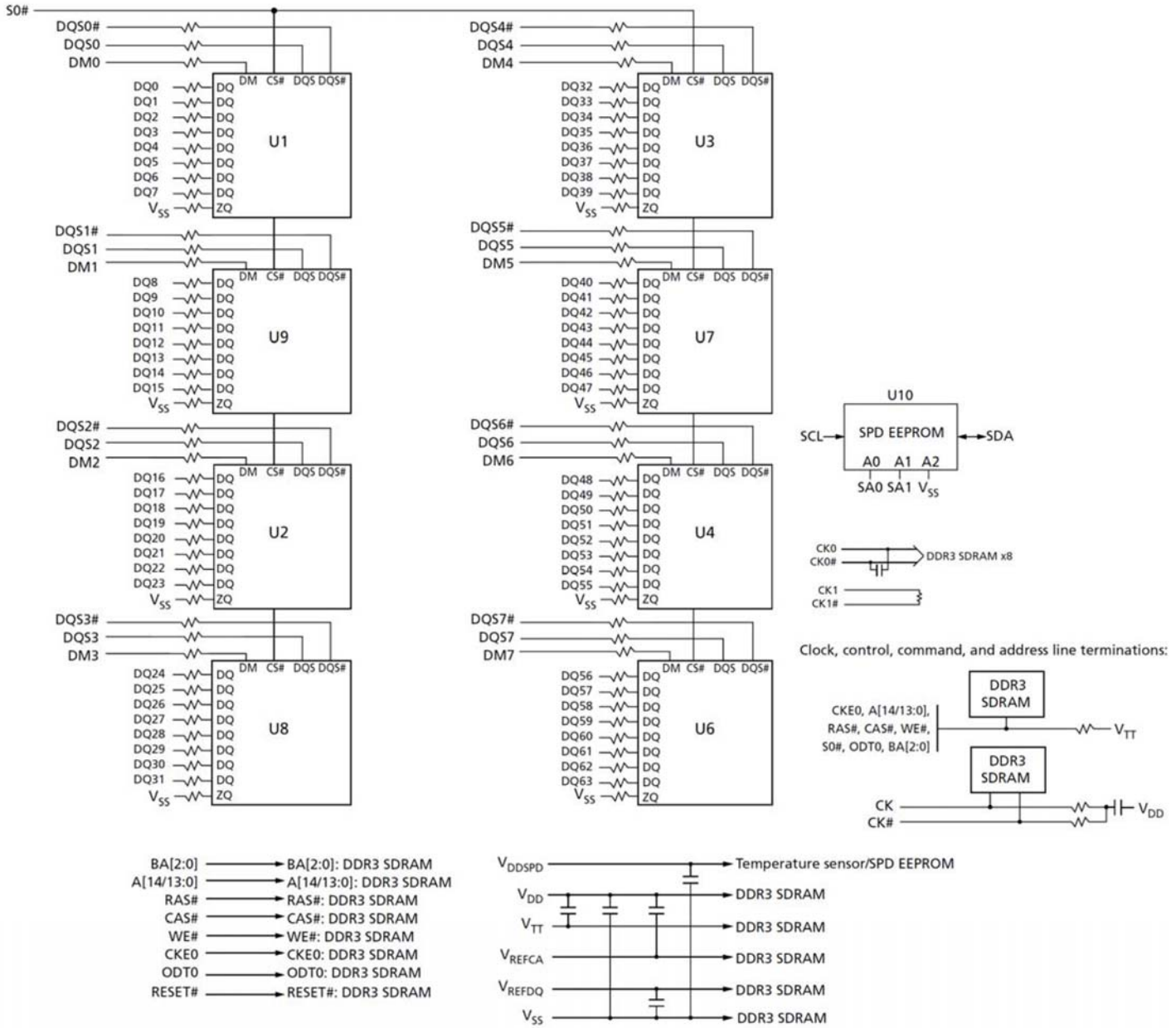


**Note:** The ZQ ball on each DDR3 component is connected to an external 240Ω resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.
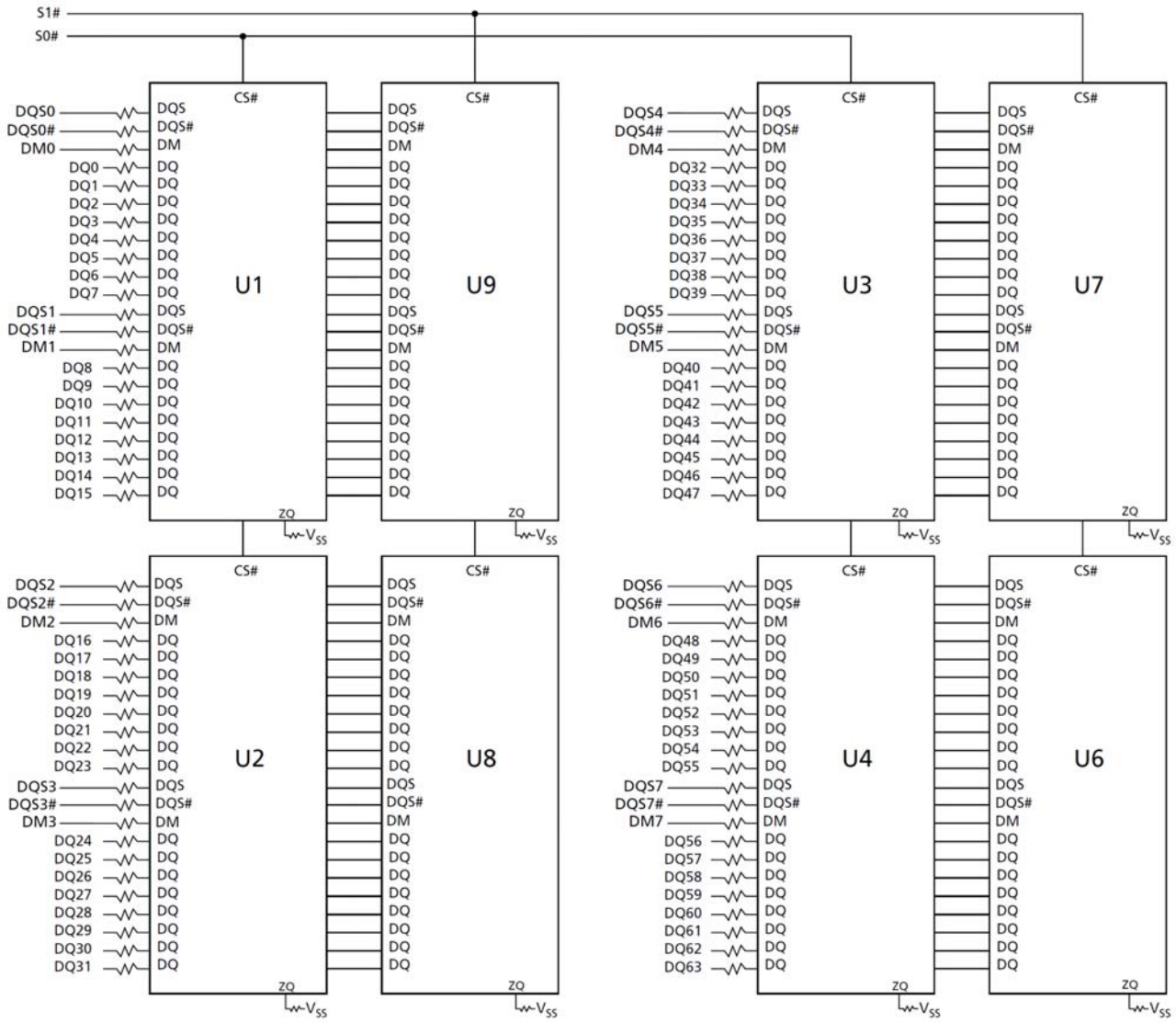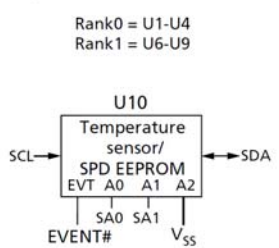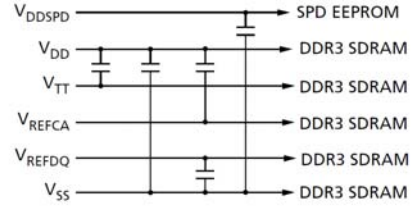
# Block Diagram(x16 1Rank)
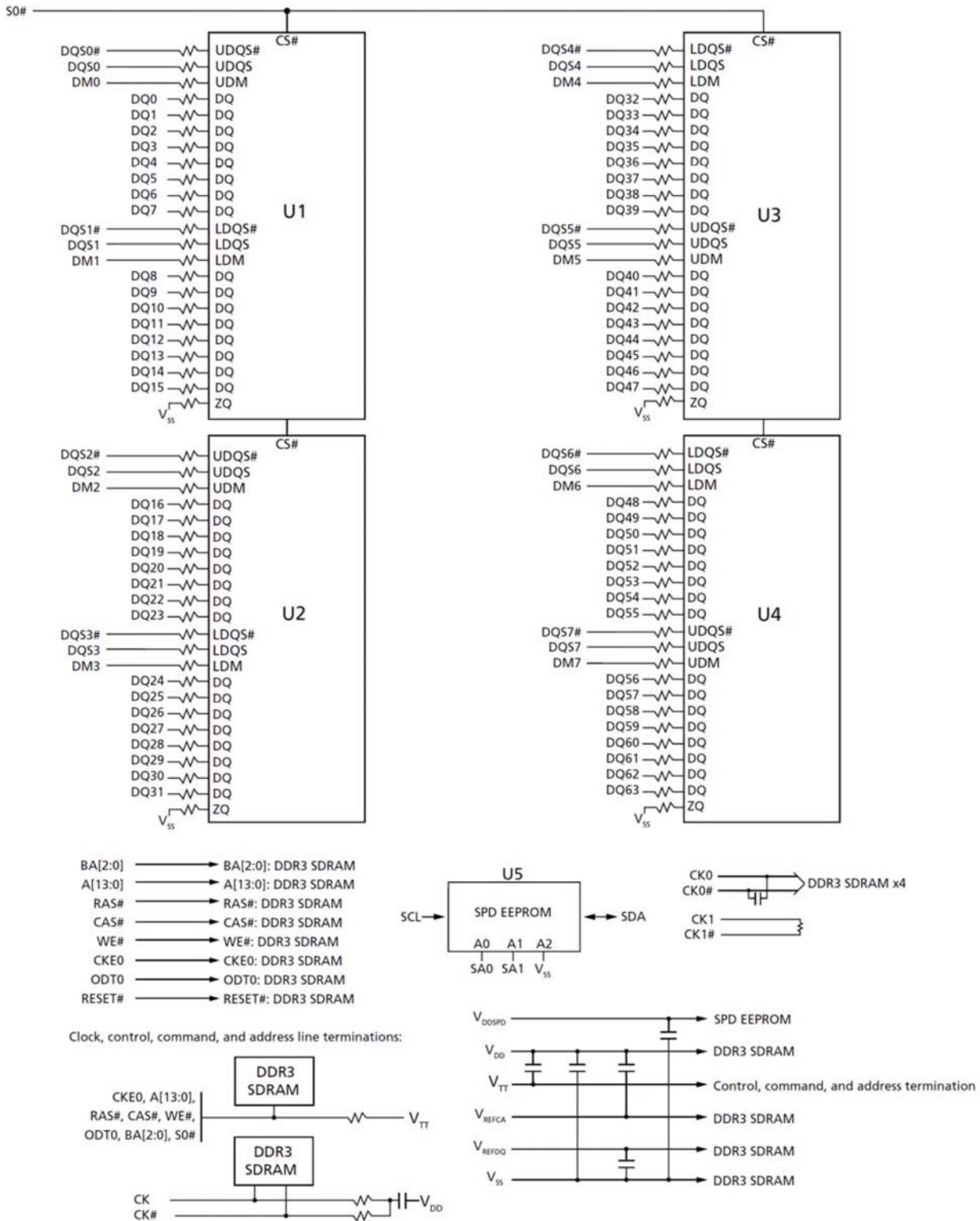


**Note:** The ZQ ball on each DDR3 component is connected to an external 240Ω resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.
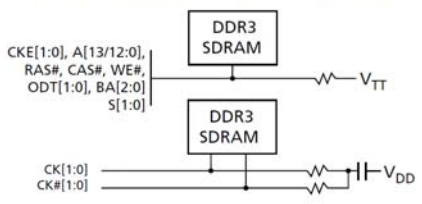
# Block Diagram(x8 2Ranks)



Rank 0 = U1, U2, U7, U9, U11, U12, U17, U19
Rank 1 = U5, U6, U8, U10, U15, U16, U18, U20

**Note:** The ZQ ball on each DDR3 component is connected to an external 240Ω resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

# Block Diagram(x16 2Ranks)



**Note:** The ZQ ball on each DDR3 component is connected to an external 240Ω resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.
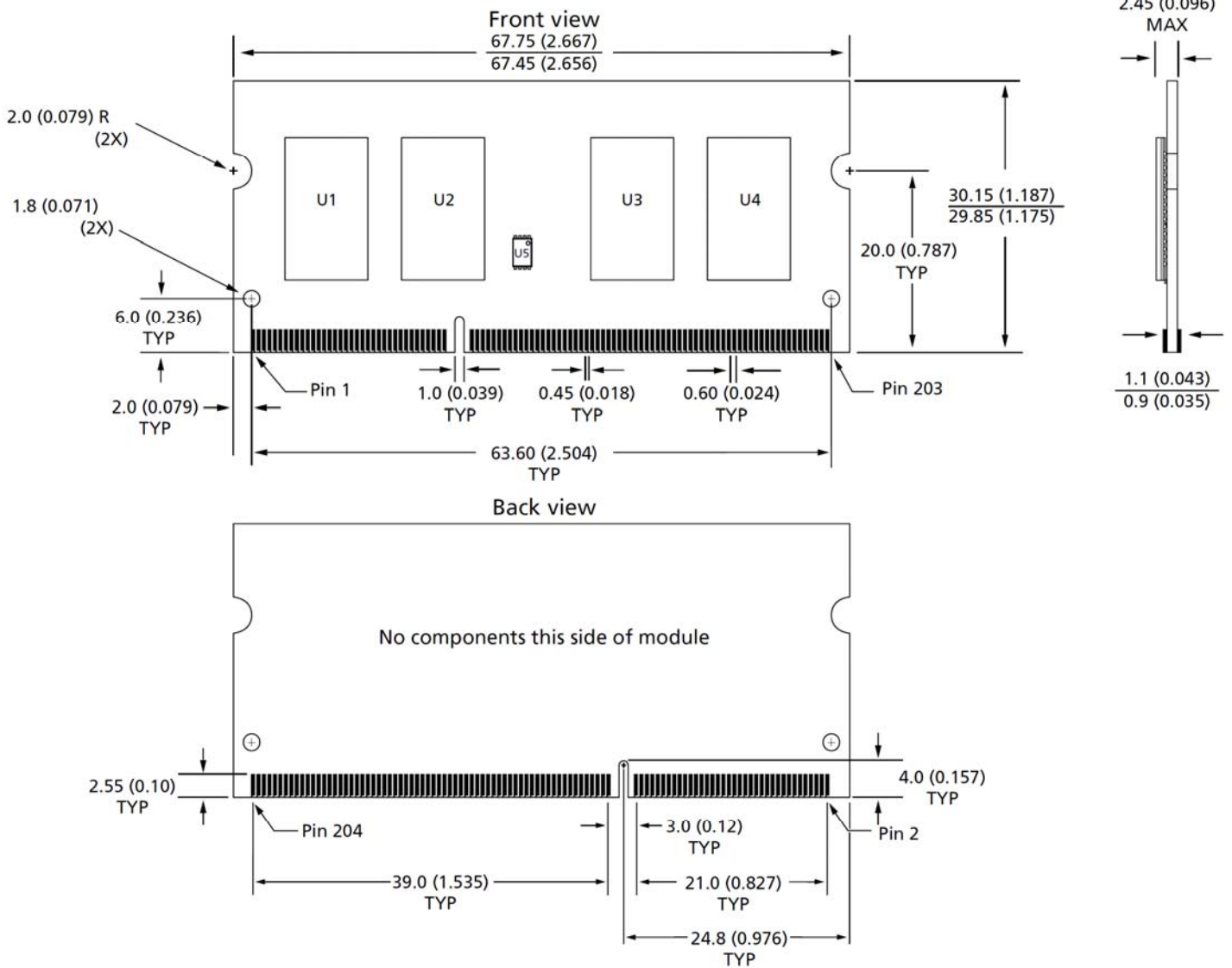
## Simplified Mechanical Drawing(x8 1Rank)
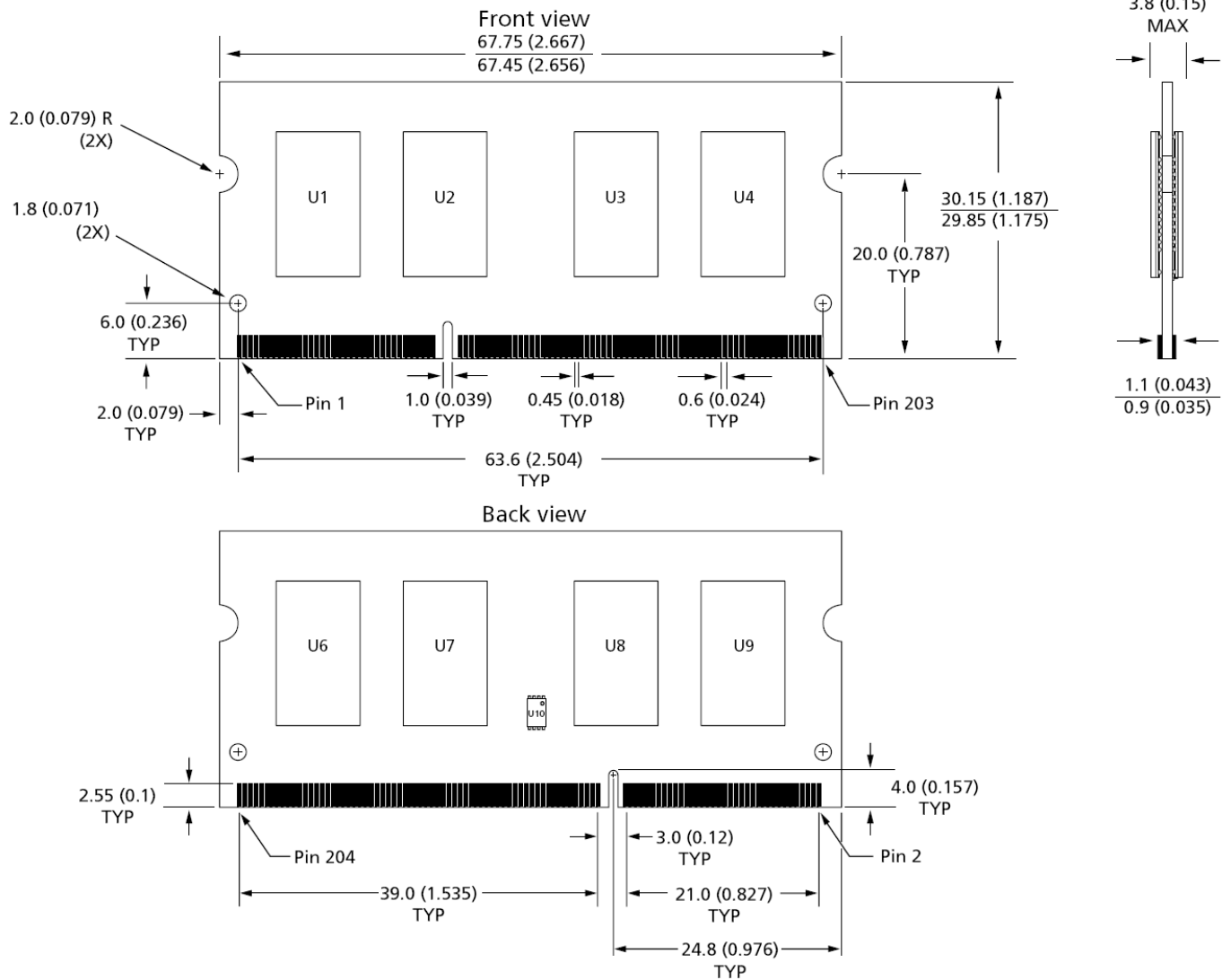
Front view
67.75 (2.667)
67.45 (2.656)

3.8 (0.15)
MAX

2.0 (0.079) R
(2X)

1.8 (0.071)
(2X)

U1    U2        U3    U4

30.15 (1.187)
29.85 (1.175)

20.0 (0.787)
TYP

6.0 (0.236)
TYP

Pin 1    1.0 (0.039)    0.45 (0.018)    0.6 (0.024)    Pin 203
TYP            TYP            TYP

2.0 (0.079)
TYP

1.1 (0.043)
0.9 (0.035)

63.6 (2.504)
TYP

Back view

U6    U7        U8    U9

U10

2.55 (0.1)
TYP

4.0 (0.157)
TYP

Pin 204    3.0 (0.12)    Pin 2
TYP

39.0 (1.535)    21.0 (0.827)
TYP            TYP

24.8 (0.976)
TYP

**Note:** 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

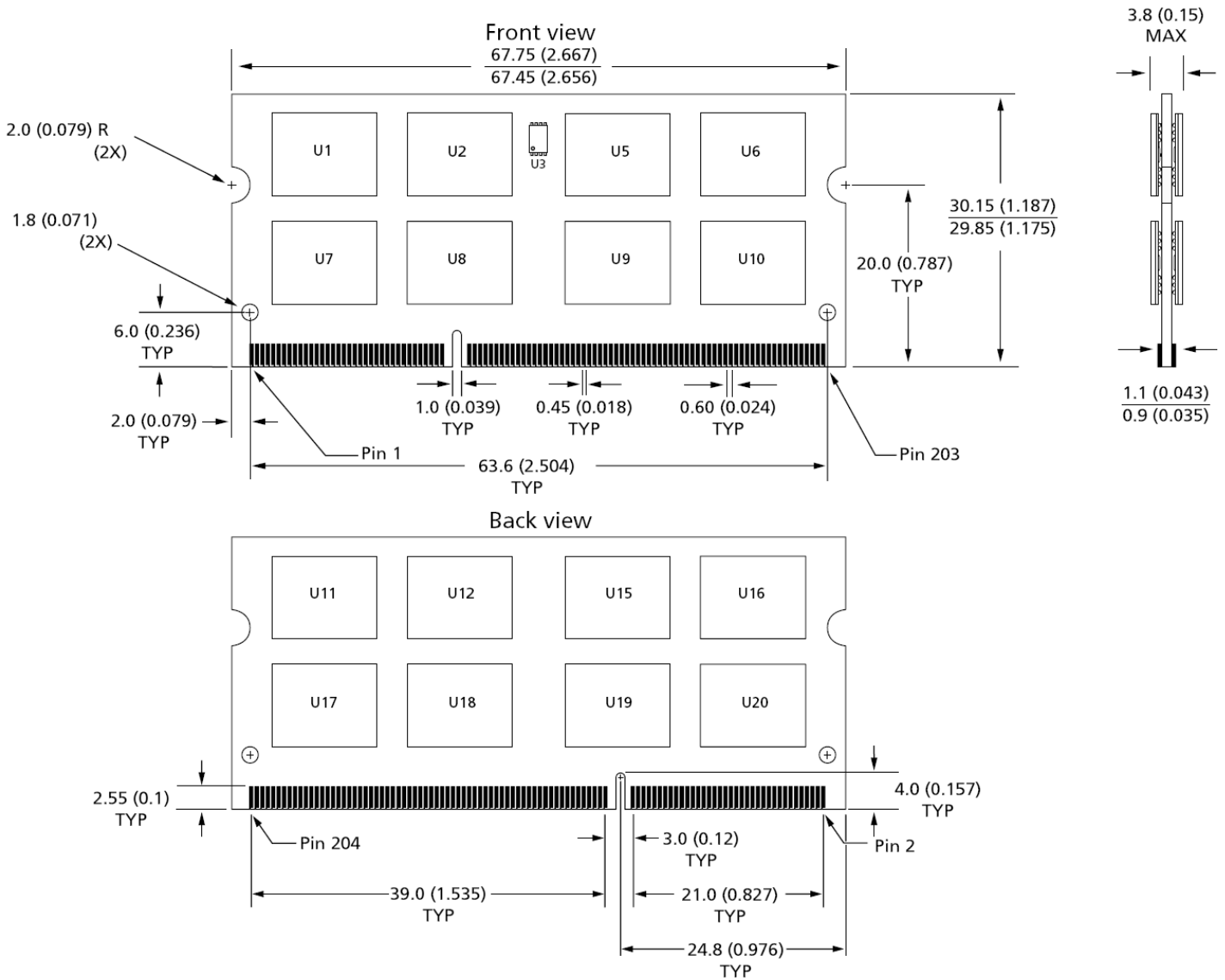**Note:** 2. The dimensional diagram is for reference only.

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# Simplified Mechanical Drawing(x16 1Rank)



**Note:** 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
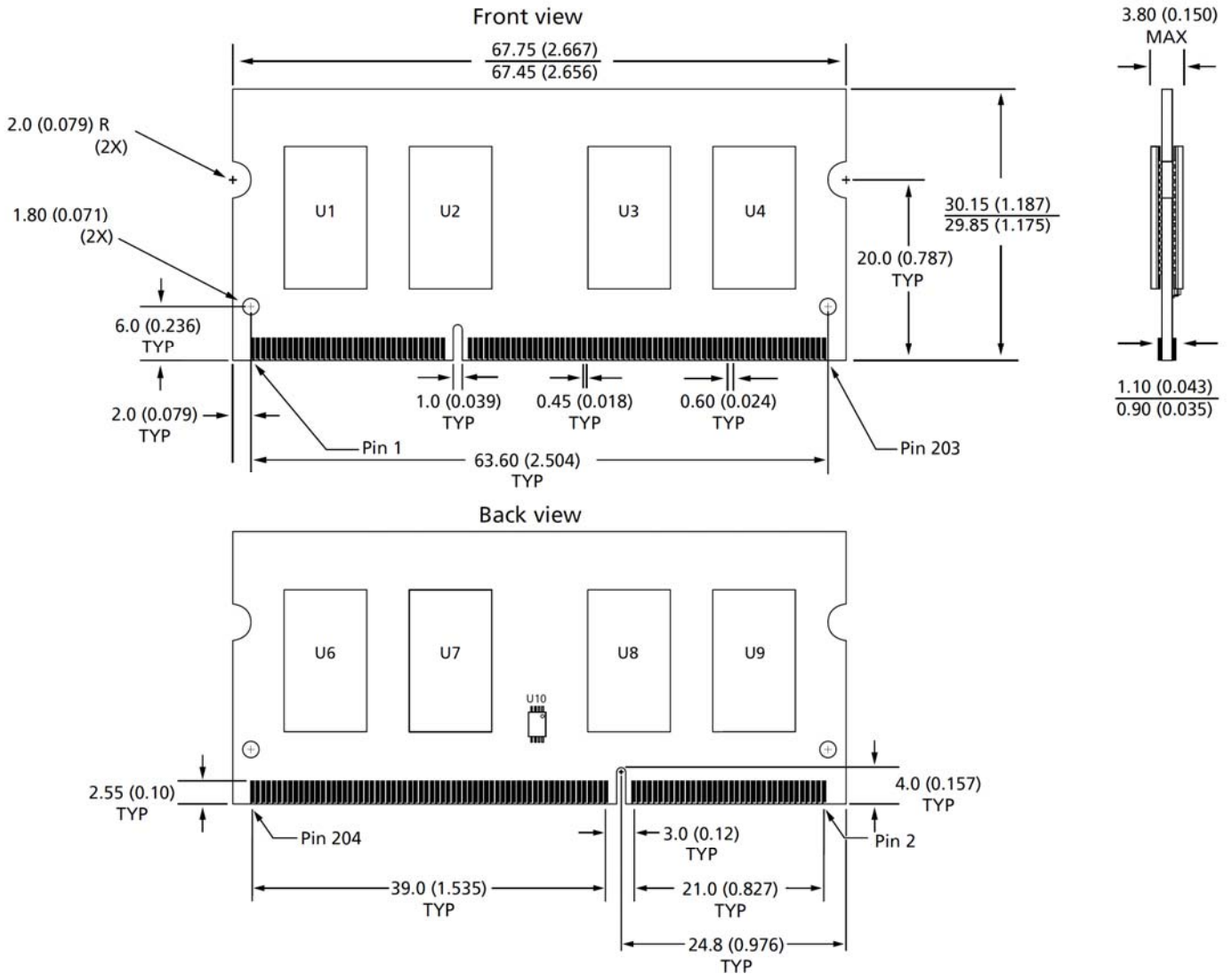
**Note:** 2. The dimensional diagram is for reference only.

# Simplified Mechanical Drawing(x8 2Ranks)



**Note 1:** All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

**Note 2:** The dimensional diagram is for reference only.

# Simplified Mechanical Drawing(x16 2Ranks)



**Note 1:** All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

**Note 2:** The dimensional diagram is for reference only.