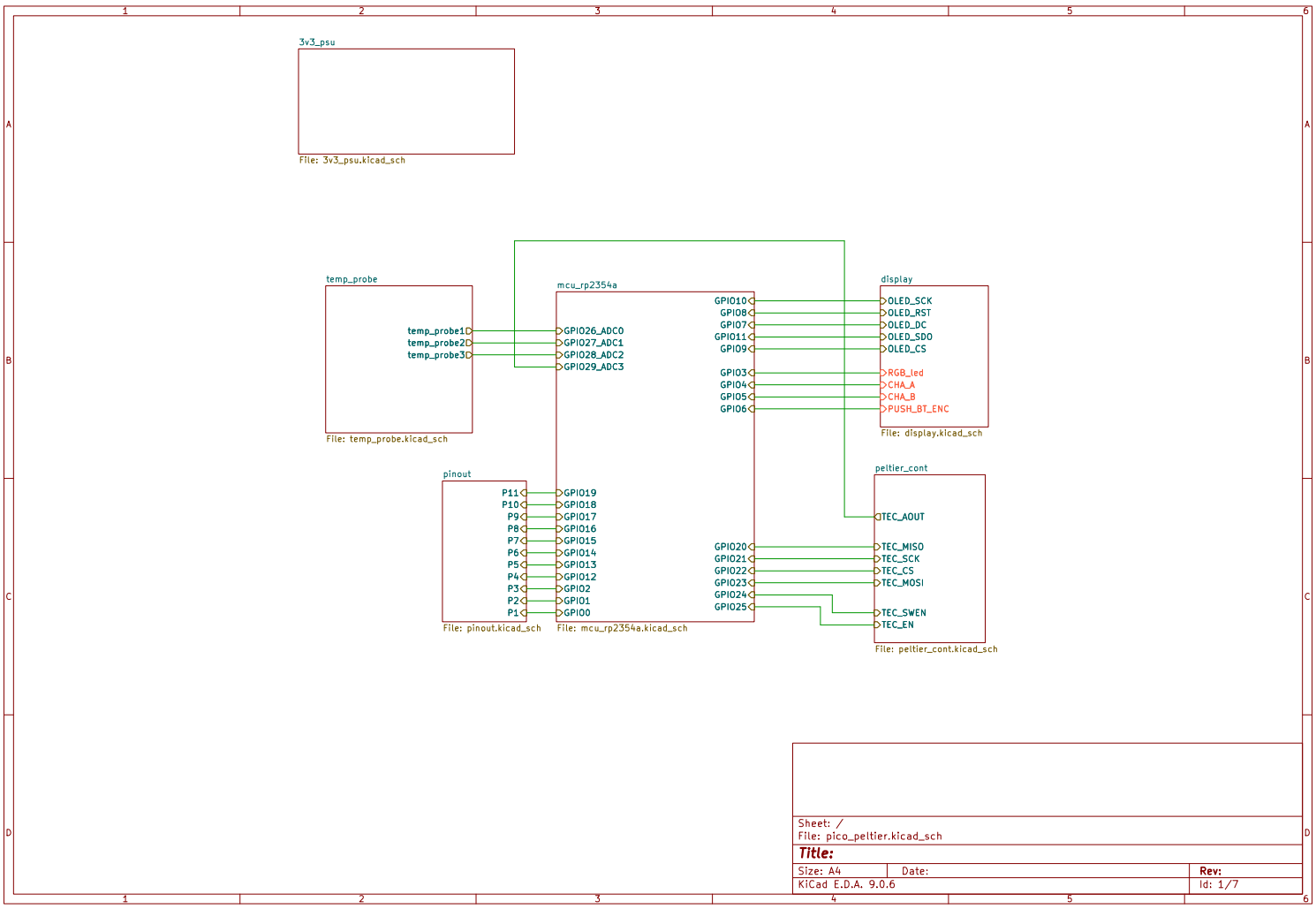
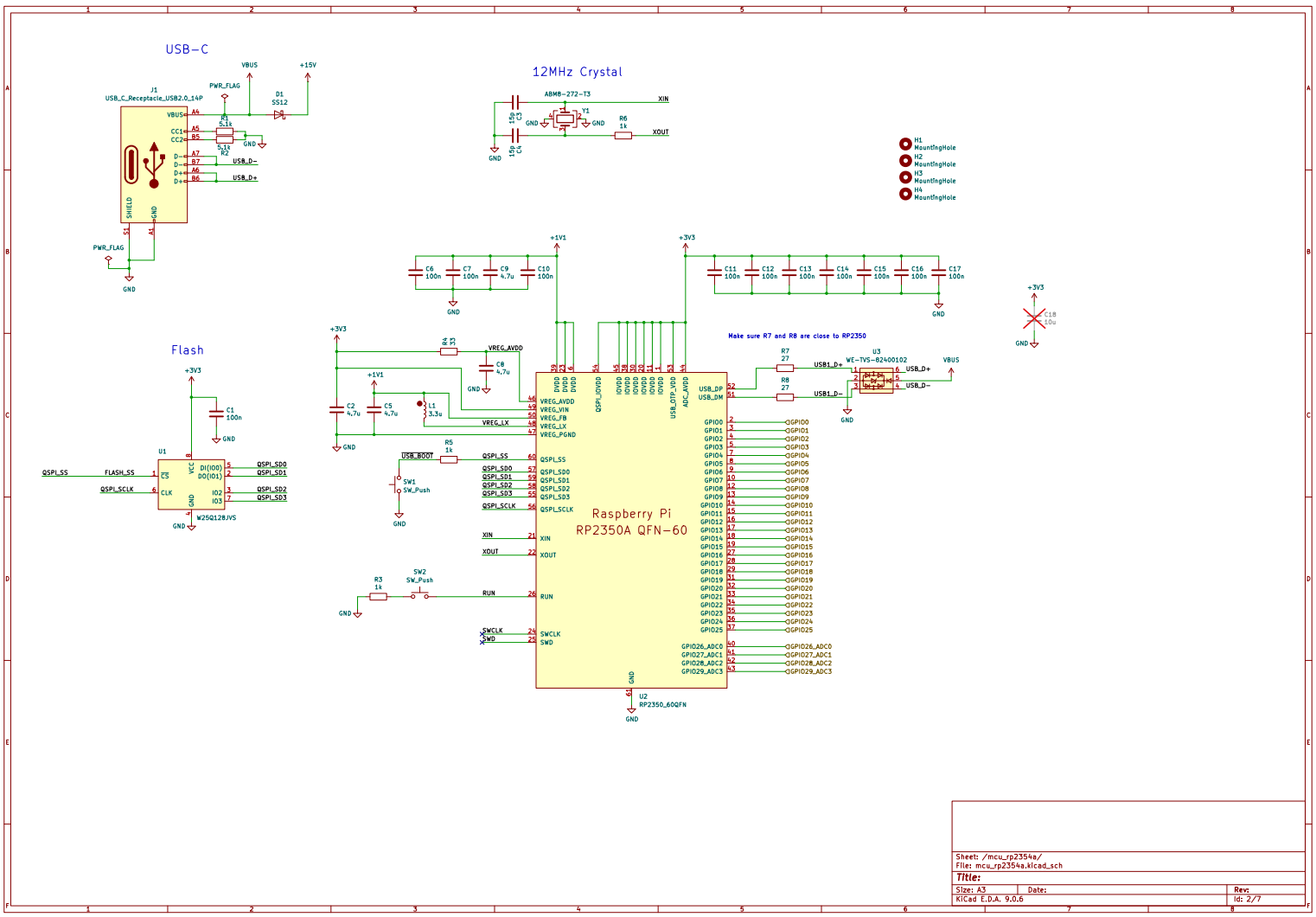
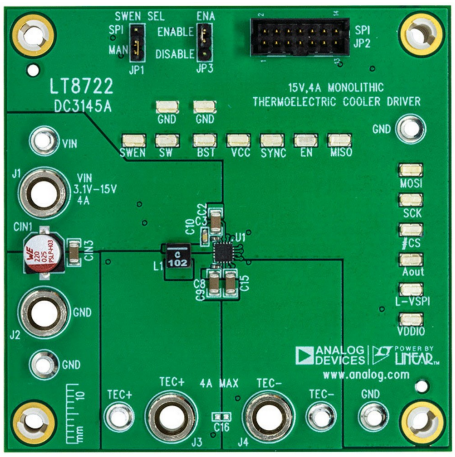
17	HSTX	SPI0 CSn	UART0 RX	I2C0 SCL	PWM0 B	SIO	PIO0	PIO1	PIO2	USB VBUS EN	
18	HSTX	SPI0 SCK	UART0 CTS	I2C1 SDA	PWM1 A	SIO	PIO0	PIO1	PIO2	USB OVCUR DET	UART0 TX
19	HSTX	SPI0 TX	UART0 RTS	I2C1 SCL	PWM1 B	SIO	PIO0	PIO1	PIO2	QMI CS1n	USB VBUS DET	UART0 RX
20		SPI0 RX	UART1 TX	I2C0 SDA	PWM2 A	SIO	PIO0	PIO1	PIO2	CLOCK GPIN0	USB VBUS EN	
21		SPI0 CSn	UART1 RX	I2C0 SCL	PWM2 B	SIO	PIO0	PIO1	PIO2	CLOCK GPOUT0	USB OVCUR DET	
22		SPI0 SCK	UART1 CTS	I2C1 SDA	PWM3 A	SIO	PIO0	PIO1	PIO2	CLOCK GPIN1	USB VBUS DET	UART1 TX

GPIO	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11
23		SPI0 TX	UART1 RTS	I2C1 SCL	PWM3 B	SIO	PIO0	PIO1	PIO2	CLOCK GPOUT1	USB VBUS EN	UART1 RX
24		SPI1 RX	UART1 TX	I2C0 SDA	PWM4 A	SIO	PIO0	PIO1	PIO2	CLOCK GPOUT2	USB OVCUR DET	
25		SPI1 CSn	UART1 RX	I2C0 SCL	PWM4 B	SIO	PIO0	PIO1	PIO2	CLOCK GPOUT3	USB VBUS DET	
26		SPI1 SCK	UART1 CTS	I2C1 SDA	PWM5 A	SIO	PIO0	PIO1	PIO2		USB VBUS EN	UART1 TX
27		SPI1 TX	UART1 RTS	I2C1 SCL	PWM5 B	SIO	PIO0	PIO1	PIO2		USB OVCUR DET	UART1 RX
28		SPI1 RX	UART0 TX	I2C0 SDA	PWM6 A	SIO	PIO0	PIO1	PIO2		USB VBUS DET	
29		SPI1 CSn	UART0 RX	I2C0 SCL	PWM6 B	SIO	PIO0	PIO1	PIO2		USB VBUS EN	



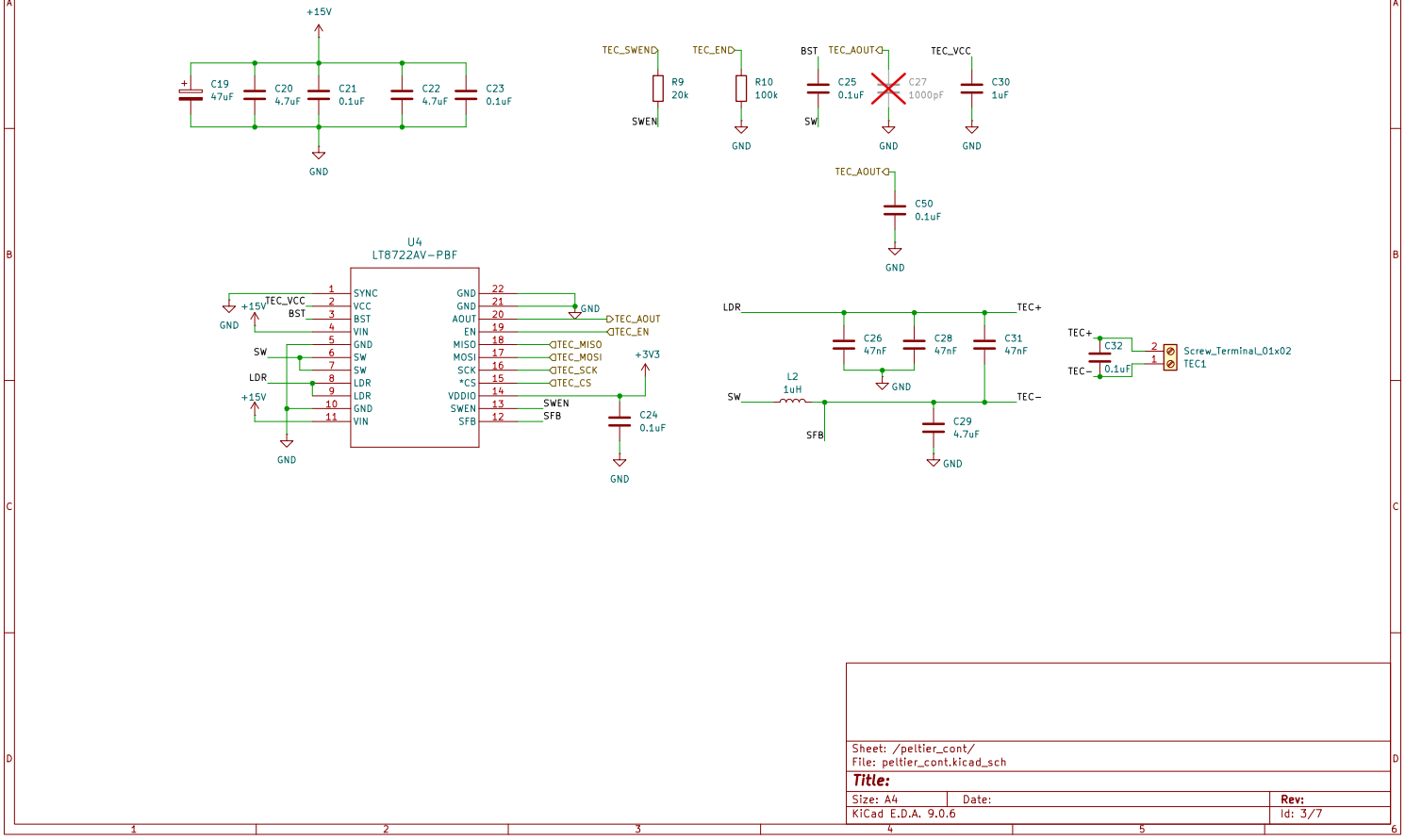
- change the usb to to usb-c [done]
- review back how the UCB C voltage supply are connected, since the main input is 15V [done]





Pin	Name	Function	Connection Note
1	SYNC	Frequency Synchronization	Tie to GND for internal clock (SPI set). Drive with ext. clock to sync.
2	VCC	Internal 3.4V Regulator Output	Do not load. Bypass with 1uF to GND.
3	BST	Boost (High-Side Gate Drive)	Connect 0.1uF capacitor between BST and SW.
4	VIN	Input Supply (Power)	Main Power. Bypass with 4.7uF + 0.1uF to GND.
5	GND	Power Ground	Connect to local ground plane.
6	SW	Switch Node (Buck Output)	Tie to Pin 7. Connect to Inductor & BST Cap.
7	SW	Switch Node (Buck Output)	Tie to Pin 6.
8	LDR	Linear Driver Output (TEC+)	Tie to Pin 9. Connect to Load (TEC+) & Filter Caps.
9	LDR	Linear Driver Output (TEC+)	Tie to Pin 8.
10	GND	Power Ground	Connect to local ground plane.
11	VIN	Input Supply (Power)	Tie to Pin 4. Bypass with 4.7uF + 0.1uF to GND.
12	SFB	Switcher Feedback (TEC-)	Connect to Inductor Output & Load (TEC-).
13	SWEN	PWM Enable & Fault Flag	Bidirectional. Input = Enable Switching: Output (Low) = Fault. Must use ~20kΩ series resistor.
14	VDDIO	Digital I/O Supply	Connect to 3.3V (or MCU Logic Level). Bypass with 0.1uF or 1uF.
15	CS	Chip Select	SPI Chip Select (Active Low).
16	SCK	Serial Clock	SPI Clock Input.
17	MOSI	Master Out Slave In	SPI Data Input.
18	MISO	Master In Slave Out	SPI Data Output.
19	EN	Master Enable	High (>0.74V) = Active, Low = Shutdown. Pull-down recommended if GPIO controlled.
20	AOUT	Analog Telemetry Output	Connect to MCU ADC. Buffers internal signals (Temp, Current, Vout).
21	GND	Exposed Pad (Thermal)	Must solder to PCB Ground. Critical for heat dissipation.
22	GND	Exposed Pad (Thermal)	Same as Pin 21.

PWM Enable & Fault Flag



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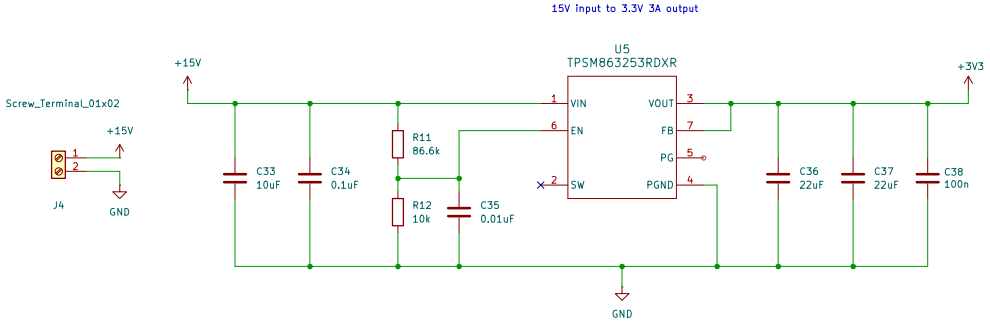

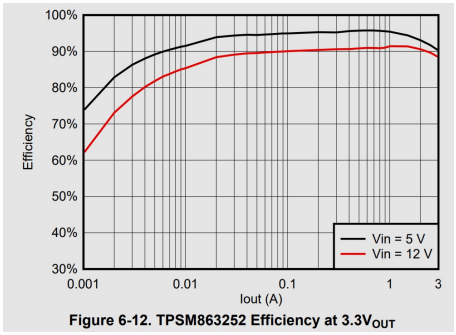

Figure 6-12. TPSM863252 Efficiency at 3.3V_{OUT}

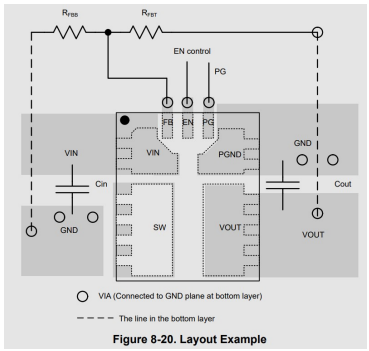

Figure 8-20. Layout Example

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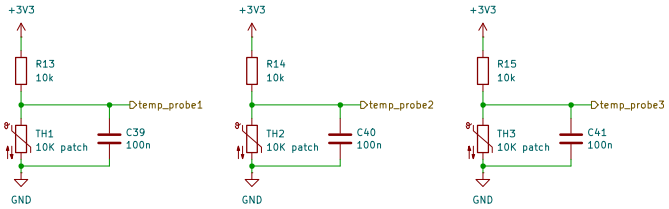
KiCad E.D.A. 9.0.6		Id: 4/7

Temp probe: cold, hot and room



Probe 1

Probe 2

Probe 3

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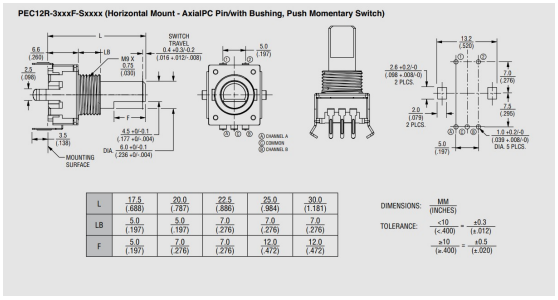
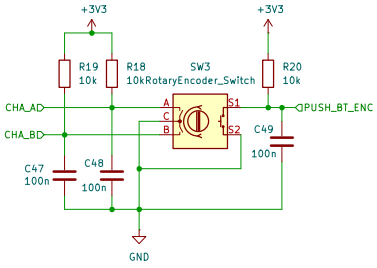
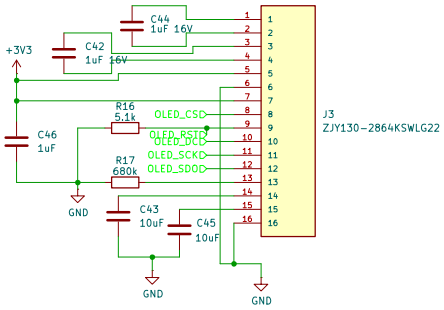
KiCad E.D.A. 9.0.6		Id: 5/7

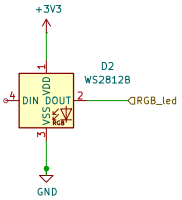


L	17.5 (.688)	20.0 (.787)	22.5 (.886)	25.0 (.984)	30.0 (1.181)
LB	5.0 (.197)	5.0 (.197)	7.0 (.276)	7.0 (.276)	7.0 (.276)
F	5.0 (.197)	7.0 (.276)	7.0 (.276)	12.0 (.472)	12.0 (.472)

Monochrome Display 1.3" 128x64
SH1106G







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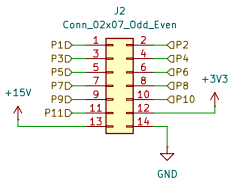

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